The requirements to comply with the MSL testing and marking requirements must be completed by 6 months from the date of this document. Before then, use of the previous method is authorized.

INCH-POUND
MIL-PRF-55365K
11 November 2024
SUPERSEDING
MIL-PRF-55365J
24 March 2017

PERFORMANCE SPECIFICATION

CAPACITOR, FIXED, ELECTROLYTIC (TANTALUM), CHIP, ESTABLISHED RELIABILITY, NON-ESTABLISHED RELIABILITY, AND HIGH RELIABILITY, GENERAL SPECIFICATION FOR

FAILURE RATE LEVELS M, P, R, AND S
ARE INACTIVE FOR NEW DESIGN AFTER 23 AUGUST 1990.
USE WEIBULL FAILURE RATE LEVELS B, C, D, OR T.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the general requirements for non-established reliability (non-ER), established reliability (ER), and high reliability (T level) tantalum dielectric, fixed, chip capacitors, primarily intended for use in thick and thin film hybrid circuits or surface mount applications for filter, bypass, coupling, and other applications where the alternating current (ac) component is small compared to the direct current (dc) rated voltage and where supplemental moisture protection is available (see 6.1). Long term exposure to humid conditions may affect the equivalent series resistance of these capacitors and possibly result in damage during solder reflow (see 6.11). The established reliability capacitors have reliability ratings established on the basis of life tests performed at specified voltage at +85°C for failure rate levels (FRL) ranging from:

a. 1.0 percent per 1,000 hours to 0.001 percent per 1,000 hours in accordance with MIL-STD-690. These FRLs are established at a 60-percent confidence level and are maintained at a 10-percent producer's risk (exponential distribution).

b. 0.1 percent per 1,000 hours to 0.001 percent per 1,000 hours at 90-percent confidence level (Weibull distribution).

The high reliability capacitors (T level) are intended for space, missile, and other high reliability applications and require the following: Weibull grading to the C FRL or lower, surge current option C (see table IV), destructive physical analysis, 100 percent radiographic inspection, 100 percent visual inspection, and DC leakage and equivalent series resistance measurements within +3 standard deviations of the lot mean. Inspection of product for delivery for T level capacitors consists of group A and subgroups I, II, and III of group C. These additional tests and inspections are expected to result in a lower FRL than the initial Weibull graded lot (see table V).

1.2 Classification. Capacitors covered by this specification are classified by style as specified (see 3.1).

1.2.1 Part or Identifying Number (PIN). The PIN should be in the following form and as specified (see 3.1):

a. For MIL-PRF-55365/4 and MIL-PRF-55365/8:

CWR06	B	C	225	J	B	B
Style (see 1.2.1.1)	Voltage (see 1.2.1.2)	Termination finish (see 1.2.1.3)	Capacitance (see 1.2.1.4)	Capacitance tolerance (see 1.2.1.5)	Product level designator (see 1.2.1.6)	Surge current option (see 1.2.1.7)

Comments, suggestions, or questions on this document should be addressed to: DLA Land and Maritime, ATTN: VAT, Post Office Box 3990, Columbus, OH 43128-3990 or e-mailed to capacitorfilter@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil

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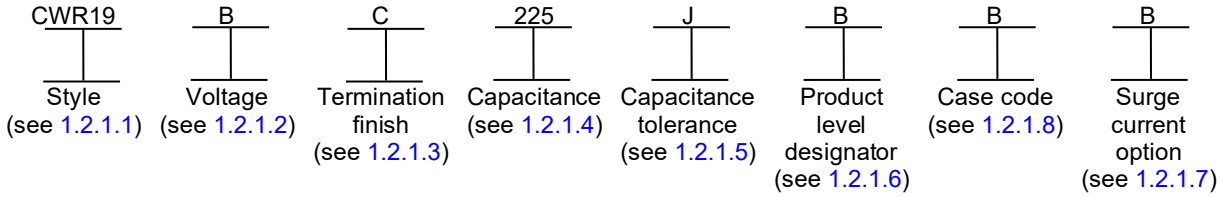
b. For specification sheets /11 and higher (PIN format includes case code):



1.2.1.1 Style. The style is identified by the three-letter symbol “CWR”, followed by the two digit number. The letters identify tantalum chip capacitors. The number identifies the design of the capacitor.

1.2.1.2 Voltage. The voltage (rated, derated, and surge) is identified by a single letter as shown in table I.

TABLE I. Voltage.

Symbol	Voltage (V_{dc})		
	Rated (+85°C)	Derated (+125°C)	Surge (+85°C)
A	2	1.3	2.7
B	3	2.0	4.0
C	4	2.7	5.3
D	6	4.0	8.0
E	8	5.3	10.7
F	10	6.7	13.3
G	12	8.0	16.0
H	15	10.0	20.0
J	20	13.3	26.7
K	25	16.7	33.3
L	30	20.0	40.0
M	35	23.3	46.7
N	50	33.3	66.7

1.2.1.3 Termination finish. The termination finish is identified by a single letter as follows:

Symbol	Termination finish
B	Gold plated (50 microinch minimum)
C	Hot solder dipped (60 microinch minimum)
H	Solder plated (100 microinch minimum)
K	Solder fused (60 microinch minimum)

At the option of the manufacturer, all termination finishes may have a barrier metal. See 6.8 for conversion from previous termination finishes.

1.2.1.4 Capacitance. The nominal capacitance value, expressed in picofarads (pF), is identified by a three-digit number. The first two digits represent significant figures and the third digit specifies the number of zeros to follow.

1.2.1.5 Capacitance tolerance. The capacitance tolerance is identified by a single letter as shown in table II.

TABLE II. Capacitance tolerance.

Symbol	Capacitance tolerance
J	± 5 percent
K	± 10 percent
M	± 20 percent

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1.2.1.6 Product level designator. The product level designator is identified by a single letter as shown in table III.

TABLE III. Product level designator.

Symbol	Product level (% per 1,000 hours)
A	non-ER
Weibull FRL (see 1.1)	
B	0.1
C	0.01
D	0.001
T	0.01 or lower
Exponential FRL (see 1.1) 1/	
M	1.0
P	0.1
R	0.01
S	0.001

1/ Inactive for new design. Use Weibull FRLs.

1.2.1.7 Surge current option. The optional surge current tests are described in table IV. This table reflects the required test temperature(s) as well as whether the surge current test is to be performed before or after the Weibull grading/voltage aging test. The surge current option is identified by a single letter.

TABLE IV. Optional surge current testing.

Option letter	Temperatures	Weibull		Exponential	
		Before Weibull grading	After Weibull grading	Before voltage aging	After voltage aging
A	+25°C ± 5°C	N/A	X	N/A	X
B	-55°C (-5°C, +0°C) and +85°C ± 5°C	N/A	X	N/A	X
C 2/	-55°C (-5°C, +0°C) and +85°C ± 5°C	X	N/A	X	N/A
Z 1/	No surge current test	N/A	N/A	N/A	N/A

1/ Not applicable to MIL-PRF-55365/4 and MIL-PRF-55365/8. When no surge current testing is required for MIL-PRF-55365/4 and MIL-PRF-55365/8 capacitors, no letter is included.
2/ Surge current option C is required for T level capacitors. When ordering T level capacitors, surge current option C must be specified in the PIN (see 1.2.1).

1.2.1.8 Case code. For specification sheets MIL-PRF-55365/11 and higher only, the capacitor PIN contains a single letter designator that defines the capacitor case size. This letter corresponds to the case code designation in the characteristic tables of the applicable specification sheets (see 3.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections 3 and 4 of this specification, whether or not they are listed.

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2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract (see 6.2).

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-55365/4	-	Capacitor, Chip, Fixed, Tantalum, Polarized, Established Reliability, Nonestablished Reliability, and High Reliability, Styles CWR06 and CWR09
MIL-PRF-55365/8	-	Capacitor, Chip, Fixed, Tantalum, Polarized, Established Reliability, Nonestablished Reliability, and High Reliability Style CWR11 (Metric)
MIL-PRF-55365/11	-	Capacitor, Chip, Fixed, Tantalum, Polarized, Established Reliability, Nonestablished Reliability and High Reliability Styles CWR19 and CWR29
MIL-PRF-55365/12	-	Capacitor, Chip, Fixed, Tantalum, Polarized, Established Reliability and Nonestablished Reliability, Style CWR15
MIL-PRF-55365/13	-	Capacitor, Chip, Fixed, Tantalum, Polarized, Established Reliability and Nonestablished Reliability, Style CWR16 and CWR26

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202	-	Electronic and Electrical Component Parts
MIL-STD-202-106	-	Method 106, Moisture Resistance
MIL-STD-202-107	-	Method 107, Thermal Shock
MIL-STD-202-108	-	Method 108, Life (at Elevated Ambient Temperature)
MIL-STD-202-204	-	Method 204, Vibration, High Frequency
MIL-STD-202-208	-	Method 208, Solderability
MIL-STD-202-209	-	Method 209, Radiographic Inspection
MIL-STD-202-210	-	Method 210, Resistance to Soldering Heat
MIL-STD-202-215	-	Method 215, Resistance to Solvents
MIL-STD-202-305	-	Method 305, Capacitance
MIL-STD-690	-	Failure Rate Sampling Plans and Procedures
MIL-STD-790	-	Established Reliability and High Reliability Qualified Products List (QPL) Systems for Electrical, Electronic, and Fiber Optic Parts Specifications
MIL-STD-1285	-	Marking of Electrical and Electronic Parts
MIL-STD-1580	-	Destructive Physical Analysis for Electronic, Electromagnetic, and Electromechanical Parts

(Copies of these documents are available online at https://assist.dla.mil/.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC INTERNATIONAL (IPC)

EIA/IPC/JEDEC J-STD-002	-	Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires
IPC/JEDEC J-STD-020	-	Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices

(Copies of these documents are available online at https://www.ipc.org/).

SAE INTERNATIONAL (SAE)

EIA554-1	-	Assessment of Average Outgoing Quality Levels in Parts Per Million (PPM)
EIA-557	-	Statistical Process Control Systems

(Copies of these documents are available online at https://www.sae.org/.)

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2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Specification sheets. The individual item requirements shall be as specified herein and in accordance with the applicable specification sheet. In the event of any conflict between the requirements of this specification and the specification sheet, the latter shall govern (see 6.2).

3.2 Qualification. Capacitors furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable qualified products list (QPL) before contract award (see 4.4 and 6.4).

3.3 QPL system. The manufacturer shall establish and maintain a QPL system for parts covered by this specification. Requirements for this system are specified in MIL-STD-790 and MIL-STD-690. In addition, the manufacturer shall also establish a Statistical Process Control (SPC) and Part Per Million (ppm) system that meets the requirements as detailed in 3.3.1 and 3.3.2 respectively

3.3.1 SPC system. As part of the overall MIL-STD-790 QPL system, the manufacturer shall establish an SPC system that meets the requirements of EIA-557. Typical manufacturing processes include: Pressing, sintering, electrochemical processing, encapsulating, and packaging.

3.3.2 PPM system. As part of the overall MIL-STD-790 QPL system, the manufacturer shall establish a ppm system of assessing the average outgoing quality of lots in accordance with EIA554-1. Data exclusion, in accordance with EIA554-1 may be used with approval of the qualifying activity. The ppm system shall identify the ppm rate at the end of each month and shall be based on a 6-month moving average. Style reporting may include non-established reliability, established reliability, and high reliability style combinations.

3.4 Materials. Materials shall be as specified herein. However, when a definite material is not specified, a material shall be used which will enable the capacitors to meet the performance requirements of this specification. Acceptance or approval of any constituent material shall not be construed as a guaranty of the acceptance of the finished product.

3.5 Radiographic inspection (T level only). When capacitors are tested as specified in 4.7.2, the following shall apply:

a. For epoxy molded cased devices, there shall be a silver epoxy attachment joining the cathode terminal to the silver coated tantalum slug. There shall be a minimum of 25 percent attachment.

b. For devices without epoxy molded cases (orange or blue), there shall be a silver epoxy attachment joining the cathode end cap to the silver coated tantalum slug. There shall be a minimum of 25 percent attachment (end of anode slug only).

c. For all styles, the conductive epoxy attaching the tantalum slug to the cathode end cap or lead shall not be separated or cracked.

d. For epoxy molded cased devices, the riser wire-to-external lead weld shall not create a misalignment greater than 15 degrees between riser and lead. Additionally, this weld shall exhibit molding compound between the end of the riser wire and the outer package edge.

e. For conformal coated capacitors (CWR06, CWR16, CWR26), there shall be no pinholes that expose any surface of the capacitor element, or cracks on the molded case of all molded capacitors, or chipouts that reduce the case wall thickness by 50%. There shall be no stress cracks on the external leads of all molded capacitors.

f. There shall be no visible cracks in the tantalum slug.

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3.6 Destructive physical analysis (DPA) (T level only). When examined as specified in 4.7.3, capacitors shall meet the requirements of MIL-STD-1580, requirement 10, paragraph 10.11 with the following exceptions:

a. For epoxy molded cased devices, there shall be a silver epoxy attachment joining the cathode terminal to the silver coated tantalum slug. There shall be a minimum of 25 percent attachment.

b. For devices without epoxy molded cases (orange or blue), there shall be a silver epoxy attachment joining the cathode end cap to the silver coated tantalum slug. There shall be a minimum of 25 percent attachment (end of anode slug only).

c. For all styles, there shall be a minimum wall thickness of .001 inch (0.025 mm).

3.7 Interface and physical dimension. Capacitors shall meet the interface and physical dimensions specified (see 3.1).

3.7.1 Body structure. The body structure shall be either conformally coated or molded form (see 3.1).

3.7.2 Terminals. Terminals shall be of a solid conductor, of the dimensions specified (see 3.1), and shall be suitably treated to facilitate soldering.

3.7.2.1 Reprocessing of terminations. The manufacturer (or his authorized category B or category C distributor) may reprocess the terminations of the capacitors supplied to this specification, provided the termination process has been approved by the qualifying activity.

3.7.2.2 Reprocessing option. If the manufacturer (or his authorized category B or category C distributor) reprocesses the terminations of the capacitors as a part of normal production, or as a corrective action for solderability failure, the following shall apply:

a. Following any reprocessing, the electrical measurements as specified in group A, subgroup 1, shall be performed on a 200 piece sample for each 8 hours of manufacturing. If there are one or more defects, the individual inspection lot, or lots, from which the defect originated shall be subjected to 100 percent testing of the electrical measurements of group A, subgroup 1, and shall meet the percent defective allowable (PDA) requirements as specified in 4.6.1.2.3.1 or 4.6.1.2.3.2.

b. PPM data following the reprocessing shall be reported every 6 months. The calculation method shall be in accordance with EIA554-1.

3.7.2.3 Tin plated finishes. The use of pure tin, as an underplate or final finish, is prohibited both internally and externally. Tin content of capacitor components and solder shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass (see 6.10).

3.8 Voltage aging (exponential only). When tested as specified in 4.7.5, capacitors shall meet the following requirements:

a. DC leakage: As specified in 3.9.

b. Capacitance: As specified in 3.10.

c. Dissipation factor: As specified in 3.11.

d. Equivalent Series Resistance (ESR): As specified in 3.17.

3.9 DC leakage. When measured as specified in 4.7.6, the dc leakage shall not exceed the applicable value specified (see 3.1).

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3.10 Capacitance. When measured as specified in 4.7.7, the capacitance shall be within the applicable tolerance specified (see 3.1).

3.11 Dissipation factor. When measured as specified in 4.7.8, the dissipation factor shall not exceed the value specified (see 3.1).

3.12 Vibration, high frequency. When capacitors are tested as specified in 4.7.9, there shall be no intermittent contacts of 0.5 ms or greater duration, or arcing, or other indication of breakdown, nor shall there be any open-circuiting or short-circuiting or evidence of mechanical damage.

3.13 Reflow conditioning. Capacitors shall be conditioned as specified in 4.7.10.

3.14 Thermal shock (unmounted). Capacitors shall be conditioned as specified in 4.7.11.

3.15 Thermal shock (mounted). When tested as specified in 4.7.12, capacitors shall meet the following requirements:

a. DC leakage: As specified in 3.9.

b. Capacitance: Shall change not more than ± 5 percent from the initial measured value.

c. Dissipation factor: As specified in 3.11.

d. ESR: As specified in 3.17.

e. Visual examination: There shall be no evidence of harmful corrosion, mechanical damage, or obliteration of marking (if applicable).

3.16 Resistance to soldering heat. When tested as specified in 4.7.13, capacitors shall meet the following requirements:

a. DC leakage: As specified in 3.9.

b. Capacitance: Shall change not more than ± 5 percent from the initial measured value.

c. Dissipation factor: As specified in 3.11.

d. Visual examination: There shall be no evidence of mechanical damage.

3.17 ESR. When measured as specified in 4.7.14, the ESR shall not exceed the specified value (see 3.1).

3.18 Moisture resistance. When tested as specified in 4.7.15, capacitors shall meet the following requirements:

a. DC leakage: Shall not exceed 200 percent of the requirement specified in 3.9.

b. Capacitance: Shall change not more than ±15 percent from the initial measured value.

c. Dissipation factor: Shall not exceed 150 percent of the requirement specified in 3.11.

d. ESR: Unless otherwise specified (see 3.1), the ESR shall not exceed 150 percent of the specified value (see 3.1).

e. Visual examination: There shall be no evidence of harmful corrosion, mechanical damage, or obliteration of marking (if applicable).

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3.19 Stability at low and high temperatures. When tested as specified in 4.7.16, capacitors shall meet the following requirements:

a. Step 1 (+25°C):

(1) DC leakage: As specified in 3.9.

(2) Capacitance: As specified in 3.10.

(3) Dissipation factor: As specified in 3.11.

(4) ESR: As specified in 3.17.

b. Step 2 (-55°C):

(1) Capacitance: Shall change not more than ± 10 percent (± 20 percent for CWR15) from the step 1 measured value.

(2) Dissipation factor: As specified in 3.11.

c. Step 3 (+25°C):

(1) DC leakage: As specified in 3.9.

(2) Capacitance: Shall change not more than ± 5 percent (± 10 percent for CWR15) from the step 1 measured value.

(3) Dissipation factor: As specified in 3.11.

d. Step 4 (+85°C):

(1) DC leakage: As specified in 3.9.

(2) Capacitance: Shall change not more than ± 10 percent (± 15 percent for CWR15) from the step 1 measured value.

(3) Dissipation factor: As specified in 3.11.

e. Step 5 (+125°C):

(1) DC leakage: As specified in 3.9.

(2) Capacitance: Shall change not more than ± 15 percent (± 20 percent for CWR15) from the step 1 measured value.

(3) Dissipation factor: As specified in 3.11.

f. Step 6 (+25°C):

(1) DC leakage: As specified in 3.9.

(2) Capacitance: Shall change not more than ± 5 percent (± 10 percent for CWR15) from the step 1 measured value.

(3) Dissipation factor: As specified in 3.11.

(4) ESR: As specified in 3.17.

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3.20 Surge voltage (exponential only, see 3.1). When tested as specified in 4.7.17, capacitors shall meet the following requirements:

a. DC leakage: As specified in 3.9.

b. Capacitance: Shall change not more than ± 5 percent from the initial measured value.

c. Dissipation factor: As specified in 3.11.

d. ESR: As specified in 3.17.

3.21 Surge current (optional, see 1.2.1.7). When tested as specified in 4.7.18, capacitors shall meet the following requirements:

a. DC leakage: As specified in 3.9.

b. Capacitance: As specified in 3.10.

c. Dissipation factor: As specified in 3.11.

3.22 Life. When capacitors are tested as specified in 4.7.19, there shall be no evidence of harmful corrosion or obliteration of marking (if applicable), mechanical damage, intermittent shorts, or permanent shorts or opens.

3.22.1 Qualification inspection. When tested as specified in 4.7.19, capacitors shall meet the following requirements:

a. At +25°C:

(1) DC leakage: As specified in 3.9.

(2) Capacitance: Shall change not more than ± 5 percent (± 10 percent for CWR15) from the initial measured value.

(3) Dissipation factor: As specified in 3.11.

(4) ESR: As specified in 3.17.

b. At +85°C: DC leakage: As specified in 3.9.

c. At +125°C: DC leakage: As specified in 3.9.

3.22.2 Periodic group C life or extended life (see 4.7.19.1). When tested as specified in 4.7.19, capacitors shall meet the following requirements:

a. At +25°C:

(1) DC leakage: Shall change not more than 200 percent of the initial requirement as specified in 3.9.

(2) Capacitance: Shall change not more than ± 5 percent (± 10 percent for CWR15) from the initial measured value

(3) Dissipation factor: As specified in 3.11.

b. At +85°C: DC leakage: Shall change not more than 200 percent of the initial requirement as specified in 3.9.

c. At +125°C: DC leakage: Shall change not more than 200 percent of the initial requirement as specified in 3.9.

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3.23 Weibull FRL grading (in lieu of 3.8) . When tested as specified in 4.7.20, capacitors shall exhibit decreasing FR with respect to time as evidenced by a value of beta (β) which is less than 0.9; and the instantaneous FR in the last interval shall be no more than the FR specified. After grading, capacitors shall meet the following requirements:

a. DC leakage: As specified in 3.9. For T level capacitors, the DC leakage shall be within +3 standard deviations of the lot mean.

b. Capacitance: As specified in 3.10.

c. Dissipation factor: As specified in 3.11.

d. ESR: As specified in 3.17. For T level capacitors, the ESR shall be within +3 standard deviations of the lot mean.

3.24 Solderability. When capacitors are tested as specified in 4.7.21, the dipped portion of the terminations shall conform to the solid-wire termination criteria of MIL-STD-202-208. Solderable surfaces shall be as specified (see 3.1).

3.25 Resistance to solvents. When marked capacitors are tested as specified in 4.7.22, marking shall remain legible and shall not smear.

3.26 Moisture sensitivity level (MSL). When determining the MSL as specified in 4.7.23, capacitors shall meet the following:

a. DC leakage: As specified in 3.9.

b. Capacitance: Shall change not more than ± 20 percent from the initial measured value.

c. Dissipation factor: As specified in 3.11.

d. ESR: As specified in 3.17.

e. Final visual inspection: There shall be no visible external cracks.

3.27 Marking. Molded style capacitors shall be marked in accordance with method I of MIL-STD-1285, and as specified (see 3.1). Polarity marking shall be as specified (see 3.1). All styles shall have the following information marked on the package.

a. “JAN” brand.

b. PIN (see 1.2.1).

c. Manufacturer’s source code in accordance with MIL-STD-1285.

d. Date code.

e. Optional marking of lot identification number on individual capacitors.

f. MSL rating.

3.27.1 JAN and J marking. The United States Government has adopted and is exercising legitimate control over the certification marks “JAN” and “J”, respectively, to indicate that items so marked or identified are manufactured to, and meet all the requirements of specifications. Accordingly, items acquired to, and meeting all of the criteria specified herein and in applicable specifications shall bear the certification mark “JAN” except that items too small to bear the certification mark “JAN” shall bear the letter “J”. The “JAN” or “J” shall be placed immediately before the part number except that if such location would place a hardship on the manufacturer in connection with such marking, the “JAN” or “J” may be located on the first line above or below the part number. Items furnished under contracts or

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orders which either permit or require deviation from the conditions or requirements specified herein or in applicable specifications shall not bear “JAN” or "J". In the event an item fails to meet the requirements of this specification and the applicable specification sheets, the manufacturer shall remove completely the military part number and the “JAN” or the “J” from the sample tested and also from all items represented by the sample. The “JAN” or “J” certification mark shall not be used on products acquired to contractor drawings or specifications. The United States Government has obtained Certificate of Registration Number 6,069,576 for the certification mark “JAN” and Registration Number 2,577,735 for the certification mark “J”.

3.27.2 Substitution of FRL and product levels. The manufacturer may substitute, with acquiring activity approval, FRL and product levels in accordance with table V. If a manufacturer only utilizes Weibull grading, then product manufactured to Weibull product levels B, C, or D may be marked as exponential product levels M, P, R, or S and supplied on the order.

TABLE V. FRL and product level substitutability.

Parts qualified to FRL	May be substituted for FRL product level
T	A, M, P, R, S, B, and C
D	A, M, P, R, S, B, and C
C	A, M, P, R, S, and B
B	A, M, P, R, and S
S	A, M, P, and R
R	A, M, and P
P	A and M
M	A

3.27.3 Substitution of capacitance tolerance and rated voltage. Parts qualified and marked to tighter capacitance tolerance or higher rated voltage, with acquiring activity approval, are substitutable for parts marked to looser capacitance or lower rated voltage, provided all other values, such as case size, characteristic, and terminations remain the same. Unless otherwise specified in the contract or order (see 6.2), the substitutable parts shall not be remarked. In the event the capacitance tolerances or rated voltages are remarked, the lot date codes on the parts shall not be changed and the workmanship criteria shall be met.

3.27.4 Surge current option substitutability. At the option of the manufacturer, surge current options may be substituted for other surge current options as shown below. Unless otherwise specified in the contract or order (see 6.2), the parts shall not be remarked.

Surge current code	May be substituted for surge current code
C	A, B, Z (or no code)
B	A, Z (or no code)
A	Z (or no code)

3.27.5 Termination finish code substitutability. Termination finish codes may be substituted for other termination finish codes, with acquiring activity approval, as shown below. Unless otherwise specified in the contract or order (see 6.2), the parts shall not be remarked.

Termination finish code	May be substituted for termination finish code
K	C
C, K	H
C, H	K

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3.28 Recycled, recovered, environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable, or biobased materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.29 Workmanship. Capacitors shall be processed in such a manner that, when examined under 10X magnification, they shall be uniform in quality and shall be free from pits, cracks, rough edges, and other defects that will affect life, serviceability, or function. The capacitors shall exhibit no de-metallization (lift-off) on the terminations.

3.29.1 Soldering. All excess flux or solder shall be removed. Electrical connections shall be electrically continuous after soldering.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.4).

b. Verification of qualification (see 4.5).

c. Conformance inspection (see 4.6).

d. Periodic group C inspection (see 4.6.1.3).

4.2 QPL system. The manufacturer shall establish and maintain a QPL system as described in 3.3. Evidence of such compliance is a prerequisite for qualification and retention of qualification.

4.3 Inspection conditions and methods.

4.3.1 Inspection conditions. Unless otherwise specified herein, all inspections shall be performed in accordance with the test conditions specified in the “GENERAL REQUIREMENTS” of MIL-STD-202.

4.3.2 Methods.

4.3.2.1 AC measurements. AC measurements shall be made at the frequency specified. The magnitude of the ac voltage shall be equal to or less than 1.0 volt root mean square (rms). The maximum dc bias voltage shall be equal to or less than 2.2 volts.

4.3.2.2 Reference measurements. When requirements are based on comparative measurements made before and after conditioning, the reference measurement shall be considered the last measurement made at +25°C ± 5°C prior to conditioning. Unless reference measurements have been made within 30 days prior to the beginning of conditioning, they shall be repeated.

4.3.3 Power supply. The power supply used for life testing shall have a regulation of ± 2 percent or less of the rated voltage. The power supply employed for dc leakage current measurements shall be stabilized to at least ±100 ppm. During measurements there must be no voltage fluctuations of sufficient amplitude to produce a variation in the current measurement as read with any dc leakage current tester used to test capacitors.

4.4 Qualification inspection. Qualification inspection shall be performed at a laboratory acceptable to the Government (see 6.4) on sample units produced with equipment and procedures normally used in production. Qualification approval will be based on the successful completion of the tests specified in table VI, and will not be withheld pending completion of the extended life test of 4.4.4.1.1a.

4.4.1 Sample size. The number and style combinations of capacitors to be subjected to qualification inspection shall be as specified in appendix A of this specification.

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TABLE VI. Qualification inspection.

Inspection 1/	Requirement paragraph	Method paragraph	Number of sample units to be inspected	Number of failures allowed
Group I				
Reflow conditioning	3.13	4.7.10		
Thermal shock (unmounted)	3.14	4.7.11		
Surge current option C 2/	3.21	4.7.18		
Voltage aging	3.8	4.7.5		
DC leakage	3.9	4.7.6		
Capacitance	3.10	4.7.7	200	N/A
Dissipation factor	3.11	4.7.8		
Equivalent series resistance	3.17	4.7.14		
Surge current options A or B 2/	3.21	4.7.18		
Visual and mechanical examination	3.4, 3.7, 3.27, and 3.29	4.7.4		
Group II				
Vibration, high frequency	3.12	4.7.9	12	
Thermal shock (mounted)	3.15	4.7.12		
Group III				
Resistance to soldering heat	3.16	4.7.13	18	
Moisture resistance	3.18	4.7.15		1
Group IV				
Stability at low and high temperatures	3.19	4.7.16	12	
Surge voltage	3.20	4.7.17		
Group V				
Life (at +125°C)	3.22	4.7.19	24	
Group VI				
Life (at +85°C)	3.22	4.7.19	102	1
Group VII				
Solderability	3.24	4.7.21	10	0
Resistance to solvents	3.25	4.7.22		
Group VIII				
Moisture sensitivity level	3.26	4.7.23	22	3/

1/ For qualification of design changes only, manufacturers may submit Weibull data instead of group V and group VI test data.

2/ The surge current option performed, if applicable, shall be the option for which qualification is being sought (see A.4.6).

3/ In accordance with J-STD-020. No failures allowed. If there are failures during testing for a particular MSL, testing may be repeated for a different level.

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4.4.2 Inspection routine. The sample shall be subjected to the inspections specified in table VI. All sample units shall be subjected to the inspections of group I. The sample units successfully completing group I inspection shall then be divided as specified in table VI for group II through group VIII inclusive, and subjected to the inspections for their particular group. For combined voltage group submissions (see A.3.1.2), the smallest and largest case size, and lowest voltage and highest voltage shall be equally represented in each voltage group (see 4.6.1.1.1) as closely as possible. The inspections within each group shall be performed in the order shown.

4.4.3 Failures. Failures in excess of those allowed in table VI shall be cause for refusal to grant qualification approval.

4.4.4 FRL and quality level verification.

4.4.4.1 FRL qualification.

4.4.4.1.1 Exponential. Exponential FR qualification shall be in accordance with the general and detailed requirements in MIL-STD-690 and the following details:

a. Procedure I: Qualification at the initial FRL. Level "M" (1.0 percent) of FRSP-60 shall apply. Sample units shall be subjected to the qualification inspection specified in group VI of table VI (see 4.4.2). Upon completion of the 2,000 hour qualification tests, the entire life test sample shall be continued on test to 10,000 hours as specified in 4.7.19.1.

b. Procedure II: Extension of qualification to lower FRLs. To extend qualification to the "P" FRL, data from two or more voltages within a style may be combined. For FRLs "R" and "S", the following styles of similar construction (see 4.6.1.1) may be combined:

Group	Styles
1	CWR09, CWR11, CWR19, CWR29
2	CWR06, CWR16, CWR26

c. Procedure III: Maintenance of FRL qualification. Maintenance period B of FRSP-10 shall apply. Regardless of the number of production lots produced during this period, the specified number of unit hours shall be accumulated to maintain qualification.

4.4.4.1.2 Weibull. Weibull FR qualification will be granted only to manufacturers who have achieved FRL P for any capacitor style covered by this specification in accordance with 4.4.4.1.1. To extend qualification to include Weibull FRLs, the manufacturer shall demonstrate the capability of Weibull FR grading (see 4.7.20) to the qualifying activity.

If during two consecutive reporting periods there has been no production of the lowest Weibull FRL for which the manufacturer is qualified, the manufacturer may be required, at the discretion of the qualifying activity, to submit a product of each style to testing in accordance with the qualification inspection requirements. Failure to meet this requirement shall result in a loss of the manufacturer's FR to the lowest FR last demonstrated.

4.4.4.2 Quality level verification. The contractor is responsible for establishing a quality system to verify the ppm defect level of lots that are subjected to the group A inspections. The ppm defect level shall be maintained for each specification sheet. The ppm defect level shall be based on a 6-month moving average.

4.5 Verification of qualification. Every 12 months, the manufacturer shall provide verification of qualification to the qualifying activity. Continued qualification is based on meeting the following requirements.

a. MIL-STD-790 program.

b. The capacitor design has not been modified.

c. Lot rejection for group A does not exceed 5 percent or one lot, whichever is greater; not applicable to table VIII.

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d. Periodic group C inspection.

e. Verification of FRLs.

f. PPM assessment. The ppm level defect shall be maintained for each performance specification sheet.

g. Continued qualification to non-ER (A level) shall be based upon continued maintenance of qualification for the ER part FRL B.

In the event that there is no production of a single style ER or non-ER device during a maintenance period and the manufacturer is listed for more than one style on the QPL, a report shall be submitted certifying that the manufacturer still has the capabilities and facilities necessary to produce that product.

For exponential ER product the manufacturer shall still maintain the required number of unit hours in the maintenance period using those styles produced in order to remain qualified to the applicable failure rate levels. In the case where the lowest failure rate for an un-produced style is M, styles need not be manufactured for testing only but the manufacturer must certify that the capability and facilities needed to produce that style are still in place. In the event that units must be built for the purpose of maintaining the required hours, they shall also undergo all required testing prior to being placed on life test. For ER exponential or non-ER parts, if during three consecutive reporting periods there has been no production of a given style, the manufacturer may be required, at the discretion of the qualifying activity, to submit a newly-produced (not from stock) representative product of that style to testing.

For Weibull parts, if during two consecutive reporting periods, there has been no production of the lowest Weibull failure rate level for which the manufacturer is qualified for any QPL style device, the manufacturer may be required, at the discretion of the qualifying activity, to submit a newly-produced (not from stock) representative product of that style to testing to the lowest Weibull failure rate in accordance with qualification inspection requirements.

4.6 Conformance inspection.

4.6.1 Inspection of product for delivery. Inspection of product for delivery shall consist of group A inspections. For T level, inspection of product for delivery shall consist of group A and group C, subgroups I, II, and III.

4.6.1.1 Inspection and production lot.

4.6.1.1.1 Inspection lot (exponential distribution). An inspection lot shall consist of capacitors of the same specification sheet (see 3.1), from the same production line or lines, of the same basic design, produced under essentially the same conditions, and offered for inspection during a single month. Capacitors of the same specification sheet must be maintained to at least the P level. The capacitance values and voltages produced shall be represented in the lot in approximately the ratio of production. Voltage groups shall be as follows:

Group	Voltage rating, V_{dc}
I	4 to 20, inclusive
II	25 to 50, inclusive

4.6.1.1.2 Inspection lot (Weibull distribution). An inspection lot shall consist of capacitors of the same specification sheet (see 3.1), voltage rating, style, and nominal capacitance rating produced in the same case size. Manufacture of all parts in the lot shall have been started, processed, assembled, and tested as a group. Lot identity shall be maintained throughout the manufacturing cycle. All anodes shall be fabricated from a single identifiable powder lot.

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4.6.1.1.3 Production lot. A production lot shall consist of all capacitors of the same style, voltage rating, nominal capacitance value, and termination finish. Manufacture of all parts in the lot shall have been started, processed, assembled, and tested as a group. Lot identity shall be maintained throughout the manufacturing cycle. All anodes shall be fabricated from a single identifiable powder lot. Non-ER and ER lots shall be kept separate.

T level only: A production lot shall consist of all the capacitors of a single nominal capacitance and voltage rating of one design and shall be processed as a single lot through all manufacturing steps on the same equipment and shall be identified with the same date and lot code designation. The lot may contain all available capacitance tolerances for the nominal capacitance value. In addition, the lot shall conform to the following:

a. Tantalum powder shall be traceable to the same lot (or batch) number and be from the same manufacturer.

b. The lot number may be assigned prior to anode formation as long as the entire lot is processed together per the requirements of 4.6.1.1.3c and d.

c. The anode shall be pressed in a continuous run on the same pressing machine. Further, it shall be sintered and temperature-processed as a complete batch (batches cannot be split during sintering or subsequent temperature conditioning).

d. The entire production lot shall be voltage-formed (at the same time and in the same tank), impregnated, and otherwise processed through final sealing as a complete batch, with all parts receiving the same processing.

4.6.1.2 Group A inspection.

4.6.1.2.1 Non-ER capacitors (A level). The manufacturer shall establish and maintain an inspection system to verify that capacitors meet the dc leakage, capacitance, dissipation factor, ESR, and mechanical examination requirements. In-line or process control may be a part of such system. The inspection system shall also include criteria for lot rejection and corrective actions. The inspection system shall be verified under the overall MIL-STD-790 QPL system.

NOTE: Since the non-ER (A level) is the ER design without the mandatory conformance inspection and FRL assessment, the product is still expected to meet the environmental qualification type requirements (e.g., moisture resistance, or thermal shock.).

4.6.1.2.2 ER capacitors. Group A inspection shall consist of the inspections specified in table VII or table VIII and shall be made on the same set of sample units. Subgroups 1a through 6 may be performed in any order after subgroup 1.

4.6.1.2.3 Subgroup 1 tests.

4.6.1.2.3.1 Exponential. Subgroup 1 tests shall be performed on a production lot basis on 100 percent of the product supplied under this specification. Capacitors failing the tests of subgroup 1 shall be removed from the lot. If during the 100 percent inspection, screening requires that more than 5 percent (5 percent PDA) of the capacitors be discarded due to catastrophic or dc leakage failures, the entire lot shall be rejected. Surge current failures do not count against the PDA.

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TABLE VII. Group A inspection for exponential distribution.

Inspection	Requirement paragraph	Test method paragraph	Sampling procedure
Subgroup 1			
Reflow conditioning	3.13	4.7.10	
Thermal shock (unmounted)	3.14	4.7.11	
Surge current option C (when specified in PIN)	3.21	4.7.18	100% inspection
Voltage aging 1/	3.8	4.7.5	
Surge current options A or B (when specified in PIN)	3.21	4.7.18	
Subgroup 2			
Mechanical examination (physical dimensions only) 2/	3.7	4.7.4	See table IX
Subgroup 3			
Visual examination			
Materials	3.4	4.7.4	13 samples
Marking	3.27		0 failures
Workmanship	3.29		
Subgroup 4			
Stability at low and high temperatures	3.19	4.7.16	13 samples 0 failures
Subgroup 5			
Surge voltage	3.20	4.7.17	13 samples 0 failures
Subgroup 6			
Solderability 3/	3.24	4.7.21	13 samples 0 failures

1/ PDA for voltage aging is 5 percent; rejects shall not be delivered on the contract or order.
2/ This can be eliminated if the manufacturer has demonstrated process control under the SPC program (see 3.3.1), and has been approved by the qualifying activity. If the design, material, construction, or processing of the part is changed or there are any quality problems or failures, the qualifying activity may require resumption of the specified testing. Deletion of testing does not relieve the manufacturer from meeting the test requirement in case of dispute.
3/ Not applicable to gold plated termination finishes.

4.6.1.2.3.2 Weibull. Subgroup 1 tests shall be performed on an inspection lot basis (see 4.6.1.1.2) on 100 percent of the product supplied under this specification. Requirements for the infant mortality period and Weibull FRL grading shall be in accordance with 4.7.20.

4.6.1.2.3.3 Subgroup 1a tests (T level only). Radiographic inspection is performed on 100% of the T level product supplied under this specification. Capacitors failing this inspection shall be removed from the lot. Destructive physical analysis shall be performed on an inspection lot. If a lot is rejected on the DPA sample, the manufacturer has the option to convert the lot to standard product (product level designators A, B, C, D, M, P, R, or S) if the DPA defect is not considered a reliability risk.

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TABLE VIII. Group A inspection for Weibull distribution.

Inspection	Requirement paragraph	Test method paragraph	Sampling procedure
Subgroup 1			
Reflow conditioning	3.13	4.7.10	
Thermal shock (unmounted)	3.14	4.7.11	
Surge current option C (when specified in PIN)	3.21	4.7.18	100% inspection
Weibull FRL grading	3.23	4.7.20	
Surge current options A or B (when specified in PIN)	3.21	4.7.18	
Subgroup 1a			
Radiographic inspection (T level only)	3.5	4.7.2	100%
Destructive physical analysis (T level only)	3.6	4.7.3	5 samples 0 failures
Subgroup 2			
Mechanical examination (physical dimensions only) 1/	3.7	4.7.4	See table IX
Subgroup 3			
Visual examination			
Materials	3.4	4.7.4	(T level 100%)
Marking	3.27		13 samples
Workmanship	3.29		0 failures
Subgroup 4			
Stability at low and high temperatures 2/	3.19	4.7.16	13 samples 0 failures
Subgroup 5			
Solderability 3/	3.24	4.7.21	13 samples 0 failures

1/ This can be eliminated if the manufacturer has demonstrated process control under the SPC program (see 3.3.1) and has been approved by the qualifying activity. If the design, material, construction, or processing of the part is changed or, there are any quality problems, or failures, the qualifying activity may require resumption of the specified testing. Deletion of testing does not relieve the manufacturer from meeting the test requirement in case of dispute.
2/ Sampling need only conform to the requirements of 4.6.1.1.1 (exponential distribution) inspection lot.
3/ Not applicable to gold plated termination finishes.

4.6.1.2.3.3 Manufacturer's production inspection. If the manufacturer performs tests similar to those specified in group A, subgroup 1, as the final step of the manufacturing process, the subgroup 1 test may be eliminated when approved by the qualifying activity. The following criteria shall be complied with:

a. The manufacturer production tests are identical or more stringent than those specified for subgroup 1 tests.

b. One hundred percent of the product shall be subjected to these tests.

c. Failure criteria are identical, the same as, or more stringent than, the subgroup 1 tests.

d. Lot rejection criteria are identical to, or more stringent than, the subgroup 1 tests.

e. Once approved, future changes require approval from the qualifying activity.

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TABLE IX. Sampling plans for group A, subgroup 2.

Lot size			Sample size
1	-	13	100%
14	-	150	13
151	-	280	20
281	-	500	29
501	-	1,200	34
1,201	-	3,200	42
3,201	-	10,000	50
10,001	-	35,000	60
35,001	-	150,000	74
150,001	-	500,000	90
500,001	-	UP	102

4.6.1.2.4 Subgroup 2 tests .

4.6.1.2.4.1 Sampling plans. Subgroup 2 tests shall be performed on an inspection lot basis. Samples subjected to subgroup 2 shall be selected in accordance with table IX based on the size of the inspection lot. In the event of one or more failures, the lot shall be rejected.

4.6.1.2.4.2 Rejected lots. The rejected lot shall be segregated from new lots and those lots that have passed inspection. The rejected lot shall be 100 percent inspected for those quality characteristics found defective in the sample. Any defectives found shall be removed from the lot. A new sample of parts shall then be randomly selected in accordance with table IX. If one or more defects are found in this second sample the lot shall be rejected and shall not be supplied to the specification.

4.6.1.2.5 Subgroup 3. Subgroup 3 shall be performed on an inspection lot basis on 13 sample units with no failures allowed. T level lots shall be 100 percent inspected. T level capacitors failing this inspection shall be removed from the lot and not supplied on the contract or order.

4.6.1.2.5.1 Rejected non-T level lots. The entire rejected inspection lot shall be segregated from new inspection lots and those inspection lots that have passed inspection. The rejected inspection lot shall be 100 percent inspected for those quality characteristics found defective in the sample. Any defectives found shall be removed from the lot. A new sample of 13 parts shall then be randomly selected. If one or more defects are found in this second sample, the lot shall be rejected and shall not be supplied to the specification.

4.6.1.2.6 Subgroup 4. Subgroup 4 shall be performed on an inspection lot basis on 13 sample units with no failures allowed.

4.6.1.2.6.1 Rejected lots. If there are one or more defects, the inspection lot shall be rejected. The manufacturer may use one or more of the following options to rework the lot.

a. The individual production lot, or lots, from which the defect originated shall be individually subjected to the subgroup 4 test as required in group A inspection, subgroup 4. Production lots that pass the subgroup 4 test are available for shipment. Production lots that fail subgroup 4 may be reworked.

b. The manufacturer shall submit the failed inspection lot to a 100 percent reprocessing. Thirteen additional samples shall then be selected and subjected to the subgroup 4 test with no defects allowed. If the inspection lot fails this test, the inspection lot shall be considered rejected and shall not be furnished against the requirements of this specification.

4.6.1.2.7 Subgroup 5 tests (exponential only). Subgroup 5 tests shall be performed with 13 sample units from the subgroup 3 or subgroup 4 tests, with no failures allowed.

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4.6.1.2.7.1 Rejected lots. The rejected inspection lot shall be segregated from new inspection lots and those inspection lots that have passed inspection. Another 13 samples shall be inspected from the production lot. If the second sample has one or more failures, the entire production lot shall be rejected and shall not be delivered on the contract or order.

4.6.1.2.7.2 Disposition of sample units. Sample units which have been subjected to subgroup 5 shall not be delivered on the contract or order.

4.6.1.2.8 Subgroup 5 (Weibull only) or subgroup 6 (exponential only) (solderability).

4.6.1.2.8.1 Sampling plan. Thirteen samples shall be selected randomly from each inspection lot, as defined in 4.6.1.1.1, and subjected to the solderability test. The manufacturer may use electrical rejects from the subgroup 1 screening tests for all or part of the samples to be used for solderability testing. If there are one or more defects, the lot shall be considered to have failed.

4.6.1.2.8.2 Rejected lots. If there are one or more defects, the inspection lot shall be rejected. The manufacturer may use one or more of the following options to rework the lot:

a. The individual production lot, or lots, from which the defect originated shall be individually subjected to the solderability test as required in 4.6.1.2.8.1. Production lots that pass the solderability test are available for shipment. Production lots that fail the solderability test may be reworked only if they are subjected to solder dip procedure in 4.6.1.2.8.2c.

b. Thirteen samples shall be selected randomly from the individual production lot, or lots, from which the defect originated and subjected to the requirements of J-STD-002. The following details shall apply:

(1) Test: S (surface mount process simulation test).

(2) Coating durability: 2, except preconditioning category C (8 hours ±15 minutes steam conditioning).

(3) Examination after test: The solderable surfaces shall be examined in accordance with J-STD-002, test S.

Production lots that conform to the criteria of J-STD-002, test S, are available for shipment. Production lots that do not conform may be reworked as specified in 4.6.1.2.8.2c.

c. The manufacturer shall submit the failed lot to a 100 percent reprocessing of the termination finish in accordance with 3.7.2.1. Thirteen additional samples shall then be selected and subjected to the solderability test with no defects allowed. If the lot fails this solderability test, the lot shall be considered rejected and shall not be furnished against the requirements of this specification.

4.6.1.2.8.3 Disposition of samples. The solderability test is considered a destructive test and samples subjected to the solderability test shall not be supplied on the contract.

4.6.1.2.9 PPM calculations. The manufacturer shall establish a ppm system in accordance with 3.3.2 for assessing and calculating average outgoing quality of capacitors. A ppm rate combining dc leakage, capacitance, dissipation factor, and ESR shall be assessed for lots that have passed the group A inspection. The manufacturer's ppm system shall also address rectification procedures for lots failing ppm assessment. Data from the rectification process shall not be used to calculate ppm.

4.6.1.3 Periodic group C inspection (ER only). Group C inspection shall consist of the tests specified in table X. Group C inspection shall be made on sample units selected from inspection lots which have passed group A inspection; however, sample units subjected to surge voltage and solderability shall not be used.

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4.6.1.3.1 Sampling plan.

4.6.1.3.1.1 Subgroup 1 through subgroup 5. There shall be 87 (up to 62 for Weibull) sample units of each specification sheet taken from production every 3 months and subdivided as specified for subgroups 1 through 5 as listed in table X and subjected to the tests specified in those subgroups, in the order shown. The maximum and minimum case sizes manufactured during that 3-month period shall be represented in the sample in at least the approximate ratio of production. Styles CWR09, CWR19, and CWR29 and styles CWR06, CWR16, and CWR26 may be combined for group C inspection. On an annual basis, all voltage groups produced, as defined in 4.6.1.1.1, shall be represented. Allowable failures shall be as specified in table X.

4.6.1.3.1.2 Subgroup 6. The number of sample units required by table X shall be selected from production every 12 months. A separate sample shall be selected for each MSL level applicable to the manufacturer. The maximum and minimum case sizes from each specification sheet (see 3.1) manufactured during that 12-month period shall be represented in the sample in at least the approximate ratio of production. Allowable failures shall be as specified in table X.

TABLE X. Group C inspection (ER only).

Inspection	Requirement paragraph	Method paragraph	Number of sample units to be inspected	Number of failures allowed
Subgroup 1 Thermal shock (mounted) 1/	3.15	4.7.12	12	1
Subgroup 2 Resistance to soldering heat Moisture resistance	3.16 3.18	4.7.13 4.7.15	18	
Subgroup 3 Life (2,000 hours at +125°C)	3.22	4.7.19	24	
Subgroup 4 Life (10,000 hours at +85°C) FR (exponential only)	3.22	4.7.19.1	25 minimum per style	See 4.4.4.1
Subgroup 5 Resistance to solvents 2/	3.25	4.7.22	8	0
Subgroup 6 Moisture sensitivity level 2/	3.26	4.7.23	22	3/

1/ If the manufacturer can demonstrate that this test has been performed five consecutive times with zero failures, this test, with the approval of the qualifying activity, can be performed on an annual basis. If the design, material, construction or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency. Group C thermal shock is not required if thermal shock (mounted) was done as part of group A inspection.

2/ If the manufacturer can demonstrate that this test has been performed five consecutive times with zero failures, this test, with the approval of the qualifying activity, can be deleted. The manufacturer, however, shall perform this test every 3 years after the deletion as part of long term design verification. If the design, material, construction or processing of the part is changed or, if there are any quality problems, the qualifying activity may require resumption of the specified testing. Deletion of testing does not relieve the manufacturer from meeting the test requirements in case of dispute.

3/ In accordance with J-STD-020. No failures allowed. If there are failures during testing for a particular MSL, testing may be repeated for a different level.

4.6.1.3.2 Disposition of sample units. Sample units which have been subjected to group C inspection shall not be delivered on the contract or order.

4.6.1.3.3 Noncompliance. If the sample fails to pass group C inspection, the supplier shall take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials and processes, and

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which are considered subject to the same failure. Acceptance of the product shall be discontinued until corrective action, acceptable to the Government, has been taken. After the corrective action has been taken, group C inspection shall be repeated on additional sample units (all inspections or the inspection that the original sample failed, at the option of the Government). Group A inspection may be reinstituted; however, final acceptance shall be withheld until the group C reinspection has shown the corrective action was successful. In the event of failure after reinspection, information concerning the failure and corrective action taken shall be furnished to the cognizant inspection activity and the qualifying activity.

4.7 Methods of inspection and test.

4.7.1 Mounting for testing. Mounting is optional for test environments; however, when specified in the test procedures, the chip capacitors shall be mounted on a suitable substrate (e.g., 96 percent alumina, G30 or FR4 glass epoxy). The substrate material shall be such that it shall not be the cause of, nor contribute to, failure of any test for which it may be used. The capacitors shall be mounted on the substrate as follows:

a. A substrate shall be prepared with metallized surface land areas of proper spacing to permit mounting of chips by soldering the terminations of the chips to the “test card” land areas.

b. Solder paste shall be applied to terminals and substrates as applicable or alternative reflow techniques may be used.

c. The chip shall then be placed across the metallized land areas of the test substrate so as to make contact between chip and substrate land areas.

d. The substrate shall be exposed to +135°C ±1 5°C for a minimum of 1 minute. The substrate shall then be transitioned to +245°C ± 5°C. The substrate shall remain at +245°C ± 5°C until the solder paste melts and reflows forming a homogenous solder bond to the metallized substrate.

e. All excess flux or solder shall be removed.

4.7.2 Radiographic inspection (T level only) (see 3.5). Capacitors shall be tested in accordance with MIL-STD-202-209. 100 percent X-ray required with one side view of the cathode attachment.

4.7.3 Destructive physical analysis (T level only) (see 3.6). Parts shall be examined in accordance with MIL-STD-1580 with the following exceptions:

a. Unless otherwise requested by the acquiring activity, DPA shall be performed by the manufacturer.

b. The manufacturer shall retain the DPA residues/samples for a period of 10 years and shall supply a DPA summary report to the acquiring activity.

c. The DPA summary report shall reflect the criteria specified in 3.6 and shall not match the example reports in MIL-STD-1580.

d. Magnification: 30X.

4.7.4 Visual and mechanical inspection. Capacitors shall be examined to verify that the materials, design, construction, physical dimensions, marking, and workmanship are in accordance with the applicable requirements (see 3.4, 3.7, 3.27, and 3.29).

4.7.5 Voltage aging (exponential only) (see 3.8). Capacitors shall be subjected to a minimum of 100 percent of dc rated voltage for 40 hours, minimum, at a temperature of +85°C ± 5°C. The voltage aging circuit shall have a series resistance of 3.0 ohms, maximum. Capacitors shall then be stabilized at room temperature and the dc leakage, capacitance, dissipation factor, and ESR shall then be measured as specified in 4.7.6, 4.7.7, 4.7.8, and 4.7.14, respectively.

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4.7.6 DC leakage (see 3.9). DC leakage shall be measured using the applicable dc rated voltage (see table I) ± 2 percent at the applicable test temperature (see 3.1), after a maximum electrification period of 5 minutes. A 1,000 ohm resistor shall be placed in series with the capacitor to limit the charging current. A steady source of power, such as a regulated power supply shall be used. Unless otherwise specified (see 3.1), measurement accuracy shall be within ± 2 percent or 0.02 microampere (μA), whichever is greater (see 4.3.3).

If the dc leakage exceeds the specified limit (see 3.1), a second measurement is allowed and shall be considered the official measurement. This second measurement shall be taken immediately following the initial measurement and following a shorting and re-electrification of the capacitor. If the second dc leakage measurement exceeds the limit specified (see 3.1), the part shall be considered a failure. Both the initial and second measurement shall be included in the test report.

T level only: Following Weibull grading, the dc leakage shall be measured at room ambient conditions. A mean and standard deviation shall be calculated for the lot from those capacitors that pass the dc leakage test. Those capacitors with DCL measurements not within +3 standard deviations of the lot mean shall be removed from the lot and shall not be supplied on the contract or order.

4.7.7 Capacitance (see 3.10) Capacitors shall be tested in accordance with MIL-STD-202-305. Unless otherwise specified (see 3.1), the following details shall apply:

a. Test frequency: 120 Hz ±5 Hz.

b. Limit of accuracy: Measurement accuracy shall be within ±2 percent of the reading.

c. Magnitude of polarizing voltage: Maximum dc bias shall be 2.2 volts for all ac measurements. The magnitude of the ac voltage shall be limited to 1.0 volt rms.

4.7.8 Dissipation factor (see 3.11). Unless otherwise specified (see 3.1), the dissipation factor shall be measured at a frequency of 120 Hz ± 5 Hz by means of a polarized capacitance bridge, impedance analyzer, or LCR meter. The instrument shall provide a dial reading of 0.1 percent dissipation factor and a measuring accuracy of ± (2 percent of the measured dissipation factor plus 0.1 percent).

4.7.9 Vibration, high frequency (see 3.12). Capacitors shall be tested in accordance with MIL-STD-202-204. The following details and exceptions shall apply:

a. Mounting of specimens: Capacitors shall be mounted on a substrate as specified in 4.7.1.

b. Electrical-load conditions: During the test, the specified dc rated voltage (see 3.1) shall be applied to the capacitors.

c. Test condition letter: D (20g).

d. Duration and direction of motion: 4 hours in each of two mutually perpendicular directions (total of 8 hours), one parallel and the other perpendicular to the axis.

e. Measurements during vibration: During the last cycle of each plane, electrical measurements shall be made to determine the intermittent open or short circuits. Intermittent contact and arcing shall also be determined. Detecting equipment shall be sufficiently sensitive to detect any interruption with a duration of 0.5 ms or greater.

f. Measurements after vibration: Not applicable

g. Examination after test: Capacitors shall be visually examined for evidence of mechanical damage.

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4.7.10 Reflow conditioning (see 3.13). Reflow conditioning is a screening process to help remove components with weak internal bonds. The following details should not be used as a production assembly guideline. Capacitors shall be conditioned as follows:

a. Mounting of specimens: Not applicable.

b. Measurements before and after conditioning: Not applicable.

c. Number of cycles: 1.

d. Peak temperature: +230°C minimum.

e. Time above +183°C: 45 seconds minimum.

f. Time at +230°C or above: 5 seconds minimum.

g. Ramp rate (+183°C to peak temperature): 1°C per second to 4°C per second.

h. Examination after test: Not applicable.

4.7.11 Thermal shock (unmounted) (see 3.14). Capacitors shall be tested in accordance with MIL-STD-202-107. The following details and exceptions shall apply:

a. Mounting of specimens: Not applicable.

b. Initial measurements: Not applicable.

c. Test condition letter: A (5 cycles), except that in step 3, sample units shall be tested at +125°C +3°C, -0°C. At the option of the manufacturer, step 3 may be performed at +150˚C +3°C, -0°C. At the option of the manufacturer, step 1 may be performed at -65°C +0°C, -5°C.

d. Measurements after thermal shock: Not applicable.

e. Examination after test: Not applicable.

4.7.12 Thermal shock (mounted) (see 3.15). Capacitors shall be tested in accordance with MIL-STD-202-107. The following details and exceptions shall apply:

a. Mounting of specimens: Capacitors shall be mounted on a substrate as specified in 4.7.1.

b. Initial measurements: Capacitance (see 4.7.7).

c. Test condition letter: B, except with 10 cycles.

d. Measurements after thermal shock: DC leakage, capacitance, dissipation factor, and ESR shall be measured as specified in 4.7.6, 4.7.7, 4.7.8, and 4.7.14, respectively.

e. Examination after test: Capacitors shall be visually examined for evidence of harmful corrosion, mechanical damage, and obliteration of marking (if applicable).

4.7.13 Resistance to soldering heat (see 3.16). Capacitors shall be tested in accordance with MIL-STD-202-210. The following details and exception shall apply:

a. Mounting of specimens: Capacitors shall be mounted on a substrate as specified in 4.7.1.

b. Measurements prior to test: DC leakage, capacitance, and dissipation factor shall be measured as specified in 4.7.6, 4.7.7, and 4.7.8, respectively.

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c. Test condition letter: J, except with only one heat cycle.

d. Measurements after test: After completion of the cleaning process and following a minimum 3 hour cooling period, the dc leakage, capacitance, and dissipation factor shall be measured as specified in 4.7.6, 4.7.7, and 4.7.8, respectively.

e. Examination after test: Capacitors shall be visually examined for evidence of mechanical damage.

4.7.14 ESR (see 3.17). The ESR shall be measured in accordance with the following:

a. Test temperature and tolerance: +25°C ± 5°C.

b. Test frequency: 100kHz ± 5 kHz.

c. Limit of accuracy: Measurement accuracy shall be within ±5.0 percent of the reading.

d. Magnitude of polarizing voltage: Unless otherwise specified (see 3.1), the maximum dc bias shall be 2.2 volts for all ac measurements. The magnitude of the ac voltage shall be limited to 0.5 volt rms maximum.

T level only: Following Weibull grading A, the ESR shall be measured at room ambient conditions. A mean and standard deviation shall be calculated for the lot from those capacitors that pass the ESR test. Those capacitors with ESR measurements not within +3 standard deviations of the lot mean shall be removed from the lot and shall not be supplied on the contract or order.

4.7.15 Moisture resistance (see 3.18). Capacitors shall be tested in accordance with MIL-STD-202-106. The following details and exceptions shall apply:

a. Mounting of specimens: Capacitors shall be mounted on a substrate as specified in 4.7.1.

b. Initial measurements: Capacitance and ESR (if applicable, see 3.1) as specified in 4.7.7 and 4.7.14.

c. Number of cycles: 20 continuous cycles except that steps 7a and 7b shall be omitted.

d. Loading voltage: Not applicable.

e. Final measurements: After removal from chamber, capacitors shall be dried for 1 hour at room temperature and, within the next hour, dc leakage, capacitance, dissipation factor, and ESR shall be measured as specified in 4.7.6, 4.7.7, 4.7.8, and 4.7.14, respectively.

f. Examination after test: Capacitors shall be visually examined for evidence of harmful corrosion, mechanical damage, and obliteration of marking (if applicable).

4.7.16 Stability at low and high temperatures (see 3.19). Capacitors shall be dried at +125°C ± 5°C for 30 minutes +4 minutes, -0 minutes, prior to start of test. DC leakage, capacitance, and dissipation factor shall then be measured as specified in 4.7.6, 4.7.7, and 4.7.8, respectively, at each of the temperatures specified in table XI, except that dc leakage measurements at -55°C (step 2) are not required. After the measurements of capacitance and dissipation factor have been made at the -55°C temperature (step 2), rated voltage shall be applied through a 33-ohm resistor for the minimum of 5 minutes. ESR (when applicable, see 3.1) shall be measured at step 1 and step 6 as specified in 4.7.14. The capacitors shall be brought to thermal stability at each temperature.

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TABLE XI. Temperature for stability test.

Step	Test temperature (°C)
1	+25 ± 3
2	-55 +0, -6
3	+25 ± 3
4	+85 +4, -0
5	+125 +4, -0
6	+25 ± 3

4.7.17 Surge voltage (see 3.20). Capacitors shall be tested in accordance with the following:

a. Initial measurements: Capacitance as specified in 4.7.7.

b. Procedure: Capacitors shall be subjected to 1,000 cycles of the applicable surge voltage specified in table I. The ambient temperate during cycling shall be +85°C ± 5°C. Each cycle shall consist of 30 seconds +2 seconds, -0 second surge voltage application followed by 30 seconds +2 seconds, -0 second discharge period. Voltage application shall be made through a resistor of 33 ohms. The tolerance of the resistor shall be ± 5 percent. Each surge voltage cycle shall be performed in such a manner so that the capacitor is shorted terminal to terminal through a copper bar, or an equivalent low resistance at the end of the 30 seconds +2 seconds, -0 second application. An alternate method of shorting the capacitor is to discharge through the same resistance that is utilized for charging.

c. Measurements after test: After the final cycle, the capacitors shall be stabilized at the inspection conditions specified in 4.3, and the dc leakage, capacitance, dissipation factor, and ESR shall be measured as specified in 4.7.6, 4.7.7, 4.7.8, and 4.7.14, respectively.

4.7.18 Surge current (optional) (see 3.21). When specified (see 1.2.1.7), surge current shall be performed on a 100 percent basis either before or after Weibull/voltage aging as indicated in 4.7.18a. Capacitors shall be subjected to ten cycles at each temperature:

a. Temperature: Option A: +25°C ± 5°C; after Weibull grading or voltage aging
Option B: -55°C (-5°C, +0°C) and +85°C ± 5°C; after Weibull grading or voltage aging
Option C: -55°C (-5°C, +0°C) and +85°C ± 5°C; before Weibull grading or voltage aging
Option Z or no option: No test required.

b. An individual test circuit is required for each capacitor under test.

c. Applied voltage: Rated dc voltage ± 2 percent from a power source having a minimum energy storage bank of 20 times the capacitor under test across the output terminals.

d. Charge cycle: 1 second minimum.

e. Discharge cycle: 1 second, minimum, to a voltage below 1 percent of rated voltage.

f. The total dc resistance (excluding the capacitor) including the wiring, fixturing, and output impedance of the regulated power supply to each test position during the charging cycle shall be a maximum of 1.0 ohm.

g. The minimum peak charge/discharge current value shall be:

$$\frac{V_r}{(1 + ESR_{CAP})}$$

Where: At +25°C and +85°C, ESR_{CAP} = ESR as specified (see 3.1)
At -55°C, ESR_{CAP} = 2 x ESR as specified (see 3.1)

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h. Failure criteria: A failure is specified as any capacitor that draws 1 ampere after the appropriate charge time (see 4.7.18i).

i. Charge time:

Charge time (ms)	Capacitance value (µF)
1	≤ 330
10	> 330 and ≤ 3300
100	> 3300

j. Measurements after test: After the final cycle, the dc leakage, capacitance, and dissipation factor shall be measured as specified in 4.7.6, 4.7.7, and 4.7.8, respectively.

4.7.19 Life (see 3.22). Capacitors shall be tested in accordance with MIL-STD-202-108. The following details and exceptions shall apply:

a. Method of mounting: As specified in 4.7.1.

b. Test temperature and tolerance:

(1) For qualification: Capacitors being subjected to the test of group V of table VI shall be at +125°C +4°C, -0°C. Capacitors being subjected to the test of group VI of table VI shall be tested at +85°C +4°C, -0°C.

(2) For group C (2,000 hours proof): Capacitors shall be tested at +125°C +4°C, -0°C.

c. Operating conditions: A minimum of dc rated voltage (see 3.1) or a minimum of derated voltage at +125°C (see table I), as applicable, shall be applied gradually (not to exceed 5 minutes either by a slow buildup of the voltage or through a resistor which shall be shorted out within 5 minutes). Voltage shall be applied continuously, except for measurement periods. The impedance of the voltage source, as seen from the terminals of each capacitor, shall not exceed 3 ohms. Storage batteries or an electronic power supply capable of supplying at least 1 ampere when a capacitor is shorted shall be used.

d. Test condition letter: F (2,000 hours).

e. Measurements during the exposure: DC leakage at the applicable high test temperature shall be measured as specified in 4.7.6 at 0 hour; 240 hours +72, -24 hours; 1,000 hours +72, -24 hours; and 2,000 hours +96, -0 hours.

f. Measurement after exposure: Capacitors shall be returned to the inspection conditions specified in 4.3, and visually examined for evidence of mechanical damage; dc leakage, capacitance, and dissipation factor shall be measured as specified in 4.7.6, 4.7.7, and 4.7.8, respectively.

4.7.19.1 Extended life (exponential only). Capacitors shall be tested as specified in 4.7.19, except that the test temperature shall be +85°C +4°C, -0°C, and the duration of the test shall be 10,000 hours. DC leakage shall be measured as specified in 4.7.6 at +85°C +4°C, -0°C at 0 hour; 240 hours +72, -24 hours; 1,000 hours +72, -24 hours; 2,000 hours +96, -24 hours; and every 2,000 hours +96, -24 hours thereafter until 10,000 hours +120, -0 hour have elapsed. Final measurements shall be as specified in 4.7.19f.

4.7.20 Weibull FRL grading (see 3.23). Capacitors shall be tested in accordance with MIL-STD-202-108. The following details and exceptions shall apply:

a. Distance of the heating source from specimens, in inches: Not applicable.

b. Method of mounting: Capacitors shall be mounted by their terminations.

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c. Test temperature and tolerance: +85°C +4°C, -0°C.

d. Operating conditions: Accelerated dc voltage, +4 percent, -0 percent, as applicable (see table XII), shall be applied gradually (not to exceed 5 minutes by a slow buildup of the voltage). Maximum nominal acceleration factor (see table XII) shall be 20,000:1. Only the capacitors used in 4.7.20e must be fused. Voltage shall be applied continuously, except for failure count periods. The impedance of the voltage source, as seen from the terminals of each capacitor, shall not exceed 1 ohm. An electronic power supply capable of supplying at least 5 amperes when a capacitor is shorted shall be used. A 1 ampere to 2 ampere fuse shall be connected in series with each capacitor. Slow-blow fuses shall not be used. The manufacturer shall be able to demonstrate that all monitored and unmonitored parts receive correct voltage. When separate equipment is used for testing the monitored sample and the unmonitored sample (rest of the lot), the following is required:

(1) Equipment shall be cross calibrated for temperature, voltage, and test duration to ensure equivalent test conditions.

(2) The ramp rate of voltage application at the start of test shall be identical for monitored and unmonitored test groups.

e. Minimum sample size for monitoring at the beginning of test prior to infant mortality period: 300 pieces, or 100 percent, whichever is less. If the sample size is less than 100 percent, the remainder shall be subject to the same accelerated dc voltage for the same amount of time.

f. Duration of test: 40 hours, minimum. The manufacturer shall record the test start and stop times for each lot tested.

Timing:

	Infant mortality period	x_1	x_2	x_3
0	0	0	0	0
	5-15 minutes	See 4.7.20i	40 hours minimum	See 4.7.20i

g. Failure definition: A failure is defined as a blown fuse or equivalent.

h. Capacitors from positions with blown fuses: Capacitors from positions with blown fuses shall be removed and shall not be delivered on the contract. These capacitors may be used for solderability testing or other destructive testing.

i. Failure count during test: The lot size (see 4.6.1.1.2) to be graded is established after removal of gross defectives (infant mortality) (5 minutes - 15 minutes). The first failure count shall be performed at 2 hours ±0.3 hour after the test was started. If there are no failures at time x_1, the manufacturer may use one of the following options:

(1) Complete a minimum of 40 hours and compute the failure from MIL-STD-690, table II FRSP-90, based on the number of failures at time x_2, or;

(2) Extend time x_1 from 2 hours to a maximum of 10 hours. A failure cannot be assumed. If there are still no failures, option 4.7.20i(1) shall be used, or;

(3) Make one restart at a higher voltage (if applicable) to induce a failure at time x_1. The manufacturer shall assume no previous hours. The restart voltage and time shall be recorded. If there are still no failures, option 4.7.20i(1) shall be used. If the sample size is less than 100 percent, the remainder of the lot must be subjected to the final determined restart time and voltage.

The number of blown fuses and the time under test shall be recorded to within ±0.1 hour. Calculate the fraction failed, p_1, at time x_1 (see 6.7.2 equation 4).

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j. Failure count after test: A failure count shall be performed 40 hours minimum after the test was started. The number of blown fuses and the time under test shall be recorded to within ±0.1 hour. Calculate the cumulative fraction failed, p_2, at time x_2 (see 6.7.2 equation 4). If there are no failures at time x_2, the manufacturer may use one of the following options:

(1) Assume one failure and calculate the cumulative fraction failed, p_2, at time x_2 (see 6.7.2 equation 4), or;

(2) Compute the FR from MIL-STD-690, table II FRSP-90, based on the accelerated part hours generated (see 6.7.2 example C), or;

(3) Continue testing. The start time and stop time shall be recorded. If there are still no failures, option (2) may be used.

k. Lot FR: Determine Z (t) from equation 3 (see 6.7.1). If the desired FR has been achieved, the lot may be removed from test.

l. Continuation grading: If the desired FR has not been reached, the lot may be continued on test. The time to reach the FR goal may be estimated from equation 5 (see 6.7.2). If the time calculated to reach the goal FR is excessive, the lot may be discarded in favor of a new lot. If the lot is continued on test, a new FR shall be performed after the extended test. Calculate the cumulative fraction failed, p_3, at time x_3 (see 6.7.2 equation 4). Determine if the FR has been achieved from 4.7.20k.

m. Measurements after exposure: Capacitors shall be removed from the test, stabilized at room ambient conditions (see 4.3.1), and the dc leakage, capacitance, dissipation factor, and ESR shall be measured as specified in 4.7.6, 4.7.7, 4.7.8, and 4.7.14, respectively. For T level capacitors, a mean and standard deviation shall be calculated for the lot from those capacitors that pass the DCL and ESR tests as specified in 4.7.6 and 4.7.14.

TABLE XII. Normal acceleration factors.

Grading stress, V_a / V_r (V_a = accelerated voltage; V_r = rated voltage)	Acceleration factor
1.0000	1.0000
1.1000	6.5355
1.2000	42.7128
1.3000	279.1496
1.4000	1,824.3833
1.5000	11,923.2626
1.5276	20,000.0000

4.7.21 Solderability (see 3.24). Capacitors shall be tested in accordance with MIL-STD-202-208. The following details and exceptions shall apply:

a. Test method: B.

b. Coating durability: 2 as specified in J-STD-002, except preconditioning category C (8 hours ± 15 minutes steam conditioning).

c. Procedure: Mounting surfaces shall be dipped to cover the normal mounting surfaces (see 3.1). After the test, the solderable surfaces shall be examined.

4.7.22 Resistance to solvents (see 3.25). Marked capacitors shall be tested in accordance with MIL-STD-202-215.

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4.7.23 Moisture Sensitivity level (see 3.26). The MSL of the capacitors specified herein shall be determined in accordance with J-STD-020. The following details and exceptions shall apply:

a. Initial electrical test: DC leakage, capacitance, dissipation factor, and ESR shall be measured as specified in 4.7.6, 4.7.7, 4.7.8, and 4.7.14 respectively. Capacitors that fail the initial measurements shall be replaced.

b. Initial inspection: Capacitors shall be inspected at a magnification of 40X for cracks. Capacitors showing external cracks shall be replaced. Acoustic microscopy is not applicable.

c. Bake: In accordance with J-STD-020.

d. Moisture soak: In accordance with J-STD-020.

e. Reflow: In accordance with the tin/lead profile in J-STD-020.

f. Final visual inspection: In accordance with J-STD-020.

g. Final electrical test: DC leakage, capacitance, DF, and ESR shall be measured at room temperature as specified in 4.7.6, 4.7.7, 4.7.8, and 4.7.14 respectively within 72 hours of reflow.

h. Final acoustic microscopy: Not applicable.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the military service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)

6.1 Intended use. Tantalum chip capacitors are intended to be used in thin or thick film hybrid circuits or surface mount applications where microcircuitry is indicated. These capacitors are not hermetic or moisture proof. These capacitors are military unique due to the fact that they must be able to operate satisfactorily in military systems under 20 Gs of high frequency vibration and extreme temperatures (-55°C to +125°C). These capacitors also offer high reliability that is verified under a qualification system. Commercial components are not designed to withstand these military environmental conditions.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, and date of the specification, the applicable specification sheet, and the complete PIN (see 1.2.1).

b. Packaging requirements (see 5.1).

c. Capacitor marking (see 3.27.3, 3.27.4, and 3.27.5)

6.3 Supplying for logistic support. Chip components require use of sophisticated equipment to remove from and install on printed wiring boards. Only requisitioners with in-house or contracted capability to replace surface mounted components should be supplied with chip components, in accordance with their specification.

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6.4 Qualification. With respect to products requiring qualification, awards will be made only for products that are, at the time of award of contract, qualified for inclusion in Qualified Products List whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQP, PO Box 3990, Columbus, OH 43218-3990, or by e-mail to vqp.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4.1 Copies of SD-6. Copies of SD-6, "Provisions Governing Qualification". A copy of this document is available online at https://quicksearch.dla.mil/.

6.5 Standard capacitor types. Equipment designers should refer to MIL-HDBK-198, “Capacitors, Selection and Use of”, for standard capacitor types and selected values chosen from this specification. MIL-HDBK-198 provides a selection of standard capacitors for new equipment design.

6.6 Soldering heat. Caution should be exercised when subjecting these sample units to soldering heat. Preheat and soldering exposure times and temperatures should be held to a minimum.

6.7 Weibull FR level determination. Weibull FR level determination is based on lot-by-lot 100 percent conformance accelerated failure rate life testing.

For example:

2,500	Capacitors have a voltage rating (V_r) of 50 V dc.
40	hours Weibull life test at 65 V dc voltage applied (V_a);
x 279.1496	acceleration factor for V_a/V_r = 1.3000. (see table XII)
27,914,960	Accelerated part hours.

Weibull FRLs are determined from actual lot performance data. Exponential FRL determination starts with several production lots which may be included in the same inspection lot. For example, 4 production lots of 2,500 capacitors having a voltage rating of 50 V dc are offered for inspection in the same inspection lot.

10,000	Capacitors with a voltage rating (V_r) of 50 V dc;
x 40	hours voltage conditioning at 50 V dc minimum.
400,000	Part hours, however, exponential lot voltage conditioning performance data are not used to determine FRLs.
110	Samples are drawn from the inspection lot of 10,000 capacitors;
x 2,000	hours group C life test at 50 V dc applied;
220,000	parts hours, however, data accumulated and used to determine FRLs.
10	Samples selected on completing each group C inspection;
x 9760	hours continuation life testing to 10,000 hours.
97,600	Rated condition part hours for FRL maintenance.

Exponential FRLs are based on the aggregate averages of a few samples drawn from many lots maintained in accordance with MIL-STD-690.

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Time ordered distribution of failures for solid tantalum capacitors is described by the Weibull equation:

Equation 1

$$F(x) = 1 - \exp(-\frac{x^{\beta}}{\alpha})$$

Where: $F(x)$ = Cumulative fraction failed (p) at time x
x = Actual test time
β = Weibull "shape parameter" (beta)
α = Weibull "scale parameter"

This relationship may be plotted on graph paper which is constructed with $\ln x$ as abscissae and $\ln(\ln(1/(1-P)))$ as ordinates. Auxiliary scales allow plotting x and p directly. A straight line is obtained. The slope of this line is β, and the y-intercept is $-\ln \alpha$. Figure 1 illustrates a typical Weibull plot.

At any time x, values for β and p can be obtained and the lot failure rate $Z(x)$ may be calculated from equation 3. A second plot of failure rate versus time may be drafted as indicated on figure 2. The slope of this line is β-1. Acceptable capacitor lots always exhibit decreasing failure rate with respect to time as evidenced by a value of β which is less than unity.

6.7.1 Acceleration factors. In order to provide the equivalent of several thousand hours of testing within a practical time frame, voltage acceleration is employed. It has been determined that the application of voltage in excess of rated voltage produces a higher failure rate than that observed when the devices are operated at the nominal voltage rating. On the Weibull plot, a straight line, parallel to the line representing rated voltage, is obtained. The increased number of failures indicated by the line representing the higher voltage results from increased dielectric stress. The slopes (β) of both lines are essentially the same, but the time (x) required to produce any specified p is reduced as voltage is increased. As a result, acceleration factors may be specified which define the relationship between operation at rated voltage and operation at higher-than-rated voltages. For example, a lot of capacitors having a voltage rating of 50 V dc might be tested at 65 V dc. In this case, the ratio of applied voltage to rated voltage is 1.30, resulting in an acceleration factor (A) of 279. In practical terms, operation of these capacitors for 1 hour at 65 V dc is equivalent to operation at 50 V dc for 279 hours. This relationship may be mathematically represented as:

Equation 2

$$Z(t) = Z(Ax) = \frac{\beta}{\alpha} x^{\beta-1} * \frac{1}{A}$$

In conjunction with equation 1, this function may be restated as:

Equation 3

$$Z(t) = F = \frac{-\beta \ln(1-p)}{x} * \frac{10^5}{A}$$

The 10^5 factor allows for expression of $Z(t)$ in terms of percent per 1,000 hours when x denotes hours. Table XII illustrates a range of acceleration factors normally used for Weibull FR determination.

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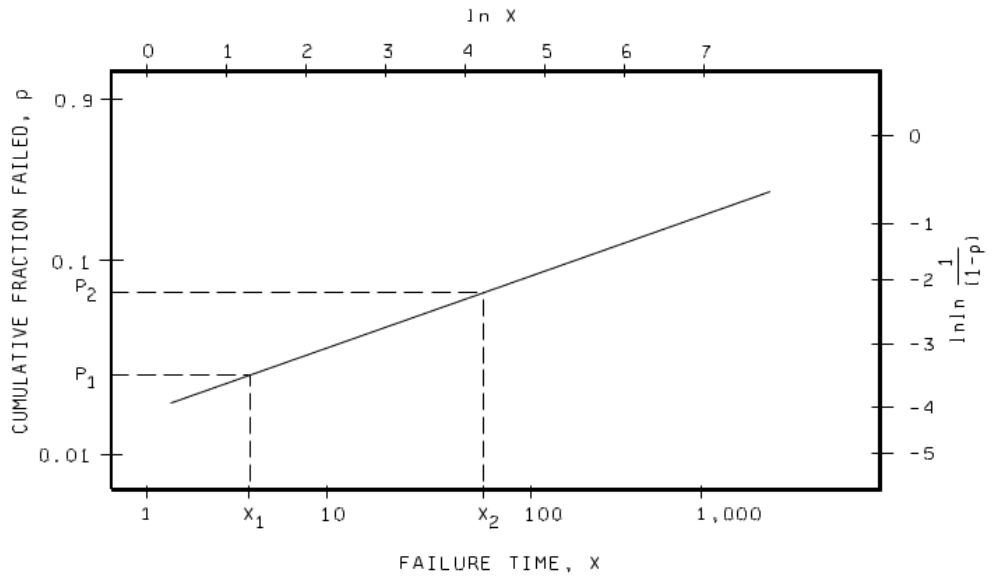

FIGURE 1. Typical Weibull plot.

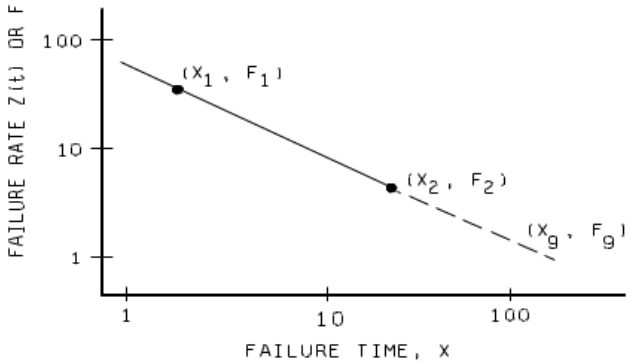

FIGURE 2. Failure rate versus time.

6.7.2 Grading calculations. On the basis of failure counts at x_1 and x_2 as specified in 4.7.17, the slope between these points is calculated as follows:

Equation 4

$$\beta = \frac{\ln(\ln(\frac{1}{(1-p_2)})) - \ln(\ln(\frac{1}{(1-p_1)}))}{\ln x_2 - \ln x_1}$$

The failure rate at time x_2 is then determined from equation 3:

$$F_2 = \frac{-\beta \ln (1-p_2) 10^5}{x_2 A}$$

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If additional grading time is required to reach the desired failure rate, the required time x_g may be determined as follows:

Equation 5

$$\ln x_g = \frac{\ln F_g - \ln F_2}{\beta - 1} + \ln x_2$$

Equation 6

$$A = 7.03412025 * 10^{-9} e^{(18.77249321 * \frac{V_a}{V_r})}$$

Where: A = Acceleration factor
e = Natural logarithm base
V_a = Accelerated voltage
V_r = Rated voltage
$\frac{V_a}{V_r}$ = Stress level

Examples:

a. 880 capacitors tested at a grading stress level of 1.2300 (75.0139 acceleration factor) for 40 hours resulted in zero failures.

880 (75.0139 x 40) = 2,640,489 hours
C = 0
FR = B level (MIL-STD-690, FRSP-90)

b. 1,350 capacitors tested at a grading stress level of 1.3300 (490.2535 acceleration factor) for 40 hours resulted in zero failures.

1,350 (490.2535 x 40) = 26,473,689 hours
C = 0
FR = C level (MIL-STD-690, FRSP-90)

c. 400 capacitors tested at a grading stress level of 1.4000 (1824.3833 acceleration factor) for 40 hours resulted in 1 failure at x_1; no additional failures at x_2.

400 (1824.3833 x 40) = 29,190,133 hours
C = 1
FR = B level (MIL-STD-690, FRSP-90)

d. 100 capacitors tested at a grading stress level of 1.4000 (1824.3833 acceleration factor) for 41 hours resulted in 3 failures at x_1; no additional failures at x_2.

100 (1824.3833 x 41) = 7,479,971.530 hours
C = 3
FR = B level (MIL-STD-690, FRSP-90)

Or, assume one additional failure at x_2.

$$\beta = \frac{\ln(\ln(\frac{1}{(1-p_2)})) - \ln(\ln(\frac{1}{(1-p_1)}))}{\ln x_2 - \ln x_1}$$

Where: x_1 = 2 hours
x_2 = 41 hours
p_1 = .03

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p_2 = .04
A = 1824.3833

$$\beta = \frac{\ln(\ln(\frac{1}{(1-.04)})) - \ln(\ln(\frac{1}{(1-.03)}))}{\ln 41 - \ln 2}$$

$$= \frac{\ln(\ln 1.041666) - \ln(\ln 1.030928)}{3.713572 - 0.693147}$$

$$= \frac{-3.1985499 - (-3.4913617)}{3.02042425}$$

$$= \frac{0.2928118}{3.02042425} = 0.096944$$

$$FRL = \frac{-\beta \ln(1-p_2)\,10^5}{x_2 A} = \frac{-0.096944 \ln(.96)\,10^5}{41(1824.3833)}$$

$$= \frac{-0.096944(-0.040822)10^5}{74799.72} = 0.000000053 * 10^5$$

$$= \frac{0.0053\%}{1{,}000 hours}$$

To compute hours needed to verify 0.001 percent per 1,000 hours FRL:

$$\ln x_g = \frac{\ln F_g - \ln F_2}{\beta - 1} + \ln x_2$$

Where: x_2 = hours at point 2
x_g = hours to test (goal)
F_2 = observed FRL at x2
F_g = Failure rate level (goal)

$$\ln x_g = \frac{\ln(0.001) - \ln(0.0053)}{-0.903056} + \ln 41$$

$$= \frac{-6.9077553 - (-5.2400485)}{-0.903056} + 3.713572$$

$$= \frac{-1.6677068}{-0.903056} + 3.713572$$

$$= 1.8467369 + 3.713572$$

$$= 5.5603089$$

$$x_g = 259.90\ hours$$

6.7.3 Weibull grading method. After determining the lot FR in accordance with 4.7.20, the balance of the lot (when applicable) should be tested to the same voltage acceleration conditions as the monitored test samples. These sample units will then be subjected to the 100-percent electrical tests shown in table VIII.

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6.8 Termination finish code conversion. Termination finish codes in this revision (see 1.2.1.3) replace those from earlier revisions in the following manner:

TABLE XIII. Termination finish code.

Termination finish codes	Replace earlier revision termination finish codes
B (gold plated)	B (gold)
C (hot solder dipped) H (solder plated) K (solder fused)	A (solder-coated nickel) C (solder-coated gold) D (solder-coated alloy 725) F (solder-coated alloy 752)

6.9 Subject term (key word) listing.

Dissipation factor
Statistical process control (SPC)
Weibull

6.10 Tin whisker growth. The use of alloys with a tin content greater than 97 percent, by mass, may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacturer and can develop under typical operating conditions, on products that use such materials. Conformal coatings applied over top of a whisker prone surface will not prevent the formation of tin whiskers. Alloys of 3 percent lead, by mass, have been shown to inhibit the growth of tin whiskers. For additional information on this matter, refer to ASTM-B545 (Standard Specification for Electrodeposited Coatings of Tin).

6.11 Moisture and handling sensitivity. Capacitors qualified to this specification may be sensitive to moisture induced stress if exposed to humidity for extended periods of time (see 6.11.1 and 6.11.2). J-STD-020 (Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices) provides a procedure to identify the moisture sensitivity level rating for non-hermetic surface mount devices so that they can be properly packaged, stored, and handled. The MSL ratings for the capacitors qualified to this specification are based on the tin/lead reflow profile specified in J-STD-020. If humidity exposure exceeds J-STD-020 limits, users may consult J-STD-033 (Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices) for general bake out and handling procedures; however, individual capacitor manufacturers may have more specific recommendations, especially for those capacitors packaged in tape and reel. Passing the criteria specified in J-STD-020 is not sufficient by itself to provide assurance of long-term reliability.

6.11.1 Solder reflow. Capacitors qualified to this specification may become susceptible to damage during solder reflow due to moisture absorption (see 6.11). Vapor pressure of moisture inside a non-hermetic package increases greatly when exposed to the high temperature of solder reflow, potentially resulting in internal cracking or damage to the capacitor. In the most severe cases, the internal pressure can cause external package cracks, commonly referred to as the “popcorn” phenomenon.

6.11.2 ESR degradation. The ESR of capacitors qualified to this specification may increase due to moisture absorption (see 6.11). Moisture can penetrate the non-hermetic package and be absorbed by the cathode elements. This absorption can reduce conductivity of the contact points which increases the resistance. This process may be reversible by eliminating the moisture within the capacitor by performing a bake out drying procedure.

6.12 Changes from previous issue. The margins of this specification are marked with vertical lines to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

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APPENDIX A

PROCEDURES FOR QUALIFICATION INSPECTION

A.1 SCOPE

A.1.1 Scope. This appendix details the procedures for submission of samples for qualification inspection of capacitors covered by this specification. The procedures for extending qualification of the required sample to other capacitors covered by this specification are also obtained herein. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 SUBMISSION

A.3.1 Sample.

A.3.1.1 Single-style submission. A sample of the size required in table VI, of the highest capacitance value in each voltage rating in each style for which qualification is sought, shall be submitted.

A.3.1.2 Combined-voltage submission (exponential). Samples shall be submitted in accordance with table A-I for each style for which qualification is sought. Each voltage group (see 4.6.1.1.1), 4 - 20 volts and 25 to 50 volts are qualified separately. The break down is the highest capacitance value in the smallest and largest case size, and lowest voltage and highest voltage.

TABLE A-I. Combined-voltage submission.

Style	PIN 1/	Number of sample units 2/	Rated voltage	Voltage group
CWR06 and CWR09	CWR0-C-225-M	45	4	I
	CWR0-C-107-M	45	4	I
	CWR0-J-474-M	45	20	I
	CWR0-J-226-M	45	20	I
	CWR0-K-334-M	45	25	II
	CWR0-K-156-M	45	25	II
	CWR0-N-154-M	45	50	II
	CWR0-N-475-M	45	50	II
CWR11	CWR11D-335-M	45	6	I
	CWR11D-686-M	45	6	I
	CWR11J-105-M	45	20	I
	CWR11J-226-M	45	20	I
	CWR11K-474-M	45	25	II
	CWR11K-156-M	45	25	II
	CWR11N-104-M	45	50	II
	CWR11N-475-M	45	50	II
CWR15	CWR15CK685-MLC	45	4	I
	CWR15CK686-MAZ	45	4	I
	CWR15FK225-MLZ	45	10	I
	CWR15FK156-MAZ	45	10	I

See footnotes at end of table.

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APPENDIX A

TABLE A-I. Combined-voltage submission.

Style	PIN 1/	Number of sample units 2/	Rated voltage	Voltage group
CWR16	CWR16C-335-MAZ	45	4	I
	CWR16C-337-MHZ	45	4	I
	CWR16J-684-MAZ	45	20	I
	CWR16J-476-MHZ	45	20	I
	CWR16K-474-MAZ	45	25	II
	CWR16K-336-MHZ	45	25	II
	CWR16M-334-MAZ	45	35	II
	CWR16M-156-MHZ	45	35	II
CWR19	CWR19C-685-MAZ	45	4	I
	CWR19C-337-MHZ	45	4	I
	CWR19J-105-MAZ	45	20	I
	CWR19J-476-MXZ	45	20	I
	CWR19K-474-MAZ	45	25	II
	CWR19K-336-MXZ	45	25	II
	CWR19M-334-MAZ	45	35	II
	CWR19M-156-MXZ	45	35	II
CWR26	CWR26C-685-MAZ	45	4	I
	CWR26C-337-MHZ	45	4	I
	CWR26J-105-MAZ	45	20	I
	CWR26J-476-MHZ	45	20	I
	CWR26K-474-MAZ	45	25	II
	CWR26K-336-MHZ	45	25	II
	CWR26N-154-MAZ	45	50	II
	CWR26N-475-MHZ	45	50	II
CWR29	CWR29C-685-MAZ	45	4	I
	CWR29C-337-MHZ	45	4	I
	CWR29J-105-MAZ	45	20	I
	CWR29J-476-MXZ	45	20	I
	CWR29K-474-MAZ	45	25	II
	CWR29K-336-MXZ	45	25	II
	CWR29N-154-MAZ	45	50	II
	CWR29N-475-MHZ	45	50	II

1/ The complete PIN shall include additional symbols to indicate style, where applicable, termination finish, and capacitance tolerance.
2/ 300 sample units for Weibull (see A.3.1.3).

A.3.1.3 Combined-voltage submission (Weibull). Three hundred sample units of the highest capacitance value of the lowest voltage and 300 sample units of the highest capacitance value of the highest voltage in each voltage group for each style for which qualification is sought shall be submitted (see table A-I). Weibull FRL grading shall be performed in accordance with 3.23 and 4.7.20 instead of voltage aging (exponential only) in group I of table VI. DC leakage, capacitance, dissipation factor, and ESR shall be performed only once. All other exponential tests in table VI shall not apply.

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APPENDIX A

A.4 EXTENT OF QUALIFICATION

A.4.1 Single-style submission. Capacitance-range qualification will be restricted to values equal to or less than the capacitance value submitted. Voltage rating qualification shall be restricted to those submitted.

A.4.2 Combined voltage submission. Capacitance range qualification will be restricted to values equal to or less than the capacitance value submitted. Voltage rating qualification shall be restricted to those submitted.

A.4.3 Weibull qualification via similarity. Capacitance range qualification will be restricted to values equal to or less than the capacitance value submitted. Voltage rating qualification shall be restricted to those submitted.

A.4.4 Non-ER capacitors (A level). Qualification of the A (non-ER) level is predicated upon meeting the qualification requirements for the established reliability FRL B.

NOTE: Since the non-ER (A level) is the ER design without the mandatory conformance inspection and FRL assessment, the product is still expected to meet the environmental qualification type requirements (e.g., moisture resistance, or thermal shock.).

A.4.5 Termination finishes. Termination qualification will be restricted to that submitted, except qualification of termination finish C or H will extend qualification to termination finish K.

A.4.6 Surge current option. Surge current qualification will extend in accordance with the following:

Qualification of surge current option:	Will qualify option:
C	A, B, Z (or no code)
B	A, Z (or no code)
A	Z (or no code)

A.4.7 Styles CWR09, CWR19 and CWR29. Qualifying to CWR29 will extend qualification to styles CWR09 and CWR19.

A.4.8 Styles CWR06, CWR16, and CWR26. Qualifying to CWR26 will extend qualification to styles CWR06 and CWR16.

A.4.9 T level. T level qualification requires that the manufacturer is qualified to weibull grade C or D of the equivalent part.

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Army - CR
Navy - EC
Air Force - 85
DLA - CC

Preparing activity:
DLA - CC

(Project 5910-2024-043)

Review activities:
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