

The documentation and process conversion measures necessary to comply with this document shall be completed by 3 February 2005.

INCH-POUND

MIL-PRF-19500/544F
 3 November 2004
 SUPERSEDING
 MIL-PRF-19500/544E
 13 March 2003

* PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, POWER,
 TYPES 2N5152, 2N5154, 2N5152L, 2N5154L, 2N5152U3, 2N5154U3
 JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, power transistors for use in high-speed power-switching applications. Four levels of product assurance are provided for each encapsulated device type and two levels of product assurance are provided for each unencapsulated device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. Figure 1 (similar to TO-5 and TO-39), figures 2, 3, and 4 (die dimensions), and figure 5 (U3).

* 1.3 Maximum ratings unless otherwise specified $T_A = +25^\circ\text{C}$.

Type	P_T $T_A = +25^\circ\text{C}$	P_T $T_C = +25^\circ\text{C}$	P_T $T_{SP} = +25^\circ\text{C}$	$R_{\theta JC}$	$R_{\theta JA}$	$R_{\theta JSP}$	V_{CBO}	V_{CEO}	V_{EBO}	I_C	I_C (1)	Reverse pulse energy (2)	T_{stg} and T_J
	<u>W</u>	<u>W</u>	<u>W</u>	$^\circ\text{C/W}$ (4)	$^\circ\text{C/W}$ (4)	$^\circ\text{C/W}$ (4)	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>mJ</u>	<u>$^\circ\text{C}$</u>
2N5152	1 (3)	15 (3)	N/A	10	175		100	80	5.5	2	10	15	-65 to +200
2N5152L	1 (3)	15 (3)	N/A	10	175		100	80	5.5	2	10	15	
2N5154	1 (3)	15 (3)	N/A				100	80	5.5	2	10	15	
2N5154L	1 (3)	15 (3)	N/A				100	80	5.5	2	10	15	
2N5152U3	N/A	100 (3)	1 (3)	1.7	N/A	170	100	80	5.5	2	10	15	
2N5154U3	N/A	100 (3)	1 (3)	1.7	N/A	170	100	80	5.5	2	10	15	

- (1) This value applies for $P_w \leq 8.3$ ms, duty cycle ≤ 1 percent.
- (2) This rating is based on the capability of the transistors to operate safely in the unclamped inductive load energy test circuit, see subgroup 5 of the group E inspection table.
- (3) For derating, see figures 6, 7, 8, and 9.
- (4) For thermal impedance curves, see figures 10, 11, and 12

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dsc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database. <http://assist.daps.dla.mil/quicksearch> or <http://assist.daps.dla.mil>

1.4 Primary electrical characteristics at $T_C = +25^\circ\text{C}$.

Limits	h_{FE2} (1) $V_{CE} = 5\text{ V}$ $I_C = 2.5\text{ A}$		$ h_{fe} $ $V_{CE} = 5\text{ V}$ $I_C = 500\text{ mA dc}$		$V_{BE(sat)2}$ (1) $I_C = 5\text{ A dc}$ $I_B = 500\text{ mA dc}$	$V_{CE(sat)2}$ (1) $I_C = 5\text{ A dc}$ $I_B = 500\text{ mA dc}$	C_{obo} $V_{CB} = 10\text{ V dc}$ $I_E = 0$ $f = 1\text{ MHz}$
	2N5152 (2)	2N5154 (2)	2N5152 (2)	2N5154 (2)			
Min	30	70	6	7	<u>Vdc</u>	<u>Vdc</u>	<u>pF</u>
Max (TO-5, TO-39)	90	200			2.2	1.5	250
Max (U3)	90	200			2.2	1.5	250

(1) Pulsed see 4.5.1.

(2) The limits specified apply to all package outlines unless otherwise stated.

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

* DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

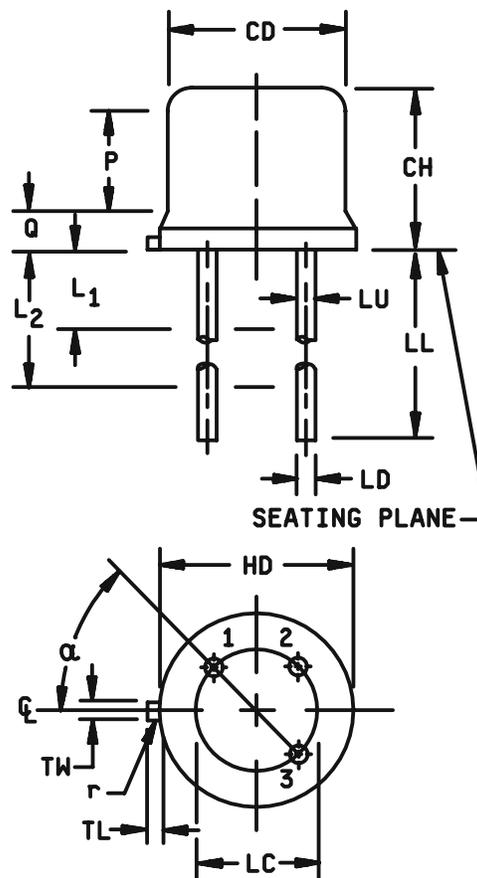
* DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

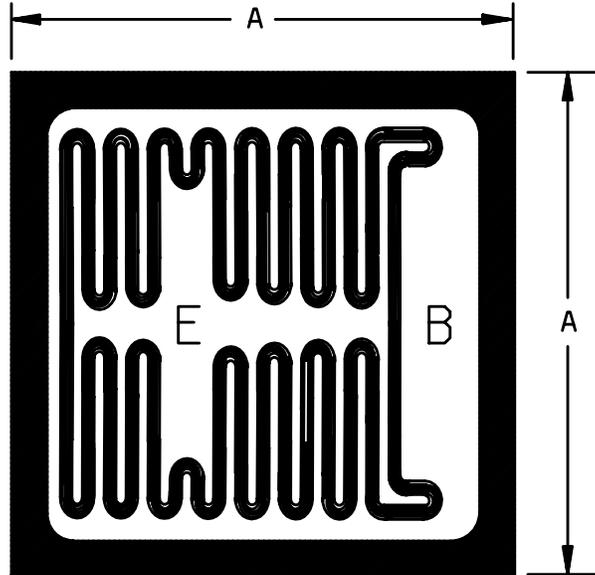
Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	6
CH	.240	.260	6.12	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		7
LD	.016	.019	0.41	0.48	8,9
LL	See note 14				
LU	.016	.019	0.41	0.48	8,9
L ₁		.050		1.27	8,9
L ₂	.250		6.35		8,9
P	.100		2.54		7
Q		.030		0.76	5
TL	.029	.045	0.74	1.14	3,4
TW	.028	.034	0.71	0.86	3
r		.010		0.25	10
α	45° TP		45° TP		7
	1, 2, 10, 12, 13, 14				



NOTES:

- Dimensions are in inches.
- Millimeters are given for general information only.
- Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
- Dimension TL measured from maximum HD.
- Body contour optional within zone defined by HD, CD, and Q.
- CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
- Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by gauging procedure.
- Dimension LU applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum. Diameter is uncontrolled in and beyond LL minimum.
- All three leads.
- The collector shall be internally connected to the case.
- Dimension r (radius) applies to both inside corners of tab.
- In accordance with ASME Y14.5M, diameters are equivalent to Φ x symbology.
- Lead 1 = emitter, lead 2 = base, lead 3 = collector.
- For L-suffix or non-S-suffix devices (T0-5), dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max. For S-suffix types (T0-39), dimension LL = .5 inch (12.70 mm) min. and .750 inch (19.05 mm) max.

FIGURE 1. Physical dimensions (similar to TO-5 and TO-39).

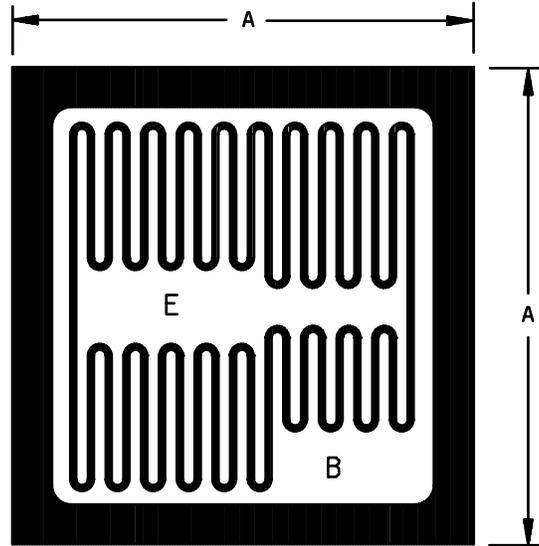


Dimensions				
LTR	Inches		Millimeters	
	Min	Max	Min	Max
A	.117	.127	2.97	3.23

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is $\pm .005$ (0.13 mm).
4. The physical characteristics of the die are;
 - Thickness: .008 (0.20 mm) to .012 (0.30 mm), tolerance is $\pm .005$ (0.13 mm).
 - Top metal: Aluminum, 40,000 Å minimum, 50,000 Å nominal.
 - Back metal: Gold 2,500 Å minimum, 3,000 Å nominal.
 - Back side: Collector.
 - Bonding pad:
 - B = .015 (0.38 mm) x .0072 (0.183).
 - E = .015 (0.38 mm) x .0060 (0.152).

FIGURE 2. JANHC and JANKC (A-version) die dimensions.

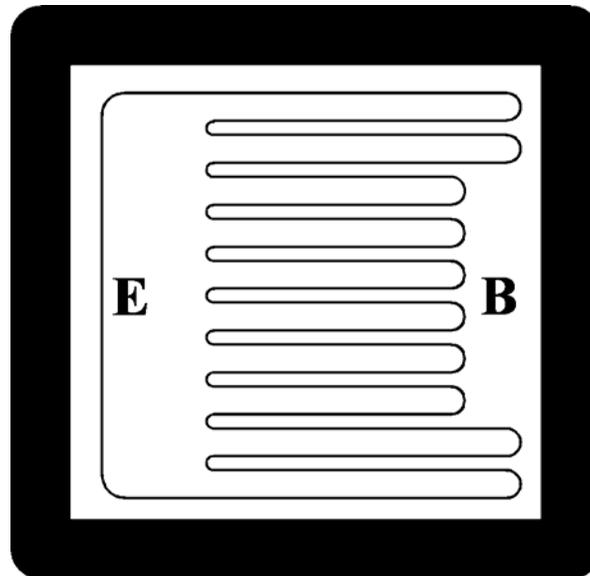


Dimensions				
LTR	Inches		Millimeters	
	Min	Max	Min	Max
A	.095	.105	2.41	2.66

NOTES:

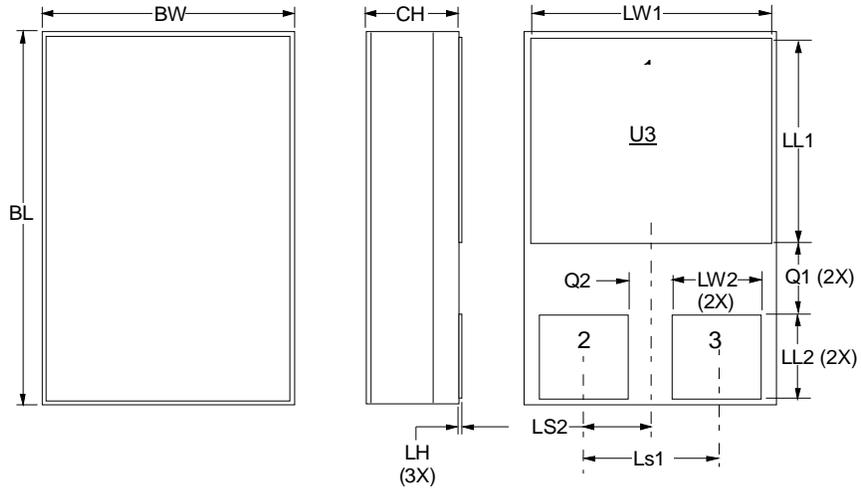
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is ± 0.005 (0.13 mm).
4. The physical characteristics of the die are:
 Thickness: .0078 (0.198 mm) nominal, tolerance is ± 0.005 (0.13 mm).
 Top metal: Aluminum, 25,000 Å minimum, 33,000 Å nominal.
 Back metal: Gold 1,500 Å minimum, 2,500 Å nominal.
 Back side: Collector.
 Bonding pad: .012 (0.305 mm) min. x .030 (0.761 mm) minimum.

FIGURE 3. JANHNC and JANKC (B-version) die dimensions.



- | | |
|------------------|---|
| 1. Die size | .120 inches (3.05 mm) x .120 inches (3.05 mm) \pm .002 inches (\pm 0.05 mm). |
| 2. Die thickness | .010 inches (0.25 mm) \pm .0015 inches nominal (\pm 0.04 mm). |
| 3. Top metal | Aluminum, 30,000Å minimum, 35,000Å nominal. |
| 4. Back metal | A. Al/Ti/Ni/Ag 12kÅ/3kÅ/7kÅ/7kÅ minimal, 15kÅ/5kÅ/10kÅ/10kÅ nominal.
B. Gold 2500Å minimum, 3000Å nominal. |
| 5. Backside | Collector |
| 6. Bonding pad | B = .052 x .012 inches (1.32 mm x 0.30 mm).
E = .084 x .012 inches (2.13 mm x 0.30 mm). |

FIGURE 4. JANHC and JANKC (C-version) die dimensions.



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH	.1085	.1205	2.76	3.06
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.41
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	
TERM 1	Collector			
TERM 2	Base			
TERM 3	Emitter			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

* FIGURE 5. Physical dimensions and configuration for surface mount (U3).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and figure 1 (similar to TO-5 and TO-39), and figures 2, 3, and 4 (die dimensions) for JANHC and JANKC, and figure 5 (U3).

3.4.1 Current density. Current density of internal conductors shall be as specified in MIL-PRF-19500.

3.4.2 Lead finish. Lead finish shall be solderable as defined in MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.6 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I herein.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I, II, and III).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

* 4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500)	Measurement	
	JANS levels	JANTX and JANTXV levels
1a 1b	Not required Required	Not required Required for JANTXV only
2	Optional	Optional
3a 3b 3c	Required Not applicable Thermal impedance, method 3131 of MIL-STD-750. See 4.3.3.	Required Not applicable Thermal Impedance, method 3131 of MIL-STD-750. See 4.3.3.
4	Required	Optional
5	Required	Not applicable
7a and 7b	Optional	Optional
8	Required	Not required
9	I_{CES1} and h_{FE2}	Not applicable
10	48 hours minimum	48 hours minimum
11	I_{CES1} and h_{FE2} ; ΔI_{CES1} = 100 percent of initial value or 100 nA dc, whichever is greater. Δh_{FE2} = \pm 20 percent.	I_{CES1} and h_{FE2}
12	See 4.3.2	See 4.3.2
13	Subgroup 2 and 3 of table I herein; ΔI_{CES1} = 100 percent of initial value or 100 nA dc, whichever is greater. Δh_{FE2} = \pm 20 percent.	Subgroup 2 of table I herein; ΔI_{CES1} = 100 percent of initial value or 100 nA dc, whichever is greater. Δh_{FE2} = \pm 20 percent.
14a and 14b	Required	Required
15	Required	Not required
16	Required	Not required

4.3.1 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500, "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.2 Power burn-in conditions. Power burn-in conditions are as follows: $V_{CB} = 10 - 30$ V dc. Power shall be applied to the device to achieve $T_J = +175^\circ\text{C}$ minimum using a minimum $P_D = 75$ percent of P_T maximum, T_A ambient rated as defined in 1.3 herein.

* 4.3.3 Thermal impedance ($Z_{\theta JX}$ measurements). The $Z_{\theta JX}$ measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{MD} , (and V_C where appropriate). The $Z_{\theta JX}$ limit used in screen 3c of 4.3 shall comply with the thermal impedance graph in figures 10, 11, and 12 (less than or equal to the curve value at the same t_H time) and/or shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.4 Conformance inspection. Conformance inspection shall be as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table VIa (JANS) and table VIb (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and 4.4.2.1 and 4.4.2.2 herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein. Delta measurements shall be in accordance with table III herein.

4.4.2.1 Group B inspection (JANS) table VIa of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B4	1037	$V_{CB} = 10$ Vdc.
B5	1027	<p>$V_{CB} = 10$ V dc; $P_D \geq 100$ percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.)</p> <p>Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table VIa, adjust T_A or P_D to achieve $T_J = +275^\circ\text{C}$ minimum.</p> <p>Option 2: 216 hours minimum, sample size = 45, $c = 0$; adjust T_A or P_D to achieve a $T_J = +225^\circ\text{C}$ minimum.</p>
B6	3131	See 4.5.2.

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a group B failure, the manufacturer may pull a new sample at double size from either the failed assembly lot or from another assembly lot from the same wafer lot. If the new assembly lot option is exercised, the failed assembly lot shall be scrapped.

<u>Step</u>	<u>Method</u>	<u>Conditions</u>
1	1027	Steady-state life: 1,000 hours minimum, $V_{CB} = 10$ V dc, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75$ percent of maximum rated P_T as defined in 1.3. $n = 45$ devices, $c = 0$. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, $T_A = +150^\circ\text{C}$, $V_{CB} = 80$ percent of rated voltage, 48 hours minimum. $n = 45$ devices, $c = 0$.
3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$. $n = 22$, $c = 0$.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. See MIL-PRF-19500.
- b. Must be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table VII of MIL-PRF-19500, and 4.4.3.1 (JANS), and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and table III herein.

4.4.3.1 Group C inspection, table VII (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E (not applicable to U3 devices).
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and applied thermal impedance curves.
C6	1027	1,000 hours, $V_{CB} = 10$ V dc, power and ambient temperature shall be applied to the device to achieve $T_J = +150^\circ\text{C}$ minimum, and minimum power dissipation of 75 percent of max rated P_T (see 1.3 herein); $n = 45$, $c = 0$. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

4.4.3.2 Group C inspection, table VII (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E (not applicable to U3 devices).
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3).
C6	1037	Not applicable.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table IX of MIL-PRF-19500 and as specified herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein. Delta measurements shall be in accordance with table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

* 4.5.2 Thermal resistance. Thermal resistance measurements shall be conducted in accordance with method 3131 of MIL-STD-750. The following details shall apply:

- a. Collector current magnitude during power application shall be 500 mA dc minimum.
- b. Collector to emitter voltage magnitude shall be 10 V dc.
- c. Reference temperature measuring point shall be the case.
- d. Reference temperature measuring point shall be within the range $+25^{\circ}\text{C} \leq T_R \leq +35^{\circ}\text{C}$. The chosen reference temperature shall be recorded before the test is started.
- e. Mounting arrangement shall be with heat sink to case.
- f. Maximum limit of $R_{\theta JC}$ shall be 10.0°C/W for TO-5 and TO-39 and 1.7°C/W for U3.

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TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
Visual and mechanical examination <u>3/</u>	2071	n = 45 devices, c = 0				
Solderability <u>3/ 4/</u>	2026	n = 15 leads, c = 0				
Resistance to solvents <u>3/ 4/ 5/</u>	1022	n = 15 devices, c = 0				
Temp cycling <u>3/ 4/</u>	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Electrical measurements <u>4/</u>		Table I, subgroup 2				
Hermetic seal <u>4/ 6/</u>	1071	n = 22 devices, c = 0				
Fine leak Gross leak						
Bond strength <u>3/ 4/</u>	2037	Precondition $T_A = +250^\circ\text{C}$ at t = 24 hours or $T_A = +300^\circ\text{C}$ at t = 2 hours n = 11 wires, c = 0				
<u>Subgroup 2</u>						
Thermal impedance	3131	See 4.3.3	$Z_{\theta JX}$			$^\circ\text{C/W}$
Breakdown voltage, collector to emitter	3011	Bias condition D, $I_C = 100$ mA dc; $I_B = 0$, pulsed (see 4.5.1)	$V_{(BR)CEO}$	80		V dc
Collector to emitter cutoff current	3041	Bias condition C, $V_{CE} = 60$ V dc; $V_{BE} = 0$	I_{CES1}		1.0	$\mu\text{A dc}$
Collector to emitter cutoff current	3041	Bias condition C, $V_{CE} = 100$ V dc; $V_{BE} = 0$	I_{CES2}		1.0	mA dc
Collector to emitter cutoff current	3041	Bias condition D, $V_{CE} = 40$ V dc, $I_B = 0$	I_{CEO}		50	$\mu\text{A dc}$

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued.						
Emitter to base cutoff current	3061	Bias condition D, $V_{EB} = 4$ V dc, $I_C = 0$	I_{EBO1}		1.0	μ A dc
Emitter to base cutoff current	3061	Bias condition D, $V_{EB} = 5.5$ V dc, $I_C = 0$	I_{EBO2}		1.0	mA dc
Forward current transfer ratio	3076	$V_{CE} = 5$ V dc, $I_C = 50$ mA dc	h_{FE1}	20 50		
2N5152, L, and U3 2/ 2N5154, L, and U3						
Forward current transfer ratio	3076	$V_{CE} = 5$ V dc, $I_C = 2.5$ A dc, pulsed (see 4.5.1)	h_{FE2}	30 70	90 200	
2N5152, L, and U3 2/ 2N5154, L, and U3						
Forward current transfer ratio	3076	$V_{CE} = 5$ V dc, $I_C = 5$ A dc, pulsed (see 4.5.1)	h_{FE3}	20 40		
2N5152, L, and U3 2/ 2N5154, L, and U3						
Base-emitter voltage (nonsaturated)	3066	Test condition B, $V_{CE} = 5$ V dc, $I_C = 2.5$ A dc, pulsed (see 4.5.1)	V_{BE}		1.45	V dc
Base-emitter saturation voltage	3066	Test condition A, $I_C = 2.5$ A dc, $I_B = 250$ mA dc, pulsed (see 4.5.1)	$V_{BE(sat)1}$		1.45	V dc
Base-emitter saturation voltage	3066	Test condition A, $I_C = 5$ A dc, $I_B = 500$ mA dc, pulsed (see 4.5.1)	$V_{BE(sat)2}$		2.2	V dc
Collector-emitter saturation voltage	3071	$I_C = 2.5$ A dc, $I_B = 250$ mA dc, pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.75	V dc
Collector-emitter saturation voltage	3071	$I_C = 5$ A dc, $I_B = 500$ mA dc, pulsed (see 4.5.1)	$V_{CE(sat)2}$		1.5	V dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u>						
High temperature operation:		$T_C = +150^\circ\text{C}$				
Collector to emitter cutoff current	3041	Bias condition A, $V_{CE} = 60\text{ V dc}$, $V_{BE} = -2\text{ V dc}$	I_{CEX}		25	$\mu\text{A dc}$
Low temperature operation		$T_C = -55^\circ\text{C}$				
Forward - current transfer ratio 2N5152, L, and U3 2/ 2N5154, L, and U3	3076	$V_{CE} = 5\text{ V dc}$, $I_C = 2.5\text{ A dc}$, pulsed (see 4.5.1)	h_{FE4}	15 25		
<u>Subgroup 4</u>						
Common-emitter, small-signal, short-circuit, forward-current transfer ratio 2N5152, L, and U3 2/ 2N5154, L, and U3	3206	$V_{CE} = 5\text{ V dc}$, $I_C = 100\text{ mA dc}$, $f = 1\text{ kHz}$	h_{fe}	20 50		
Magnitude of common-emitter, small-signal short-circuit, forward-current, transfer ratio 2N5152, L, and U3 2/ 2N5154, L, and U3	3306	$V_{CE} = 5\text{ V dc}$, $I_C = 500\text{ mA dc}$, $f = 10\text{ MHz}$	$ h_{fe} $	6 7		
Open-circuit output capacitance	3236	$V_{CB} = 10\text{ V dc}$, $I_E = 0$, $f = 1\text{ MHz}$	C_{obo}		250	pf
Switching time		$I_C = 5\text{ A dc}$, $I_{B1} = 500\text{ mA dc}$	t_{on}		0.5	μs
		$I_{B2} = -500\text{ mA dc}$	t_s		1.4	μs
		$V_{BE(off)} = 3.7\text{ V dc}$	t_f		0.5	μs
		$R_L = 6\Omega$; (see figure 13)	t_{off}		1.5	μs

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/ <u>Subgroup 5</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Safe operating area (dc)	3051	Pre-pulse condition for each test: $T_C = +25^\circ\text{C}$				
Test # 1		Pulse condition for each test $t_p = 1$ sec. 1 cycle, $T_C = +25^\circ\text{C}$, (see figure 14)				
Test # 2		$V_{CE} = 5.0$ V dc, $I_C = 2$ A dc for TO-39, TO-5, and U3				
Test # 3		$V_{CE} = 32$ V dc, $I_C = 310$ mA dc.				
Safe operating area (unclamped inductive)		$T_C = +25^\circ\text{C}$, $R_{BB1} = 10\Omega$ $R_{BB2} = 100\Omega$, $L = 0.3$ mH, $RL = 0.1\Omega$, $V_{CC} = 10$ V dc, $V_{BB1} = 10$ V dc, $V_{BB2} = 4$ V dc, $I_{CM} = 10$ A dc, (see figure 15)				
End-point electrical measurements	See table I, subgroup 2					
<u>Subgroups 6 and 7</u>						
Not applicable						

1/ For sampling plan see MIL-PRF-19500.

2/ For resubmission of failed subgroup 1 of table I, double the sample size of the failed test or sequence of tests. A failure in subgroup 1, of table II, shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

4/ Not required for JANS devices.

5/ Not required for laser marked devices.

6/ Hermetic seal test is an end-point to temperature cycling in addition to electrical measurements.

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* TABLE II. Group E inspection (all quality levels) – for qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal			
Fine leak	1071		
Gross leak			
Electrical measurements		See table I, subgroup 2 and table III herein.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	V _{CB} = 10 V dc, 6,000 cycles.	
Electrical measurements		See table I, subgroup 2 and table III herein.	
<u>Subgroup 4</u>			sample size N/A
Thermal impedance, thermal resistance curves		Each supplier shall submit their (typical) design thermal impedance curves. In addition, test conditions and Z _{θJX} limit shall be provided to the qualifying activity in the qualification report	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroups 6</u>			3 devices c = 0
ESD (electrostatic discharge)	1020		
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition A for devices ≥ 400 V Condition B for devices < 400 V	

TABLE III. Groups B, C and E delta and electrical measurements. 1/ 2/ 3/ 4/

Step	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1.	Forward - current transfer ratio	3076	$I_C = 2.5$ A dc, $V_{CE} = 5$ V dc, pulsed (see 4.5.1)	Δh_{FE2}	± 20 percent change from initial reading.		

1/ The delta measurements for table VIa (JANS) of MIL-PRF-19500 are as follows: Subgroups 4 and 5, see table III herein, step 1.

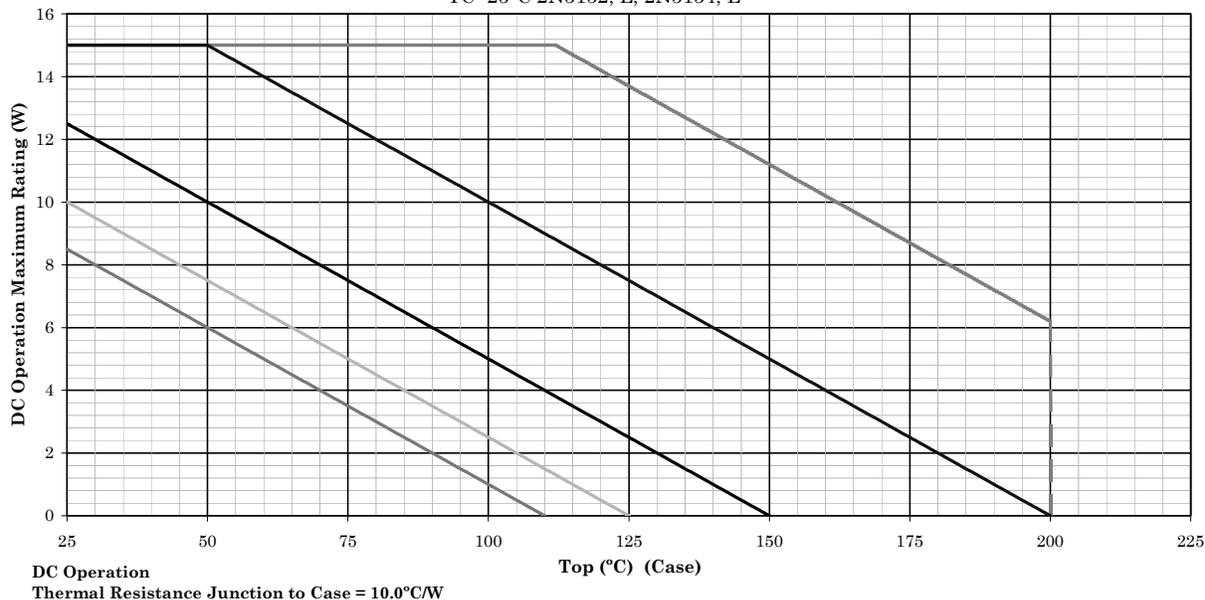
2/ The delta measurements for 4.2.2.2 (JAN, JANTX and JANTXV) are as follows: All steps, see table III herein, step 1.

3/ The delta measurements for table VII of MIL-PRF-19500 are as follows: Subgroup 6, see table III herein, step 1.

4/ The delta measurements for 4.4.4 are as follows: Subgroups 1 and 2, see table III herein, step 1.

Temperature-Power Derating Curve

TC=25°C 2N5152, L, 2N5154, L



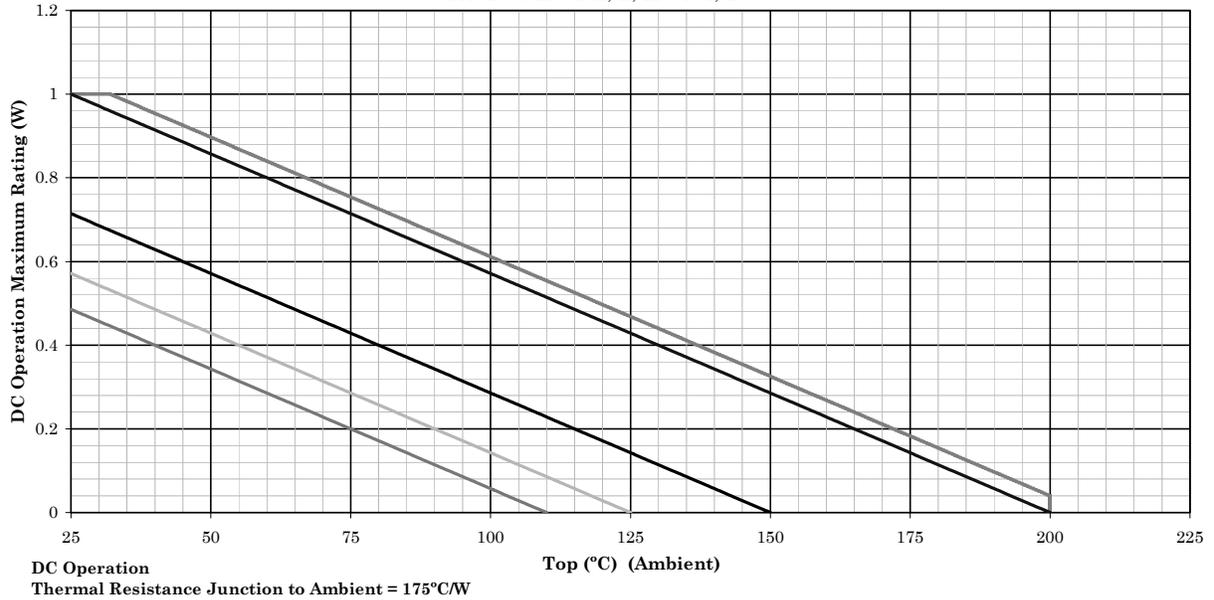
NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 6. Temperature-power derating for 2N5152, 2N5152L, 2N5154 and 2N5154L, (TO-5 and TO-39).

Temperature-Power Derating Curve

TA=25°C 2N5152, L, 2N5154, L



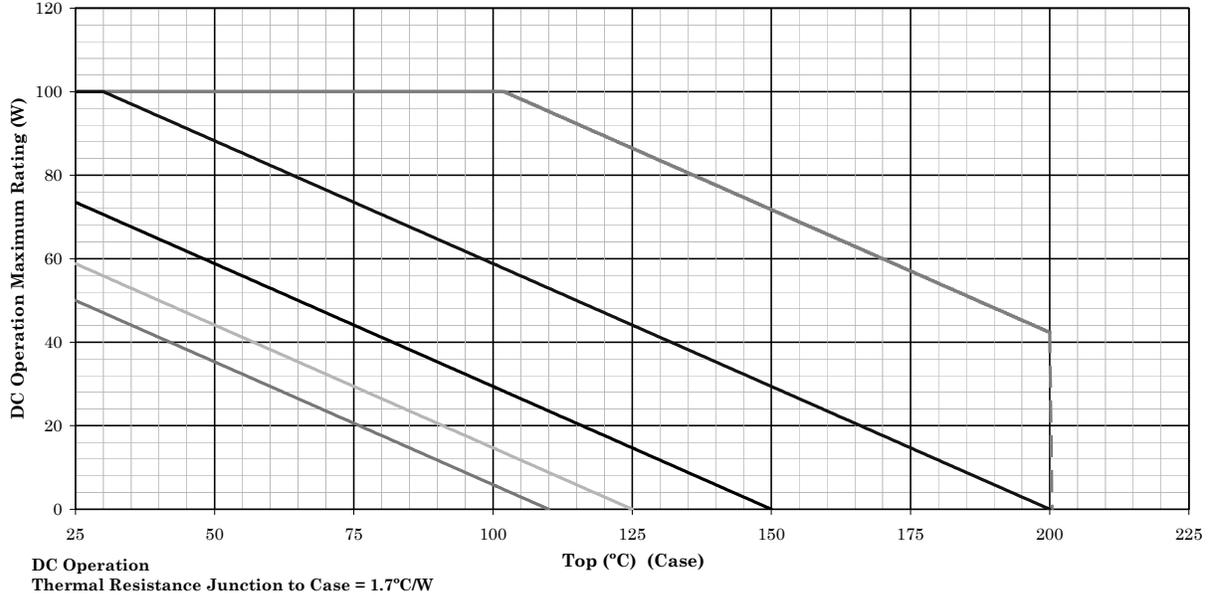
NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 7. Temperature-power derating for 2N5152, 2N5152L, 2N5154 and 2N5154L, (TO-5 and TO-39).

Temperature-Power Derating Curve

TC=25°C 2N5152U3, 2N5154U3



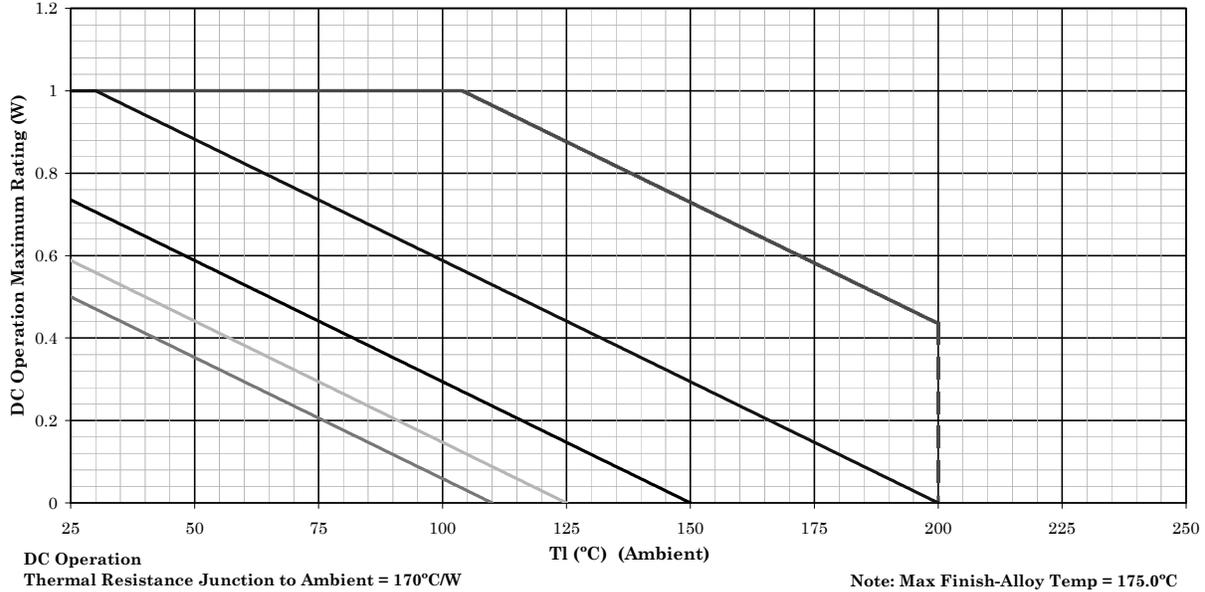
NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 8. Temperature-power derating for 2N5152U3, and 2N5154U3.

Temperature-Power Derating Curve

TA=25°C 2N5152U3, 2N5154U3

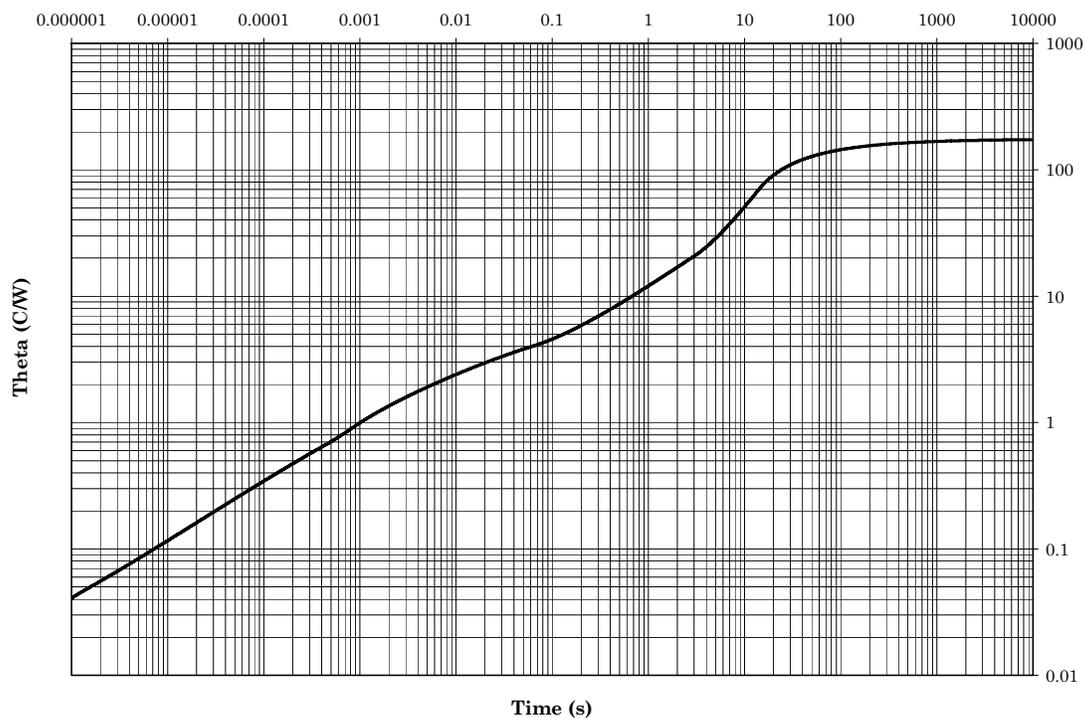


NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 9. Temperature-power derating for 2N5152U3, and 2N5154U3.

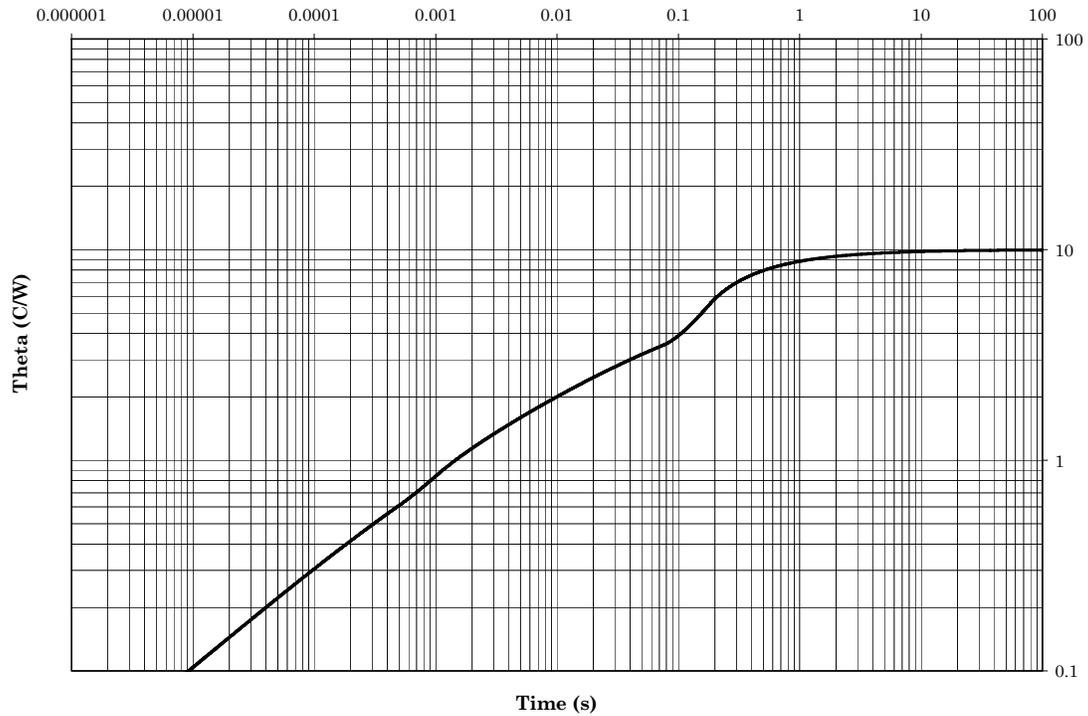
Maximum Thermal Impedance



$T_A = +25^\circ\text{C}$, Thermal resistance $R_{\theta JA} = 175^\circ\text{C/W}$.

* FIGURE 10. Thermal impedance graph ($R_{\theta JA}$) for 2N5152, 2N5154, 2N5152L, and 2N5154L (TO-5 and TO-39).

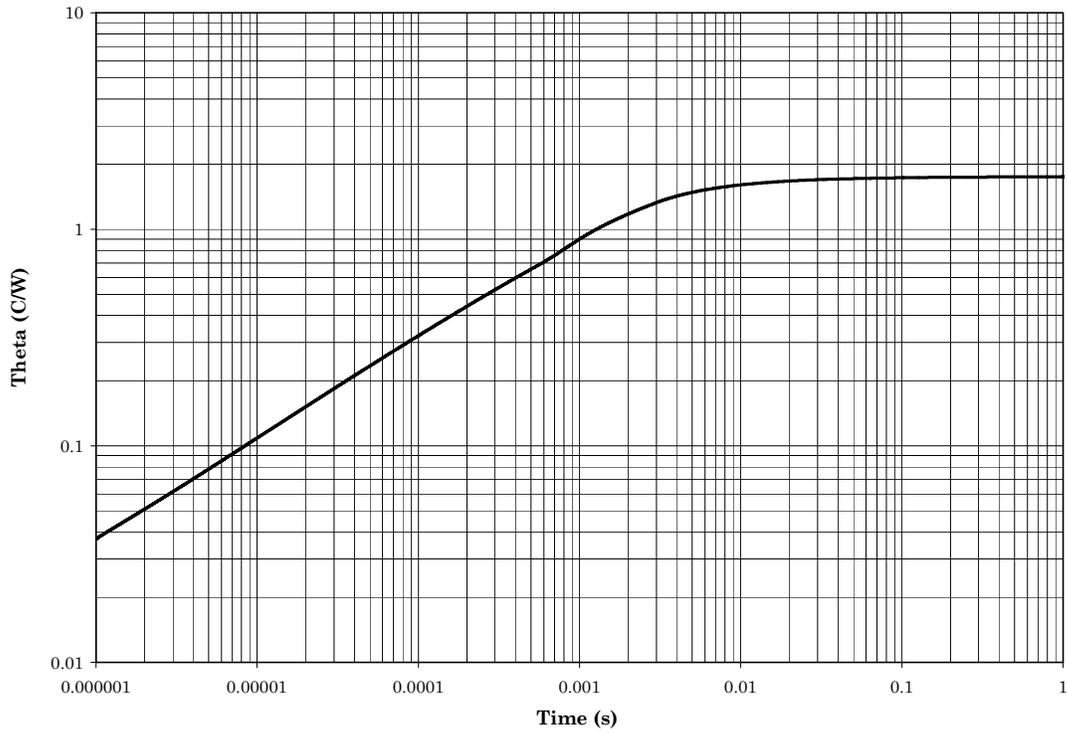
Maximum Thermal Impedance



T_c = +25°C, Thermal resistance R_{θJC} = 10°C/W

* FIGURE 11. Thermal impedance graph (R_{θJC}) for 2N5152, 2N5154, 2N5152L, and 2N5154L (TO-5 and TO-39).

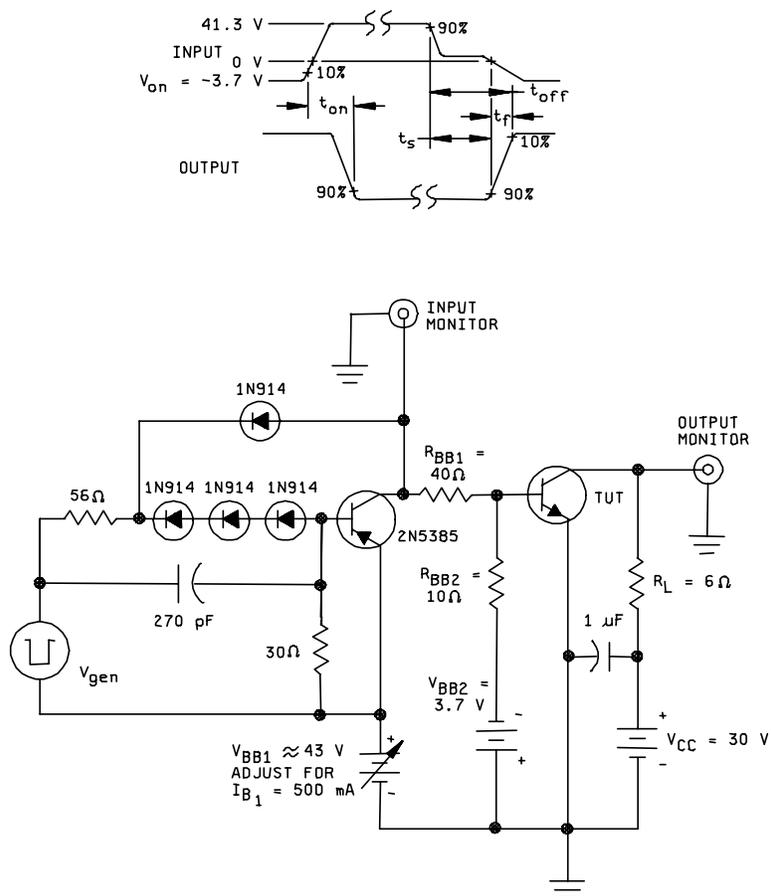
Maximum Thermal Impedance



$T_C = +25^\circ\text{C}$. Thermal resistance $R_{\theta JC} = 1.7^\circ\text{C/W}$

FIGURE 12. Thermal impedance graph ($R_{\theta JC}$) for 2N5152 and 2N5154 (U3).

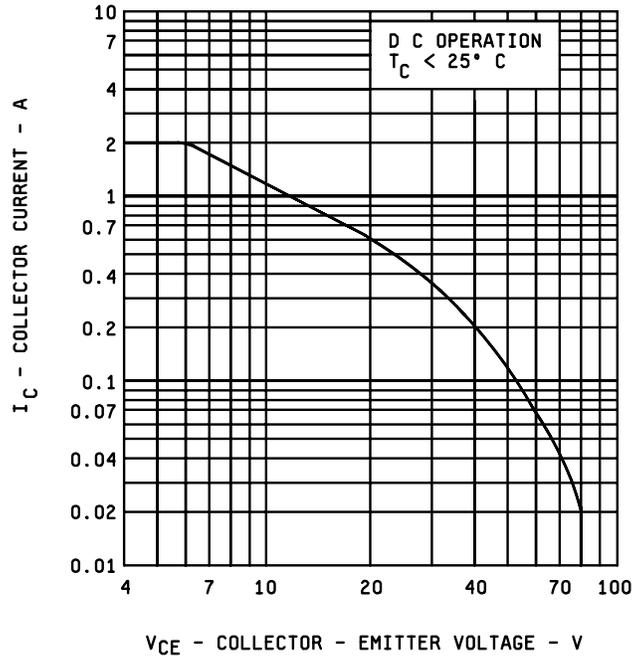
MIL-PRF-19500/544F



NOTES:

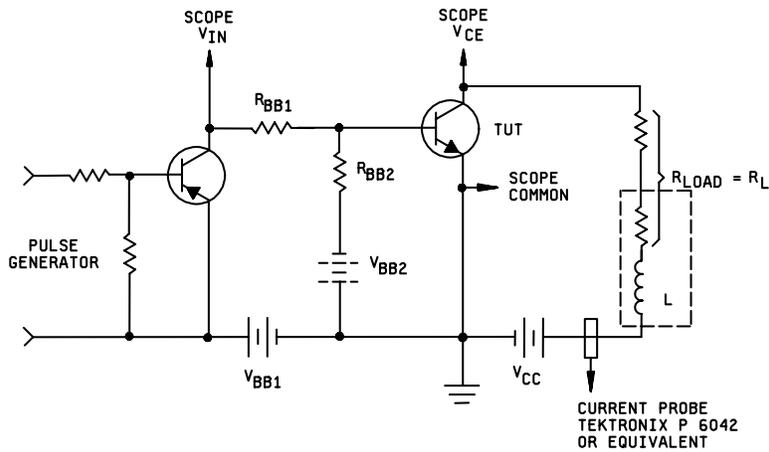
1. V_{gen} is a -30 pulse (from 0 V) into a 50 ohm termination.
2. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50$ ohm, duty cycle $\leq 2\%$, $t_w = 20$ μ s.
3. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 1$ ns, $R_{in} \geq 10$ M ohm, $C_{in} \leq 11.5$ pF.
4. Resistors must be non-inductive types.
5. The dc power supplies may require additional bypassing in order to minimize ringing.
6. An equivalent drive circuit may be used

* FIGURE 13. Switching time test circuit.



* FIGURE 14. Maximum safe operating area.

- $R_{BB1} = 10\Omega$
- $R_{BB2} = 100\Omega$
- $L = 0.3 \text{ mH}$
- $R_L = 0.1\Omega$
- $V_{CC} = 10 \text{ V dc}$
- $I_{CM} = 10 \text{ A}$
- $V_{BB1} = 10 \text{ V dc}$
- $V_{BB2} = 4 \text{ V dc}$



* FIGURE 15. Unclamped inductive load energy test circuit.

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.2).
- d. Product assurance level and type designator.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example JANHCA2N5152) will be identified on the QML.

JANHC and JANKC ordering information			
PIN	Manufacturer		
	33178	34156	43611
2N5152	JANHCA2N5152	JANHCB2N5152	JANHCC2N5152
2N5154	JANHCA2N5154	JANHCB2N5154	JANHCC2N5154
2N5152	JANKCA2N5152	JANKCB2N5152	JANKCC2N5152
2N5154	JANKCA2N5154	JANKCB2N5154	JANKCC2N5154

6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2790)

Review activity:
Navy - MC
Air Force - 19, 71

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