

PERFORMANCE SPECIFICATION

PRINTED WIRING BOARD, RIGID, SINGLE AND DOUBLE LAYER, WOVEN E-GLASS REINFORCED THERMOSETTING RESIN BASE MATERIAL, WITH OR WITHOUT PLATED HOLES, FOR SOLDERED PART MOUNTING

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Statement of scope. This specification covers the generic requirements for rigid, single and double sided (one or two conductor layer) printed wiring boards with or without plated holes that will use soldering for component/part mounting (see 6.1.1).

1.2 Classification. Printed wiring boards are classified as rigid, type 1 (single-sided printed board) or type 2 (double-sided printed board), as specified (see 3.3 and 6.2).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government specifications. The following document forms a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

DEPARTMENT OF DEFENSE

MIL-PRF-31032 - Printed Circuit Board/Printed Wiring Board, General Specification for.

(Unless otherwise indicated, copies of the above document are available from the Standardization Document Order Desk, Building 4D, 700 Tabor Avenue, Philadelphia, PA 19111-5094.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation (see 6.2).

INSTITUTE FOR INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS (IPC)

J-STD-003 - Solderability Tests for Printed Boards.
IPC-D-275 - Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies.
IPC-TM-650 - Test Methods Manual.

(Application for copies should be addressed to the Institute for Interconnecting and Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, IL 60062-6135.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM E345 - Standard Test Methods of Tension Testing of Metallic Foils.

(Application for copies should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103-1187.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Printed board detail requirements. Printed wiring boards delivered under this specification shall be in accordance with the requirements as specified herein, and documented in the printed board procurement documentation.

3.1.1 Conflicting requirements. The order of precedence of conflicting requirements shall be in accordance with MIL-PRF-31032.

3.1.2 Reference to printed board procurement documentation. For the purposes of this specification, when the term "specified" is used without additional reference to a specific location or document, the intended reference shall be to the applicable printed board procurement documentation.

3.2 Qualification. Printed wiring boards furnished under this specification shall be technologies that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3).

3.3 Design (see 6.2b). Printed wiring boards shall be of the design specified. Unless otherwise specified, if individual design parameters are not specified, then the baseline design parameters shall be as specified in IPC-D-275, class 3, type 1 or 2, as applicable. Test coupons shall be as specified in the applicable design standard and shall reflect worst case design conditions of the printed board(s) they represent.

3.4 Printed board materials. All materials used in the construction of compliant printed wiring boards shall comply with the applicable specifications referenced in the printed board procurement documentation. If materials needed in the production of printed wiring boards are not specified, then it is the manufacturer's responsibility to use materials which will meet the performance requirements of this specification. Acceptance or approval of any printed board material shall not be construed as a guarantee of the acceptance of the finished printed wiring board.

3.5 Visual and dimensional requirements. The finished production printed wiring boards, supporting test coupons, or qualification test specimens (hereafter referred to as printed wiring board test specimens) shall conform to the requirements specified in 3.5.1 through 3.5.6, as applicable.

3.5.1 Base material.

3.5.1.1 Edges of base material. Burrs, chips, nicks, haloing, and other penetrations along the base material edges of finished printed wiring boards shall be acceptable provided the defect does not reduce the edge spacing specified by more than 50 percent.

3.5.1.2 Surface imperfections. Surface imperfections (such as scratches, pits, dents, cuts or exposed reinforcement material fibers) shall be acceptable providing the imperfections meets all of the following:

- a. The imperfection does not bridge between conductors.
- b. The dielectric spacing between the imperfection and a conductor is not reduced below the specified minimum conductor spacing requirements.

3.5.1.3 Subsurface imperfections. Subsurface imperfections (such as blistering, haloing, and delamination) shall be acceptable providing the imperfection meets the following:

- a. The imperfections do not bridge more than 25 percent of the distance between conductors or plated-through holes. No more than two percent of the printed wiring board area on each side shall be affected.
- b. The imperfections do not reduce conductor or dielectric spacing below the specified minimum requirements.
- c. The imperfections do not propagate as a result of testing (such as rework simulation, thermal stress, or thermal shock).
- d. The longest dimension of any single imperfection is no greater than 0.80 mm (.0315 inch). In non-circuitry areas, the maximum size shall not be greater than 2 mm (.079 inch) in the longest dimension or 0.01 percent of the printed wiring board area, maximum.

3.5.2 Conductor pattern.

3.5.2.1 Annular ring, external. The external annular ring shall be as specified. Unless otherwise specified, the external annular ring may have in isolated areas a 20 percent reduction of the specified minimum external annular ring due to defects such as pits, dents, nicks, or pinholes.

3.5.2.2 Bonding of conductor to base material. There shall be no peeling or lifting of any conductor from the base material.

3.5.2.3 Conductor imperfections. The conductor pattern shall contain no cracks, splits or tears. Unless otherwise specified, any combination of edge roughness, nicks, pinholes, cuts or scratches exposing the base material shall not reduce each conductor width by more than 20 percent of its minimum specified width. There shall be no occurrence of the 20 percent reductions greater than 13 mm (.51 inch) or 10 percent of a conductor length, whichever is less.

3.5.2.4 Conductor finish (plating or coating). The conductor finish shall be as specified.

3.5.2.4.1 Coverage. The conductor finish shall completely cover the exposed conductor pattern. Complete coverage does not apply to the vertical conductor edges.

3.5.2.4.2 Thickness (non destructive). The plating or coating thickness of the conductor finish shall be as specified.

3.5.2.4.3 Whiskers. There shall be no whiskers of solder or other platings on the surface of the conductor pattern.

3.5.2.5 Conductor spacing. The conductor spacing shall be as specified.

3.5.2.6 Conductor thickness (non destructive). The conductor thickness on printed wiring boards shall be as specified. Unless otherwise specified, the minimum final metal foil thickness shall not be reduced by more than 10 percent from the starting metal foil nominal thickness as converted from the area weight of the foil.

3.5.2.7 Conductor width. The conductor width shall be as specified.

3.5.3 Dimensions. The finished printed wiring board shall meet the dimensional requirements specified.

3.5.4 Hole pattern accuracy. The size and location of the hole pattern in the printed wiring board shall be as specified.

3.5.5 Lifted lands. The finished printed wiring board shall not exhibit any lifted lands.

3.5.6 Solder resist. Unless otherwise specified, the solder resist conditions below shall apply.

3.5.6.1 Coverage. Solder resist coverage imperfections (such as blisters, skips, and voids) shall be acceptable providing the imperfection meets all of the following:

- a. In areas containing parallel conductors, the solder resist imperfection shall not expose two isolated conductors whose spacing is less than 0.5 mm (.020 inch) unless one of the conductors is a test point or other feature area which is purposely left uncoated for subsequent operations.

- b. The exposed conductor shall not be bare copper.
- c. The solder resist imperfection does not expose tented via holes.

3.5.6.2 Discoloration. Discoloration of metallic surfaces under the cured solder resist is acceptable.

3.5.6.3 Registration. The solder resist shall be registered to the land or terminal patterns in such a manner as to meet the requirements specified. If no requirements are specified, the following apply:

- a. Unless otherwise specified, solder resist shall not encroach onto surface mount lands.
- b. Solder resist misregistration onto plated-through component hole lands (plated-through holes to which solder connections are to be made) shall not reduce the external annular ring below the specified minimum requirements.
- c. Solder resist shall not encroach into plated-through hole barrels or onto other surface features (such as connector fingers or lands of unplated holes) to which solder connections will be made.
- d. Solder resist is permitted in plated-through vias or holes in which no lead is to be soldered.
- e. Test points (intended for assembly testing) shall be free of solder resist unless a partial coverage allowance is specified.

3.5.6.4 Thickness. Solder resist thickness shall be as specified.

3.6 Microsection requirements (double sided only). Printed wiring board test specimens shall conform the requirements in 3.6.1 through 3.6.7, as applicable.

3.6.1 Conductor finish (plating or coating) thickness (destructive). The plating or coating thickness of the conductor finish shall be as specified.

3.6.2 Conductor thickness (destructive). The conductor thickness on printed wiring boards shall be as specified. Unless otherwise specified, the minimum final metal foil thickness shall not be reduced by more than 10 percent from the starting metal foil nominal thickness as converted from the area weight of the foil.

3.6.3 Copper plating defects. Nodules, plating folds, plating inclusions or plated reinforcement material protrusions that project into the plated-through hole shall be acceptable provided that the hole diameter and the copper thickness are not reduced below their specified limits. There shall be no separations or contamination between the horizontal edge of the external layer copper and the copper plating. Copper plating separations along the vertical edge of the external copper foil shall be acceptable. Anomalies resulting from vertical edge copper foil/copper plating separation shall not be cause for rejection.

3.6.4 Copper plating thickness. The copper plating thickness shall be as specified. Any reduction from the specified copper plating thickness shall be isolated (non-continuous). Any copper plating less than 80 percent of the specified thickness shall be treated as a void.

3.6.4.1 Copper plating voids. The copper plating in the plated-through hole shall not exhibit any void in excess of the following:

- a. There shall be no more than one plating void per panel, regardless of length or size.
- b. There shall be no plating void longer than five percent of the total printed wiring board thickness.
- c. There shall be no plating voids evident at the interface of any conductive layer and plated hole wall.

Conductor finish plating or coating material between the base material and copper plating (i.e., behind the hole copper plating) is evidence of a void. Any plated hole exhibiting this condition shall be counted as one void for panel acceptance purposes.

3.6.5 Dielectric layer thickness. The minimum dielectric thickness for printed wiring boards shall be as specified.

3.6.6 Laminate voids. Laminate voids with the longest dimension of 0.08 mm (.0032 inch) or less shall be acceptable provided the conductor spacing is not reduced below the minimum dielectric spacing requirements, laterally or vertically, as specified.

3.6.7 Lifted lands (after thermal stress, rework simulation or thermal shock). After undergoing rework simulation (see 3.7.4.5), thermal stress (see 3.7.6.2) or thermal shock (see 3.7.6.3), the maximum allowed lifted land distance from the base material surface to the outer lower edge of the land shall be the thickness (height of metal foil and plating, when applicable) of the terminal area or land.

3.6.8 Metallic cracks. There shall be no cracks in the platings or coatings. For terminal or land areas plated with copper, cracks are permissible in the outer copper foil provided they do not extend or propagate into the plating.

3.7 Performance requirements. The performance requirements specified in 3.7.1 through 3.7.6 shall be verified by the test methods detailed in 4.6. Unless otherwise specified, test optimization in accordance with MIL-PRF-31032 may be used, but printed wiring boards shall meet all of the performance requirements specified herein, regardless of the verification method used.

3.7.1 Acceptability (of printed wiring boards). When examined as specified in 4.6.1, the printed wiring boards shall be in accordance with the acceptance requirements specified in 3.3 (design), 3.4 (material), 3.5 (visual and dimensional), 3.8 (marking), and 3.9 (workmanship).

3.7.2 Microsection evaluation (of printed wiring board test specimens)(see 6.2.1a). When printed wiring board test specimens (finished printed wiring boards, supporting test coupons, or qualification test specimens) are microsectioned and examined as specified in 4.6.2, the requirements specified in 3.6 shall be met.

3.7.3 Chemical requirements.

3.7.3.1 Cleanliness. When printed wiring board test specimens are tested in accordance with 4.6.3.1, the levels of cleanliness shall be in accordance with the requirements of 3.7.3.1.1 or 3.7.3.1.2, as applicable.

3.7.3.1.1 Prior to the application of solder resist. Unless otherwise specified, prior to the application of solder resist, the level of ionic contamination shall not exceed 1.56 micrograms/square centimeter (10.06 micrograms/square inch).

3.7.3.1.2 Completed printed wiring board (when specified, see 6.2.1b). The levels of cleanliness for completed printed wiring boards shall be as specified.

3.7.3.2 Copper plating characteristics.

3.7.3.2.1 Elongation. When copper plating is tested in accordance with 4.6.3.2, the elongation shall be 6 percent minimum.

3.7.3.2.2 Tensile strength. When copper plating is tested in accordance with 4.6.3.3, the tensile strength shall be 248 MPa (36,000 psi) minimum.

3.7.4 Physical requirements.

3.7.4.1 Adhesion, marking. After marking is tested in accordance with 4.6.4.1, any specified markings which are missing in whole or in part, faded, smeared, or shifted (dislodged) to the extent that it cannot be readily identified shall constitute failure. A slight change in the color of ink or paint markings after the test shall be acceptable.

3.7.4.2 Adhesion, plating. When tested as specified in 4.6.4.2, there shall be no plating particles or conductor patterns removed from the printed wiring board test specimen except for outgrowth.

3.7.4.3 Adhesion, solder resist (when applicable). When tested as specified in 4.6.4.3, the maximum percentage of cured solder resist lifted from the surface of the base material, conductors, and lands of the coated printed wiring board test specimen shall not exceed the following limits:

- a. Bare copper or base material: 0 percent.
- b. Non-melting metals (e.g., gold or nickel plating): 5 percent.
- c. Melting metals (e.g., tin-lead plating, solder coating, indium, bismuth, etc.): 10 percent.

3.7.4.4 Bow and twist. When printed wiring boards are tested as specified in 4.6.4.4, the maximum limit for bow and twist shall be as specified.

3.7.4.5 Rework simulation.

3.7.4.5.1 Unsupported holes. After undergoing the test specified in 4.6.4.5.1, the lands on printed wiring board test specimens with unsupported holes shall withstand 2.27 kg (5 pounds) pull or 3.45 MPa (500 lb/in²), whichever is less.

3.7.4.5.2 Plated holes. After undergoing the test specified in 4.6.4.5.2, the printed wiring board test specimens shall be microsectioned and inspected in accordance with 4.6.2 and the requirements specified in 3.6 shall be met.

3.7.4.6 Solderability (see 6.2.1c).

3.7.4.6.1 Hole solderability. After undergoing the test specified in 4.6.4.6, the printed wiring board test specimen shall conform to the class 3 acceptance criteria specified in J-STD-003.

3.7.4.6.2 Surface solderability. After undergoing the test specified in 4.6.4.6, the printed wiring board test specimen shall conform to the class 3 acceptance criteria specified in J-STD-003.

3.7.5 Electrical requirements.

3.7.5.1 Continuity (when specified, see 6.2.1d). When tested in accordance with 4.6.5.1, unless otherwise specified (see 3.1), there shall be no circuit whose resistance exceeds 10 ohms. For referee purposes, 0.5 ohm maximum per 25 mm (.98 inch) of circuit length shall apply.

3.7.5.2 Isolation (when specified, see 6.2.1d). When tested as specified in 4.6.5.2, the resistance between mutually isolated conductors shall be greater than 2 megohms.

3.7.6 Environmental requirements.

3.7.6.1 Moisture and insulation resistance. When tested as specified in 4.6.6.1, the printed wiring board test specimen shall have a minimum of 500 megohms of resistance between conductors. After the test, the printed wiring board test specimen shall not exhibit blistering, measling or delamination in excess of that allowed in 3.5.1.

3.7.6.2 Thermal stress.

3.7.6.2.1 Unsupported holes. After undergoing the test specified in 4.6.6.2, the printed wiring board test specimen shall be inspected in accordance with 4.6.1 and shall not exhibit any cracking or separation of plating and conductors, lands shall not lift in excess of that allowed in 3.6.7 and blistering or delamination shall not exceed the limits allowed in 3.5.

3.7.6.2.2 Plated holes. After undergoing the test specified in 4.6.6.2, the printed wiring board test specimen shall meet the requirements specified in 3.5 when inspected as specified in 4.6.1. The printed wiring board test specimen shall then be microsectioned and inspected in accordance with 4.6.2 and shall meet the requirements of 3.7.2.

3.7.6.3 Thermal shock. After undergoing the test specified in 4.6.6.3, the printed wiring board test specimens shall meet the following requirements:

- a. Visual inspection: When inspected as specified in 4.6.1, there shall be no evidence of plating cracks, blistering, crazing, or delamination in excess of that allowed in 3.5.
- b. Continuity: When tested as specified in 4.6.5.1, the change in resistance between the first high temperature cycle and the last high temperature cycle shall not be more than 10 percent.
- c. Microsection (double sided with plated holes only): The printed wiring board test specimen shall be microsectioned and inspected in accordance with 4.6.2 and the requirements specified in 3.6 shall be met.

3.8 Marking. Marking shall be in accordance with MIL-PRF-31032.

3.9 Workmanship. Printed wiring boards shall be processed in such a manner as to be uniform in quality and shall be free from defects that will affect life, serviceability or appearance.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-PRF-31032, and as specified herein.

4.2 Standard test and inspection conditions. Unless otherwise specified by the applicable test method or procedure, inspections and tests may be performed at ambient conditions.

4.3 Qualification inspection. Unless otherwise specified by the Technical Review Board (TRB) approved qualification test plan, qualification inspection shall be in accordance with MIL-PRF-31032 and as specified herein.

4.3.1 Qualification test vehicles. The qualification test vehicle(s) to be subjected to qualification inspection shall be in accordance with the TRB approved qualification test plan and the applicable qualification test vehicle specification(s).

4.3.2 Sample. The number of qualification test vehicle(s) to be subjected to qualification inspection shall be in accordance with TRB approved qualification test plan.

4.3.3 Test routine. The qualification test vehicle(s) shall be subjected to the inspections and tests specified in tables I and II.

4.3.4 Qualification by similarity. A production lot may be considered qualified by similarity if the dimension parameters are within twenty-five percent of that which is currently qualified. This window is applicable on an associated specification basis.

4.4 Lot conformance inspection. Lot conformance inspection shall be in accordance with MIL-PRF-31032 and table I herein. Lot conformance inspection testing by subgroup or within a subgroup may be performed in any sequence.

4.4.1 Sample inspections. Panels and printed wiring boards to be delivered in accordance with this specification shall have been subjected to and passed all the inspections of table I. A sample of printed wiring boards (or test coupon that represent them) shall be randomly selected from each inspection lot.

TABLE I. Lot conformance inspection.

Inspection	Requirement paragraph	Method paragraph	Specimen to test ^{1/}				Sample plan ^{2/}
			PWB	THM	SMT	MIX	
Subgroup 1 Thermal stress	3.7.6.2	4.6.6.2		B	B	B	Plan TJ
Subgroup 2 Acceptability ^{3/}	3.7.1	4.6.1	X				Plan BH ^{3/}
Subgroup 3 Cleanliness ^{4/}	3.7.3.1	4.6.3.1	X				Plan *N
Subgroup 4 Adhesion, marking	3.7.4.1	4.6.4.1	<u>5/</u>	5/	5/	5/	Plan BH or TJ ^{6/}
Adhesion, plating	3.7.4.2	4.6.4.2	X	C	C	C	Plan BH or TJ ^{5/} ^{6/}
Adhesion, solder mask	3.7.4.3	4.6.4.3	X	G	T	G/T	Plan BH or TJ ^{6/} ^{7/}
Bow and twist	3.7.4.4	4.6.4.4	X				Plan BH
Solderability							
Hole ^{8/}	3.7.4.6.1	4.6.4.6		A or S	C or M	A or S	Plan TJ ^{8/}
Surface ^{9/}	3.7.4.6.2	4.6.4.6		C	C or M	C or M	Plan TJ ^{9/}

^{1/} Test coupons are in accordance with IPC-D-275. PWB is a production board; THM is a test coupon from through-hole mount design; SMT is a test coupon from a surface mount design; MIX is test coupons from a mixed mounting design

^{2/} See MIL-PRF-31032 for C = 0 sampling plans.

^{3/} Surface imperfections (3.5.1.2) and subsurface imperfections (3.5.1.3) shall be inspected prior to solder resist application.

^{4/} Inspection shall be performed prior to solder resist application.

^{5/} Test coupon or production printed wiring board, manufacturer's option.

^{6/} For production printed wiring boards use sample plan H ("BH"); for test coupons use sample plan J ("TJ").

^{7/} Test coupon T shall be used when production printed wiring boards have tented via holes.

^{8/} For designs containing plated holes (type 2 with plated-through holes).

^{9/} For designs with unsupported holes only (type 1 or type 2 without plated holes).

4.4.2 Panel acceptance. Not applicable.

4.4.3 100 percent inspection. Not applicable.

4.5 Periodic conformance inspection. Periodic conformance inspection shall be in accordance with MIL-PRF-31032 and table II herein.

TABLE II. Periodic conformance inspection baseline test coverage.

Inspection	Requirement paragraph	Method paragraph	Tests frequency
Elongation	3.7.3.2.1	4.6.3.2	Monthly
Tensile strength	3.7.3.2.2	4.6.3.3	Monthly
Rework simulation	3.7.4.5	4.6.4.5	Monthly
Moisture and insulation resistance	3.7.6.1	4.6.6.1	Monthly
Thermal shock	3.7.6.3	4.6.6.3	Annually

4.6 Methods of inspection.

4.6.1 Visual and dimensional inspection. The printed wiring board specimen shall be inspected in accordance with IPC-TM-650, method 2.1.8, except that the magnification shall be 4 diopters, minimum.

4.6.2 Microsection inspection (double sided). Microsection examination shall be in accordance with IPC-TM-650, method 2.1.1 or 2.1.1.2. Referee inspections shall be accomplished at a magnification of 200x.

4.6.3 Chemical test methods.

4.6.3.1 Cleanliness. The sodium chloride (NaCl) salt equivalent ionic contamination tests of 4.6.3.1.1 or an automated test, of 4.6.3.1.2 shall be used to test for ionic cleanliness.

4.6.3.1.1 Manual method. The manual test for cleanliness shall be performed in accordance with IPC-TM-650, method 2.3.25.

4.6.3.1.2 Automated methods. The automated test for cleanliness shall be performed in accordance with IPC-TM-650, method 2.3.26 or 2.3.26.1.

4.6.3.2 Elongation of copper. The test for elongation of copper shall be performed in accordance with ASTM E345. The travel speed of testing shall be 50 mm \pm 1 mm (1.97 \pm .03 inches) per minute. Samples shall be baked for 6 hours minimum at 135° C (275° F) minimum prior to testing.

4.6.3.3 Tensile strength of copper. The test for tensile strength of copper shall be performed in accordance with ASTM E345. The travel speed of testing shall be 50 mm \pm 1 mm (1.97 \pm .03 inches) per minute. Samples shall be baked for 6 hours minimum at 135° C (275° F) minimum prior to testing.

4.6.4 Physical test methods.

4.6.4.1 Adhesion, marking. Test specimens which represent all types of marking used on the lot (except etched marking) shall be subjected to the solderability test in 4.6.4.6. The side of the test specimen that is marked shall be placed against the solder. After the test, the test specimen shall be examined in accordance with 4.6.1 and the requirements of 3.7.4.1 shall be met.

4.6.4.2 Adhesion, plating. The test for plating adhesion shall be performed in accordance with IPC-TM-650, method 2.4.1.

4.6.4.3 Adhesion, solder resist. The test for solder resist adhesion shall be performed in accordance with IPC-TM-650, method 2.4.28.1.

4.6.4.4 Bow and twist. The tests for bow and twist shall be performed in accordance with IPC-TM-650, method 2.4.22.

4.6.4.5 Rework simulation.

4.6.4.5.1 Single and double sided without plated holes. The rework simulation test shall be performed in accordance with IPC-TM-650, method 2.4.20.

4.6.4.5.2 Double sided with plated holes. The rework simulation test shall be performed in accordance with IPC-TM-650, method 2.4.36.

4.6.4.6 Solderability. The tests for hole or surface solderability shall be performed in accordance with J-STD-003.

4.6.5 Electrical test methods.

4.6.5.1 Continuity (see 3.7.6.3b). A current shall be passed through each conductor or group of interconnected conductors by applying electrodes on the terminals at each end of the conductor or group of conductors. The current passed through the conductors shall not exceed those specified in the applicable design standard for the smallest conductor in the circuit.

4.6.5.2 Isolation (circuit shorts). A test voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer (when applicable). The test voltage shall be the minimum rated voltage for the printed wiring board. If the maximum rated voltage of the printed wiring board is not specified, the test voltage shall be 40 volts minimum.

4.6.6 Environmental test methods.

4.6.6.1 Moisture and insulation resistance. The test for moisture and insulation resistance shall be performed in accordance with IPC-TM-650, method 2.6.3, class 3.

4.6.6.2 Thermal stress. The test for thermal stress shall be performed in accordance with IPC-TM-650, method 2.6.8.

4.6.6.3 Thermal shock. The test for thermal shock shall be performed in accordance with IPC-TM-650, method 2.6.7.2, except that the temperature extremes shall be -65 °C and +125 °C for all base materials.

5. PACKAGING

5.1 Packaging requirement. The requirement for packaging shall be in accordance with MIL-PRF-31032.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Notes. The notes in MIL-PRF-31032 are applicable to this specification.

6.1.1 Intended use. This associated specification was developed for the use of verifying performance characteristics of rigid woven E-glass, thermoset resin base materials, for single or double sided (1 or 2 conductor layers) printed wiring boards with or without plated holes, that will use soldering for component/part joining. Printed wiring boards of other base material types (such as thermoplastic base materials) or printed board construction styles (such as multilayered) can be verified to the performance requirements contained in this document, however, the performance parameters and baseline verification methods of other associated specifications are more suitable for those technologies. The supplement for MIL-PRF-31032 lists all of the applicable and current associated specifications at the time of its date.

6.2 Acquisition requirements. Acquisition documents must specify the following:

- a. Title, number, and date of this specification (with any amendments).
- b. Issue of DODISS to be cited in the solicitation and, if required, the specific issue of individual documents referenced (see section 2).

- c. Title, number and date of applicable printed board procurement documentation or drawing and identification of the originating design activity.
- d. The complete printed board procurement documentation part number (see 3.1).
- e. The printed wiring board classification (type 1 or 2, see 3.1 and 3.3).
- f. Levels of preservation and packing required.
- g. If special or additional identification marking is required.
- h. Any other additional, optional, or special requirements (see 6.2.1).

6.2.1 Optional acquisition data. The following items are optional and are only applicable when specified in the printed board procurement documentation.

- a. Special requirements for destructive microsection inspections (see 3.7.2).
- b. Special or additional cleanliness is required (see 3.7.3.1).
- c. The durability of coating rating (accelerated aging for solderability testing) if other than category 2 (see J-STD-003).
- d. If electrical testing is to be performed (see 3.7.5).
- e. Disposition of lot conformance inspection sample units.
- f. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the product inspection lot to be supplied with each shipment by the QML manufacturer, if applicable.
- g. Requirements for failure analysis, corrective action and reporting of results.
- h. Requirements for certificate of compliance, if applicable.
- i. Requirements for notification of change of product or process to the acquiring activity in addition to notification to the qualifying activity, if applicable.

6.3 Replacement information. This specification includes a majority of the performance requirements of previous revisions of MIL-P-55110 and MIL-PRF-55110 for types 1 and 2 printed wiring boards constructed using base material types GB, GF, GH, GM, and GI. Printed wiring boards conforming to this associated specification would be comparable to and/or substitutable for printed wiring boards conforming to MIL-P-55110 and MIL-PRF-55110.

CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 85

Preparing activity:
DLA - ES
(Project 5998-0062-02)

Review activities:
Army - MI
Navy - MC
Air Force - 99