

PERFORMANCE SPECIFICATION

CAPACITORS, FIXED, CERAMIC DIELECTRIC,  
(TEMPERATURE STABLE AND GENERAL PURPOSE), HIGH RELIABILITY,  
GENERAL SPECIFICATION FOR

This amendment forms a part of MIL-C-123B, dated 6 August 1990, and is approved for use by all Departments and Agencies of the Department of Defense.

PAGE 1

1.2.1, first sentence, delete and substitute: "Capacitors specified herein (see 3.1) are identified by a military part number which consists of the basic number of the military specification sheet followed by a series of coded characters."

1.2.1, third sentence, delete "The coded number shall provide" and substitute "The coded number provides"

1.2.1, fourth sentence, delete and substitute: "The military part number is in the following form:"

1.2.1.1, first sentence, delete.

PAGE 2

1.2.1.4, second sentence, delete and substitute: "When the nominal value is less than 10 pF, the letter 'R' is used to indicate the decimal point and the succeeding digit(s) of the group represent significant figure(s)."

PAGE 3

TABLE IV, delete and substitute:

"TABLE IV. Termination.

| Leaded capacitors |                                                          | Nonleaded capacitors |                                                                                                |
|-------------------|----------------------------------------------------------|----------------------|------------------------------------------------------------------------------------------------|
| Symbol            | Termination type                                         | Symbol               | Termination type                                                                               |
| A                 | Copper-iron-zinc alloy (194 alloy)                       | G                    | Silver-nickel-gold                                                                             |
| C                 | Copper, solder coated, 60 microinches minimum            | M                    | Palladium/silver alloy                                                                         |
| W                 | Copper clad steel, solder coated, 60 microinches minimum | R                    | Palladium/silver alloy, solder coated                                                          |
|                   |                                                          | S                    | Guarded, solder coated <u>1/</u> <u>2/</u>                                                     |
|                   |                                                          | T                    | Guarded, solder dipped                                                                         |
|                   |                                                          | W                    | Base metallization - barrier metal - tinned (tin or tin-lead alloy) <u>3/</u>                  |
|                   |                                                          | Y                    | Base metallization - barrier metal - tin                                                       |
|                   |                                                          | Z                    | Base metallization - barrier - solder plated (tin/lead alloy with a minimum of 4 percent lead) |

1/ A guarded termination is one in which the interelectrode metallization is separated from the final finish by a barrier or guard metal; e.g., copper or nickel, etc.

2/ Capacitors with termination types T or Z may, with procuring agency approval, be remarked with termination type S.

3/ Capacitors with termination types S, T, Y, or Z may, with procuring agency approval, be remarked with termination type W. "

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2.1.1, SPECIFICATIONS; delete QQ-S-571 and MIL-C-39028.

2.1.1, STANDARDS, MIL-STD-790; title, delete and substitute: "Standard Practice for Established Reliability and High Reliability Qualified Products List (QPL) Systems for Electrical, Electronic, and Fiber Optic Parts Specifications".

PAGE 4

2.2, before Electronic Industries Association, add:

"AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

ANSI/J-STD-006 - Requirements for Electronic Grade Solder Alloys and Fluxed and Non-fluxed Solid Solders for Electronic Soldering Applications."

(Application for copies should be addressed to American National Standards Institute, 11 West 42nd Street, New York, NY 10036.)"

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3.3, delete and substitute:

"3.3 Qualified Product List (QPL) system. The manufacturer shall establish and maintain a QPL system for capacitors covered by this specification. This QPL system shall be established and maintained in accordance with the procedures and requirements specified in MIL-STD-790 and herein."

3.4, delete and substitute:

"3.4 Interface and physical dimensions. Capacitors shall meet the interface and physical dimensions specified (see 3.1)."

3.4.1, delete and substitute:

"3.4.1 Dielectric parameters. Capacitors supplied to this specification shall have a minimum dielectric thickness of 0.8 mil for 50 volt rated capacitors or 1 mil for capacitors with ratings above 50 volts. Dielectric thickness is the actual measured thickness of the fired ceramic dielectric layer. Voids, or the cumulative effect of voids, shall not reduce the total dielectric thickness by more than 50 percent (see figure1). Maximum dielectric constant shall be 3000."

3.4.2, last line; delete "plastic" and substitute "liquidus".

3.5, first sentence, delete and substitute: "Prior to termination, all capacitors delivered to this specification shall be subjected to ultrasonic examination or some other method approved by the qualifying activity."

3.5, delete last sentence.

3.5.1, delete.

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3.8, second sentence, delete "until rupture and the level recorded".

3.9.a, delete and substitute:

"a. There shall be no evidence of improperly made connections, substandard soldering, structural weakness, or solder bridging that reduces the distance between terminals to less than 50 percent."

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3.9.c, delete and substitute:

"c. The encapsulation material shall have a minimum thickness of .005 inch (0.13 mm) (dimension T, figure E-3), on all external surfaces of the chip and any protrusions of termination, solder, or lead frame, with the exception of the lead side of the radial leaded capacitors, which shall have a minimum thickness of .010 inch (0.25 mm) (dimensions T<sub>R</sub>, figure E-3)."

3.9.e, delete.

3.9.f, delete and substitute:

"f. Extraneous particles, such as solder spikes or solder balls, shall not exceed .015 inch (0.38 mm) in any dimension, nor shall the total encapsulation thickness be reduced to less than the thickness T or T<sub>R</sub> as defined in 3.9.c. Total encapsulation thickness is the combined measurement of the encapsulation thickness on either side of the particle."

PAGE 7

3.12, delete and substitute:

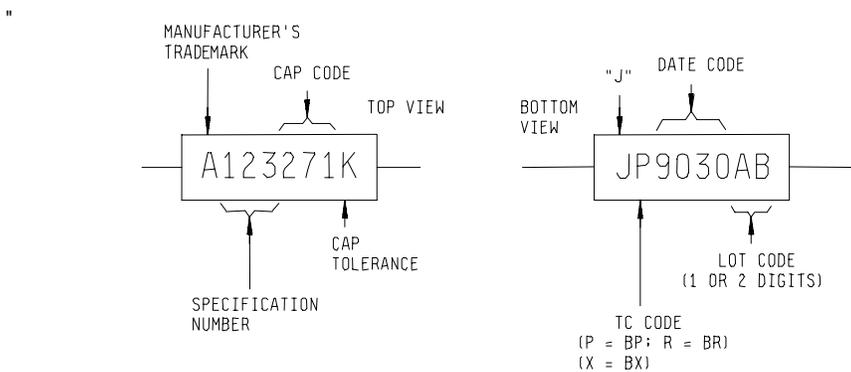
"3.12 Dissipation factor (DF). When determined as specified in 4.6.8, the dissipation factor shall not exceed 2.5 percent for BX and BR characteristics, 0.15 percent for BP characteristic, and 0.05 percent for BG characteristic, unless otherwise specified (see 3.1). For capacitors of less than 10 pF (chips) and 30 pF (leaded devices), the dissipation factor shall not exceed 0.25 percent for BP and 0.15 percent for BG. (A negative reading is not considered a failure.)"

3.15, second line, delete "of EIA standard RS-469" and substitute "specified herein".

3.17.2 first sentence, delete and substitute: "When nonleaded capacitors are tested as specified in 4.6.13.2, the immersed metallized surface shall be at least 85 percent covered with a smooth solder coating."

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FIGURE 3, example 6, delete and substitute:



Example 6 "

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3.27.3 delete and substitute:

"3.27.3 Marking (chip capacitors except high frequency). Capacitors shall be legibly marked in a contrasting color in accordance with either of the two options. (NOTE: Packaging containers shall be marked with the PIN, capacitance, capacitance tolerance, voltage, "JAN" brand, lot date code, and the Commercial and Government Entity (CAGE) code.) Other markings which in any way interfere with, obscure, or confuse those specified herein are prohibited.

- a. Option A: In accordance with table VII.
- b. Option B: In accordance with table VII-1 using a two character system. The first character shall be an alphabetic symbol and shall designate the first and second significant figures. The second character shall be a numerical digit and shall designate the decimal multiplier of capacitance in pF (e.g., A1 =  $1 \times 10^1 = 10$  pF, J5 =  $2.2 \times 10^5 = 0.22 \times 10^6 = 0.22 \mu\text{F}$ ). The marking shall appear in black or legible contrast. The size and orientation of the marking shall be the option of the manufacturer. At the option of the manufacturer, the capacitor may be laser marked with the manufacturer's trademark or symbol and the capacitance code in accordance with table VII-1.

Additional marking may appear provided that it does not interfere with the required marking. "

Add the following table:

" TABLE VII-1 Optional marking for chip capacitors.

| First character      |                     |                      |                     | Second character    |                    |
|----------------------|---------------------|----------------------|---------------------|---------------------|--------------------|
| Alphabetic character | Significant figures | Alphabetic character | Significant figures | Numerical character | Decimal multiplier |
| A                    | 1.0                 | T                    | 5.1                 | 0                   | $10^0$             |
| B                    | 1.1                 | U                    | 5.6                 | 1                   | $10^1$             |
| C                    | 1.2                 | V                    | 6.2                 | 2                   | $10^2$             |
| D                    | 1.3                 | W                    | 6.8                 | 3                   | $10^3$             |
| E                    | 1.5                 | X                    | 7.5                 | 4                   | $10^4$             |
| F                    | 1.6                 | Y                    | 8.2                 | 5                   | $10^5$             |
| G                    | 1.8                 | Z                    | 9.1                 | 6                   | $10^6$             |
| H                    | 2.0                 | a                    | 2.5                 | 7                   | $10^7$             |
| J                    | 2.2                 | b                    | 3.5                 | 8                   | $10^8$             |
| K                    | 2.4                 | d                    | 4.0                 | 9                   | $10^9$             |
| L                    | 2.7                 | e                    | 4.5                 |                     |                    |
| M                    | 3.0                 | f                    | 5.0                 |                     |                    |
| N                    | 3.3                 | m                    | 6.0                 |                     |                    |
| P                    | 3.6                 | n                    | 7.0                 |                     |                    |
| Q                    | 3.9                 | t                    | 8.0                 |                     |                    |
| R                    | 4.3                 | y                    | 9.0                 |                     |                    |
| S                    | 4.7                 |                      |                     |                     |                    |

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3.27.4, delete and substitute:

"3.27.4 Marking (high frequency chip capacitors) These capacitors shall be marked with a contrasting color dot placed on the side of the capacitor to indicate the vertical plate orientation to that side. Capacitors may be laser marked with the manufacturer's trademark or symbol, the two digit or three digit capacitance code, and the tolerance code as shown in the following examples:

|                    | <u>Example 1 (3 lines)</u>                 | <u>Example 2 ( 2 lines)</u>                |
|--------------------|--------------------------------------------|--------------------------------------------|
| (Trademark/Symbol) | XXX                                        | XXX                                        |
| (Capacitance)      | 100 (or A1, 2 digit code; see table VII-1) | 100 F (or A1F) (Capacitance and tolerance) |
| (Tolerance)        | F                                          |                                            |

When parts are laser marked, the marking shall be on the surface which is parallel to the plane of the embedded electrodes (this is the larger area which is normally the imprint area). If the capacitor is so marked, the vertical plate orientation is defined and the contrasting color dot to indicate plate orientation is optional."

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4. delete "QUALITY ASSURANCE PROVISIONS" and substitute "VERIFICATION".

4.1 and 4.1.1, delete.

4.1.2, delete and substitute:

"4.1.2 QPL system. The manufacturer shall establish and maintain a QPL system in accordance with 3.3. Evidence of such compliance is a prerequisite for qualification and retention of qualification."

4.1.3, delete and substitute:

"4.1.3 Manufacturing lot performance information. Lot performance information relating to material, process, lot conformance, inspections, and product shall be retained by the manufacturer for 10 years from the date of the manufacture of the parts."

4.1.3.1, delete.

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4.1.3.2 and 4.1.3.3, delete.

4.3.1, after last sentence, add: "All test temperatures above 25°C shall have a tolerance of +4°C, -0°C unless otherwise specified herein."

4.4.4, delete and substitute:

"4.4.4 Verification of qualification. Every 12 months, the manufacturer shall provide verification of qualification to the qualifying activity. Continuation of qualification shall be based on meeting the following requirements:

- a. MIL-STD-790 program.
- b. Product design has not been modified.
- c. Certification that the manufacturer still maintains the capabilities and facilities necessary to produce these items.
- d. Verification of the results of group A, group B, and group C inspections including identification of failed lots and subgroups and failure modes."

4.5.1, delete and substitute:

"4.5.1 In-process inspection. Each production lot of parts shall be inspected in accordance with table IX. The nondestructive internal examination used (if other than ultrasonic examination) shall be approved by the qualifying activity. Other screening examinations may be applied at the option of the manufacturer, as approved by the qualifying activity."

TABLE IX, under visual examination test, add the following test:

|                                                                 |      |        |                     |   |
|-----------------------------------------------------------------|------|--------|---------------------|---|
| "Post termination, unencapsulated destructive physical analysis | 3.15 | 4.6.11 | Table XV-1, group I | " |
|-----------------------------------------------------------------|------|--------|---------------------|---|

4.5.2.1, first paragraph, delete and substitute: "An inspection/production lot shall consist of all capacitors of a single nominal capacitance/voltage rating of one design, from the same dielectric material batch, and processed as a single lot through all manufacturing steps on the same equipment. The lot may contain all available capacitance tolerances for the nominal capacitance value. In addition, the lot shall conform to the following:"

4.5.2.1.a, first sentence, after "terminations," add "solder,".

4.5.2.1.d, first sentence, delete and substitute: "End termination material shall be consistent in formulation and traceable to a single batch and shall be fired in the same kiln with one temperature profile during the process."

4.5.2.1.e, delete.

4.5.2.1.g, delete and substitute: "The lot date code (LDC) shall be assigned prior to lead attachment for leaded devices and prior to final end termination for nonleaded devices."

TABLE X, inspection column, subgroup 1, thermal shock and voltage conditioning, and voltage conditioning at 85°C tests: Add "3/" (two places).

TABLE X, sampling procedure column, subgroup 3: Delete "XIII" and substitute "XV-1".

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TABLE X, subgroup 4, delete.

TABLE X, bottom of table, after footnote 2/, add:

"3/ The DWV post test is not applicable if optional voltage conditioning was performed at 250 percent or more of the rated voltage."

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4.5.3, delete and substitute:

"4.5.3 Periodic inspection. Periodic inspection shall consist of group C inspection. Delivery of products which have passed group A and group B inspections shall not be delayed pending the results of periodic inspection."

4.5.3.1, delete and substitute:

"4.5.3.1 Group C inspection. Group C inspection shall consist of the tests specified in table XII in the order shown. Samples shall be selected from lots that have passed group A and have been submitted for group B inspection. Separate samples of nonleaded, dual-in-line package, axial, and radial leaded capacitors shall be selected every 2 months in accordance with table XII."

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TABLE XII, delete and substitute:

TABLE XII. Group C inspection.

| Inspection                                                             | Requirement paragraph | Test method paragraph | Number of units to be inspected | Number of defectives permitted |
|------------------------------------------------------------------------|-----------------------|-----------------------|---------------------------------|--------------------------------|
| Subgroup 1 (leaded devices)                                            |                       |                       |                                 |                                |
| Subgroup 1a:<br>Terminal strength                                      | 3.16                  | 4.6.12.1              | 6                               | 1                              |
| Subgroup 1b:<br>Solderability                                          | 3.17.1                | 4.6.13.1              | 6                               |                                |
| Subgroup 1c:<br>Resistance to soldering heat<br>Resistance to solvents | 3.18.1<br>3.22        | 4.6.14.1<br>4.6.18    | 6                               |                                |
| Subgroup 2 (chip devices)                                              |                       |                       |                                 |                                |
| Subgroup 2a:<br>Terminal strength                                      | 3.16                  | 4.6.12.2              | 6                               | 1                              |
| Subgroup 2b:<br>Solderability                                          | 3.17.2                | 4.6.13.2              | 6                               |                                |
| Subgroup 2c:<br>Resistance to soldering heat                           | 3.18.2                | 4.6.14.2              | 6                               |                                |

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4.5.3.2, second sentence, delete "15" and substitute "10".

4.5.4, delete.

4.6.1.1, delete.

4.6.1.2, delete "and as defined in baseline documentation (see 3.3)".

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TABLE XIII, title, delete and substitute: "Pretermination destructive physical analysis sample size."

4.6.3, first sentence, delete "100 percent".

TABLE XIV, sample size column entries, delete and substitute: " 5 samples".

TABLE XIV, footnote " 1 ", delete.

4.6.5.a(1) and 4.6.5.a(2); delete and substitute:

- "a. Number of views: One view perpendicular to the plane of the leads for both axial and radial lead style capacitors (see appendix E, figure E-2)."

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4.6.5.e, delete "15" and substitute "10".

4.6.6.2.1, delete and substitute:

"4.6.6.2.1 Standard voltage conditioning (see 3.10). Standard voltage conditioning shall be started after completion of the thermal shock test. The voltage conditioning shall consist of applying twice the rated voltage to the units at the maximum rated temperature of +125°C for a minimum of 168 hours and a maximum of 264 hours. The voltage conditioning may be terminated at any time during the 168 hour to 264 hour time interval that failures (blown fuses or less than 95 percent voltage) meet the requirements for the PDA during the last 48 hours listed in table XV. Voltage shall be applied and shall reach maximum value within 1 second, maximum. To assure that at least 95 percent of the applied test voltage is maintained for the duration of the exposure period, the circuit on figure 4 shall be used. After completion of the exposure period, the following electrical tests shall be performed:

- a. Insulation resistance (+125°C).
- b. Dielectric withstanding voltage.
- c. Insulation resistance (+25°C).
- d. Capacitance.
- e. Dissipation factor.

The manufacturer has the option of performing these electrical tests in any order except dielectric withstanding voltage shall always precede insulation resistance (+25°C). If the voltage conditioning test is performed with individual fuses in series with each part, any part tested in a position where a fuse fails shall be tested for insulation resistance and dielectric withstanding voltage. If the part meets the initial requirements for insulation resistance and dielectric withstanding voltage, the part shall be rejected but shall not count against the PDA in table XV. The manufacturer also has the option to not test parts with fuse failures and count these toward the PDA."

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TABLE XV, after "PDA last 48 hours during voltage conditioning at +125°C" heading, add "1/".

TABLE XV, after table, add the following:

"1/ For optional voltage conditioning, the time required for meeting the PDA shall be calculated with the T(test) PDA equation in 4.6.6.2.2."

4.6.6.2.2, delete and substitute:

"4.6.6.2.2 Optional voltage conditioning (see 3.10). The manufacturer, with approval from the qualifying activity, may perform an optional voltage conditioning test instead of the standard voltage conditioning test of 4.6.6.2.1. All conditions of 4.6.6.2.1 apply, with the exception of the voltage applied, the test time, and the time required for meeting the PDA. The accelerated condition selected for the optional voltage conditioning shall be used for the duration of the test. At no time shall a combination of standard and optional voltage conditioning be allowed on the same samples. The minimum time duration, T(test) minimum, and the time required for meeting the PDA, T(test) PDA, shall be calculated as follows:

$$T(\text{test}) \text{ minimum} = \frac{1344}{(E \text{ test}/E \text{ rated})^3}$$

$$T(\text{test}) \text{ PDA} = \frac{384}{(E \text{ test}/E \text{ rated})^3}$$

Where:  $2 \times E \text{ rated} \leq E \text{ test} \leq 4 \times E \text{ rated}$

T(test) minimum = Minimum test time in hours

T(test) PDA = Time required for meeting the PDA

E test = Applied voltage

E rated = Rated voltage of the capacitor "

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4.6.7, NOTE; delete.

4.6.9.1.a, delete "250 percent" and substitute "250 percent to 400 percent".

4.6.9.2, title, delete and substitute: "Body insulation (qualification only)".

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4.6.11, delete and substitute:

"4.6.11 Destructive physical analysis (see 3.4.1 and 3.15). Capacitors shall be examined in accordance with 4.6.11.1 (group 1), 4.6.11.2 (group 2), and table XV-1.

4.6.11.1 Group 1.

4.6.11.1.1 Leaded capacitors. After lead attachment and before encapsulation, or after removing the encapsulation. Group 1 samples shall be inspected for lead attachment, other assembly-related defects in accordance with appendix A of EIA-469, and the applicable criteria of appendix B of this specification.

4.6.11.1.2 Nonleaded capacitors. To be performed after the application of the final termination coating. The criteria of appendix C of this specification shall be used.

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4.6.11.2 Group 2.

4.6.11.2.1 Leaded capacitors. Without removing the encapsulation. Group 2 samples shall be inspected in accordance with appendix B of EIA-469 and for the following encapsulation defects:

- a. Voids between the encapsulant and the capacitor body or lead wires.
- b. Cracks or voids in the encapsulation. There shall be no voids in the encapsulant greater in diameter than 50 percent of the encapsulant wall thickness.

4.6.11.2.2 Nonleaded capacitors. The group 2 samples shall be inspected in accordance with 5.1.7 through 5.1.9 inclusive, of EIA-469. Primary metallization shall only be included if it was not included in the chip lot in-process DPA.

TABLE XV-1. Destructive physical analysis sample size.

| Lot size         | Minimum sample size <u>1/</u> |                   |
|------------------|-------------------------------|-------------------|
|                  | Group 1 <u>2/</u>             | Group 2 <u>3/</u> |
| 1 - 500          | 5                             | 3                 |
| 501 - 10,000     | 10                            | 4                 |
| 10,001 - 35,000  | 25                            | 7                 |
| 35,001 - 500,000 | 40                            | 10                |

1/ No failures allowed.

2/ See 4.6.11.1.

3/ See 4.6.11.2. "

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\* 4.6.13.2.a, delete.

4.6.13.2.b, at the end of the sentence add: "or the entire capacitor may be immersed."

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4.6.15, delete and substitute:

"4.6.15 Voltage-temperature limits (see 3.19). The temperature of each capacitor shall be varied as specified in table XVI. Capacitance measurements shall be made at the frequency and voltage specified in 4.6.7. The dc rated voltage need only be applied to the capacitor in each of step E through step G inclusive, until voltage stability is reached and the capacitance measurement is made. Capacitance measurements shall be made at each step specified in table XVI and at a sufficient number of intermediate points between step B and step G to establish a true characteristic curve. Capacitance measurements at each temperature shall be taken at 5 minute intervals and shall be stopped and recorded when two successive readings indicate a capacitance change of less than one percent."

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4.6.16.1.c, delete and substitute:

- "c. Final measurements: On completion of the above test, remove capacitors from the chamber and allow 3 hours, 30 minutes, ± 30 minutes to dry and stabilize at +25°C before performing the insulation resistance (IR), through a 100 kilohm resistor at 1.3 volts ± 0.25 volts, and capacitance in accordance with 4.6.10 and 4.6.7, respectively."

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4.6.19.d, delete and substitute:

"d. Capacitors shall be subjected to the voltage and circuit specified in 4.6.6.2.1. In the event of a fuse failure, the procedure specified in 4.6.6.2.1 shall apply."

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5.1, delete and substitute:

"5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department or Defense Agency, or within the Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity."

6.2, add:

"e. Packaging requirements".

6.3, third sentence, delete and substitute: "The activity responsible for the Qualified Products List is the Defense Supply Center Columbus (DSCC-VQP), 3990 East Broad Street, Columbus, OH 43216-5000."

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10.1, first and second sentences, delete and substitute: "This appendix specifies the procedure for the ultrasonic examination of CKS ceramic capacitors."

20, delete and substitute: "20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix."

20.1, delete.

30. through 30.7 inclusive, delete.

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40.1, delete and substitute:

"40.1 Equipment. The test equipment used shall be capable of performing the required tests. The ultrasonic test equipment shall be cleaned and maintained in accordance with the test equipment manufacturer's instructions."

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40.1.a through 40.1.i inclusive, delete.

40.3, delete.

40.4, delete and substitute:

"40.4 Operating procedure. The test facility shall establish a setup and operating procedure in accordance with the applicable test equipment manufacturer's instructions."

40.5, first sentence, delete and substitute: "Each facility shall have a responsible person who has successfully completed a nondestructive testing course for the ultrasonic test equipment."

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Footnote " 1/ ", bottom of page, delete.

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40.6, delete and substitute:

"40.6 Equipment usage. Testing shall be done in accordance with the test equipment manufacturer's instructions and the test facility's operating procedures."

40.7, delete and substitute:

"40.7 Verification. The test facility shall maintain adequate verification of the results of the ultrasonic examination."

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40.3 and FIGURE B-8, delete.

PAGE 50

30.2.2.d, first sentence, delete and substitute:

"Edge chip-outs shall not be greater in depth than .003 inch (0.08 mm) with respect to either plane."

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FIGURE C-7, delete and substitute:

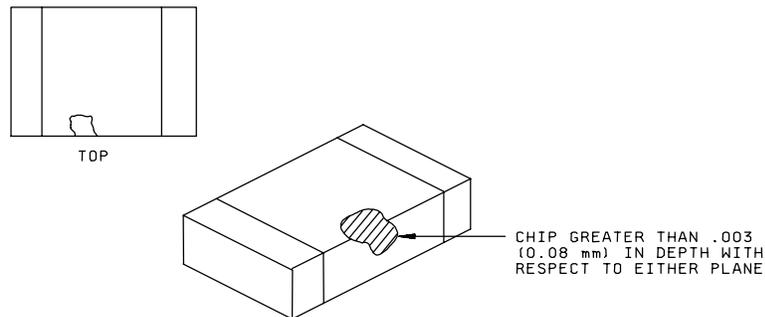


FIGURE C-7. Chip-outs. "

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30.1, delete and substitute:

"30.1 Gauge and test stand. The test equipment used shall be capable of performing the required tests."

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40.1, second sentence, delete "until rupture occurs." and substitute "until the limits specified in table XIV are exceeded."

40.1, last sentence, delete.

40.2, delete and substitute:

"40.2 Axial devices. Firmly clamp both leads into the test fixture. Gradually apply an increasing force (see figure D-1) until the limits specified in table XIV are exceeded."

40.3.a, delete and substitute:

"a. Place the DIP device in the test fixture in accordance with the test equipment instructions and the test facility's operating procedure."

40.3.b, first sentence, delete "until a rupture occurs." and substitute "until the limits specified in table XIV are exceeded."

40.3.c, delete.

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FIGURE D-1, delete and substitute:

"

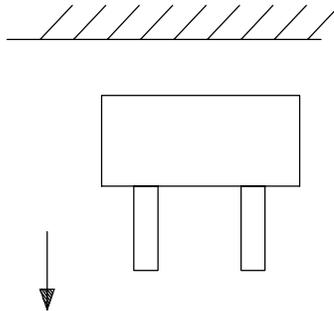


FIGURE D-1. Lead-pull direction."

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FIGURE D-2, delete.

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Add:

"10.4 Alternative x-ray system and procedures. The manufacturer has the option, with the qualifying activity approval, to use an alternative x-ray system and procedures to detect the defect criteria identified in this specification. This alternative system and procedures shall be documented in the MIL-STD-790 program.

PAGE 71

APPENDIX G, delete.

PAGE 75

30.4, first sentence, delete "and the baseline documentation".

The margins of this amendment are marked with an asterisk to indicate where changes from the previous amendment were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous amendment.

Custodians:  
Navy - EC  
Air Force - 19  
DLA - CC  
NASA - NA

Preparing activity:  
DLA - CC  
(Project 5910-2149)

Review activities:  
Army - CR  
Air Force -11