The documentation and process conversion measures necessary to comply with this revision shall be completed by 20 June 2007

INCH - POUND

MIL-STD-750E
20 November 2006
SUPERSEDING
MIL-STD-750D
28 FEBRUARY 1995

DEPARTMENT OF DEFENSE

TEST METHOD STANDARD

TEST METHODS FOR SEMICONDUCTOR DEVICES

AMSC N/A

FSC 5961

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FOREWARD

1. This Standard is approved for use by all Departments and Agencies of the Department of Defense.

2. This entire standard has been revised.

3. Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAT, 3990 E. Broad Street, Columbus, OH 43218-5000, or emailed to semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

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Test Methods

Method number	Title
Environmental tests (1000 series).	
1001.2	Barometric pressure (reduced).
1011.1	Immersion.
1015.1	Steady-state primary photocurrent irradiation procedure (electron beam).
1016	Insulation resistance.
1017.1	Neutron irradiation.
1018.3	Internal gas analysis.
1019.5	Steady-state total dose irradiation procedure.
1020.2	Electrostatic discharge sensitivity (ESDS) classification.
1021.3	Moisture resistance.
1022.5	Resistance to solvents.
1026.5	Steady-state operation life.
1027.3	Steady-state operation life (sample plan).
1031.5	High-temperature life (nonoperating).
1032.2	High-temperature (nonoperating) life (sample plan).
1033	Reverse voltage leakage stability
1036.3	Intermittent operation life.
1037.2	Intermittent operation life (sample plan).
1038.4	Burn-in (for diodes, rectifiers, and zeners).
1039.4	Burn-in (for transistors).
1040	Burn-in (for thyristors (controlled rectifiers)).
1041.3	Salt atmosphere (corrosion).
1042.3	Burn-in and life test for power MOSFET's or insulated gate bipolar transistors (IGBT).
1046.3	Salt spray (corrosion).
1048	Blocking life.
1049	Blocking life (sample plan).
1051.6	Temperature cycling (air to air).
1054.1	Potted environment stress test.
1055.1	Monitored mission temperature cycle.
1056.7	Thermal shock (liquid to liquid).
1057.1	Resistance to glass cracking.
1061.1	Temperature measurement, case and stud.
1066.1	Dew point.
1071.8	Hermetic seal.
1080	Single event burnout and single event gate rupture test.

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Test Methods

Method number	Title
Mechanical characteristics tests (2000 series).	
2005.2	Axial lead tensile test.
2006	Constant acceleration.
2016.2	Shock.
2017.2	Die attach integrity.
2026.11	Solderability.
2031.3	Resistance to soldering heat.
2036.4	Terminal strength.
2037.1	Bond strength.
2046.2	Vibration fatigue.
2051.1	Vibration noise.
2052.4	Particle impact noise detection (PIND) test.
2056	Vibration, variable frequency.
2057.2	Vibration, variable frequency (monitored).
2066	Physical dimensions.
2068	External visual for nontransparent, glass-encased, double plug, noncavity, axial leaded diodes.
2069.2	Pre-cap visual, power MOSFET's.
2070.2	Pre-cap visual microwave discrete and multichip transistors.
2071.6	Visual and mechanical examination.
2072.6	Internal visual transistor (pre-cap) inspection.
2073.1	Internal inspection for die (semiconductor diode).
2074.4	Internal visual inspection (discrete semiconductor diodes).
2075.1	Decap internal visual design verification.
2076.3	Radiography.
2077.3	Scanning electron microscope (SEM) inspection of metallization.
2078	Internal visual for wire bonded diodes/rectifiers
2081	Forward instability, shock (FIST).
2082	Backward instability, vibration (BIST).
2101.1	DPA procedures for diodes.
2102	DPA for wire bonded devices.
2103	Design verification for surface mount devices

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Test Methods

Method number	Title
Electrical characteristics tests for bipolar transistors (3000 series).	
3001.1	Breakdown voltage, collector to base.
3005.1	Burnout by pulsing.
3011.2	Breakdown voltage, collector to emitter.
3015	Drift.
3020	Floating potential.
3026.1	Breakdown voltage, emitter to base.
3030	Collector to emitter voltage.
3036.1	Collector to base cutoff current.
3041.1	Collector to emitter cutoff current.
3051	Safe operating area (continuous dc).
3052	Safe operating area (pulsed).
3053	Safe operating area (switching).
3061.1	Emitter to base cutoff current.
3066.1	Base emitter voltage (saturated or nonsaturated).
3071	Saturation voltage and resistance.
3076.1	Forward-current transfer ratio.
3086.1	Static input resistance.
3092.1	Static transconductance.
Circuit-performance and thermal resistance measurements (3100 series).	
3100	Junction temperature measurement
3101.4	Thermal impedance testing of diodes.
3103	Thermal impedance measurements for insulated gate bipolar transistor (delta gate-emitter on voltage method).
3104	Thermal impedance measurements of GaAs MOSFET's (constant current forward-biased gate voltage method).
3105.1	Measurement method for thermal resistance of a bridge rectifier assembly.
3126	Thermal resistance (collector-cutoff-current method).
3131.5	Thermal impedance measurements for bipolar transistors (delta base-emitter voltage method).
3132	Thermal resistance (dc forward voltage drop, emitter base, continuous method).
3136	Thermal resistance (forward voltage drop, collector to base, diode method).
3141	Thermal response time.
3146.1	Thermal time constant.
3151	Thermal resistance, general.
3161.1	Thermal impedance measurements for vertical power MOSFET's (delta source-drain voltage method).
3181	Thermal resistance for thyristors.
Low frequency tests (3200 series).	
3201.1	Small-signal short-circuit input impedance.
3206.1	Small-signal short-circuit forward-current transfer ratio.
3211	Small-signal open-circuit reverse-voltage transfer ratio.
3216	Small-signal open-circuit output admittance.
3221	Small-signal short-circuit input admittance.
3231	Small-signal short-circuit output admittance.
3236	Open circuit output capacitance.
3240.1	Input capacitance (output open-circuited or short-circuited).
3241	Direct interterminal capacitance.
3246.1	Noise figure.
3251.1	Pulse response.
3255	Large signal power gain.
3256	Small signal power gain.
3261.1	Extrapolated unity gain frequency.
3266	Real part of small-signal short circuit input impedance.

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Test Methods

Method number	Title
High frequency tests (3300 series)	
3301	Small-signal short-circuit forward-current transfer-ratio cutoff frequency.
3306.4	Small-signal short-circuit forward-current transfer ratio.
3311	Maximum frequency of oscillation.
3320	RF power output, RF power gain, and collector efficiency.
Electrical characteristics tests for MOS field-effect transistors (3400 series)	
3401.1	Breakdown voltage, gate to source.
3402	Mosfet gate equivalent series resistance
3403.1	Gate to source voltage or current.
3404	MOSFET threshold voltage.
3405.1	Drain to source on-state voltage.
3407.1	Breakdown voltage, drain to source.
3411.1	Gate reverse current.
3413.1	Drain current.
3415.1	Drain reverse current.
3421.1	Static drain to source on-state resistance.
3423	Small-signal, drain to source on state resistance.
3431	Small-signal, common-source, short-circuit, input capacitance.
3433	Small-signal, common-source, short-circuit, reverse-transfer capacitance.
3453	Small-signal, common-source, short-circuit, output admittance.
3455	Small-signal, common-source, short-circuit, forward transadmittance.
3457	Small-signal, common-source, short-circuit, reverse transfer admittance.
3459	Pulse response (FET).
3461	Small-signal, common-source, short-circuit, input admittance.
3469	Repetitive unclamped inductive switching.
3470.2	Single pulse unclamped inductive switching.
3471.2	Gate charge.
3472.2	Switching time test.
3473.1	Reverse recovery time (t_{rr}) and recovered charge (Q_{rr}) for power MOSFET (drain-to-source) and power rectifiers with t_{rr} • 100 ns.
3474.1	Safe operating area for power MOSFET's or insulated gate bipolar transistors.
3475.1	Forward transconductance (pulsed dc method) of power MOSFET's or insulated gate bipolar transistors.
3476	Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors.
3477.1	Measurement of insulated gate bipolar transistor total switching losses and switching times.
3478.1	Power transistor electrical dose rate test method.
3479	Short circuit withstand time.
3490	Clamped inductive switching safe operating area for MOS gated power transistors.
Electrical characteristics tests for Gallium Arsenide transistors (3500 series)	
3501	Breakdown voltage, drain to source.
3505	Maximum available gain of a GaAs FET.
3510	1 dB compression point of a GaAs FET.
3570	GaAs FET forward gain (Mag S21).
3575	Forward transconductance.

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Test Methods

Method number	Title
Electrical characteristics tests for diodes (4000 series).	
4000	Condition for measurement of diode static parameters.
4001.1	Capacitance.
4011.4	Forward voltage.
4016.4	Reverse current leakage.
4021.2	Breakdown voltage (diodes).
4022	Breakdown voltage (voltage regulators and voltage-reference diodes).
4023.2	Scope display.
4026.3	Forward recovery voltage and time.
4031.4	Reverse recovery characteristics.
4036.1	"Q" for voltage variable capacitance diodes.
4041.2	Rectification efficiency.
4046.1	Reverse current, average.
4051.3	Small-signal reverse breakdown impedance.
4056.2	Small-signal forward impedance.
4061.1	Stored charge.
4064	Avalanche energy test for schottky diodes
4065	Peak reverse power test
4066.4	Surge current.
4071.1	Temperature coefficient of breakdown voltage.
4076.1	Saturation current.
4081.3	Thermal resistance of lead mounted diodes (forward voltage, switching method).
Electrical characteristics tests for microwave diodes (4100 series)	
4101.3	Conversion loss.
4102	Microwave diode capacitance.
4106	Detector power efficiency.
4111.1	Figure of merit (current sensitivity).
4116.1	IF impedance.
4121.2	Output noise ratio.
4126.2	Overall noise figure and noise figure of the IF amplifier.
4131.1	Video resistance.
4136.1	Standing wave ratio (SWR).
4141.1	Burnout by repetitive pulsing.
4146.1	Burnout by single pulse.
4151	Rectified microwave diode current.
Electrical characteristics tests for thyristors (controlled rectifiers) (4200 series)	
4201.2	Holding current.
4206.1	Forward blocking current.
4211.1	Reverse blocking current.
4216	Pulse response.
4219	Reverse gate current.
4221.1	Gate-trigger voltage or gate-trigger current.
4223	Gate-controlled turn-on time.
4224	Circuit-commutated turn-off time.
4225	Gate-controlled turn-off time.
4226.1	Forward "on" voltage.
4231.2	Exponential rate of voltage rise.

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Test Methods

Method number	Title
Electrical characteristics tests for tunnel diodes (4300 series)	
4301	Junction capacitance.
4306.1	Static characteristics of tunnel diodes.
4316	Series inductance.
4321	Negative resistance.
4326	Series resistance.
4331	Switching time.
High reliability space application tests (5000 series)	
5001.2	Wafer lot acceptance testing.
5002	Capacitance-voltage measurements to determine oxide quality.
5010	Clean room and workstation airborne particle classification and measurement.

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1. SCOPE

1.1 Purpose. This standard establishes uniform methods for testing semiconductor devices, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military operations, and physical and electrical tests. For the purpose of this standard, the term "devices" includes such items as transistors, diodes, voltage regulators, rectifiers, tunnel diodes, and other related parts. This standard is intended to apply only to semiconductor devices. The test methods described herein have been prepared to serve several purposes:

a. To specify suitable conditions obtainable in the laboratory that give test results equivalent to the actual service conditions existing in the field, and to obtain reproducibility of the results of tests. The tests described herein are not to be interpreted as an exact and conclusive representation of actual service operation in any one geographic location, since it is known that the only true test for operation in a specific location is an actual service test at that point.

b. To describe in one standard all of the test methods of a similar character which now appear in the various joint-services semiconductor device specifications, so that these methods may be kept uniform and thus result in conservation of equipment, man-hours, and testing facilities. In achieving this objective, it is necessary to make each of the general tests adaptable to a broad range of devices.

c. The test methods described herein for environmental, physical, and electrical testing of devices shall also apply, when applicable, to parts not covered by an approved military sheet-form standard, specification sheet, or drawing.

1.2 Numbering system. The test methods are designated by numbers assigned in accordance with the following system:

1.2.1 Classification of tests. The tests are divided into five areas. Test methods numbered 1001 to 1999 inclusive, cover environmental tests; those numbered 2001 to 2999 inclusive, cover mechanical- characteristics tests. Electrical- characteristics tests are covered in two groups; 3001 to 3999 inclusive, covers tests for transistors and 4001 to 4999 inclusive, covers tests for diodes. Test methods numbered 5000 to 5999 inclusive, are for high reliability space applications.

1.2.2 Revisions. Revisions are numbered consecutively using a period to separate the test method number and the revision number. For example, 4001.1 is the first revision of test method 4001.

1.3 Method of reference. When applicable, test methods contained herein shall be referenced in the individual specification by specifying the method number of this standard, and the details required in the summary of the applicable method. To avoid the necessity for changing specifications that refer to this standard, the revision number should not be used when referencing test methods. (For example: use 4001, not 4001.1.)

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2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this standard. This section does not include documents cited in other sections of this standard or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500	-	Semiconductor Devices, General Specification for.
TT-I-735	-	Isopropyl Alcohol

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202	-	Test Method Standard Electronic and Electrical Component Parts.
MIL-STD-1686	-	Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) (Metric).
MIL-PRF-680	-	Degreasing solvent

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-263	-	Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) (Metric).

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

* 2.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DRAWINGS - JAN

103-JAN	-	Filter for Testing Crystal Rectifier 1N23, 1N23A and 1N23B.
107-JAN	-	Mixer for Testing Crystal Rectifier Type 1N26.
124-JAN	-	Mixer and Coupling Circuit for Crystal Rectifiers 1N21B.
174-JAN	-	Mixer for Electron Tube Type 1N53.
233-JAN	-	Loss Measuring Equipment for 1N25 Crystals Schematic Diagram.
234-JAN	-	Loss Measuring Equipment for 1N25 Crystals Bill of Material.
266-JAN	-	Mixer Holder, Narrow, Band, for 1N263.

DRAWINGS - DESC ASSEMBLY

B66054	-	Adaptor For Burn-Out Test.
C64169	-	Sliding Load (S-Band) Used with D64100.
C65017	-	Assembly, Tri-polar Diode Holder.
C65042	-	Sliding Load (X-Band) Used with D65019.
C65101	-	Sliding Load (Ku-Band) Used with D65064.
C66053	-	Mixer Holder, Narrow Band, for 1N1838.
C66058	-	Burn-Out Tester For Microwave Diodes.
D64100	-	Diode Test Holder, 3,060 MHz (S-Band).
D65019	-	Diode Test Holder, 9,375 GHz (X-Band).
D65064	-	Diode Test Holder, 16 GHz (Ku-Band).

(Copies of these documents are available online at http://www.dscc.dla.mil/Programs/MilSpec or from the Defense Supply Center, DSCC-VAC, P.O. Box 3990, Columbus, Ohio 43218.)

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* 2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ANSI/NCSL-Z540-1-1994

(Copies of this document are available online at http://www.ansi.org or from the American National Standards Institute, 1819 L Street, NW, Suite 600, Washington, DC 20036)

ASME Y14.38M - Abbreviations and Acronyms

(Copies of this document are available online at http://www.asme.org or from the ASME International, Three Park Avenue, New York, NY 10016-5990)

ASTM Test Method D1120 - Standard Test Method for Boiling Point of Engine Coolants
ASTM Test Method D1331 - Standard Test Methods for Surface and Interfacial Tension of Solutions of Surface-Active Agents
ASTM Test Method D2109 - Standard Test Methods for Nonvolatile Matter in Halogenated Organic Solvents and Their Admixtures
ASTM Test Method D877 - Standard Test Method for Dielectric Breakdown Voltage of Insulating Liquids Using Disk Electrodes
ASTM Test Method D941 - Standard Test Method for Density and Relative Density (Specific Gravity) of Liquids by Lipkin Bicapillary Pycnometer
ASTM Test Method D971 - Standard Test Method for Interfacial Tension of Oil Against Water by the Ring Method
ASTM Test Method F134 - Standard Test Methods for Determining Hermeticity of Electron Devices with a Helium Mass Spectrometer Leak Detector
ASTM Test Method F50 - Standard Practice for Continuous Sizing and Counting of Airborne Particles in Dust-Controlled Areas and Clean Rooms Using Instruments Capable of Detecting Single Sub-Micrometre and Larger Particles
ASTM Test Method F25 - Standard Test Method for Sizing and Counting Airborne Particulate Contamination in Cleanrooms and Other Dust-Controlled Areas
ASTM Test Method F-1192 - Standard Guide for he Measurement of Single-Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices

(Copies of these documents are available online at http://www.astm.org or from the American Society for Testing and Materials, P O Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959)

EIA/JESD57 - Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation.

(Copies of this document are available online at http://www.eia.org or from the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834; or from IPC, 2215 Sanders Road, Northbrook, IL 60062-6135.)

NBS Handbook 59 - Permissible Dose From External Sources of Ionizing Radiation, Recommendations of National Committee on Radiation Protection.
NBS Handbook 73 - Protection Against Radiations from Sealed Gamma Sources.
NBS Handbook 76 - Medical X-Ray Protection Up to 3 Million Volts.

(Application for copies should be addressed to the Superintendent of Documents, Washington, DC 20402.)

SAE-ARP-743 - Procedure for the Determination of Particulate Contamination of Air in Dust Controlled Spaces by the Manual Particle Count Method

(Copies of these documents are available online at http://www.sae.org or from the SAE World Headquarters 400 Commonwealth Drive, Warrendale, PA 15096-0001 USA)

Standard Handbook for Electrical Engineers.

(Application for copies should be addressed to the McGraw-Hill Book Company, Inc., New York, N.Y. 42840.)

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2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. DEFINITIONS

3.1 Abbreviations, symbols, and definitions. For the purposes of this standard, the abbreviations, symbols, and definitions specified in MIL-PRF-19500, ASME Y14.38M, and herein shall apply.

3.1.1 Abbreviations used in this standard. Abbreviations used in this standard are defined as follows:

a. ATE - Automatic test equipment.

b. BIST - Backward instability shock test.

c CFM - Cubic Feet per Minute.

d. DPA - Destructive physical analysis.

e. DUT - Device under test.

f. ESD - Electrostatic discharge.

g. ESDS - Electrostatic discharge sensitivity.

h. FET - Field-effect transistor.

i. FIST - Forward instability shock test.

j. FWHM - Full-width half-max.

k. GaAs - Gallium Arsenide.

l. HTRB - High temperature reverse bias.

m. Hz - Hertz.

n. IF - Intermediate frequency.

o IGBT - Insulated gate bipolar transistor.

p. LCC - Leadless chip carrier.

q. LINAC - Linear accelerator.

r. mH - Microhenries.

s. MOSFET - Metal oxide semiconductor field-effect transistor.

t. NIST - National Institute of Standards and Technology.

u. ns - Nanosecond.

v. PIND - Particle impact noise detection.

w. pF - Picofarad.

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x.	RH	-	Relative humidity.
y.	SEM	-	Scanning electron microscope.
z.	SOA	-	Safe operating area.
aa.	SSOP	-	Steady-state operating power.
bb.	STU	-	Sensitivity test unit.
cc.	SWR	-	Standing wave ratio.
dd.	TLD	-	Thermoluminescence dosimetry.
ee.	TSP	-	Temperature sensitive parameter.
ff.	UHF	-	Ultra high frequency.

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4. GENERAL REQUIREMENTS

4.1 Test conditions. Unless otherwise specified herein or in the individual specification, all measurements and tests shall be made at thermal equilibrium at an ambient temperature of 25°C ±3°C and at ambient atmospheric pressure and relative humidity and the specified test condition C (at environmentally elevated and reduced temperatures) shall have a tolerance of ±3 percent or +3°C, whichever is greater. Whenever these conditions must be closely controlled in order to obtain reproducible results, the referee conditions shall be as follows: Temperature 25°C ±1°C, relative humidity 50 ±5 percent, and atmospheric pressure from 650 to 800 millimeters of mercury. Unless otherwise specified in the detail test method, for mechanical test methods, 2000 series, the ambient temperature may be 25°C ±10°C.

4.1.1 Permissible temperature variation in environmental chambers. When chambers are used, specimens under test shall be located only within the working area defined as follows:

a. Temperature variation within working area: The controls for the chamber shall be capable of maintaining the temperature of any single reference point within the working area within ±2°C or ±4 percent, whichever is greater.

b. Space variation within working area: Chambers shall be so constructed that, at any given time, the temperature of any point within the working area shall not deviate more than ±3°C or ±3 percent, whichever is greater, from the reference point, except for the immediate vicinity of specimens generating heat.

c. Chambers with specified minimum temperatures (such as those used in burn-in and life tests): When test requirements involve a specified minimum test temperature, the controls and chamber construction shall be such that the temperature of any point within the working area shall not deviate more than +8°C, -0°C; or +8 percent, -0 percent, whichever is greater, from the specified minimum temperature, except for the immediate vicinity of the specimens generating heat.

4.1.2 Electrical test frequency. Unless otherwise specified, the electrical test frequency shall be 1,000 ±25 Hertz (Hz).

4.1.3 Accuracy. The specified limits are for absolute (true) values, obtained with the specified (nominal) test conditions. Proper allowance shall be made for measurement errors (including those due to deviations from nominal test conditions) in establishing the working limits to be used for the measured values, so that the true values of the device parameters (as they would be under nominal test conditions) are within the specified limits.

The following electrical test tolerances and precautions, unless otherwise specified in the applicable acquisition document, shall be maintained for all device measurements to which they apply (3000, 4000 series and other specified electrical measurements). Wherever test conditions are specified in the applicable acquisition document to a precision tighter than the tolerances indicated below, the specified conditions shall apply and take precedence over these general requirements.

a. Bias conditions shall be held to within 3 percent of the specified value.

b. Such properties as input pulse characteristics, repetition rates, and frequencies shall be held to within 10 percent. Nominal values should be chosen so that ±10 percent variation (or the actual test equipment variation, if less than 10 percent) does not affect the accuracy or validity of the measurement of the specified value.

c. Voltages applied in breakdown testing shall be held within 1 percent of specified value.

d. Resistive loads shall be ±5 percent tolerance.

e. Capacitive loads shall be ±10 percent or ±1 picofarad (pF) tolerance, whichever is greater.

f. Inductive loads shall be ±10 percent or ±5 microhenries (mH) tolerance, whichever is greater.

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g. Static parameters shall be measured to within 1 percent.

h. Switching parameters shall be measured to within 5 percent or 1 nanosecond (ns), whichever is greater.

4.1.3.1 Test methods and circuits. Unless otherwise stated in the specific test method, the methods and circuits shown are given as the basic measurement method. They are not necessarily the only method or circuit which can be used, but the manufacturer shall demonstrate to the acquiring activity that alternate methods or circuits which they may desire to use are equivalent and give results within the desired accuracy of measurement (see 4.1.3).

4.1.4 Calibration requirements. Calibration and certification procedures shall be provided in accordance with ANSI/NCSL-Z540-1-1994 for plant standards and instruments used to measure or control production processes and semiconductor devices under test. For those measurements that are not traceable to the National Institute of Standards and Technology (NIST), correlation samples shall be maintained and used as the basis of proving acceptability when such proof is required. In addition, the following requirements shall apply:

a. The accuracy of a calibrating instrument shall be at least four times greater than that of the item being calibrated, unless the item being calibrated is state of the art equipment, which may be near or equal in accuracy to the state of the art calibrating equipment, in which case the four time requirement does not apply. However, the instrument shall be calibrated to correlate with standards established by the NIST.

b. Except in those cases where the NIST recommends a longer period and concurrence is obtained from the qualifying activity, calibration intervals for plant electrical standards shall not exceed one year, and for plant mechanical standards shall not exceed two years.

4.2 Orientations:

X is the orientation of a device with the main axis of the device normal to the direction of the accelerating force, and the major cross section parallel to the direction of the accelerating force.

Y is the orientation of a device with the main axis of the device parallel to the direction of the accelerating force, and the principal base toward (Y_1), or away from (Y_2), the point of application of the accelerating force.

Z is the orientation of a device with the main axis and the major cross section of the device normal to the direction of the accelerating force. Z is 90 degrees of X.

NOTE: For case configurations, other than those shown on figures 1 and 2, the orientation of the device shall be as specified in the individual specification.

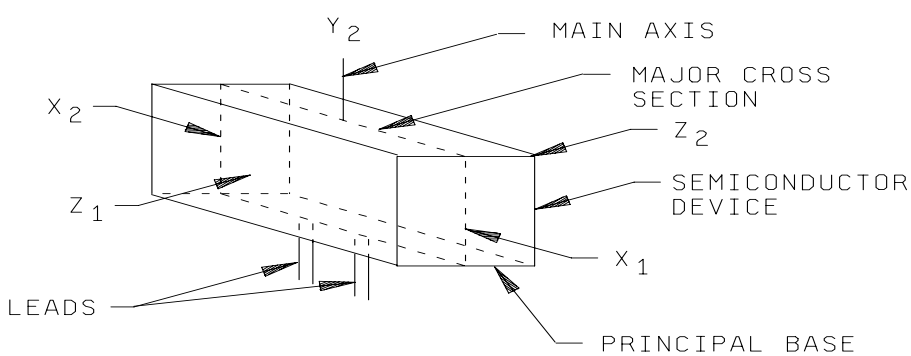

FIGURE 1. Orientation of noncylindrical semiconductor device to direction of accelerating force.

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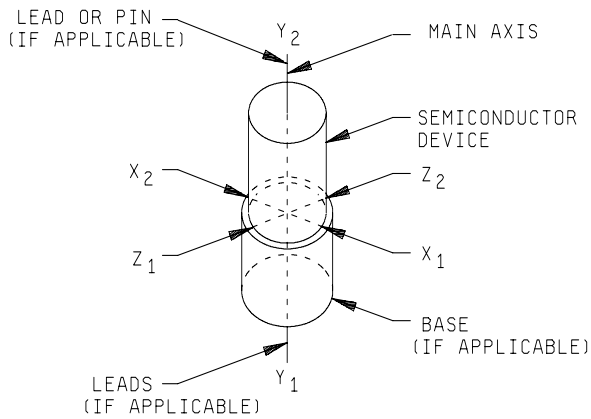

FIGURE 2. Orientation of cylindrical semiconductor device to direction of accelerating force.

4.3 General precautions. The following precautions shall be observed in testing the devices.

4.3.1 Transients. Devices shall not be subjected to conditions in which transients cause the rating to be exceeded.

4.3.2 Test conditions for electrical measurements. Unless otherwise required for a specified test method, semiconductor devices should not be subjected to any condition that will cause any maximum rating of the device to be exceeded. The precautions should include limits on maximum instantaneous currents and applied voltages. High series resistances (constant current supplies) and low capacitances are usually required. If low cutoff, or reverse current devices are to be measured; for example, nanoampere units, care should be taken to ensure that parasitic circuit currents or external leakage currents are small, compared with the cutoff or reverse current of the device to be measured.

4.3.2.1 Steady-state dc measurements (method 4000). Unless otherwise specified, all steady-state dc parameters are defined using steady-state dc conditions.

4.3.2.2 Pulse measurements (method 4000). When device static or dynamic parameters are measured under pulsed conditions, in order to avoid measurement errors introduced by device heating during the measurement period, the following items should be covered in the performance specification sheet:

a. The statement "pulsed test" shall be placed by the test specified.

b. Unless otherwise specified, the pulse time (t_p) shall be ≤10 milliseconds and the duty cycle shall be a maximum of 2 percent; within this limit the pulse must be long enough to be compatible with test equipment capability and the accuracy required, and short enough to avoid heating.

4.3.3 Test circuits. The circuits shown are given as examples which may be used for the measurements. They are not necessarily the only circuits which can be used but the manufacturer shall demonstrate to the Government that other circuits which they may desire to use will give results within the desired accuracy of measurement. Circuits are shown for PNP transistors in one circuit configuration only. They may readily be adapted for NPN devices and for other circuit configurations.

4.3.3.1 Test method variation. Variation from the specified test methods used to verify the electrical parameters are allowed provided that it is demonstrated to the preparing activity or their agent that such variations in no way relax the requirements of this specification and that they are approved before testing is performed. For proposed test variations, a test method comparative error analysis shall be made available for checking by the preparing activity or their agent.

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4.3.4 Soldering. Adequate precautions shall be taken to avoid damage to the device during soldering required for tests.

4.3.5 Order of connection of leads. Care should be taken when connecting a semiconductor device to a power source. The common terminal shall be connected first.

4.3.6 Radiation precautions. Due precautions shall be used in storing or testing semiconductor devices in substantial fields of X-rays, neutrons, or other energy particles.

4.3.7 Handling precautions.

4.3.7.1 UHF and microwave devices. Handling precautions for UHF and microwave devices shall be as follows:

a. Ground all equipment.

b. Make hand contact to the equipment while holding the base end and maintain hand contact with the equipment until the device is in place.

c. Where applicable, keep devices in metal shields until they are inserted in the equipment or until necessary to remove for test.

4.3.7.2 Electrostatic discharge sensitive devices. Handling precautions shall be observed in accordance with MIL-HDBK-263 during testing of Electrostatic Discharge Sensitive (ESDS) devices. The area where ESDS device tests are performed shall meet the requirements of an ESD Protected Area of MIL-STD-1686.

4.4 Continuity verification of burn-in and life tests. The test setup shall be monitored at the test temperature initially and at the conclusion of the test to establish that all devices are being stressed to the specified requirements. The following is the minimum acceptable monitoring procedure:

a. Device sockets. Initially and at least each 6 months thereafter, each test board or tray shall be checked to verify continuity to connector points to assure that the correct voltage bias will be applied. Except for this initial and periodic verification, each device or device socket does not have to be checked; however, random sampling techniques shall be applied prior to each time a board is used and shall be adequate to assure that there are correct and continuous electrical connections to the Device under test (DUT).

b. Connectors to test boards or trays. After the test boards are loaded with devices, inserted into the system, and brought up to the specified operating conditions, each required test voltage and signal condition shall be verified in at least one location on each test board or tray so as to assure electrical continuity and the correct application of specified electrical stresses for each connection or contact pair used in the applicable test configuration. The system may be opened for a maximum of 10 minutes.

c. At the conclusion of the test period, prior to removal of devices from temperature and bias conditions, the voltage and signal condition verification of 4.4b shall be repeated.

d. For class S devices, each test board or tray and each test socket shall be verified prior to test to assure that the specified bias conditions are applied to each device. This may be accomplished by verifying the device functional response at each device output(s) or by performing a socket verification on each socket prior to loading. An approved alternate procedure may be used.

4.4.1 Bias interruption. Where failures or open contacts occur which result in removal of the required bias stresses for any period of the required bias duration, the bias time shall be extended to assure actual exposure for the total minimum specified test duration. Any loss(es) or interruption(s) of bias in excess of 10 minutes total duration while the chamber is at temperature during the final 8 hours of burn-in shall require extension of the bias duration for an uninterrupted 8 hours minimum, after the last bias interruption.

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4.5 Requirements for High Temperature Reverse Bias (HTRB) and burn-in.

a. The temperature of +20°C minimum is the ambient air temperature to which all devices should be exposed during power screening where room ambient is specified.

b. An increase in effective ambient temperature from cumulative induced power to DUTs shall not result in device junction temperature exceeding maximum ratings.

c. Ambient temperature shall not be measured in the convection current (above) or downstream (Fan Air) of DUTs.

d. Moving air greater than 30 CFM (natural convection) may be allowed for the purpose of temperature equalization within high device density burn-in racks.

e. High velocity or cooled air shall not be used for the purpose of increasing device ratings.

f. Power up of burn-in racks may occur when ambient is less than specified. When thermal equilibrium has been reached, or five hours maximum has occurred, the ambient shall be at the specified value. Time accrued prior to reaching specified ambient shall not be chargeable to the life test duration.

g. If the ambient, at or beyond the five hour point is not the specified value, a nonconformance shall exist requiring corrective action.

h. Time is not chargeable during the period when specified conditions are not maintained. If device maximum ratings (if life test, finish the test and use for credit; if shippable, use this criteria) are exceeded and the manufacturer intends to submit the lot affected, the product on test shall be evaluated by re-starting the burn-in or HTRB from zero hours at the specified temperature and verifying that the end-point failure rate is typical for this product type from a review of established records.

i. Chamber temperature for HTRB and burn-in shall be controlled to ±3 percent of the specified value (unless otherwise specified in 4.1.1). This temperature shall be maintained within the chamber. Forced air may be used to equalize temperature within the chamber but shall not be used as a coolant to increase device power capability.

4.6 Bias requirements.

a. Bias errors at the power supply source caused by changing power supply loads during temperature transitions shall not exceed ±5 percent of that specified value.

b. Bias values at the source, during stabilized conditions, shall not exceed ±3 percent of the specified value.

c. Burn-in apparatus shall be arranged so as to result in the approximate average power dissipation for each device whether devices are tested individually or in a group. Bias and burn-in circuitry tolerances should not vary test conditions to individual devices by more than ±5 percent of specified conditions.

d. Normal variation in individual device characteristics need not be compensated for by burn-in circuitry.

e. Burn-in equipment shall be arranged so that the existence of failed or abnormal devices in a group does not negate the effect of the test for other devices in the group. Periodic verification will assure that specified conditions are being maintained. Verification shall be performed, as a minimum, at the starting and the end of screening.

f. Lead, stud, or case mounted devices shall be mounted in their normal mounting configuration and the point of mechanical connection shall be maintained at no less than the specified ambient.

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4.7 Destructive tests. Unless otherwise demonstrated, the following MIL-STD-750 tests are classified as destructive:

Method Number	Test
1017	Neutron irradiation
1019	Steady-state total dose irradiation
1020	ESDS classification
1021	Moisture resistance
1036,1037	Intermittent operation life
1041	Salt atmosphere
1042 (Condition D)	Burn-in/life test for power MOSFETs
1046	Salt spray
1056	Thermal shock (glass strain)
2017	Die shear test
2031	Soldering heat
2036	Terminal strength
2037	Post seal bond strength
2075	Decap internal visual design verification
2077	SEM

All other mechanical or environmental tests (other than those listed in 4.8) shall be considered destructive initially, but may subsequently be considered nondestructive upon accumulation of sufficient data to indicate that the test is nondestructive. The accumulation of data from five repetitions of the specified test on the same sample of product, without significant evidence of cumulative degradation in any device in the sample, is considered sufficient evidence that the test is nondestructive for the device of that manufacturer. Any test specified as a 100-percent screen shall be considered nondestructive for the stress level and duration or number of cycles applied as a screen.

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4.8 Nondestructive tests. Unless otherwise demonstrated, the following MIL-STD-750 tests are classified as nondestructive:

Method number	Test
1001	Barometric pressure
1022	Resistance to solvents
1026, 1027	Steady-state life
1031, 1032	High temperature life (non-operating)
1038, 1039, 1040	Burn-in screen
1042 (Condition A, B, and C)	Burn-in/life test for power MOSFETs
1051 (100 cycles or less)	Thermal shock (temperature cycling)
1071	Hermetic seal tests
2006	Constant acceleration
2016	Shock
2026	Solderability (if the original lead finish is unchanged and if the maximum allowable number of reworks is not exceeded.)
2052	PIND test
2056	Vibration, variable frequency
2066	Physical dimensions
2069, 2070, 2072, 2073, 2074	Internal visual (pre-cap)
2071	External visual
2076	Radiographic inspection
2081	FIST
2082	BIST
3101	Thermal impedance testing of diodes
3103	Thermal impedance measurements for IGBTs
3104	Thermal impedance measurements for GaAs
3051, 3052, 3053 (with limited supply voltage)	SOA (condition A for method 3053)
3131	Thermal resistance (emitter to base forward voltage, emitter-only switching method)
4066	Surge current
4081	Thermal resistance of lead mounted diode (forward voltage, switching method)

When the junction temperature exceeds the device maximum rated junction temperature for any operation or test (including electrical stress test), these tests shall be considered destructive except under transient surge or nonrepetitive fault conditions or approved accelerated screening when it may be desirable to allow the junction temperature to exceed the rated junction temperature. The feasibility shall be determined on a part by part basis and in the case where it is allowed adequate sample testing, shall be performed to provide the proper reliability safeguards.

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4.9 Laboratory suitability. Prior to processing any semiconductor devices intended for use in any military system or sub-system, the facility performing the test(s) must be audited by the Defense Electronics Supply Center, Sourcing and Qualification Division (DESC-ELST) and be granted written Laboratory Suitability status for each test method to be employed. Processing of any devices by any facility without Laboratory Suitability status for the test methods used shall render the processed devices nonconforming.

4.10 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

5. DETAILED REQUIREMENTS

This section is not applicable to this standard.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended Use. The intended use of this standard is to establish appropriate conditions for testing semiconductor devices to give test results that simulate the actual service conditions existing in the field. This standard has been prepared to provide uniform methods, controls, and procedures for determining with predictability the suitability of such devices within Military, Aerospace and special application equipment.

6.2 International standardization agreement. Certain provisions of this standard are the subject of international standardization agreement. When amendment, revision, or cancellation of this standard is proposed which will affect or violate the international agreement concerned, the preparing activity will take appropriate reconciliation action through international standardization channels, including departmental standardization offices, if required.

6.3 Subject term (key word) listing.

Environmental tests
Mechanical characteristics tests
Electrical characteristics tests for bipolar transistors
Circuit-performance and thermal resistance measurements
Low frequency tests
High frequency tests
Electrical characteristics tests for MOS field-effect transistors
Electrical characteristics tests for Gallium Arsenide transistors
Electrical characteristics tests for diodes
Electrical characteristics tests for microwave diodes
Electrical characteristics tests for tunnel diodes
High reliability space application tests

6.4 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extent of the changes.

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1000 Series

Environmental tests

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METHOD 1001.2

BAROMETRIC PRESSURE (REDUCED)

1. Purpose. The purpose of this test is to check the device capabilities under conditions simulating the low pressure encountered in the nonpressurized portions of aircraft in high altitude flight.

2. Apparatus. The apparatus used for the barometric-pressure test shall consist of a vacuum pump and a suitable sealed chamber having means for visual observation of the specimen under test when necessary. A suitable pressure indicator shall be used to measure the simulated altitude in feet in the sealed chamber.

3. Procedure. The specimens shall be mounted in the test chamber as specified and the pressure reduced to the value indicated in one of the following test conditions, as specified. Previous references to this method do not specify a test condition; in such cases, test condition B shall be used. While the specimens are maintained at the specified pressure, and after sufficient time has been allowed for all entrapped air in the chamber to escape, the specimens shall be subjected to the specified test.

Test condition	Pressure - Maximum		Altitude	
	Inches of mercury	Millimeters of mercury	Feet	Meters
A	8.88	226.00	30,000	9,144
B	3.44	87.00	50,000	15,240
C	1.31	33.00	70,000	21,336
D	0.315	8.00	100,000	30,480
E	0.043	1.09	150,000	45,720
F	17.300	439.00	15,000	4,572
G	9.436×10^{-8}	2.40×10^{-6}	656,000	200,000

In addition the following is required:

a. Twenty minutes before and during the test, the test temperature shall be +25°C ±3°C.

b. The specified voltage shall be applied and monitored over the range from atmospheric pressure to the specified minimum pressure and returned so that any device malfunctions, if they exist, will be detected.

4. Failure criteria. A device which exhibits arc-overs, harmful coronas, or any other defect or deterioration that may interfere with the operation of the device shall be considered a failure.

5. Summary. The following conditions must be specified in the performance specification sheet:

a. Voltage (see 3.b.).

b. Maximum pressure (see 3.b).

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METHOD 1011.1

IMMERSION

1. Purpose. This test is performed to determine the effectiveness of the seal of component parts. The immersion of the part under evaluation into liquid at widely different temperatures subjects it to thermal and mechanical stresses which will readily detect a defective terminal assembly, or a partially closed seam or molded enclosure. Defects of these types can result from faulty construction or from mechanical damage such as might be produced during physical or environmental tests. The immersion test is generally performed immediately following such tests because it will tend to aggravate any incipient defects in seals, seams, and bushings which might otherwise escape notice. This test is essentially a laboratory test condition, and the procedure is intended only as a measurement of the effectiveness of the seal following this test. The choice of fresh or salt water as a test liquid is dependent on the nature of the component part under test. When electrical measurements are made after immersion cycling to obtain evidence of leakage through seals, the use of a salt solution instead of fresh water will facilitate detection of moisture penetration. This test provides a simple and ready means of detection of the migration of liquids. Effects noted can include lowered insulation resistance, corrosion of internal parts, and appearance of salt crystals. The test described is not intended as a thermal-shock or corrosion test, although it may incidentally reveal inadequacies in these respects.

2. Procedure. The test consists of successive cycles of immersions, each cycle consisting of immersion in a hot bath of fresh (tap) water at a temperature of 65°C +5°C, -0°C (149°F +9°F, -0°F) followed by immersion in a cold bath. The number of cycles, duration of each immersion, and the nature and temperature of the cold bath shall be as indicated in the applicable test condition listed in the specified test. .

Test condition	Number of cycles	Duration of each immersion (Minutes)	Immersion bath (cold)	Temperature of cold bath (°C)
A	2	15	Fresh (tap) water	25, +10, -5
B	2	15	Saturated solution of sodium chloride and water.	25, +10, -5
C	5	60	Saturated solution of sodium chloride and water.	0 ± 3

The transfer of specimens from one bath to another shall be accomplished as rapidly as practicable. After completion of the final cycle, specimens shall be thoroughly and quickly washed and all surfaces wiped or air-blasted clean and dry.

3. Measurements. Unless otherwise specified, measurements shall be made at least 4 hours, but not more than 24 hours, after completion of the final cycle. Measurements shall be made as specified.

4. Summary. The following details are to be specified in the individual specification:

a. Test condition letter (see 2).

b. Time after final cycle allowed for measurements, if other than that specified (see 3).

c. Measurements after final cycle (see 3).

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METHOD 1015.1

STEADY-STATE PRIMARY PHOTOCURRENT IRRADIATION PROCEDURE (ELECTRON BEAM)

1. Purpose. This test procedure establishes the means for measuring the steady-state primary photocurrent (I_{PH}) generated in semiconductor devices when these devices are exposed to ionizing radiation. In this test method, the test device is irradiated in the primary electron beam of a linear accelerator (LINAC).

1.1 Definitions. The following definitions shall apply for this test method.

1.1.1 Primary photocurrent (I_{PH}). The flow of excess charge carriers across a P-N junction due to ionizing radiation creating electron-hole pairs in the vicinity of the P-N junction.

1.1.2 Measurement interferences. A current measured in the test circuits that does not result from primary photocurrent (see appendix herein).

2. Apparatus.

2.1 Ionizing pulse source. The ionizing pulse shall be produced by an electron LINAC. The ionizing pulse shall have dose rate variations within ±15 percent of nominal during the pulse and shall consist of electrons with an energy equal to or greater than 10 MeV.

2.2 Pulse recording equipment. Pulse recording equipment shall be provided that will display and record both the photocurrent and the pulse-shape monitor signal. It may consist of oscilloscopes with recording cameras, appropriate digitizing equipment, or other approved recording equipment. The equipment shall have an accuracy and resolution of five percent of the pulse width and maximum amplitude of the ionizing source.

2.3 Test circuits. One of the following test circuits shall be selected, radiation-shielded, and close enough to the DUT in order to meet the requirements of 3.2.

2.3.1 Resistor sampling circuits. The resistor sampling circuits shall be as shown on figure 1015-1.

2.3.2 Current transformer circuit. The current transformer circuit shall be as shown on figure 1015-2.

2.4 Irradiation pulse-shape monitor. One of the following devices shall be used to develop a signal proportional to the dose rate delivered to the DUT. Any time constants which degrade the linear response of the monitor signal shall be less than 10 percent of the beam pulse width. The dose rate at the monitor shall be proportional to the dose rate at the DUT and the variation from proportionality shall not exceed ±3 percent.

2.4.1 Signal diode. The signal diode selected shall have a response that is linear within ±5 percent of the dose rate over the selected irradiation range. Depending on the sensitivity of the diode, it may be positioned at a point within the beam from the ionizing source at which it will remain in the linear region. The signal diode shall be placed in one of the test circuits described in 2.3, and it shall be back biased at not more than fifty percent of the diode breakdown voltage.

2.4.2 P-type-intrinsic-N-type (P-I-N) diode. A P-I-N diode shall be used as stated in 2.4.1.

2.4.3 Current transformer. A transformer with a hollow central axis that shall be mounted around the output of the ionizing source.

2.4.4 Secondary-emission monitor. The secondary-emission monitor shall consist of a thin foil mounted in a chamber evacuated to ≤ .134 Pa (0.01 mmHg), which is located in the path of the beam from the ionizing source. The foil shall be biased negatively with respect to ground, or shielded with positively biased grids.

2.5 Dosimeter. The dosimeter shall be used to calibrate the output of the pulse-shape monitor in terms of dose rate. The dosimeter type shall be a commercial thermoluminescent detector (TLD), thin calorimeter, or other system as specified. The dosimetry measurement technique shall be accurate to ±20 percent.

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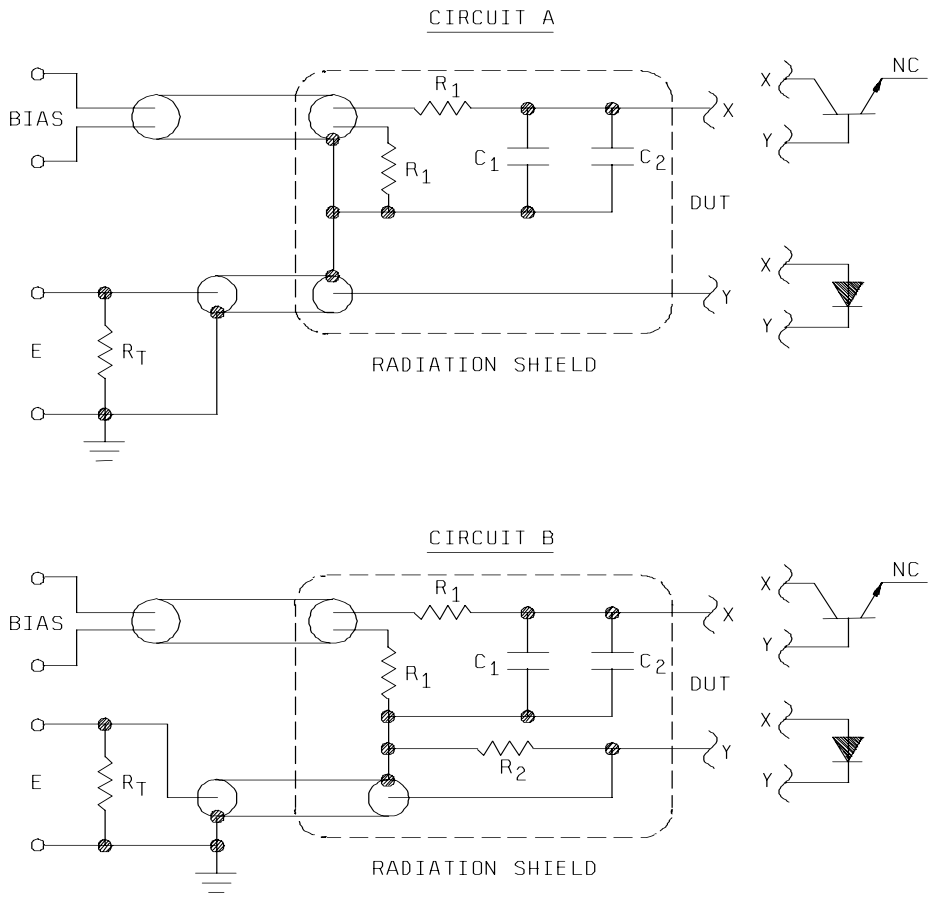

NOTES:

1. R_1 = 1,000 Ω, 5 percent.
2. R_2 = 5 Ω, 1 percent.
3. C_1 = 15 μF, 5 percent.
4. C_2 = .01 μF, 5 percent.
5. R_T = Characteristic termination for coaxial cable.
6. Circuit B shall be used for large photocurrents (those for which more than 10 percent of the bias appears across resistor R_T in circuit A).
7. Photocurrent for circuit A:

$$I_{PH} = \frac{\text{Steady - state signal (E)}}{\text{Cable termination } (R_T)}$$

8. Photocurrent for circuit B:

$$I_{PH} = \frac{[\text{Steady - state signal (E)}][\text{Cable termination } (R_T) + R_2]}{[\text{Cable termination}(R_T)][R_2]}$$

FIGURE 1015-1. Resistor sampling circuits.

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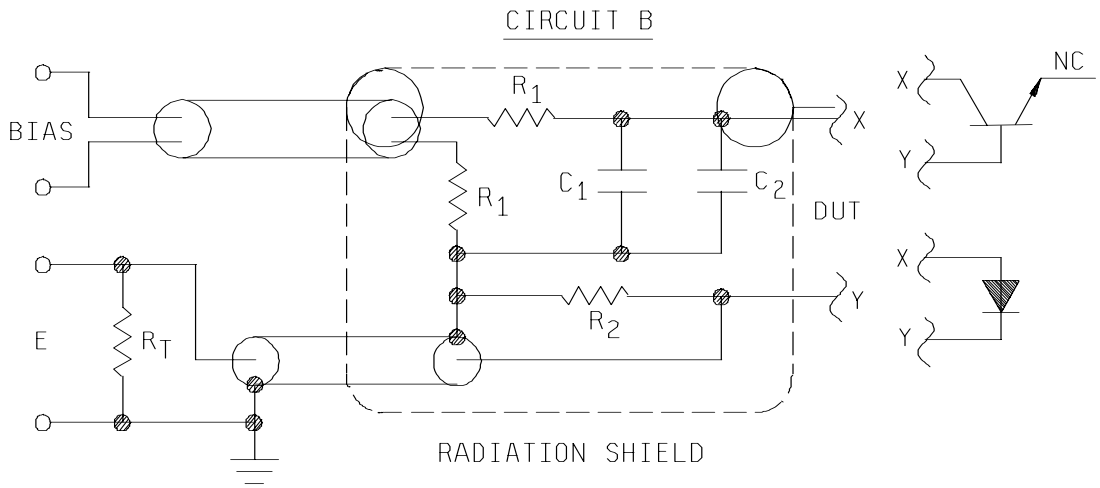

NOTES:

1. R_1 = 1,000 Ω, 5 percent.
2. C_1 = 15 μF, 5 percent.
3. C_2 = .01 μF, 5 percent.
4. R_T = Characteristic termination for coaxial cable.
5. Photocurrent calculation:

$$I_{PH} = \frac{\textit{Steady - state signal (E)}}{\textit{Sensitivity of current transformer}}$$

FIGURE 1015-2. Current transformer circuit.

3. Procedure.

3.1 General. The test facility shall select a test fixture and pulse shape monitor. The test fixture and monitor shall be aligned with the beam from the ionizing source. In addition, any shielding, collimation, or beam scattering equipment shall be properly positioned. If repositioning of any equipment or the test circuit is required to accomplish the device testing, the repositioning shall be demonstrated to be reliable and repeatable.

3.2 Test circuit check-out. The ionizing source shall be pulsed either with an empty device package or without the DUT in the test circuit and with all required bias applied. The ionizing source shall be adjusted to supply the dose rate required for this test. The recorded current from the pulse recording equipment shall be no more than 10 percent of the steady-state photocurrent expected to be measured for this test (see 3.4.3). If this condition is not met, see appendix herein.

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3.3 Ionizing source calibration. Mount the selected dosimeter in place of the DUT. Pulse the ionizing source, record the pulse-shape monitor signal, and determine the radiation dose measured by the dosimeter. Calculate a dose rate factor as follows:

$$Doseratefactor = \frac{Measureddosimeterdose[rad(Si)]}{Integratedpulseshapemonitorsignal(voltsxseconds)}$$

This measurement shall be repeated five times, and the average of the six dose rate factors obtained shall be the dose rate factor used for the test. One dosimeter may be used repetitively if the dose is read for each pulse.

3.4 Device test.

3.4.1 Mounting. Mount the DUT in the beam from the ionizing source and connect it to the rest of the test circuit. The bias applied shall be as specified in the device specification; or if not specified, the bias shall be fifty percent of the specified breakdown voltage of the DUT.

3.4.2 Dose rate. Either adjust the ionizing source beam current or use an alternate method (i.e., scatterers or a different sample location) to obtain the specified dose rate ±20 percent. Pulse the ionizing source and record the pulse-shape monitor signal and the photocurrent signal from the DUT.

3.4.3 Calculate photocurrent. The steady-state photocurrent shall be calculated as expressed on the figure selected for the test circuit in 2.3.

3.4.4 Verify test circuit. Check the current recorded in the test circuit in 3.2 and verify that the value of the current does not exceed 10 percent of the photocurrent recorded in 3.4.3.

3.5 Test circuit checkout. Repeat the device test (see 3.4) for each dose rate that is required by the device specification. The calibration (see 3.3) shall be performed for each dose rate to be tested. The test circuit checkout (see 3.2) shall be performed when a new device type is tested or when any change is made in the position of the test circuit or DUT supporting structure.

4. Summary. The following conditions shall be specified in the performance specification:

a. The pulse width requirements of the ionizing pulse source. (The pulse width must exceed the semiconductor minority lifetime by at least a factor of two .)

b. The bias applied to the device (see 3.4.1).

c. The irradiation dose rate(s) applied (see 3.4.2).

d. When required, any total dose restrictions.

e. When required, a description of the placement of the device in the beam with respect to the junction.

f. When required, for multi-junction devices, the device terminals that are to be monitored.

g. When required, the procedure for approval of the test facility and dosimetry.

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APPENDIX

MEASUREMENT INTERFERENCES

1. Scope. The following problems commonly arise when electronics are tested in a radiation environment. Most of these interferences are present when the test circuit is irradiated under bias with the DUT removed. This Appendix is not a mandatory part of the standard. The information contained herein is intended for guidance only.

1.1 Air ionization. The irradiation pulse can ionize the air around the test circuit and provide a spurious conduction path. The air ionization contribution to the signal is proportional to the applied bias. The effect of air ionization is minimized by reducing the circuit components exposed to the beam pulse, by coating exposed leads with a thick nonconducting layer or by performing the test in a vacuum.

1.2. Secondary emission. The beam pulse irradiating any electrical lead or component can cause a net charge to enter or leave the exposed surfaces. This spurious current alters the measured photocurrent. Secondary emission effects are reduced by minimizing the circuit components exposed to the direct beam.

1.3. Perturbed irradiation field. Any material exposed to the beam pulse will scatter and modify the incident radiation of the beam. A nearby DUT or dosimeter will then be exposed to a noncharacterized and unexpected form of radiation. These field perturbations are reduced by minimizing the mass of the structure supporting the DUT and the dosimeter that is exposed to the beam. All materials should have a low atomic number; e.g., plastics and aluminum.

1.4. RF pickup. The ionizing pulse source discharges large amounts of electromagnetic energy at the same time the photocurrent is being measured. Good electrical practice is necessary to eliminate resonant structure, noise pick-up on signal cables, common mode pick-up, ground loops, and similar interferences.

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METHOD 1016

INSULATION RESISTANCE

1. The device shall be tested in accordance with method 302 of MIL-STD-202.

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METHOD 1017.1

NEUTRON IRRADIATION

1. Purpose. The neutron irradiation test is performed to determine the susceptibility of discrete semiconductor devices to degradation in the neutron environment. This test is destructive. Objectives of the test are:

a. To detect and measure the degradation of critical semiconductor device electrical characteristics as a function of neutron fluence.

b. To determine if specified semiconductor device electrical characteristics are within specified limits after exposure to a specified level of neutron fluence (see 2.4.1 4).

2. Apparatus.

2.1 Test instruments. Test instrumentation to be used in the radiation test shall be standard laboratory electronic test instruments such as power supplies, digital voltmeters, and picoammeters, capable of measuring the electrical parameters required. Parameter test methods and calibration shall be in accordance with this general specification.

2.2 Radiation source. The radiation source used in the test shall be in a TRIGA Reactor or a Fast Burst Reactor. Operation may be in either pulse or steady-state repetitive pulse conditions as appropriate. The source shall be one that is acceptable to the acquiring activity.

2.3 Dosimetry equipment.

a. Fast-neutron threshold activation foils such as ^{32}S, ^{54}Fe, and ^{58}Ni.

b. CaF_2 TLD.

c. Appropriate activation foil counting and TLD readout equipment.

2.4 Dosimetry measurements.

2.4.1 Neutron fluence. The neutron fluence used for device irradiation shall be obtained by measuring the amount of radioactivity induced in a fast-neutron threshold activation foil such as ^{32}S, ^{54}Fe, or ^{58}Ni, irradiated simultaneously with the device. A standard method for converting the measured radioactivity in the specific activation foil employed into a neutron fluence is given in the following (DoD) adopted (ASTM) standards:

ASTM E263	Standard Test Method for Measuring Fast-Neutron Flux by Radioactivation of Iron.
ASTM E264	Standard Test Method for Measuring Fast-Neutron Flux by Radioactivation of Nickel.
ASTM E265	Standard Test Method for Measuring Fast-Neutron Flux by Radioactivation of Sulfur.

The conversion of the foil radioactivity into a neutron fluence requires a knowledge of the neutron spectrum incident on the foil. If the spectrum is not known, it shall be determined by use of the following DoD adopted ASTM standards, or their equivalent:

ASTM E720	Standard Guide for Selection of a Set of Neutron-Activation Foils for Determining Neutron Spectra used in Radiation-Hardness Testing of Electronics.
ASTM E721	Standard Method for Determining Neutron Energy Spectra with Neutron-Activation Foils for Radiation-Hardness Testing of Electronics.
ASTM E722	Standard Practice for Characterizing Neutron Energy Fluence Spectra in Terms of an Equivalent Monoenergetic Neutron Fluence for Radiation-Hardness Testing of Electronics.

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Once the neutron energy spectrum has been determined and the equivalent monoenergetic fluence calculated, then an appropriate monitor foil (such as ^{32}S, ^{54}Fe, or ^{58}Ni) should be used in subsequent irradiations to determine the neutron fluence as discussed in E722. Thus, the neutron fluence is described in terms of the equivalent monoenergetic neutron fluence in accordance with the unit monitor response. Use of a monitor foil to predict the equivalent monoenergetic neutron fluence is valid only if the energy spectrum remains constant.

2.4.2 If absorbed dose measurements of the gamma-ray component during the device test irradiations are required, then such measurements shall be made with CaF_2 TLDs, or their equivalent. These TLDs shall be used in accordance with the recommendations of the following DoD adopted ASTM standard:

E668	Standard Practice for the Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices.

3. Procedure.

3.1 Safety requirements. Neutron irradiated parts may be radioactive. Handling and storage of test specimens or equipment subjected to radiation environments shall be governed by the procedures established by the local Radiation Safety Officer or health physicist.

NOTE: The receipt, acquisition, possession, use, and transfer of this material after irradiation is subject to the regulations of the U.S. Nuclear Regulatory Commission, Radioisotope License Branch, Washington, DC 20555. A by-product license is required before an irradiation facility will expose any test devices. (U.S. Code, see 10 CFR 30-33.)

3.2 Test samples. Unless otherwise specified, a test sample shall be randomly selected and consist of a minimum of ten parts. All sample parts shall have met all the requirements of the governing specification for that part. Each part shall be serialized to enable pre and post test identification and comparison.

3.3 Pre-exposure.

3.3.1 Electrical tests. Pre-exposure electrical tests shall be performed on each part as required. Where delta parameter limits are specified, the pre-exposure data shall be recorded.

3.3.2 Exposure set-up. Each device shall be mounted unbiased and have its terminal leads either all shorted or all open. For Metal oxide semiconductor (MOS) devices all leads shall be shorted. An appropriate mounting fixture which will accommodate both the sample and the required dosimeters (at least one actuation foil and one CaF_2 TLD) shall be used. The configuration of the mounting fixture will depend on the type of reactor facility used and should be discussed with reactor facility personnel. Test devices shall be mounted such that the total variation of fluence over the entire sample does not exceed 20 percent. Reactor facility personnel shall determine both the position of the fixture and the appropriate pulse level or power time product required to achieve the specified neutron fluence level.

3.4 Exposure. The test devices and dosimeters shall be exposed to the neutron fluence as specified. The exposure level may be obtained by operating the reactor in either the pulsed or power mode. If multiple exposures are required, the post-irradiation electrical tests shall be performed (see 3.5.1) after each exposure. A new set of dosimeters are required for each exposure level. Since the effects of neutrons are cumulative, each additional exposure level will have to be determined to give the specified total accumulated fluence. All exposures shall be made at 20°C ±10°C and shall be correlated to a 1 MeV equivalent fluence.

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3.5 Post-exposure.

3.5.1 Electrical tests. Test devices shall be removed only after clearance has been obtained from the health physicist at the test facility. The temperature of the sample devices shall be maintained at +20°C ±10°C from the time of the exposure until the post-electrical tests are made. The post-exposure electrical tests shall be made within 24 hours after the completion of the exposure. If the residual radioactivity level determined by the local Radiation Safety Officer is too high for device handling purposes, the elapsed time before post-test electrical measurements are made shall be extended to 1 week or remote testing shall be utilized. All required data must be recorded for each device after each exposure.

3.5.2 Failure analysis. Devices which exhibit anomalous behavior (e.g., non-linear degradation of 1/ß) shall be subjected to failure analysis.

3.6 Reporting. In reporting the results of radiation tests on discrete devices, adequate identification of the devices is essential. As a minimum, the report shall include the device type number, serial number, the manufacturer, controlling specification, the date code, and other Part or Identifying Numbers (PINs) provided by the manufacturer. Each data sheet shall include radiation test date, electrical test conditions, radiation test levels, and ambient conditions, as well as the test data. When other than specified electrical test circuits are employed, the parameter measurement circuits shall accompany the data. Any anomalous incidents during the test shall be fully explained in footnotes to the data.

4. Summary. The following conditions shall be specified in the request for test, or when applicable, the performance specification:

a. Device types.

b. Quantities of each device type to be tested if other than specified in 3.2.

c. Electrical parameters to be measured in pre- and post-exposure tests.

d. Criteria for pass, fail, record actions on tested devices.

e. Criteria for anomalous behavior designation.

f. Radiation exposure levels.

g. Test instrument requirements.

h. Radiation dosimetry requirements if other than 2.3.

i. Ambient temperature, if other than specified herein.

j. Requirements for data reporting and submission, where applicable.

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METHOD 1018.3

INTERNAL GAS ANALYSIS

1. Purpose. The purpose of this test is to measure the atmosphere inside a metal or ceramic hermetically-sealed device. Of particular interest is the measurement of the moisture content to determine if the device meets the specified moisture criteria. Also of interest is the measurement of all the other gases because they reflect upon the quality of the sealing process and provide information about the long term chemical stability of the atmosphere inside the device. This test is destructive.

2. Apparatus. The apparatus for the internal water-vapor content test shall be as follows:

a. A mass spectrometer meeting the following requirements:

(1) Spectra range. The mass spectrometer shall be capable of reading a minimum spectra range of 1 to 100 atomic mass units (AMUs).

(2) Detection limit. The mass spectrometer shall be capable of reproducibly detecting the specified moisture content for a given volume package with signal to noise ratio of 20 to 1 (i.e., for a specified limit of 5,000 parts per million volume (ppmv), .01 cc, the mass spectrometer shall demonstrate a 250 ppmv minimum detection limit to moisture for a package volume of .01 cc). The smallest volume shall be considered the worst case.

(3) System calibration. The calibration of the mass spectrometer shall be accomplished quarterly with a moisture level in the 4,500 to 5,500 ppmv range and with a moisture level in the 2,000 to 3,000 ppmv range, and with a moisture level in the 7,000 to 8,000 range using the same sensitivity factor. This calibration needs to be performed for each calibrator volume to demonstrate a linear response and to detect offset. A minimum of three data points for each moisture level shall be collected. Package simulators which have the capability of generating at least three known volumes of gas ±10 percent on a repetitive basis by means of a continuous sample volume purge of known moisture content ±5 percent shall be used. Moisture content shall be established by the standard generation techniques (i.e., 2 pressure, divided flow, or cryogenic method). The dew point hygrometer shall be recalibrated a minimum of once per year using equipment traceable to National Institute of Standards and Technology (NIST) or by a suitable commercial calibration services laboratory using equipment traceable to NIST standards. The dew point hygrometer shall be capable of measuring the dew point temperature to an accuracy of $\pm 0.2^{o}$C. The system shall have a pressure sensor to measure the pressure in line with the temperature dew point sensor to an accuracy of $\pm$0.1 inches of Hg for the range of pressure being used. In addition, the test laboratory shall have a procedure to calculate the concentration of moisture, in units of ppmv, from the dew point temperature measurement and the pressure measurement. Gas analysis results obtained by this method shall be considered valid only in the moisture range or limit bracketed by at least two (volume or concentration) calibration points (i.e., 5,000 ppmv between .01 to .1 cc or 1,000 to 5,000 ppmv between .01 to .1 cc). A best fit curve shall be used between volume calibration points. Systems not capable of bracketing may use an equivalent procedure as approved by the qualifying activity. Corrections of sensitivity factors deviating greater than 10 percent from the mean between calibration points shall be required.

NOTE: It is recommended that the percentage of water vapor contained in a gas flowing through the gas humidifier be compared to the dewpoint sensor reading for accuracy of the sensor. The following equation may be used to calculate the percent of water vapor contained in a gas flowing through the gas humidifier.

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$$\%H2O = \frac{100\ (Pv\ \text{mb})}{68.95\ \text{mb/psi}\ \ Pg + 1.33\ \text{mb/mm}\ \ Pa}$$

Where:
P_v = vapor pressure of water in the GPH based on water temperature in degrees centigrade,
P_g = gauge pressure in psi, and
P_a = atmospheric pressure in mm Hg.

(4) Annual calibration for other gases. Calibration shall be required for all gases found in concentrations greater than .01 percent by volume. As a minimum, this shall include all gases listed in 3b. The applicable gases shall be calibrated at approximately 1 percent concentrations requirements, with the exception of fluorocarbons, which may use a concentration of approximately 200 ppmv; NH_3 which may use a concentration of approximately 200 ppmv; hydrogen, which may use a concentration of approximately 200 ppmv; nitrogen, which may use a concentration of approximately 80 percent; helium, which may use a concentration of approximately 10 percent; and oxygen, which may use a concentration of approximately 20 percent.

(5) Daily calibration check. The system calibration shall be checked on the day of test prior to any testing. This shall include checking the calibration by in-letting a sample with a moisture level in the 4,500-5,500 ppmv range at the required volumes and comparing the result with the dew point hygrometer. The resulting moisture reading shall be within 250 ppmv of the moisture level in the calibration sample. NOTE: Equipment error needs to be determined and subtracted from the allowed maximum deviation of 250 ppmv. The calibration check shall be performed using the same conditions used for testing devices (e.g. background pressure, background environment, time between sample inlets, package simulator volume etc) Calibration performed on the day of test prior to any testing may be substituted for this calibration check. Calibration records shall be kept on a daily basis.

(6) Performed on the day of test prior to any testing may be substituted for this calibration check.

(7) Precision tuning shall be performed following significant maintenance or repair of the ion source.

(8) A record of all changes made to the sensitivity factors shall be maintained.

b. A vacuum opening chamber which can contain the device and a vacuum transfer passage connecting the device to the mass spectrometer of 2.a. A vacuum transfer passage shall efficiently (without significant loss of moisture from adsorption) transfer the gas from the device to the mass spectrometer ion source for measurement.

For initial certification of systems or extension of suitability, device temperature on systems using an external fixture shall be characterized by placing a thermocouple into the cavity of a blank device of similar mass, internal volume, construction, and size. This shall be a means for proving the device temperature that has been maintained at 100°C ±5°C for the minimum 10 minutes. This also applies to devices prebaked in an external oven but tested with the external fixture to adjust for any temperature drop during the transfer. These records shall be maintained by the test laboratory.

c. A piercing arrangement functioning within the opening chamber or transfer passage of 2.b, which can pierce the specimen housing (without breaking the mass spectrometer chamber vacuum and without disturbing the package sealing medium), thus allowing the specimen's internal gases to escape into the chamber and mass spectrometer.

NOTE: A sharp-pointed piercing tool, actuated from outside the chamber wall via a bellows to permit movement shall be used to pierce both metal and ceramic packages. For ceramic packages, or devices with thick metal lids, the package lid or cover should be locally thinned by abrasion to facilitate localized piercing.

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d. A pressure sensing device located in the transfer passage to measure the pressure rise in the transfer passage during the test. This pressure sensor is used to read a relative pressure change when the device is punctured. This relative pressure change indicates the relative quantity of gas in the device when comparing the test results of one device to another device. The significance of the reading is not intended to be absolute. Although the pressure gauge reading is reported, the pressure gauge is for indication only.

3. Procedure. All devices shall be prebaked for 16 to 24 hours at 100°C ±5°C prior to test. Ovens shall have a means to indicate if a power interruption occurs during the prebaking period and for how long the temperature drops below 100°C ±5°C. Devices whose temperature drops below 100°C ±5°C for more than 1 hour shall undergo another prebake to begin a minimum of 12 hours later.

A maximum 5 minute transfer time from prebake to hot insertion into apparatus shall be allowed. If 5 minutes is exceeded, device shall be returned to the prebake oven and prebake continued until device reaches 100°C ±5°C.

The system shall be maintained at a stable temperature equal to or above the device temperature. The fixturing in the vacuum opening chamber shall position the specimen as required by the piercing arrangement of 2.c, and maintain the device at 100°C ±5°C for a minimum of 10 minutes prior to piercing.

After device insertion, the device and chamber shall be pumped down and baked out at a temperature of 100°C ±5°C until the background pressure level will not prevent achieving the specified measurement accuracy and sensitivity. The background vacuum spectra shall be acquired and shall later be subtracted from the sample spectra. After pump down, the device case or lid shall be punctured and the following properties of the released gases shall be measured, using the mass spectrometer:

a. The water-vapor content of the released gases, as a percent by unit volume or ppmv of the total gas content.

b. The proportions (by volume) of the other following gases: N_2, He, Mass 69 (fluorocarbons), O_2, Ar, H_2, CO_2, CH_4, NH_3, and other solvents, if available. Calculations shall be made and reported on all gases present. Data reduction shall be performed in a manner, which will preclude the cracking pattern interference from other gas specie in the calculations of moisture content. Data shall be corrected for any system dependent matrix effects such as the presence of hydrogen in the internal ambient.

c. The increase in chamber pressure as the gases are released by piercing the device package. A pressure change of ±25 percent from expected for that package volume and pressurization may indicate that (1) the puncture was not fully accomplished, (2) the device package was not sealed hermetically, or (3) does not contain the normal internal pressure.

d. The test laboratory should provide comments describing the spectra of unknowns or gases that are present but not in sufficient concentration to be identified or quantified with reasonable certainty.

e. If the test laboratory has reason to believe that the test results may be invalid due to reasons such as improper puncture of the device or equipment malfunction, the results shall be reported as “no test” with additional comments provided. The device may be replaced with another.

NOTE: The device shall be hermetic in accordance with test method 1071 of this standard, and free from any surface contaminants which may interfere with accurate water vapor content measurement. The internal water vapor content laboratory is not required to test for hermeticity in accordance with test method 1071 of this standard. It is recommended that samples submitted for testing shall include information about the manufacturing process, including sealing pressure, sealing gas, free internal cavity volume, lid thickness at puncture site, lid material, and the location of the puncture site.

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3.1 Failure criteria.

a. The Internal gas analysis (IGA) laboratory shall not classify devices as passed or failed.

b. A device being tested in a batch system which exhibits an abnormally low total gas content, as defined in 3.c, shall constitute a hermeticity failure not an IGA failure. Such a device may be replaced by another device from the same population; if the replacement device exhibits normal total gas content for its type, neither it nor the original device shall constitute a failure for this cause.

4. Implementation. Suitability for performing method 1018 analysis is granted by the qualifying activity for specific limits and volumes. Method 1018 calibration procedures and the suitability survey are designed to guarantee ±20 percent lab-to-lab correlation in making a determination whether the sample passes or fails the specified limit. Water vapor contents reported either above or below the range of suitability are not certified as correlatable values. This out of specification data has meaning only in a relative sense and only when one laboratory's results are being compared. The specification limit of 5,000 ppmv shall apply to all package volumes (unless otherwise specified), with the following correction factors permitted, to be used by the manufacturer provided they are documented and shown to be applicable:

a. For package volumes less than .01 cc internal free volume which are sealed while heated in a furnace:

$$C_T = \frac{T_r + 273}{T_s + 273}$$

Where:
C_T = correction factor (temperature)
T_r = room temperature (°C)
T_s = sealing temperature (°C).

b. For package volumes of any size sealed under vacuum conditions:

$$C_P = \frac{P_s}{P_a}$$

C_P = correction factor (pressure)
P_s = sealing pressure
P_a = atmospheric pressure (pressures may be in Torr or mm Hg).

The correction factor, if used, shall be applied as follows:

Water vapor (corrected) = water vapor (measured) x C_X; where C_X is the applicable correction factor.

The range of suitability for each laboratory will be extended by the qualifying activity when the analytical laboratories demonstrate an expanded capability. Information on current analytical laboratory suitability status can be obtained by contacting Defense Supply Center, Columbus, ATTN: DSCC-VQE, P.O. Box 3990, Columbus, OH 43216-5000 or e-mail vqe.chief@dla.mil.

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5. Surrogate monitors. Surrogate monitors are only applicable for packages less than .01 cc to evaluate the process baseline. Surrogate monitors will be subject to IGA testing in accordance with method 1018 herein. A production lot will be validated by the performance of its monitors. It is well known and established that pre-seal bake and storage conditions of packaging materials will severely impact the levels of moisture detected in almost any package type. The use of the surrogate monitors without a controlled and disciplined manufacturing line is of questionable value. The proposed test is not, nor is it intended to be, a direct measurement of small packaged product internal moisture. However, it is a quantifiable indicator that the process and controls used are consistent. This is an improvement over the existing situation in which there is a requirement for control of internal moisture and no accurate and repeatable method of measurement.

5.1. Requirements. Surrogate monitors are to be procured from the same manufacturer and be manufactured in the same technology as the production headers, using the same materials, plating, processing, and technology. For example, the UB packages: Kyocera header, multilayer cofired ceramic technology; SemiAlloys lid, Alloy 52, nickel underplate, and gold plate.

a. The device manufacturer shall use the same preconditioning on surrogate monitors and production product, i.e. vacuum bake time and temperature, storage conditions, die attach materials and process.

b. Surrogate monitors shall be sealed at the same time and using the same process as the production parts.

c. To optimize the effect of preconditioning, the transit time from the oven to the seal furnace shall be controlled and minimal.

d. A typical process would include:

(1) Batch high-vacuum bake headers and lids.

(2) Store baked material in dry nitrogen.

(3) Second vacuum bake overnight (a minimum of 12 hrs) just prior to seal.

(4) Minimize the post second bake exposure to atmosphere.

e. Surrogate monitor packages will be under baseline documentation control. Full traceability from procurement to utilization shall be maintained.

f. Initially, the surrogate monitors will be used at the beginning of the seal operation and at 2 hour intervals. A minimum of six monitors must be processed for each seal lot (a "seal lot" may consist of multiple production lots if they go through sealing without interruptions (other than the scheduled breaks) and have identical traceability of headers and lids).

g. It is expected that it will take approximately 6 months for a manufacturer to collect enough lots and data to establish a baseline. Later modifications of the preconditioning process will be evaluated against this baseline.

h. The device manufacturer will submit to DSCC the results from a minimum of three seal lots to establish the effectiveness of the process baseline. Additional testing will be retained and available to DSCC upon request.

6. Summary. The following details shall be specified in the applicable acquisition document: The maximum allowable water vapor content if other than 5,000 ppmv.

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METHOD 1019.5

STEADY-STATE TOTAL DOSE IRRADIATION PROCEDURE

1. Purpose. This test procedure defines the requirements for testing discrete packaged semiconductor devices for ionizing radiation (total dose) effects from a cobalt-60 (^{60}Co) gamma ray source. In addition, this procedure provides an accelerated annealing test for estimating low dose rate ionizing radiation effects on devices. This annealing test is important for low dose-rate or certain other applications in which devices may exhibit significant time dependent effects. This procedure addresses only steady-state irradiations, and is not applicable to pulse type irradiations. This test may produce severe degradation of the electrical properties of irradiated devices and thus should be considered a destructive test.

1.1 Definitions. Definitions of terms used in this procedure are given below:

a. Ionizing radiation effects: The changes in the electrical parameters of a device resulting from radiation-induced charge. It is also referred to as total dose effects.

b. In-flux tests: Electrical measurements made on devices during radiation exposure.

c. Not in-flux tests: Electrical measurements made on devices at any time other than during irradiation.

d. Remote tests: Electrical measurements made on devices which are physically removed from the irradiation location for the measurements.

e. Time dependent effects. Significant changes in electrical parameters caused by the growth or annealing, or both, of radiation induced trapped charge and interface traps after irradiation. Similar effects also take place during irradiation.

f. Accelerated annealing test. A procedure utilizing elevated temperature to accelerate time-dependent effects.

2. Apparatus. The apparatus shall consist of the radiation source, electrical test instrumentation, test circuit board(s), cable, interconnect board or switching system, if used, and appropriate dosimetry measurement system, if used. Adequate precautions shall be observed to obtain an electrical measurement system with sufficient insulation, ample shielding, satisfactory grounding, and with suitable low noise from the main power supply.

2.1 Radiation source. The radiation source used in the test shall be the uniform field of a ^{60}Co gamma ray source. Uniformity of the radiation field in the volume where devices are irradiated shall be within ±10 percent as measured by the dosimetry system, unless otherwise specified. The intensity of the gamma ray field of the ^{60}Co source shall be known with an uncertainty of no more than ±5 percent. Field uniformity and intensity can be affected by changes in the location of the device with respect to the radiation source and the presence of radiation absorption and scattering materials.

2.1.1 Cobalt-60 source. The gamma ray field of a Cobalt-60 source shall be calibrated at least every 3 years to an uncertainty of no more than ±5 percent as measured with an appropriate dosimetry system whose calibration is traceable to the NIST. Corrections for Cobalt-60 source decay shall be made monthly.

2.2 Dosimetry system. An appropriate dosimetry system shall be provided which is capable of carrying out the measurements required in 3.3. The following American Society for Testing and Materials (ASTM) standards, or other appropriate standards, shall be used:

ANSI/ASTM E 666	-	Standard Method for Calculation of Absorbed Dose from Gamma or X Radiation.
ANSI/ASTM E 668	-	Standard Practice for the Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices.
ASTM E 1250	-	Standard Method for Application of Ionization Chambers to Assess the Low Energy Gamma Component of Cobalt 60 Irradiators Used in Radiation Hardness Testing of Silicon electronic Devices.

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ASTM E 1275 - Standard Practice for Use of a Radiochromic Film Dosimetry System.

ASTM E 1249 - Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices.

These industry standards address the conversion of absorbed dose from one material to another and the proper use of various dosimetry systems.

(Application for copies should be addressed to ASTM International, 100 Barr Harbor Drive, PO Box C700, West Conshohocken, PA, 19428-2959, http://www.astm.org.)

2.3 Electrical test instruments. All instrumentation used for electrical measurements shall have stability, accuracy, and resolution required for accurate measurement of the electrical parameters. Any instrumentation required to operate in a radiation environment above 10 REM per hour shall be appropriately shielded, or the radiation level must be less than the instrumentation manufacturer's recommended maximum.

2.4 Test circuit board(s). Devices to be irradiated shall be mounted on, or connected to, circuit boards together with any associated circuitry necessary for device biasing during irradiation or for in-site measurements. Unless otherwise specified, all device input terminals and any others which may affect the radiation response shall be electrically connected during irradiation, i.e., not left floating. The geometry and materials of the completed board shall allow uniform irradiation of the device under test (DUT). Good design and construction practices shall be used to prevent oscillations, minimize leakage currents, prevent electrical damage, and obtain accurate measurements. Only sockets, which are radiation resistant and do not exhibit significant leakages (relative to the DUT) shall be used to mount devices and associated circuitry to the test board(s). All apparatus used repeatedly in radiation fields shall be checked periodically for physical or electrical degradation. Components which are placed on the test circuit board, other than DUTs, shall be insensitive to the accumulated radiation, or they shall be shielded from the radiation. Test fixtures shall be made such that materials will not perturb the uniformity of the radiation field intensity at the DUT. Leakage current shall be measured out of the radiation field. With no devices installed in the sockets, the test circuit board shall be connected to the test system such that all expected sources of noise and interference are operative. With the maximum specified bias for the test device applied, the leakage current between any two terminals shall not exceed ten percent of the lowest current limit value in the pre-irradiation device specification. Test circuit boards used to bias devices during accelerated annealing must be capable of withstanding the temperature requirements of the accelerated annealing test and shall be checked before and after testing for physical and electrical degradation.

2.5 Cabling. Cables connecting the test circuit boards in the radiation field to the test instrumentation shall be as short as possible. If long cables are necessary, line drivers may be required. The cables shall have low capacitance and low leakage to ground, and low leakage between wires.

2.6 Interconnect or switching system. This system shall be located external to the radiation environment location, and provides the interface between the test instrumentation and the DUTs. It is part of the entire test system and subject to the limitation specified in 2.4 for leakage between terminals.

2.7 The environmental chamber. The environmental chamber for time-dependent effects.

3. Procedure. The test devices shall be irradiated and subjected to accelerated annealing (if required for time-dependent effects testing) as specified by a test plan. This plan shall specify the device description, irradiation conditions, device bias conditions, dosimetry system, operating conditions, measurement parameters and conditions, and accelerated annealing test conditions (if required). See figure 1019-I herein.

3.1 Sample selection and handling. Only devices which have passed the electrical specification as defined in the test plan shall be submitted to radiation testing. Unless otherwise specified, the test samples shall be randomly selected from the parent population and identically packaged. Each part shall be individually identifiable to enable pre- and post-irradiation comparison. For device types which are ESD sensitive, proper handling techniques shall be used to prevent damage to the devices.

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3.2 Burn-in. For some devices, there are differences in the total dose radiation response before and after burn-in. Unless it has been shown by prior characterization or by design that burn-in has negligible effect (parameters remain within post-irradiation specified electrical limits) on the total dose radiation response, then one of the following shall be done:

a. The manufacturer shall subject the radiation samples to the specified burn-in conditions prior to conducting total dose radiation testing.

b. The manufacturer shall develop a correction factor (which is acceptable to the parties to the test), taking into account the changes in total dose response resulting from subjecting product to burn-in. The correction factor shall then be used to accept product for total dose response without subjecting the test samples to burn-in.

3.3 Dosimetry measurements. The radiation field intensity at the location of the DUT shall be determined prior to testing by dosimetry or by source decay correction calculations, as appropriate, to assure conformance to test level and uniformity requirements. The dose to the DUT shall be determined one of two ways: (1) by measurement during the irradiation with an appropriate dosimeter, or (2) by correcting a previous dosimetry value for the decay of the Cobalt-60 source intensity in the intervening time. Appropriate correction shall be made to convert the measured or calculated dose in the dosimeter material to the dose in the DUT.

3.4 Lead/aluminum (Pb/Al) container. Test specimens shall be enclosed in a Pb/Al container to minimize dose enhancement effects caused by low-energy, scattered radiation. A minimum of .059 inch (1.5 mm) Pb, surrounding an inner shield of at least .028 inch (0.7 mm) Al, is required. This Pb/Al container produces an approximate charged particle equilibrium for Si and for TLDs such as CaF_2. The radiation field intensity shall be measured inside the Pb/Al container: (1) initially, (2) when the source is changed, or (3) when the orientation of configuration of the source, container, or test-fixture is changed. This measurement shall be performed by placing a dosimeter (e.g., a TLD) in the device irradiation container at the approximate test device position. If it can be demonstrated that low-energy scattered radiation is small enough that it will not cause dosimetry errors due to dose enhancement, the Pb/Al container may be omitted.

3.5 Radiation level(s). The test devices shall be irradiated to the dose level(s) specified in the test plan within ±10 percent. If multiple irradiations are required for a set of test devices, then the post-irradiation electrical parameter measurements shall be performed after each irradiation.

3.6 Radiation dose rate.

3.6.1 Condition A. The dose rate range shall be between 50 and 300 rads (Si)/s (0.5 and 3 Gy(Si)/s) for Cobalt-60. (The SI unit for the quantity absorbed dose is the gray symbol Gy. 100 rad = 1 Gy.) The dose rates may be different for each radiation dose level in a series; however, the dose rate shall not vary by more than ±10 percent during each irradiation.

3.6.2 Condition B. For condition B, for MOS devices only, if the maximum dose rate is < 50 rad(Si)/s in the intended application, the parties to the test may agree to perform the test at a dose rate greater than or equal to the maximum dose rate of the intended application. Unless the exclusions in 3.12.1b are met, the accelerated annealing test of 3.12.2 shall be performed.

3.6.3 Condition C. As an alternative, the test may be performed at the dose rate of the intended application, if this is agreed to by the acquisition activity.

3.7 Temperature requirements. Since radiation effects are temperature dependent, DUTs shall be irradiated in an ambient temperature of +24°C ±6°C as measured at a point in the test chamber in close proximity to the test fixture. The electrical measurements shall be performed in an ambient temperature of +25°C ±5°C. If devices are transported to and from a remote electrical measurement site, the temperature of the test devices shall not be allowed to increase by more than +10°C from the irradiation environment. If any other temperature range is required, it shall be specified.

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3.8 Electrical performance measurements. The electrical parameters to be measured, and functional tests to be performed, shall be specified in the test plan. As a check on the validity of the measurement system and pre- and post-irradiation data, at least one control sample shall be measured using the operating conditions provided in the governing device specifications. For automatic test equipment (ATE), there is no restriction on the test sequence provided that the rise in the device junction temperature is minimized. For manual measurements, the sequence of parameter measurements shall be chosen to allow the shortest possible measurement period. When a series of measurements is made, the tests shall be arranged so that the lowest power dissipation in the device occurs in the earliest measurements and the power dissipation increases with subsequent measurements in the sequence. The pre- and post-irradiation electrical measurements shall be done on the same measurement system and the same sequence of measurements shall be maintained for each series of electrical measurements of devices in a test sample. Pulse type measurements of electrical parameter should be used as appropriate to minimize heating and subsequent annealing effects. Devices which will be subjected to the accelerated annealing testing (see 3.12) may be given a pre-irradiation burn-in to eliminate burn-in related failures.

3.9 Test conditions The use of in-flux or not in-flux shall be specified in the test plan. (This may depend on the intended application for which the data is being obtained.) The use of in-flux testing may help to avoid variations introduced by post-irradiation time dependent effects. However, errors may be incurred for the situation where a device is irradiated in-flux with static bias, but where the electrical testing conditions require the use of dynamic bias for a fraction of the total irradiation period. Not in-flux testing generally allows for more comprehensive electrical testing, but can be misleading if significant post-irradiation time dependent effects occur.

3.9.1 In-flux testing. Each test device shall be checked for operation within specifications prior to being irradiated. After the entire system is in place for the in-flux radiation test, it shall be checked for proper interconnections, leakage (see 2.4), and noise level. To assure the proper operation and stability of the test setup, a control device with known parameter values shall be measured at all operational conditions called for in the test plan. This measurement shall be done either before the insertion of test devices or upon completion of the irradiation after removal of the test devices or both.

3.9.2 Remote testing. Unless otherwise specified, the bias shall be removed and the device leads placed in conductive foam (or similarly shorted) during transfer from the irradiation source to a remote tester and back again for further irradiation. This minimizes post-irradiation time dependent effects.

3.9.3 Bias and loading conditions. Bias conditions for test devices during irradiation or accelerated annealing shall be within ±10 percent of those specified by the test plan. (If known, the bias applied to the test devices shall be selected to produce the greatest radiation induced damage or the worst-case damage for the intended application.) The specified bias shall be maintained on each device in accordance with the test plan. Bias shall be checked immediately before and after irradiation. Care shall be taken in selecting the loading such that the rise in the junction temperature is minimized.

3.10 Post-irradiation procedure. Unless otherwise specified, the following time intervals shall be observed:

a. The time from the end of an irradiation to the start of electrical measurements shall be a maximum of 1 hour.

b. The time to perform the electrical measurements and to return the devices for a subsequent irradiation, if any, shall be within two 2 hours of the end of the prior irradiation.

To minimize time dependent effects, these intervals shall be as short as possible. The sequence of parameter measurements shall be maintained constant through the test series.

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3.11 Extended room temperature anneal test. The tests of 3.1 through 3.10 are known to be overly conservative for some devices in a very low dose rate environment (e.g. dose rates characteristic of space missions). The extended room temperature anneal test provides an estimate of the performance of a device in a very low dose rate environment even though the testing is performed at a relatively high dose rate (e.g. 50 to 300 rad(Si)/s). The procedure involves irradiating the device in accordance with tests 3.1 through 3.10 and post-irradiation subjecting the DUT to a room temperature anneal for an appropriate period of time (see 3.11.2c) to allow leakage related parameters that may have exceeded their pre-irradiation specification to return to within specification. The procedure is known to lead to a higher rate of device acceptance in cases:

a. Where device failure, when subjected to the tests in 3.1 through 3.10, has been caused by the buildup of trapped positive charge in relatively soft oxides, and

b. Where this trapped positive charge anneals at a relatively high rate.

3.11.1 Need to perform an extended room temperature anneal test. The following criteria shall be used to determine whether an extended room temperature anneal test is appropriate:

a. The procedure is only appropriate for MOS devices.

b. The procedure is appropriate where only parametric failures (as opposed to functional failure) occurs. The parties to the test shall take appropriate steps to determine that the DUT is subject to only parametric failure over the total ionizing dose testing range.

c. The procedure is appropriate where the natural annealing response of the DUT will serve to correct the out of specification of any parametric response. Further, the procedure is known to lead to a higher rate of device acceptance in cases where the expected application irradiation dose rate is sufficiently low that ambient temperature annealing of the radiation induced trapped positive charge can lead to a significant improvement of device behavior. Cases where the expected application dose rate is lower than the test dose rate, and lower than 0.1 rad(Si)/s, should be considered candidates for the application of this procedure. The parties to the test shall take appropriate steps to determine that the technology under test can provide the required annealing response over the total ionizing dose testing range.

3.11.2 Extended room temperature anneal test procedure. If the device fails the irradiation and testing specified in 3.1 through 3.10, an additional room temperature annealing test may be performed as follows:

a. Following the irradiation and testing of 3.1 through 3.10, subject the DUT to a room temperature anneal under worst-case static bias conditions. For information on worst case bias see 3.9.3.

b. The test will be carried out in such a fashion that the case of the DUT will have a temperature within the range 24ºC ± 6ºC.

c. Where possible, the room temperature anneal should continue for a length of time great enough to allow device parameters that have exceeded their pre-irradiation specification to return to within specification or post-irradiation parametric limit (PIPL) as established by the manufacturer. However, the time of the room temperature anneal shall not exceed t_{max}, where

$$t_{max} = \frac{D_{spec}}{R_{max}}$$

D_{spec} is the total ionizing dose specification for the part and R_{max} is the maximum dose rate for the intended use.

d. Test the DUT for electrical performance as specified in 3.7 and 3.8. If the DUT passes electrical performance tests following the extended room temperature anneal, this shall be considered acceptable performance for a very low dose rate environment in spite of having previously failed the post-irradiation and electrical tests of 3.1 through 3.10.

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3.12 MOS accelerated annealing test. The accelerated annealing test provides an estimate of worst-case degradation of MOS devices in low dose rate environments. The procedure involves heating the device following irradiation at a specified temperature, time, and bias conditions. An accelerated annealing test (see 3.12.2) shall be performed for cases where time dependent effects (TDE) can cause a device to degrade significantly or fail. Only standard testing shall be performed as specified in 3.1 through 3.10 for cases where TDE are known not to cause significant device degradation or failure (see 3.12.1), or where they do not need to be considered, as specified in 3.12.1.

3.12.1 Need to perform accelerated annealing test. The parties to the test shall take appropriate steps to determine whether accelerated annealing testing is required. The following criteria shall be used:

a. The tests called out in 3.12.2 shall be performed for any MOS device.

b. TDE tests may be omitted if:

(1) The device does not contain MOS elements, or

(2) The ionizing dose in the application, if known, is below 5 krad(Si), or

(3) The lifetime of the device from the onset of the irradiation in the intended application, if known, is short compared with TDE times, or

(4) The test is carried out at the dose rate of the intended application, or

(5) The device has been demonstrated via characterization testing not to exhibit TDE changes in device parameters greater than experimental error (or greater than an otherwise specified upper limit) and the variables that affect TDE response are demonstrated to be under control for the specific vendor processes.

c. This document provides no guidance on the need to perform accelerated annealing tests on non-MOS devices.

3.12.2 Accelerated annealing test procedure. If the device passes the tests in 3.1 through 3.10, or if it passes 3.11 (if that procedure is used), to the total ionizing dose level specified in the test plan or device specification or drawing and the exclusions of 3.12.1 do not apply, the accelerated annealing test shall be conducted as follows:

a. Overtest. Irradiate each test device to an additional 0.5 times the specified dose using the standard test conditions (3.1 through 3.10). Note that no electrical testing is required at this time.

b. Accelerated annealing. Heat each device under worst-case static bias conditions in an environmental chamber according to one of the following conditions:

(1) At 100°C ±5°C for 168 ±12 hours, or

(2) At an alternate temperature and time that has been demonstrated via characterization testing to cause equal or greater change in the parameter(s) of interest, in each test device as that caused by 3.12.2.b.1, or

(3) At an alternate temperature and time which will cause trapped hole annealing of >60 percent and interface state annealing of <10 percent as determined via characterization testing.

c. Electrical testing. Following the accelerated annealing, the electrical test measurements shall be performed as specified in 3.8 and 3.9.

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3.13 Bipolar transistor delta($1/h_{FE}$) post irradiation [h_{FE}] gain calculations. Bipolar transistors require special calculations to report their post-irradiation performance. One of the following two calculations may be required:

(a) Delta($1/h_{FE}$): Let h_{FE1} be the measured h_{FE} at a specific test point (Vce, Ic) prior to irradiation. Let h_{FE2} be the measured h_{FE} post-irradiation at that same test point. Then: Delta($1/h_{FE}$) = $\Delta(1/h_{FE}) = 1/h_{FE2} - 1/h_{FE1}$ and is unitless as is h_{FE}.

Example: h_{FE1} = 200 before irradiation and post-irradiation it has decreased to h_{FE2} = 125. Then: $\Delta\ (1/h_{FE}) = 1/125 - 1/200 = 0.00300$.

(b) [h_{FE}] calculation is not a directly measured value of h_{FE} but, rather, a calculated value used by system analysis engineers. It signifies exactly how well the bipolar transistor will perform in the system after exposure to a radiation fluence. This [h_{FE}] is denoted in square brackets [ ] to delineate it from any measured value of h_{FE} and uses the calculated values from 3.13.a but adds one additional term. Calculate as follows:

Let h_{FE}(min) be the pre-irradiation spec minimum h_{FE} limit at the same test point in 3.13.a. Then: [h_{FE}] = inverse { $\Delta(1/h_{FE}) + 1/h_{FE}$)min }

Example: h_{FE}(min) = 100 and, in accordance with 3.13.a, $\Delta(1/h_{FE}) = 0.00300$. Then: [$h_{FE}$] = inverse { 0.00300 + 1/100 } = inverse { 0.003 + 0.01 } = 1 / { 0.013} = 76.92.

Note that [h_{FE}] can never exceed h_{FE} (min)

(c) When $\Delta(1/h_{FE})$, [h_{FE}] or both are required by the control specification, these calculations will only be required on the irradiation test samples. The test report in 3.14 shall then contain, in spreadsheet fashion, the appropriate pre and post h_{FE} measurements as well as the required calculation results. Unless otherwise specified, all devices shall adhere to the specification maximum h_{FE} limits that were imposed pre-irradiation.

3.14 Test report. As a minimum, the report shall include the device type number, serial number, CAGE code of the manufacturer, package type, controlling specification, date code, and any other identifying numbers given by the manufacturer. The bias circuit, parameter measurement circuits, the layout of the test apparatus with details of distances and materials used, and electrical noise and current leakage of the electrical measurement system for in-flux testing shall be reported using drawings or diagrams as appropriate. Each data sheet shall include the test date, the radiation source used, the bias conditions during irradiation, the ambient temperature around the devices during irradiation and electrical testing, the duration of each irradiation, the time between irradiation and the start of the electrical measurements, the duration of the electrical measurements and the time to the next irradiation when step irradiations are used, the irradiation dose rate, electrical test conditions, dosimetry system and procedures, and the radiation test levels. The pre- and post-irradiation data shall be recorded for each part and retained with the parent population data in accordance with the requirements of MIL-PRF-19500. Any anomalous incidents during the test shall be fully documented and reported. The accelerated annealing procedure, if used, shall be described. Any other radiation test procedures or test data required for the delivery shall be specified in the device specification, drawing, or order.

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4. Summary. The following details shall be specified in the applicable acquisition document as required.

   a. Device-type number(s), quantity, and governing specification (see 3.1).

   b. Radiation dosimetry requirements (see 3.3).

   c. Radiation test levels including dose and dose rate (see 3.5 and 3.6).

   d. Irradiation, electrical test, and transport temperature; if other than as specified in 3.7.

   e. Electrical parameters to be measured and device operating conditions during measurement (see 3.8).

   f. Test conditions, i.e., in-flux or not in-flux type tests (see 3.8 and 3.9).

   g. Bias conditions for devices during irradiation (see 3.9.3).

   h. Time intervals of the post-irradiation measurements (see 3.10).

   i. Requirement for extended room temperature anneal test, if required (see 3.11).

   j. Requirement for accelerated annealing test, if required (see 3.12).

   k. Documentation required to be delivered with devices (see 3.14).

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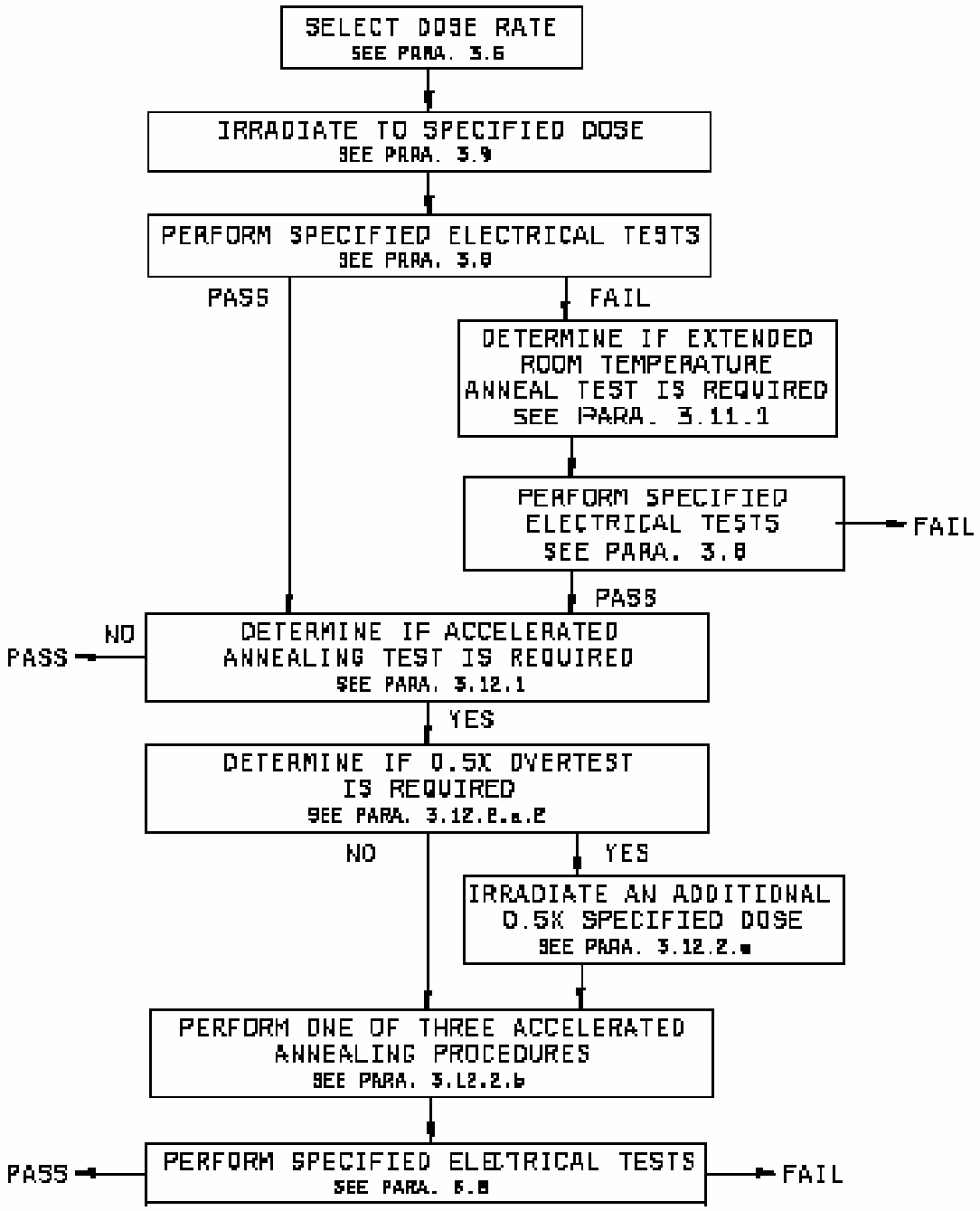

Figure 1019-I. Flow diagram for ionizing radiation test procedure.

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METHOD 1020.2

ELECTROSTATIC DISCHARGE SENSITIVITY CLASSIFICATION

1. Purpose. This method establishes the procedure for classifying semiconductors according to their susceptibility to damage or degradation by exposure to electrostatic discharge (ESD). This classification is used to specify appropriate packaging and handling requirements in accordance with MIL-PRF-19500, and to provide classification data to meet the requirements of MIL-STD-1686.

1.1 Definitions. The following definition shall apply for the purposes of this test method.

1.1.1 ESD. A transfer of electrostatic charge between two bodies at different electrostatic potentials.

2. Apparatus.

2.1 Test apparatus. ESD pulse simulator and device under test (DUT) socket equivalent to the circuit of figure 1020-1, and capable of supplying pulses with the characteristics required by figure 1020-2.

2.2 Measurement equipment. Equipment, including an oscilloscope and current probe, to verify conformance of the simulator output pulse to the requirements of figure 1020-2.

2.2.1 Oscilloscope and amplifier. The oscilloscope and amplifier combination shall have a 350 MHz minimum bandwidth and a visual writing speed of 4 cm/ns minimum.

2.2.2 Current probe. The current probe shall have a minimum bandwidth of 350 MHz (e.g., Tektronix CT-1 at 1,000 MHz).

2.2.3 Charging of voltage probe. The charging voltage probe shall have a minimum input resistance of 1,000 M and a division ratio of 4 percent maximum (e.g., HP 34111A).

2.3 Calibration. Periodic calibration shall include, but not be limited to, the following.

2.3.1 Charging voltage. The meter used to display the simulator charging voltage shall be calibrated to indicate the actual voltage at points C and D of figure 1020-1, over the range specified in table 1020-I.

2.3.2 Effective capacitance. Effective capacitance shall be determined by charging C1 to the specified voltage (see table 1020-I), with no device in the test socket and the test switch open, and by discharging C1 into an electrometer, coulombmeter, or calibrated capacitor connected between points A and B of figure 1020-1. The effective capacitance shall be 100 pF ±10 percent over the specified voltage range and shall be periodically verified at 1,000 volts. (NOTE: A series resistor may be needed to slow the discharge and obtain a valid measurement.)

2.3.3 Current waveform. The procedure of 3.2 shall be performed for each voltage step of table 1020-I. The current waveform at each step shall meet the requirements of figure 1020-2.

2.4 Qualification. Apparatus acceptance tests shall be performed on new equipment or after major repair. Testing shall include, but not be limited to, the following.

2.4.1 Current waveform verification. Current waveform shall be verified at every pin of each test fixture using the pin nearest terminal B (see figure 1020-1) as the reference point. All waveforms shall meet the requirements of figure 1020-2. The pin pair representing the worst case (closest to the limits) waveform shall be identified and used for the verification required by 3.2.

3. Procedure.

3.1 General.

3.1.1 Test circuit. Classification testing shall be performed using a test circuit equivalent to figure 1020-1 to produce the waveform shown on figure 1020-2.

3.1.2 Test temperature. Each device shall be stabilized at room temperature prior to and during testing.

3.1.3 ESD classification testing. ESD classification testing of devices shall be considered destructive.

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3.2 ESD simulator current waveform verification. To ensure proper simulator operation, the current waveform verification procedure shall be done, as a minimum, at the beginning of each shift when ESD testing is performed, or prior to testing after each change of the socket/board, whichever is sooner. At the time of initial facility certification and recertifications, photographs shall be taken of the waveforms observed as required by 3.2.c. through 3.2.e. and be kept on file for purposes of audit and comparison. (Stored digitized representations of the waveforms are acceptable in place of photographs.)

a. With the DUT socket installed on the simulator, and with no DUT in the socket, place a short (see figure 1020-1) across two pins of the DUT socket and connect one of the pins to simulator terminal A and the other pin to terminal B.

b. Connect the current probe around the short near terminal B (see figure 1020-1). Set the simulator charging voltage source V_S to 4,000 volts corresponding to step 4 of table 1020-1.

c. Initiate a simulator pulse and observe the leading edge of the current waveform. The current waveform shall meet the rise time, peak current, and ringing requirements of figure 1020-2.

d. Initiate a simulator pulse again and observe the complete current waveform. The pulse shall meet the decay time and ringing requirement of figure 1020-2.

e. Repeat the above verification procedure using the opposite polarity (V_S = 4,000 volts).

f. It is recommended that the simulator output be checked to verify that there is only one pulse per initiation, and that there is no pulse while capacitor C1 is being charged. To observe the recharge transient, set the trigger to the opposite polarity, increase the vertical sensitivity by approximately a factor of ten, and initiate a pulse.

TABLE 1020-1. Simulator charging voltage (V_S) steps versus peak current (I_P).

Step	V_S (volts)	I_P (amperes)
1	500	0.33
2	1,000	0.67
3	2,000	1.33
4	4,000	2.67

3.3 Classification testing.

a. A sample of devices (see 4.c) shall be characterized for the device ESD failure threshold using the voltage steps shown in table 1020-I, as a minimum. Finer voltage steps may optionally be used to obtain a more accurate measure of the failure voltage. Testing may begin at any voltage step, except for devices which have demonstrated healing effects, including those with spark gap protection, which shall be started at the lowest step. Examination of known technology family input or output V/I damage characteristics (i.e., curve tracer), or other simplified test verification techniques may be used to validate the failure threshold (e.g., cumulative damage effects may be eliminated by retesting at the failure voltage step using a new sample of devices and possibly passing the step).

b. A new sample of devices shall be selected and subjected to the next lower voltage step used. Each device shall be tested using three positive and three negative pulses using each of the pin combinations shown in table 1020-II. A minimum of one-second delay shall separate the pulses.

c. The sample device shall be electrically tested to group A, subgroup II of the specification sheet as applicable (room temperature dc parameters).

d. If one or more of the devices fail, the testing of 3.3.b and 3.3.c shall be repeated at the next lower voltage step used.

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e. If none of the devices fail, record the failure threshold determined in 3.3.a. Note the highest step passed and use it to classify the device in accordance with table 1020-III.

TABLE 1020-II. Junction polarities for ESD conditions test.

Device type	Junction/polarity
Bipolar transistor (NPN)	E+ to B-
Bipolar transistor (PNP)	E- to B+
Junction FET's (N-channel)	G+ to S-
Junction FET's (P-channel)	G- to S+
MOSFET's (N- or P-channel)	G to S (both polarities)
Gate protected FET's (P-channel)	G to S (both polarities)
Rectifiers (include hot carrier and schottky)	A- to K+
Thyristors	G to K (both polarities)
Unijunctions	G to B1 (both polarities)
Darlingtons	E to B (both polarities)
Small signal diodes	A to K (both polarities)

3.4 Pin combinations to be tested.

Using table 1020-II, select the terminal to be used for the ESD tests.

TABLE 1020-III. Device ESD failure threshold classification.

Class	Voltage
Class 0	Less than 250 volts
Class 1A	250 to 499 volts
Class 1B	500 to 999 volts
Class 1C	1,000 to 1,999 volts
Class 2	2,000 to 3,999 volts
Class 3A	4,000 to 7,999 volts
Class 3B	8,000 to 15,999 volts
Nonsensitive	Above 15,999 volts

3.5 Classification criteria.

a. Devices which fail the post test electrical at +25°C of group A, subgroup 2 of the specification sheet shall be considered class 1 devices.

b. All devices subjected to this test shall be considered destroyed and shall not be shipped for use in any application.

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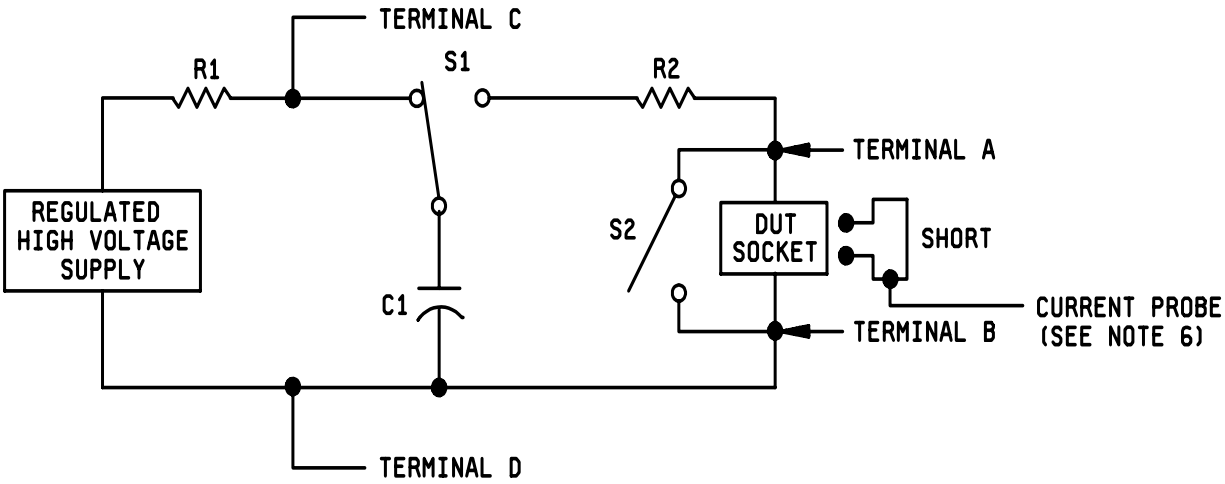
4. Summary. The following details shall be specified in the applicable order or contract, if other than specified herein.

a. Post test electricals.

b. Special additional or substitute pin combinations, if applicable.

c. Sample size, if other than three devices.



R1 = 10^6 Ω to 10^7 Ω
C1 = 100 pF ±10 percent (Insulation resistance 10^{12} Ω minimum)

R2 = 1,500 Ω ±1 percent
S1 = High voltage relay (Bounceless, mercury wetted, or equivalent

S2 = Normally closed switch (Open during discharge pulse and capacitance measurement)

NOTES:
1. The performance of this simulator circuit is strongly influenced by parasitics. Capacitances across relays and resistor terminals, and series inductance in wiring and in all components, shall be minimized.
2. As a precaution against transients upon recharge of C1, the supply voltage V_S may be reduced before switch S1 is returned to the charging position.
3. Piggybacking DUT sockets is not permitted during verification or classification testing.
4. Switching terminals A and B internal to the simulator to obtain opposite polarity is not recommended.
5. C1 represents the effective capacitance (see 2.3.2).
6. The current probe connection shall be made with double shielded cable into a 50 Ω termination at the oscilloscope. The cable length shall not exceed 3 feet.

FIGURE 1020-1. ESD classification test circuit (human body model).

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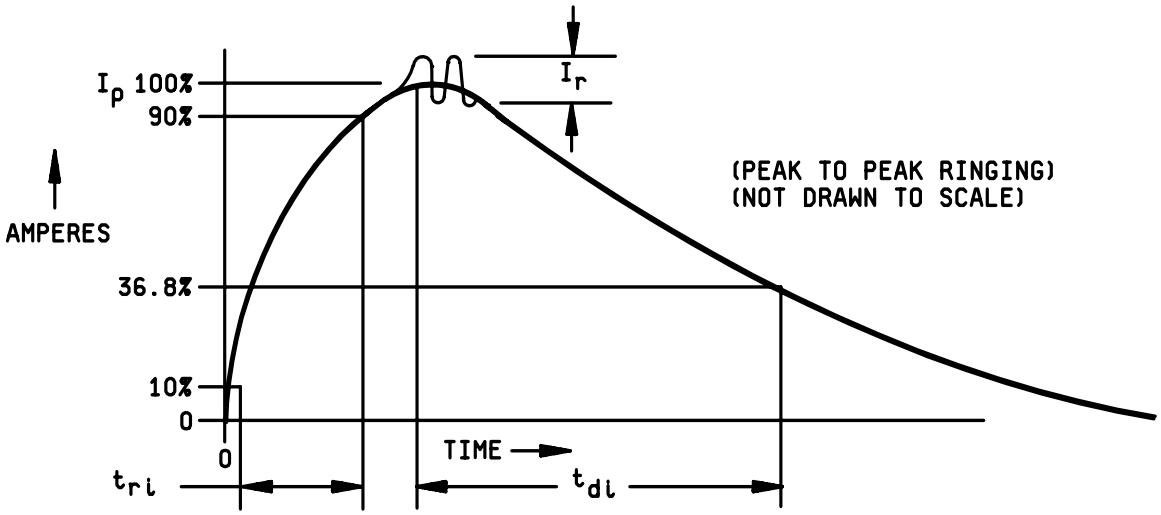

CURRENT WAVEFORM

NOTES:

1. The current waveforms shown shall be measured as described in the waveform verification procedure of 3.2, using equipment meeting the requirements of section 2 herein.
2. The current pulse shall have the following characteristics:

t_{ri} (rise time) - - - - - - -	Less than 10 ns.
t_{di} (delay time) - - - - - -	150 ±20 ns.
I_p (peak current) - - - - -	Within ±10 percent of the I_P value shown in table 1020-II for the voltage step selected.
I_r (ringing) - - - - - - - -	The decay shall be smooth, with ringing, break points, double time constants, or discontinuities less than 15 percent I_p maximum, but not observable 100 ns after start of the pulse.

FIGURE 1020-2. ESD classification test circuit waveforms (human body model).

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METHOD 1021.3

MOISTURE RESISTANCE

1. Purpose. The moisture resistance test is performed for the purpose of evaluating, in an accelerated manner, the resistance of component parts and constituent materials to the deteriorative effects of the high-humidity and heat conditions typical of tropical environments. Most tropical degradation results directly or indirectly from absorption of moisture vapor and films by vulnerable insulating materials, and from surface wetting of metals and insulation. These phenomena produce many types of deterioration, including corrosion of metals; constituents of materials; and detrimental changes in electrical properties. This test differs from the steady-state humidity test and derives its added effectiveness in its employment of temperature cycling, which provides alternate periods of condensation and drying essential to the development of the corrosion processes and, in addition, produces a "breathing" action of moisture into partially sealed containers. Increased effectiveness is also obtained by use of a higher temperature, which intensifies the effects of humidity. The test includes a low-temperature subcycle that acts as an accelerator to reveal otherwise indiscernible evidences of deterioration since stresses caused by freezing moisture tend to widen cracks and fissures. As a result, the deterioration can be detected by the measurement of electrical characteristics (including such tests as voltage breakdown and insulation resistance) or by performance of a test for sealing. Provision is made for the application of a polarizing voltage across insulation to investigate the possibility of electrolysis, which can promote eventual dielectric breakdown. This test also provides for electrical loading of certain components, if desired, in order to determine the resistance of current-carrying components, especially fine wires and contacts, to electrochemical corrosion. Results obtained with this test are reproducible and have been confirmed by investigations of field failures. This test has proved reliable for indicating those parts which are unsuited for tropical field use.

2. Apparatus. The apparatus used for the moisture resistance test shall include temperature-humidity chambers capable of maintaining the cycles and tolerance described on figure 1021-1 and electrical test equipment capable of performing the measurements in 3.6 and 4.

3. Procedure. Specimens shall be tested in accordance with 3.2 through 3.7 inclusive, and figure 1021-1. Specimens shall be mounted in a manner that will expose them to the test environment.

3.1 Initial conditioning. Unless otherwise specified and prior to mounting specimens for the moisture resistance test, the device leads shall be subjected to a bending stress, initial conditioning in accordance with test condition E of method 2036. Where the specific sample devices being subjected to the moisture resistance test have already been subjected to the required initial conditioning, as part of another test employing the same sample devices, the lead bend need not be repeated.

3.2 Initial measurements. Prior to step 1 of the first cycle, the specified initial measurements shall be made at room ambient conditions, or as specified. When specified, the initial conditioning in a dry oven (see figure 1021-1) shall precede initial measurements and the initial measurements shall be completed within 8 hours after removal from the drying oven.

3.3 Number of cycles. Specimens shall be subjected to ten continuous cycles, each as shown on figure 1021-1. In the event of no more than one unintentional test interruption (power interruption or equipment failure) prior to the completion of the specified number of cycles (except for the last cycle) the cycle shall be repeated and the test may continue. Unintentional interruptions occurring during the last cycle require a repeat of the cycle plus an additional uninterrupted cycle. Any intentional interruption, or any unintentional interruption of greater than 24 hours, requires completion of missing cycles plus one additional cycle.

3.4 Subcycle of step 7. During at least five of the ten cycles, a low temperature subcycle shall be performed. At least 1 hour, but not more than 4 hours, after step 7 begins, the specimens shall be either removed from the humidity chamber, or the temperature of the chamber shall be reduced, for performance of the subcycle. Specimens during the subcycle shall be conditioned at -10°C +2°C, -5°C, with humidity not controlled, for 3 hours minimum as indicated on figure 1021-1. When a separate cold chamber is not used, care should be taken to assure that the specimens are held at -10°C +2°C, -5°C for the full period. After the subcycle, the specimens shall be returned to +25°C at 80 percent RH minimum and kept there until the next cycle begins.

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3.5 Applied voltage. During the moisture resistance test as specified on figure 1021-1, when specified (see 4), the device shall be biased in accordance with the specified bias configuration which should be chosen to maximize the voltage differential between chip metallization runs or external terminals, minimize power dissipation, and to utilize as many terminals as possible to enhance test results.

3.6 Conditions (see figure 1021-1). The rate of change of temperature in the chamber is unspecified; however, specimens shall not be subject to the radiant heat from the chamber conditioning processes. Unless otherwise specified, the circulation of air in the chamber shall be at a minimum cubic rate per minute equivalent to five times the volume of the chamber. The steady-state temperature tolerance is ±2°C of the specified temperature at all points within the immediate vicinity of the specimens and at the chamber surfaces. Specimens weighing 25 pounds or less shall be transferred between temperature chambers in less than 2 minutes.

3.7 Final measurements. Following step 6 of the final cycle (or step 7 if the subcycle of 3.3 is performed during the tenth cycle), devices shall be conditioned for 24 hours at room ambient conditions after which either an insulation resistance test in accordance with method 1016, or the specified +25°C electrical end-point measurements shall be performed. Electrical measurements may be made during the 24 hour conditioning period. However, any failures resulting from this testing shall be counted, and any retesting of these failures later in the 24 hour period for the purpose of obtaining an acceptable result is prohibited. No other test (e.g., seal) shall be performed during the 24 hour conditioning period. The insulation resistance test or the alternative +25°C electrical end-point measurements shall be completed within 48 hours after removing the devices from the chamber. When the insulation resistance test is performed, the measured resistance shall be no less than 10 MΩ and the test shall be recorded and data submitted as part of the end-point data. If the package case is electrically connected to the die substrate by design, the insulation resistance test shall be omitted and the specified +25°C electrical end-point measurements shall be completed within 48 hours after removal of the device from the chamber. A visual examination and any other specified end-point electrical parameter measurements (see 4.c) shall also be performed.

3.8 Failure criteria. No device shall be acceptable that exhibits:

a. Specified markings which are missing in whole or in part, faded, smeared, blurred, shifted, or dislodged to the extent that they are not legible. This examination shall be conducted with normal room lighting and with a magnification of 1X to 3X.

b. Evidence of corrosion over more than five percent of the area of the finish or base metal of any package element (i.e., lid, lead, or cap) or any corrosion that completely crosses the element when viewed with a magnification of 10X to 20X.

c. Leads missing, broken, or partially separated.

d. Corrosion formations which bridge between leads, or between leads and metal case.

e. Electrical end-point or insulation resistance test failures.

NOTE: The finish shall include the package and entire exposed lead area from meniscus to the lead tip (excluding the sheared off tip itself) and all other exposed metal surfaces.

4. Summary. The following details shall be specified in the applicable acquisition document:

a. Initial measurements and conditions, if other than room ambient see 3.1.

b. Applied voltage, when applicable see 3.5, and bias configuration, when required. This bias configuration shall be chosen in accordance with the following guidelines:

(1) Only one supply voltage (V) either positive or negative is required, and an electrical ground (GND) or common terminal. The magnitude of V will be the maximum such that the specified absolute maximum ratings are not exceeded and test conditions are optimized.

(2) Unless otherwise specified, all normally specified voltage terminals and ground leads shall be connected to GND.

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(3) Unless otherwise specified, all data inputs shall be connected to V. The polarity and magnitude of V is chosen to minimize internal power dissipation and current flow into the device. Unless otherwise specified, all extender inputs shall be connected to GND.

(4) All additional leads (e.g. clock, set, reset, outputs) considered individually, shall be connected to V or GND, whichever minimizes current flow.

(5) Leads with no internal connection shall be biased to V or GND whichever is opposite to an adjacent lead.

c. Final measurements (see 3.7). Final measurements shall include all electrical characteristics and parameters which are specified as end-point electrical parameters.

d. Number of cycles, if other than ten see 3.3.

e. Conditioning in dry oven before initial measurements, if required see 3.2.

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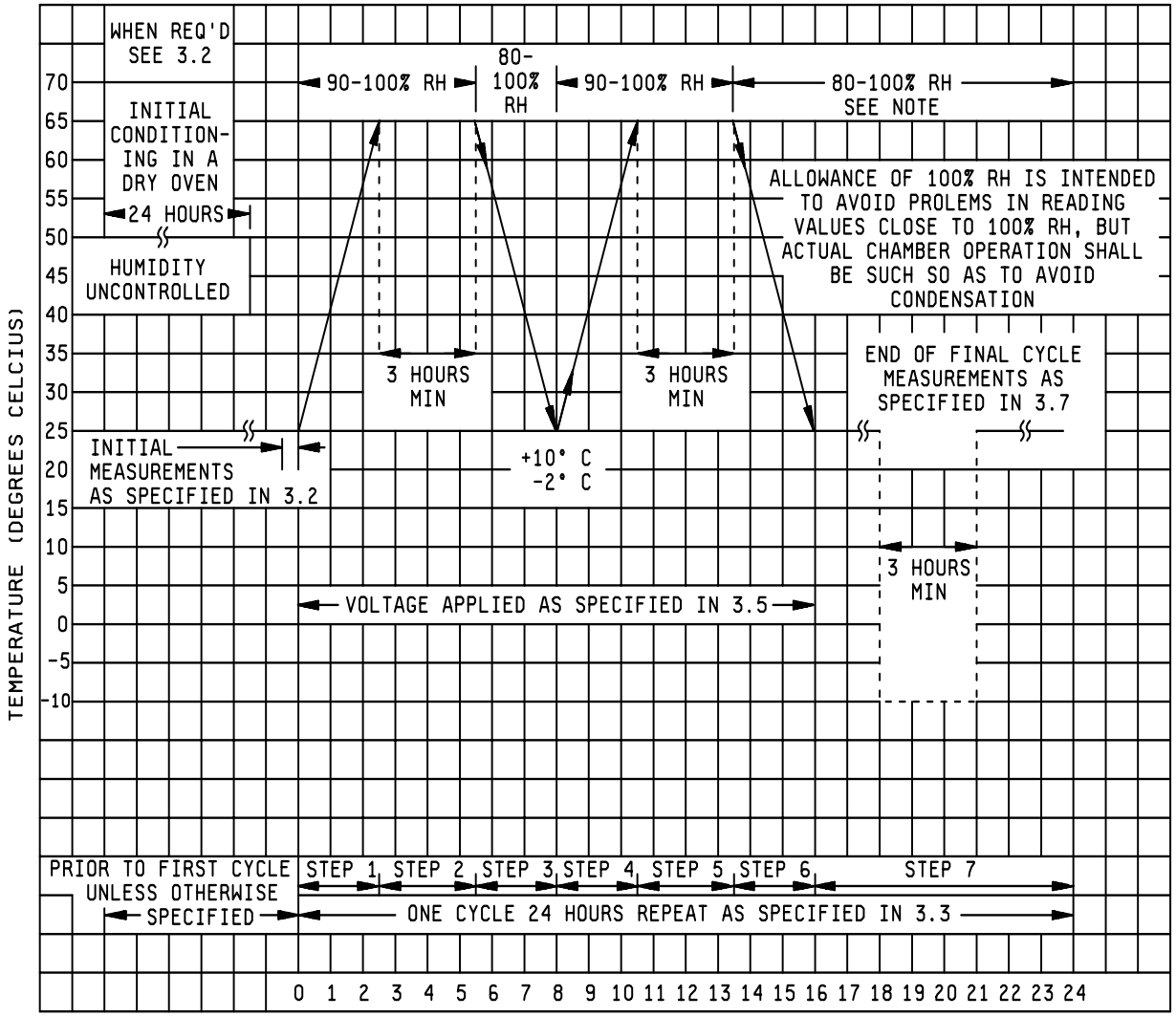

NOTE: The subcycle of step 7 (see 3.4) shall be performed for a minimum of five of the ten cycles. Humidity is uncontrolled for the -10°C portion of step 7.

FIGURE 1021-1. Graphical representation of moisture-resistance test.

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METHOD 1022.5

RESISTANCE TO SOLVENTS

1. Purpose. The purpose of this test is to verify that the markings will not become illegible on the component parts when subjected to solvents. The solvents will not cause deleterious, mechanical or electrical damage, or deterioration of the materials or finishes.

1.1 Formulation of solvents. The formulation of solvents herein is considered typical and representative of the desired stringency as far as the usual coatings and markings are concerned. Many available solvents which could be used are either not sufficiently active, too stringent, or even dangerous to humans when in direct contact or when the fumes are inhaled.

1.2 Check for conflicts. When this test is referenced, care should be exercised to assure that conflicting requirements, as far as the properties of the specified finishes and markings are concerned, are not invoked.

2. Materials.

2.1 Solvent solutions. The solvent solutions used in this test shall consist of the following:

a. A mixture consisting of the following:

(1) One part by volume of isopropyl alcohol, A.C.S. (American Chemical Society) Reagent Grade, or isopropyl alcohol in accordance with TT-I-735, grade A or B.

(2) Three parts by volume of mineral spirits in accordance with MIL-PRF-680, type II, grade A, or three parts by volume of a mixture of 80 percent by volume of kerosene and 20 percent by volume ethylbenzene.

b. A semiaqueous based solvent (defluxer (e.g., a turpene)) consisting of a minimum of 60 percent Limonene and a surfactant heated to +32°C ±5°C. 1/

c. At +63°C to +70°C, a mixture consisting of the following: 2/

(1) 42 parts by volume of deionized water.

(2) 1 part by volume of propylene glycol monomethyl ether.

(3) 1 part by volume of monoethanolamine.

2.1.1 Solvent solutions, safety aspects. Solvent solutions listed in 2.1 herein exhibit some potential for health and safety hazards. The following safety precautions should be observed:

a. Avoid contact with eyes.

b. Avoid prolonged contact with skin.

c. Provide adequate ventilation.

d. Avoid open flame.

e. Avoid contact with very hot surfaces.

1/ Or any equivalent Environmental Protection Agency (EPA) approved Hydrochlorofluorocarbons (HCFC) or terpene solvent or demonstrated equivalent.

2/ Normal safety precaution for handling this solution (e.g., same as those for diluted ammonium hydroxide) based on Occupational Safety and Health Administration (O.S.H.A.) rules for monoethanolamine.

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2.2 Vessel. The vessel shall be a container made of inert material, and of sufficient size to permit complete immersion of the specimens in the solvent solutions specified in 2.1.

2.3 Brush. The brush shall be a brush with a handle made of a nonreactive material. The brush shall have three long rows of hard bristles, the free ends of which shall lie substantially in the same plane. The brush shall be used exclusively with a single solvent and when there is any evidence of softening, bending, wear, or loss of bristles, it shall be discarded.

3. Procedure. The specimens subjected to this test shall be divided into three groups. Metal lidded leadless chip carrier (LCC) packages shall be preconditioned by immersing the specimens in room temperature ROL1 flux (in accordance with J-STD-004A, Requirements for Soldering Fluxes) for 5 to 10 seconds. The specimens shall then be subjected to an ambient temperature of +215°C ±5°C for 60 seconds +5, -0 seconds. After the preconditioning, each device lid shall be cleaned with isopropyl alcohol. Each group shall be individually subjected to one of the following procedures:

a. The first group shall be subjected to the solvent solution as specified in 2.1.a. maintained at a temperature of +25°C ±5°C.

b. The second group shall be subjected to the solvent solution as specified in 2.1.b. maintained at a temperature of +32°C ±5°C.

c. The third group shall be subjected to the solvent solution as specified in 2.1.c. maintained at a temperature of +63°C to +70°C.

The specimens and the bristle portion of the brush shall be completely immersed for 1 minute minimum in the specified solution contained in the vessel specified in 2.2. Immediately following immersion, the specimen shall be brushed with normal hand pressure (approximately 2 to 3 ounces) for ten strokes on the portion of the specimen where marking has been applied, with the brush specified in 2.3. Immediately after brushing, the above procedure shall be repeated two additional times, for a total of three immersions followed by brushings. The brush stroke shall be directed in a forward direction, across the surface of the specimen being tested. After completion of the third immersion and brushing, devices shall be rinsed and all surfaces air blown dry. After 5 minutes, the specimens shall be examined to determine the extent, if any, of deterioration that was incurred.

3.1 Optional procedure for the third group. The test specimens shall be located on a test surface of known area which is located 6 ±1 inches (15.24 ±2.54 centimeters) below a spray nozzle(s) which discharges 0.139 gpm (0.6 ±.0.02 liters/ minute) of solution (see 2.1.c) 1 in^2 (6.5 square centimeters) of surface area at a pressure of 20 ±5 psi (137.90 ±34.41 kilopascal). The specimens shall be subjected to this spray for a period of 10 minutes minimum. Within five minutes after removal of the specimens, they shall be examined in accordance with 3.1.1. The specimens may be rinsed with clear water and air blown dried prior to examination.

3.1.1 Failure criteria. After subject to the test, evidence of damage to the device and any specified markings which are missing in whole or in part, faded, smeared, blurred, or shifted (dislodged) to the extent that they cannot be readily identified from a distance of at least 6 inches (15.24 cm) with normal room lighting, and without the aid of magnification, or with a viewer having a magnification no greater than 3X, shall constitute a failure.

4. Summary. The number of specimens to be tested shall be specified in the individual specification (see 3.).

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METHOD 1026.5

STEADY-STATE OPERATION LIFE

1. Purpose. The purpose of this test is to determine compliance with the specified lambda (λ) for devices subjected to the specified conditions.

2. Procedure. The semiconductor device shall be subjected to the steady-state operation life test at the temperature specified for the time period in accordance with the life test requirements of MIL-PRF-19500 and herein. The device shall be operated under the specified conditions.

Unless otherwise specified, lead-mounted devices should be mounted by the leads with jig mounting clips at least .375 inch (9.5 mm) from the body, or from the lead tabulation, if the lead tubulation projects from the body. Unless otherwise specified, mounting and connections to surface mount devices shall be made only at their terminations. Unless a free-air life test is specified, case mounted device types (e.g., stud, flange, disc) shall be mounted by their normal case surface. The point of connection shall be maintained at a temperature not less than the specified temperature.

After the termination of the test, or in accordance with the period specified in MIL-PRF-19500 and the performance specification, if otherwise defined, the sample units shall be removed from the specified test conditions and allowed to reach standard test conditions. Specified end-point measurements for qualification and quality conformance inspection shall be completed within 96 hours after removal of sample units from the specified test conditions. Additional readings may be taken at the discretion of the manufacturer. If end-point measurements cannot be performed within the specified time, the devices shall be subjected to the same test conditions for a minimum of 24 additional hours before post test measurements are performed.

3. Summary. The following conditions shall be specified in the performance specification:

   a. Test type and details; rectifying or forward dc current and V_r for rectifiers and signal diodes, dc power (or current) for zener diodes, power (and range of V_{CE} and V_{DS}) for bipolar and FETs (see 2).

   b. Test temperature, if other than room ambient.

   c. Test mounting, if other than that specified (see 2).

   d. End-point measurements (see 2).

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METHOD 1027.3

STEADY-STATE OPERATION LIFE (SAMPLE PLAN)

1. Purpose. The purpose of this test is to determine compliance with the specified sample plan for devices subjected to the specified conditions.

2. Procedure. Unless otherwise specified, the semiconductor device shall be subjected to the steady-state operation test at the temperature specified for 340 hours minimum. The device shall be operated under the specified conditions.

Unless otherwise specified, lead-mounted devices should be mounted by the leads with jig mounting clips at least .375 inch (9.5 mm) from the body or from the lead tubulation if the lead tubulation projects from the body. Unless otherwise specified, mounting and connections to surface mount devices shall be made only at their terminations. Unless free-air life test is specified, case mounted device types (e.g., stud, flange, disc) shall be mounted by their normal case surface. The point of connection shall be maintained at a temperature not less than the specified temperature.

After the termination of the test, or in accordance with the period specified by MIL-PRF-19500 and the performance specification if otherwise defined, the sample units shall be removed from the specified test conditions and allowed to reach standard test conditions. Specified end-point measurements for qualification and quality conformance inspection shall be completed within 96 hours after removal of sample units from the specified test conditions. Additional readings may be taken at the discretion of the manufacturer. If end-point measurements cannot be performed within the specified time, the devices shall be subjected to the same test conditions for a minimum of 24 additional hours before post test measurements are performed.

3. Summary. The following conditions shall be specified in the detail specification:

   a. Test type and details; rectifying or forward dc current and V_r for rectifiers and signal diodes, dc power (or current) for zener diodes, power (and range of V_{CE} and V_{DS}) for bipolar and FETs (see 2).

   b. Test temperature, if other than room ambient.

   c. Test time, if other than 340 hours (see 2).

   d. Test mounting, if other than that specified (see 2).

   e. End-point measurements (see 2).

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METHOD 1031.5

HIGH-TEMPERATURE LIFE (NONOPERATING)

1. Purpose. The purpose of this test is to determined compliance with the specified lambda (λ) for devices subjected to the specified conditions.

2. Procedure. The device shall be stored under the specified ambient conditions (normally the maximum temperature) for a time period in accordance with the life test requirements of MIL-PRF-19500. In accordance with the life test period specified by MIL-PRF-19500, the sample units shall be removed from the specified ambient conditions and allowed to reach standard test conditions. Specified end-point measurements for qualification and quality conformance inspection shall be completed within 96 hours after removal of sample units from the specified ambient conditions. If measurements can not be performed within the specified time, the devices shall be subjected to the same test conditions for a minimum of 24 additional hours before post test measurements are performed. Additional readings may be taken at the discretion of the manufacturer.

2.1 Visual examination. The markings shall be legible after the test. There shall be no evidence (when examined without magnification) of flaking or pitting of the finish or corrosion that will interfere with the mechanical and electrical application of the device.

3. Summary. The following conditions shall be specified in the detail specification:

a. Test conditions (see 2).

b. End-point measurements (see 2).

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METHOD 1032.2

HIGH-TEMPERATURE (NONOPERATING) LIFE (SAMPLE PLAN)

1. Purpose. The purpose of this test is to determine compliance with the specified sample plan for devices subjected to the specified conditions.

2. Procedure. Unless otherwise specified, the device shall be stored under the specified ambient conditions (normally the maximum temperature) 340 hours minimum. The sample units shall be removed from the specified ambient conditions and allowed to reach standard test conditions. Specified end-point measurements for qualification and quality conformance inspection shall be completed within 96 hours after removal of sample units from the specified ambient conditions. If measurements cannot be performed within the specified time, the devices shall be subjected to the same test conditions for a minimum of 24 hours before post test measurements are performed. Additional readings may be taken at the discretion of the manufacturer.

2.1 Visual examination. The markings shall be legible after the test. There shall be no evidence (when examined without magnification) of flaking or pitting of the finish or corrosion that will interfere with the mechanical and electrical application of the device.

3. Summary. The following conditions shall be specified in the performance specification:

a. Test conditions (see 2).

b. Test time, if other than 340 hours (see 2).

c. End point measurements (see 2).

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METHOD 1033

REVERSE VOLTAGE LEAKAGE STABILITY

1. Purpose. This test method is designed to evaluate the short tem leakage stability of product under reverse bias conditioning. It is not intended to replace, nor does it duplicate, the high temperature reverse bias conditioning. The failure mechanisms that are addressed in this test method are not sustained upon the removal of applied bias to the device. As an example; certain semiconductor designs are quite susceptible to unstable reverse leakage due to the presence of hydrogen in the device. This method can be used to ascertain the susceptibility of a technology to this type of a problem or the effectiveness of countermeasures.

2. Procedure. Condition A: Apply to the DUT at room temperature, +25°C, a minimum of 80 percent of the specified V_{cb}, V_{ds}, V_r as applicable. Apply bias and measure and record the leakage current.

Retain uninterrupted bias on the device for 1 hour minimum.

After 1 hour minimum re-measure and record the reverse leakage of the device. Interruption of the applied bias for any reason between the pre- and post-leakage measurements invalidates the test. Bias shall not be interrupted to make the reverse leakage measurement.

3. Failure criteria. The following shall be used as the pass/fail criteria for this test:

For measured Ir < 100nA	Delta Ir = 100 nA max.
For measured Ir 100 nA < Ir < 1μA	Delta Ir = 200 nA max.
For measured Ir > 1 μA	Delta Ir = Less than 50 percent of initial measurement.

4. Condition B. Sweep the voltage in the BVCEO mode until the breakdown of the device is observed and study the breakdown leakage plot for a minimum of 10 seconds for stability. An unstable plot will be considered any device which exhibits one or more of the following:

a. Collapsing.

b. Leakage increasing.

A device will be considered passing when none of the instability modes are noticed from 4.a and 4.b after a period of approximately 10 seconds. The device will be then subjected to a leakage test.

Sweep the voltage of the device to the maximum leakage identified on the applicable performance specification sheet. Observe the amplitude of the leakage. Leakage is defined as I_{cbo}, I_{ces}, or I_{cex} as specified in the applicable performance specification.

After 30 seconds minimum, the maximum change in leakage allowed is as specified for burn-in in the performance specification.

Perform the breakdown and leakage on the specified number of samples in accordance with the individual performance specification. One hundred percent must be performed on the entire lot if any device from the sample fails the above tests.

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METHOD 1036.3

INTERMITTENT OPERATION LIFE

1. Purpose. The purpose of this test is to determine compliance with the specified lambda (λ) for devices subjected to the specified conditions.

2. Procedure. The device shall be subjected intermittently to the specified operating and nonoperating conditions for the time period in accordance with the life test requirements of MIL-PRF-19500. The on- and off-periods shall be initiated by sudden, not gradual, application or removal of the specified operating conditions. Lead-mounted devices should be mounted by the leads with jig mounting clips at least .375 inch (9.5 mm) from the body or lead tubulation, if the lead tubulation projects from the body. The point of connection shall be maintained at a temperature not less than the specified temperature. Within the time interval of 24 hours before to 72 hours after termination of the test, in accordance with the life test period specified by MIL-PRF-19500, the sample units shall be removed from the specified test conditions and allowed to reach standard test conditions. Specified end-point measurements for qualification and quality conformance inspection shall be completed within 96 hours after removal of sample units from the specified test conditions. Additional readings may be taken at the discretion of the manufacturer.

3. Summary. The following conditions shall be specified in the performance specification:

   a. Test conditions (see 2).

   b. Operating and nonoperating cycles (see 2).

   c. Test temperature (case or ambient).

   d. Test mounting, if other than that specified (see 2).

   e. End point measurements (see 2).

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METHOD 1037.2

INTERMITTENT OPERATION LIFE (SAMPLE PLAN)

1. Purpose. The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.

2. Mounting. Clips or fixtures appropriate for holding the device terminations and reliably conducting the heating current shall be used. This method is intended to allow the case temperature to rise and fall appreciably as the junction is heated and cooled; thus it is not appropriate to use a large heat sink. Lead-mounted devices, when specified, should be mounted by the leads with jig mounting clips at least .375 inch (9.5 mm) from the body, or from the lead tubulation if it projects from the body.

3. Procedure. All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly, not gradually, to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors) +15°C, -5°C, followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature. Auxiliary (forced) cooling is permitted during the off period only.

DC current shall be used for the power required during the "on" period except, for rectifiers and thyristors, equivalent half sine wave (or full sine wave for triacs) is permissible. The test power, or current, shall be at least the free air rating. For disc types, where functional mounting requires heat sinking, it shall be at least 25 percent of the continuous, case referenced, rating. The on time (leaded and axial leaded devices) shall be at least 30 seconds. Unless otherwise specified, for TO-3, DO-5, and larger devices it shall be at least one minute. Specified end-point measurements for qualification and quality conformance inspection shall be completed within 96 hours after removal of sample units from the specified test conditions. Additional readings may be taken at the discretion of the manufacturer. If measurements cannot be performed within the specified time, the devices shall be subjected to the same test conditions for a minimum of 200 additional cycles before post test measurements are performed.

4. Summary. The following conditions shall be specified in the performance specification:

   a. Test conditions (power or current, see 3).

   b. Number of operating cycles (see 3), if other than 2,000.

   c. Test mounting, if other than that specified (see 2).

   d. End-point measurements (see 3.1).

NOTE: Heat sinks are not intended to be used in this test, however, small heat sinks may be used when it is otherwise difficult to control case temperature of test samples, such as with small package types (e.g., TO-39).

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METHOD 1038.4

BURN-IN (FOR DIODES, RECTIFIERS, AND ZENERS)

1. Purpose. This test is performed to eliminate marginal devices or those with defects resulting from manufacturing aberrations that are evidenced as time and stress dependent failures. Without the burn-in, these defective devices would be expected to result in early lifetime failures under normal use conditions. It is the intent of this test to operate the semiconductor device at specified conditions to reveal electrical failure modes that are time and stress dependent.

a. HTRB screens for mobile or temperature activated impurities within (and without) the device's passivation layers. It is equally effective on most device types including diodes, rectifiers, zeners, and transient voltage suppressors.

b. SSOP, when properly specified, simulates actual device operation but with accelerated conditions. Some of the elements of HTRB are combined with screening for die bond integrity. It is effective on some device types including diodes, rectifiers, and zeners. The conditions used for zeners provide the desired HTRB screen concurrently with the SSOP screen.

2. Mounting. Unless otherwise specified in the performance specification, mounting shall be in accordance with the following.

2.1 Test condition A, HTRB. The method of mounting is usually optional for high temperature bias since little power is dissipated in the device. (Devices with normally high reverse leakage current may be mounted to heat sinks to prevent thermal run-away conditions.)

2.2 Test condition B, SSOP.

a. Devices with leads projecting from the body (e.g., axial) shall be mounted by their leads at least .375 inch (9.73 mm) from the body or lead tabulation.

b. Unless otherwise specified, devices designed for case mounting (e.g., stud, flange, and disc) shall be mounted by the stud or case according to the design specifications for the package. Care must be exercised to avoid stressing or warping of the package. Thermally conductive compounds may optionally be used provided that they are removed afterwards and do not leave a residue on the package.

c. Surface mount types shall be held by their electrical terminations.

3. Procedure. The semiconductor device shall be subjected to the burn-in at the temperature and for the time specified herein or on the performance specification. Pre-burn-in measurements shall be made as specified. The failure criteria shall be as specified in the appropriate performance specification. If measurements cannot be performed within the specified time, the devices shall be subjected to the same test conditions for a minimum of 24 additional hours before test measurements are performed.

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3.1 Test condition A, HTRB. Unless otherwise specified, HTRB is performed with the cathode positively biased at an artificially elevated temperature for 48 hours minimum. These conditions apply to both rectifiers and to avalanche and zener voltage regulators.

a. The junctions of rectifiers shall be reverse biased at 50 to 80 percent in accordance with figure 1038-1 of their rated working peak reverse voltage; avalanche and zener voltage regulators, when specified, shall be reverse biased at 80 percent of their minimum avalanche or zener voltages except when voltage exceeds 2,500, see figure 1038-1. The reverse bias shall be a dc bias with less than 20 percent ripple except where rectified (pulsating) dc is permitted. The ambient or case test temperature shall be as specified (normally +150°C for silicon devices) (see figure 1038-1).

b. At the end of the high-temperature test time, as specified, the ambient temperature shall be lowered. The test voltage shall be maintained on the devices until a case temperature of +30°C ±5°C is attained. Testing shall be completed within 24 hours after the removal of voltage. After removal of the bias voltage, no other voltage shall be applied to the device before taking the post HTRB reverse current measurement. Post HTRB measurements shall be taken as specified.

Uni-directional transient voltage suppressors shall be treated as avalanche and zener voltage regulators for the purposes of conducting HTRB.

Bi-directional transient voltage suppressors shall be treated as two discrete avalanche or zener voltage regulators (when specified) with each polarity taking turns receiving HTRB and post HTRB testing. Post HTRB testing of one must be completed before reversing the device and commencing HTRB with opposite polarity bias voltage. The second polarity may be achieved either electrically or by mechanically reversing the devices.

3.2 Test condition B, steady-state operating power. Unless otherwise specified, the devices shall be subjected to the maximum rated test conditions for a minimum of 96 hours. The test temperature shall be as specified. Unless otherwise specified, post burn-in readings shall be taken within 96 hours. If ambient temperature is specified, it shall comply with the general requirements for HTRB or burn-in of this specification (see 4.5). The following indicates the test conditions to be specified for each of the three types of power burn-in tests:

a. Rectifying test. Unless otherwise specified, average rectified current, peak reverse voltage, frequency, and temperature (case, junction, or ambient) are as specified in the performance specification.

b. Forward bias test. Unless otherwise specified, forward current and temperature (case or junction) are as specified in the performance specification.

c. Voltage regulator (zener) test. Unless otherwise specified, voltage regulator diode current and temperature (case or junction) are as specified in the performance specification. At the end of the test time, the power level shall be reduced to five percent of the operating level. If the ambient is artificially elevated, it shall also be reduced to room temperature. The object is to let the devices cool down under bias. When the junction or case temperature has stabilized to below +50°C, the bias may be removed and the devices tested within 96 hours after removal of reverse bias. No other voltage may be applied to the devices until completion of electrical test.

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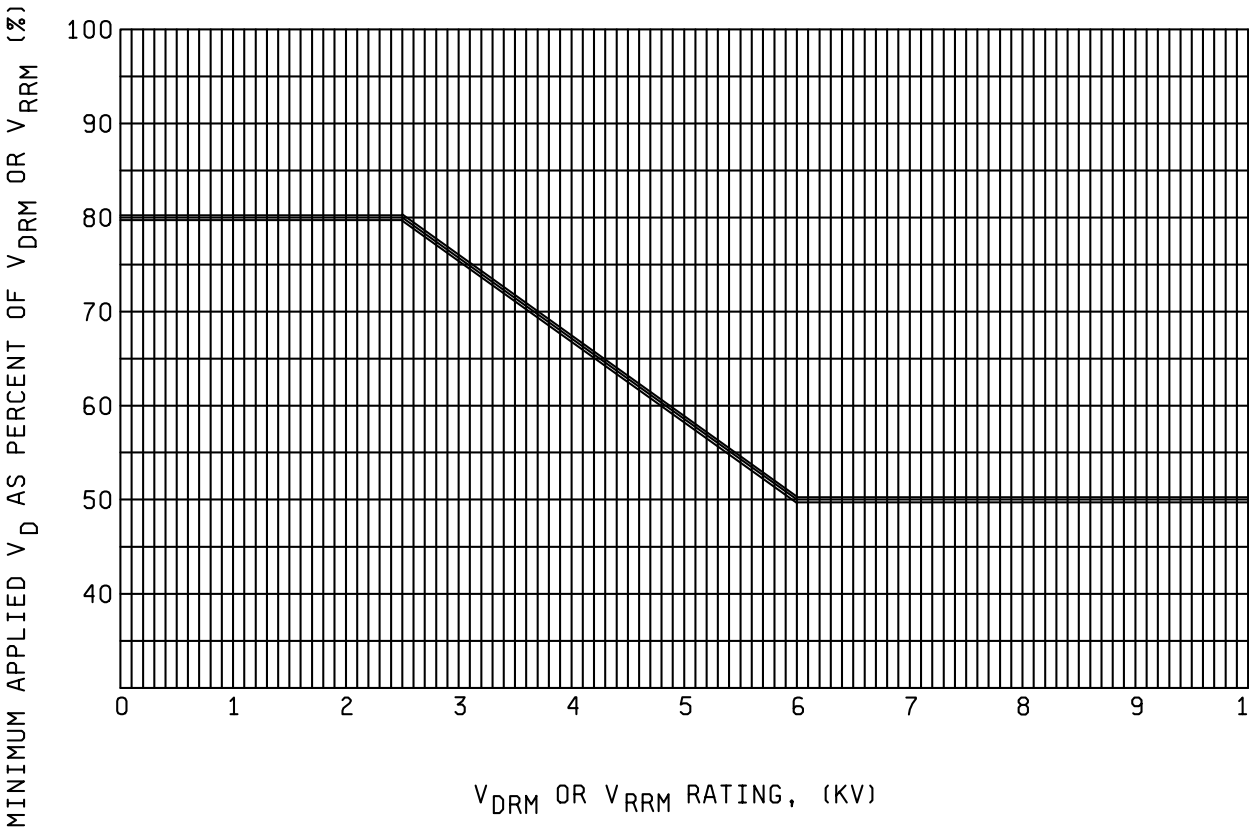

FIGURE 1038-1. Voltage requirement.

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4. Summary. The test condition letter (A or B) and the following details shall be specified in the applicable performance specification.

4.1 Test condition A, HTRB.

a. Test temperature (see 3.1).

b. Test conditions (see 2.1 and 3.1).

c. Test time (see 3.1).

d. Preburn-in and post burn-in measurements (see 3. and 3.1).

e. Time for completion of post burn-in measurements, if other than 24 hours (see 3.1).

f. Criteria for failure (see 3.).

4.2 Test condition B, steady-state operating power.

a. Test temperature (see 3.2).

b. Test conditions (see 2.2 and 3.2).

c. Burn-in time if other than 96 hours (see 3.2).

d. Pre-burn-in and post burn-in measurements (see 3. and 3.2).

e. Time for completion of post burn-in measurements, if other than 96 hours (see 3.2).

f. Criteria for failure (see 3.).

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METHOD 1039.4

BURN-IN (FOR TRANSISTORS)

1. Purpose. This test is performed to eliminate marginal devices or those with defects resulting from manufacturing aberrations that are evidenced as time and stress dependent failures. Without the burn-in, these defective devices would be expected to result in early lifetime failures under normal use conditions. It is the intent of this test to operate the semiconductor device at specified conditions to reveal electrical failure modes that are time and stress dependent.

2. Procedure. The semiconductor device shall be subjected to the burn-in at the temperature and for the time specified herein. Preburn-in measurements shall be made as applicable. The failure criteria shall be as specified.

2.1 Mounting. Devices with leads projecting from the body shall be mounted by their leads at least .250 inch (6.35 mm) from the seating plane. Unless otherwise specified, devices with studs or case shall be mounted by the stud or case.

2.1.1 Test condition A, steady-state reverse bias. The transistor primary blocking junction, as specified, shall be reverse biased for 48 hours minimum, except PNP bipolar transistors shall be 24 hours, at the ambient temperature specified (normally +150°C) and at 80 percent of its maximum rated collector-base voltage. For bipolar transistors, the V_{CB} base is not to exceed the maximum collector-emitter voltage rating. For field-effect (signal or low power) transistors, the gate to source voltage, with drain to source shorted, shall be as specified. At the end of the high-temperature test time, specified herein, the ambient temperature shall be lowered. The test voltage shall be maintained on the devices until T_C = +30°C ±5°C is attained. After room ambient temperature has been established, the bias voltage shall be removed. After removal of the bias voltage, no other voltage shall be applied to the device before taking the post burn-in reverse-current measurement(s). Unless otherwise specified, after burn-in voltage is removed, post burn-in measurements shall be completed within 24 hours. If measurements cannot be performed within the specified time, the devices shall be subjected to the same test conditions for a minimum of 24 additional hours before post test measurements are performed.

2.1.2 Test condition B, steady-state power. All devices shall be operated at the maximum rated power related to the test temperature for 160 hours minimum at the specified test conditions (excluding microwave).

a. For bipolar transistors, the temperature and power shall be specified. Unless otherwise specified, the temperature shall be as follows:

   T_A = room ambient as defined in, 4.5 of the general specification. for small signal, switching, and medium power devices intended for printed circuit board mounting; T_J = maximum rated temperature, +0°C, -25°C, for devices intended for chassis or heat sink mounting. Case temperature burn-in at maximum ratings (typically T_C = +100°C) may be substituted on the chassis or heat sink mounted devices at the supplier's option. If the voltage conditions specified herein cause the SOA rating to be exceeded, then the voltage shall be decreased until the SOA rating is met while maintaining the full rated power condition. For microwave bipolar transistors, the temperature, voltage, and current shall be as specified in the detail specification.

b. For unijunction and field-effect (signal and low power) transistors, the temperature, voltage, and current shall be as specified.

c. Post burn-in measurements shall be as specified.

d. Unless otherwise specified, post burn-in readings shall be taken within 96 hours. If measurements cannot be performed within the specified time, the devices shall be subjected to the same test conditions for a minimum of 24 additional hours before post test measurements are performed.

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3. Summary. Test condition letter and the following conditions shall be specified in the performance specification.

3.1 Test condition A:

a. Junction to be reverse biased (see 2.1.1).

b. Gate to source voltage for FETs (see 2.1.1).

c. Test temperature (see 2.1.1).

d. Test time for FETs (see 2.1.1).

e. Voltage for post burn-in reverse current measurement (see 2.1.1).

f. Time for completion of post burn-in measurements, if other than 24 hours (see 2.1.1).

g. Criteria for failure (see 2.).

3.2 Test condition B:

a. Test temperature, if other than as specified in 2.1.2.

b. Test conditions (see 2.1.2).

c. Power for bipolar transistors (see 2.1.2).

d. Voltage and current for unijunction and FETs (see 2.1.2).

e. Preburn-in and post burn-in measurements (see 2.1.2).

f. Time for completion of post burn-in measurements, if other than as specified in 2.1.2.

g. Criteria for failure (see 2.).

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METHOD 1040

BURN-IN (FOR THYRISTORS
(CONTROLLED RECTIFIERS))

1. Purpose. The purpose of this test is to eliminate marginal or defective semiconductor devices by operating them at specified screening conditions which reveal electrical failure modes that are time and stress dependent. In the absence of burn-in, these defective devices would be expected to result in early lifetime failures under normal use conditions.

2. Procedure. Lead mounted devices shall be mounted by the leads at least .375 inch (9.5 mm) from the body or lead tubulation, if the lead tubulation projects from the body. Unless otherwise specified, stud or case mounted devices shall be mounted by the stud or case respectively. The devices shall then be subjected to the burn-in screen(s) at the temperature and for the time specified. Pre burn-in and postburn-in measurements shall be made as specified.

2.1 Test condition A (ac blocking voltage). The rated peak reverse and the rated peak forward blocking voltage shall be alternately applied, each in the form of a 60 Hz half wave sinusoidal pulse using the circuit of figure 1040-1. The test temperature shall be as specified. At the end of the specified high temperature test time, the ambient temperature shall be lowered. The test voltage shall be maintained on the devices until T_C = +30°C ±5°C is attained. After bias is removed and prior to post-test measurements, the devices shall be maintained at room ambient temperature and no voltage shall be applied prior to that voltage specified for the post-test measurements. The post-test end-points shall be completed within the specified time after the bias voltage is removed. Any device which switches from the off-state to the on-state as indicated by a blown fuse shall be removed from the lot.

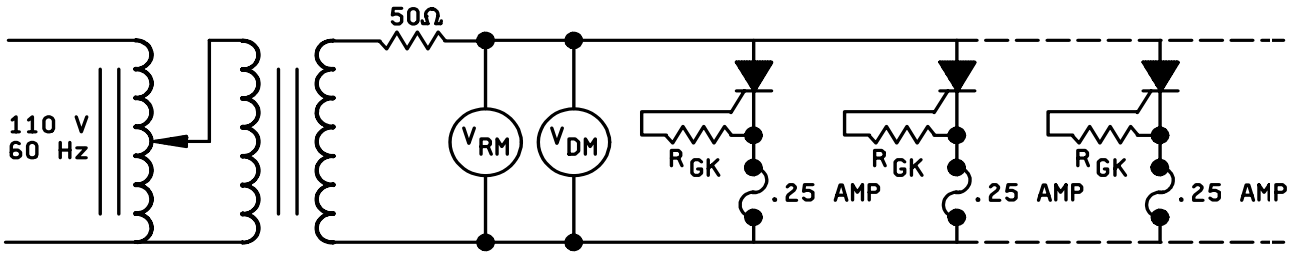

FIGURE 1040-1. AC blocking voltage circuit.

2.2 Test condition B (dc forward blocking voltage). The rated dc forward blocking voltage shall be applied as indicated in the circuit on figure 1040-2. The test temperature shall be as specified. At the end of the specified high-temperature test time, the ambient temperature shall be lowered. The test voltage shall be maintained on the devices until T_C = +30°C ±5°C is attained. After bias is removed and prior to post test measurements, the devices shall be maintained at room ambient temperature and no voltage shall be applied prior to that voltage specified for the post test measurements. The post test end points shall be completed within the specified time after the bias voltage is removed. Any device which switches from the off-state to the on-state as indicated by a blown fuse shall be removed from the lot.

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3. Measurements. Initial readings shall be taken prior to burn-in. Post-test readings shall be taken within 96 hours.

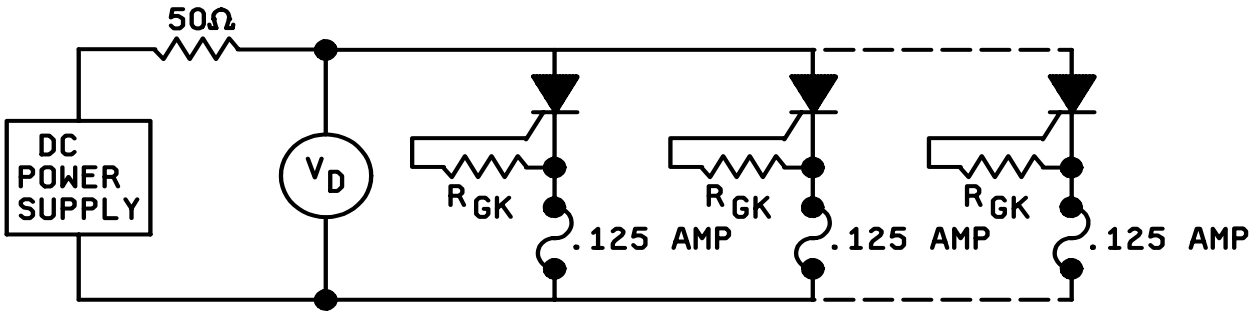

FIGURE 1040-2. DC forward blocking voltage circuit.

4. Summary. The test condition letter and the following conditions shall be specified in the performance specification:

a. Test condition A:

1. Peak forward and reverse blocking voltage (see 2.1).
2. Test temperature (see 2.1).
3. Duration of burn-in (see 2.1).
4. R_{GK} (see figure 1040-1).
5. Preburn-in and postburn-in measurements (see 3.).

b. Test condition B:

1. DC forward blocking voltage (see 2.2).
2. Test temperature (see 2.2).
3. Duration of burn-in (see 2.2).
4. R_{GK} (see figure 1040-2).
5. Preburn-in and postburn-in measurements (see 3.).

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METHOD 1041.3

SALT ATMOSPHERE (CORROSION)

1. Purpose. This test is an accelerated laboratory corrosion test simulating the effects of seacoast atmospheres on devices.

2. Apparatus. Apparatus used in the salt-atmosphere test shall include the following:

   a. Exposure chamber with racks for supporting devices.

   b. Salt-solution reservoir.

   c. Means for atomizing the salt solution, including suitable nozzles and compressed-air supply.

   d. Chamber-heating means and controls.

   e. Means for humidifying the air at a temperature above the chamber temperature.

3. Procedure. The device shall be placed within the test chamber. Unless otherwise specified, a salt atmosphere fog having a temperature of +35°C (+95°F) shall be passed through the chamber for a period of 24 +2, -0 hours. The fog concentration and velocity shall be adjusted so that the rate of salt deposit in the test area is between 10 and 50 g/m^2/day.

4. Examinations. Unless otherwise specified, upon completion of the test, and to aid in the examinations, devices shall be prepared in the following manner: Salt deposits shall be removed by a gentle wash or dip in running water not warmer than +37°C (+100°F) and a light brushing, using a soft-hair brush or plastic bristle brush. A device with illegible markings, leads missing, broken, or partially separated, evidence (when examined with 10X magnification) of flaking or pitting of the finish or corrosion exceeding five percent of the package area or five percent of the lead shall be considered a failure. Discoloration of the plating or lead finish shall not be considered a failure. The marking legibility requirement shall not apply to characters with a height of less than .030 inches (0.76 mm).

5. Summary. The following conditions shall be specified in the performance specification:

   a. Time of exposure, if other than that specified (see 3.).

   b. Measurements and examinations after test (see 4.).

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METHOD 1042.3

BURN-IN AND LIFE TEST FOR POWER MOSFETs OR INSULATED GATE BIPOLAR TRANSISTORS (IGBT)

1. Purpose. Test conditions A, B, and C are performed to eliminate marginal devices or those with defects resulting from manufacturing aberrations that are evidenced as time and stress failures under normal use conditions. Test condition D is performed to eliminate marginal lots with manufacturing defects. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Procedure. The semiconductor device shall be subjected to the burn-in at the temperature and for the time specified herein. Preburn-in measurements shall be made as applicable. The failure criteria shall be as specified.

2.1.1 Test condition A, steady-state reverse bias. All devices shall be operated at 80 percent of the maximum rated drain to source voltage at the specified test temperature for 160 hours minimum, at the specified test conditions. The drain to source voltage, with gate to source shorted, shall be as specified. At the end of the high-temperature test time, specified herein, the ambient temperature shall be lowered. The burn-in voltage shall be maintained on the devices until T_C = 30°C ±5°C is attained. The interruption of bias for up to one minute for the purpose of moving devices to cool down positions separate from the chamber, within which life testing was performed, shall not be considered removal of bias.

After removal of the burn-in voltage, no other voltage shall be applied to the device before taking the postburn-in reverse current measurement(s). After burn-in voltage is removed, postburn-in measurements shall be completed within 96 hours, unless otherwise specified. (See figure 1042-1.) Unless otherwise specified, the burn-in temperature shall be T_A = 150°C. The V_{DS} burn-in voltage shall be as follows. For IGBT devices, burn-in temperature shall be T_J = 150°C, -15°C to +0°C, and test time shall be 96 hours minimum.

If $V_{(BR)DSS}$ is 20 V	V_{DS} shall be 16 V
30 V	24 V
40 V	32 V
60 V	48 V
80 V	64 V
90 V	72 V
100 V	80 V
120 V	96 V
150 V	120 V
170 V	136 V
200 V	160 V
240 V	192 V
350 V	280 V
400 V	320 V
450 V	360 V
500 V	400 V
600 V	480 V

$V_{(BR)DSS}$ voltages in between shall revert to the next lower V_{DS} burn-in voltage.

2.1.1.1 Temperature accelerated test details. In an accelerated test, devices are subjected to bias conditions at a temperature exceeding the maximum rated junction temperature. The maximum ambient temperature for MOSFETs is +175°C for a minimum of 48 hours. It is recommended that an adequate sample of devices be exposed to the high temperature while measuring the voltage(s) and current(s) of the devices to assure that the applied stresses do not induce damaging overstress. An adequate sample which has completed the accelerated test should also be subjected to a 1,000 hour steady-state reverse bias at standard test conditions to assure the devices have not been deleteriously affected. Details of the accelerated test will be found in the performance and /or general specification.

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2.1.2 Test condition B, steady-state gate bias. All devices shall be operated at 80 percent of the maximum rated gate to source voltage at the specified temperature for a minimum of 48 hours. (See figure 1042-2.) For MOSFET power transistors, the temperature and voltage shall be as specified. Unless otherwise specified, the temperature (T_A) shall be 150°C.

If maximum rated V_{GS} is	10 V	Burn-in voltage (V_{GS}) shall be	8 V
	15 V		12 V
	20 V		16 V
	30 V		24 V
	40 V		32 V

V_{GS} voltages in between shall revert to the next lower voltage.

2.1.3 Test condition C, steady-state power. All devices shall be operated at the maximum junction temperature +0°C, 24°C by means of applying power to the device while maintaining an ambient temperature of +25°C +10°C, -5°C. The junction temperature shall be verified by means of measuring junction temperature using the change in body diode voltage drop or calculated by applying the following equations:

$T_J = R_{\Theta JA} \times P_D + T_A$ No heat sink used

or

$T_J = R_{\Theta JC} \times P_D + T_C$ Heat sink used

T_C = Temperature of case

T_A = Ambient air temperature

T_S = Temperature of heat sink

$P_D = V_{DS} \times I_D$

V_{DS} = Drain-source voltage

I_D = Drain-source current

NOTE: The power indicated by the safe operating curve shall not be exceeded.

2.1.4 Test condition D, intermittent power. 1/ All devices shall be subjected to the number of cycles as specified. A cycle shall consist of applying power to the device for the time necessary to achieve a +100°C +15°C, -10°C minimum rise in junction temperature followed by an off period for the time necessary for the junction to cool. Forced air cooling is permitted during the off period only.

The power level, power-on time, and heat sink used, if any, shall be chosen to ensure that at the end of the heating cycle, the case temperature is not more than 15°C below the junction temperature. The rise in junction temperature during the on period shall be verified by means of measuring junction temperature using the change in body diode voltage drop or calculated by applying the following equation.

$\Delta T_J = P_T R_{\Theta JA} (1 - \text{Exp} - t/T_p)$, where $P_T = V_{DS} I_D$

T_P = thermal time constant of device package, and the heat sink used.

t = heating time, $R_{\Theta JA}$ = thermal resistance junction to ambient, for the period of heating time specified, of the device and any necessary heat sink used.

This test is intended to allow the case temperature to rise and fall appreciably as the junction is heated and cooled; thus, it is not appropriate to use a large heat sink or a high power short pulse.

1/ This test condition is destructive.

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3. Summary. Test condition letter and the following details shall be specified in the individual performance specification.

3.1 Test condition A.

a. Drain to source voltage for MOSFET power field-effect transistors (V_{DS}) (see 2.1.1).

b. Test temperature, if other than specified (see 2.1.1).

c. Test time, if other than specified (see 2.1.1).

d. Voltage for post burn-in reverse current measurement (see 2.1.1).

e. Criteria for failure.

3.2 Test condition B.

a. Test temperature, if other than as specified (see 2.1.2).

b. Test conditions (see 2.1.2).

c. Voltage for MOSFET power field-effect transistors (see 2.1.2).

d. Preburn-in and post burn-in measurements.

e. Criteria for failure.

3.3 Test condition C.

a. Ambient temperature and thermal resistance (see 2.1.3).

b. Voltage and current, if other than specified (see 2.1.3).

c. Preburn-in and postburn-in measurements.

d. Total test time (see 2.1.3).

e. Criteria for failure.

3.4 Test condition D.

a. Ambient temperature (if one is desired) and thermal resistance (see 2.1.4).

b. Voltage and current, if other than specified (see 2.1.4).

c. Pretest and post test measurements.

d. Number of cycles (see 2.1.4).

e. Criteria for failure.

f. Minimum heating time.

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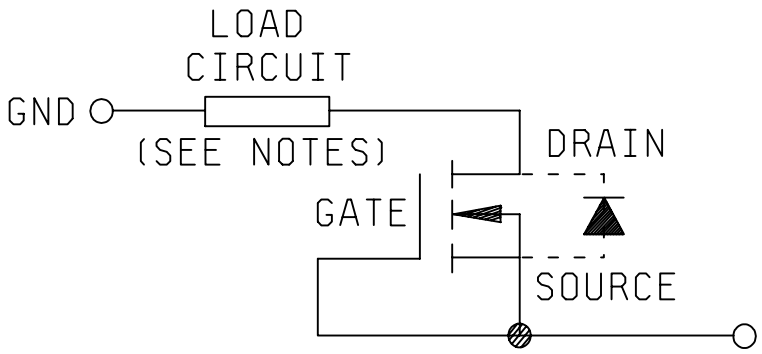

NOTES:

1. The load circuit shall be selected or designed to ensure that the voltage across the load circuit of each acceptable device shall not exceed 10 percent of the specified test voltage. The load circuit may be a resistor, fuse, or circuit which:
   a. Protects the power supply.
   b. Isolates the defective devices from the other devices under test.
   c. Insures a minimum of 98 percent of the specified test voltage is applied across the DUT.
2. If the circuit does not maintain bias on a failed device, then means must be provided to identify that device.

FIGURE 1042-1. High temperature reverse bias test circuit.

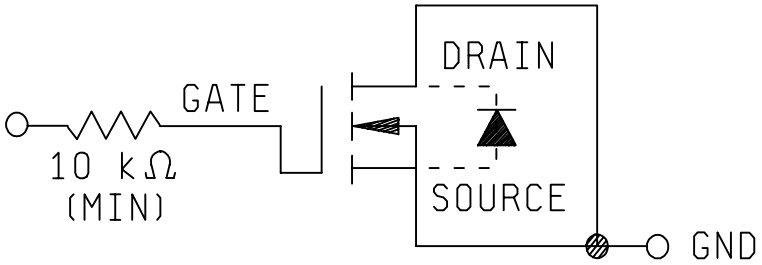

FIGURE 1042-2. High temperature gate bias circuit.

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METHOD 1046.3

SALT SPRAY (CORROSION)

1. Purpose. This test is proposed as an accelerated laboratory corrosion test simulating the effects of seacoast atmosphere on devices. This test can also be used to detect the presence of free iron contaminating the surface of another metal, by inspection of the corrosion products.

2. Apparatus. Apparatus used in the salt-spray test shall include the following:

a. Exposure chamber with racks for supporting specimens.

b. Salt-solution reservoir with means for monitoring an adequate level of solution.

c. Means for atomizing the salt solution, including suitable nozzles and compressed-air supply.

d. Chamber-heating means and control.

e. Means for humidifying the air at a temperature above the chamber temperature.

2.1 Chamber. The chamber and all accessories shall be made of material which will not affect the corrosiveness of the fog, such as glass, hard rubber, or plastic. Wood or plywood shall not be used since they are resiniferous. Materials shall not be used if they contain formaldehyde or phenol in their composition. In addition, all parts which come in contact with test specimens shall be of materials that will not cause electrolytic corrosion. The chamber and accessories shall be so constructed and arranged that there is no direct impinging of the spray or dripping of the condensate on the specimens, so that the spray circulates freely about all specimens to the same degree, and so that no liquid which has come in contact with the test specimens returns to the salt-solution reservoir. The chamber shall be properly vented to prevent pressure build up and allow uniform distribution of salt spray. The discharge end of the vent shall be protected from strong drafts which can cause strong air current in the chamber.

2.2 Atomizers. The atomizer of atomizers used shall be of such design and construction as to produce a finely divided, wet dense fog. The atomizing nozzle shall be made of material which does not react with the salt solution.

2.3 Air supply. The compressed air entering the atomizers shall be free from all impurities such as oil and dirt. Means shall be provided to humidify and warm the compressed air as required to meet the operating conditions. The air pressure shall be suitable to produce a finely divided dense fog with the atomizer or atomizers used. To insure against clogging the atomizers by salt deposition, the air should have a relative humidity of 95 to 98 percent at the point of release from the nozzle. A satisfactory method is to pass the air in very fine bubbles through a tower containing heated water. The temperature of the water shall be +95°F (+35°C) or higher. The permissible temperature is increased with increasing volume of air and with decreasing heat insulation of the chamber and temperature of its surroundings. It shall not exceed a value above which an excess of moisture is introduced into the chamber (for example, +110°F (+43.3°C) at an air pressure of 12 pounds per square inch), or a value which makes it impossible to meet the requirement for operating temperature.

2.4 Salt solution. The salt solution concentration shall be 5 percent by weight. The salt used shall be sodium chloride containing on the dry basis of more than 0.1 percent of sodium iodide, and not more than 0.5 percent of total impurities. The 5 percent solution shall be prepared by dissolving 5 ±1 parts by weight of salt in 95 parts by weight of distilled or other water. Distilled or other water used in the preparation of solutions shall contain not more than 200 parts per million of total solids. The solution shall be kept free from solids by filtration using a filter similar to that shown on figure 1046-1, and located in the salt solution reservoir in a manner such as that illustrated on figure 1046-2. The solution shall be adjusted to, and maintained at, a specific gravity in accordance with figure 1046-3. The pH shall be maintained between 6.5 and 7.2 when measured at temperature between +93°F and +97°F (+33.9°C and +36.1°C). Only dilute chemically pure (cp) grade hydrochloric acid or sodium hydroxide shall be used to adjust the pH. The pH measurement shall be made electrometrically using a glass electrode with a saturated potassium-chloride bridge or by a colorimetric method such as bromothymol blue, provided the results are equivalent to those obtained with the electrometric method.

2.5 Filter. A filter fabricated of noncorrosive materials similar to that shown on figure 1046-1 shall be provided in the supply line and immersed in the reservoir in a manner such as shown on figure 1046-2.

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2.6 Preparation of specimens. Specimens shall be given a minimum of handling, particularly on the significant surfaces, and shall be prepared for test immediately before exposure. Unless otherwise specified, uncoated metallic or metallic-coated specimens shall be thoroughly cleaned of oil, dirt, and grease as necessary until the surface is free from water break. The cleaning methods shall not include the use of corrosive solvents nor solvents which deposit wither corrosive or protective films, nor the use of abrasives other than a paste of pure magnesium oxide. Specimens having an organic coating shall not be solvent cleaned. Those portions of specimens which comes in contact with the support and, unless otherwise specified in the case of coated specimens or samples, cut edges and surfaces not required to be coated, shall be protected with a suitable coating of wax or similar substance impervious to moisture.

3. Procedure. The following exceptions shall apply:

a. At the conclusion of the test, the device will be dried for 24 hours at +40°C ±5°C before the examination. A device with illegible marking, evidence (when examined without magnification) of flaking or pitting of the finish, or corrosion that will interfere with the application of the device shall be considered a failure.

b. Unless otherwise specified, salt solution shall be 20 percent by weight.

3.1 Location of specimens. Unless otherwise specified, flat specimens and, where practicable, other specimens shall be supported in such a position that the significant surface is approximately 15º degrees from the vertical and parallel to the principal direction of horizontal flow of the fog through the chamber. Other specimens shall be positioned so as to ensure most uniform exposure. Whenever practicable, the specimens shall be supported from the bottom or from the side. When specimens are suspended from the top, suspension shall be by means of glass or plastic hooks or wax string; if plastic hooks are used, they shall be fabricated of material which is nonreactive to the salt solution such as Lucite. The use of metal hooks is not permitted. Specimens shall be positioned so that they do not contact each other, so that they do not shield each other from the freely settling fog, and so that corrosion products and condensate from one specimen do not fall upon another.

3.2 Operating conditions.

3.2.1 Temperature. The test shall be conducted with a temperature in the exposure zone maintained at +95°F +2°F, -3°F (+35°C +1.1°C, -1.7°C). Satisfactory methods for controlling the temperature accurately are by housing the apparatus in a properly controlled constant-temperature room, by thoroughly insulating the apparatus and preheating the air to the proper temperature prior to atomization, and by jacketing the apparatus and controlling the temperature of the water or of the air used. The use of immersion heaters for the purpose of maintaining the temperature within the chamber is prohibited.

3.2.2 Atomization. The conditions maintained in all parts of the exposure zone shall be such that a suitable receptacle placed at any point in the exposure zone will collect from 0.5 to 3.0 milliliters of solution per hour for each 80 square centimeters of horizontal collecting area (10 centimeters diameter) based on an average run of at least 16 hours. The 5-percent solution thus collected shall have a sodium-chloride content of from 4 to 6 percent (specific gravity) in accordance with figure 1046-3 when measured at a temperature between +93°F and +97°F (+33.9°C and +36.1°C). At least two clean fog-collecting receptacles shall be used, one placed near any nozzle and one placed as far as possible from all nozzles. Receptacles shall be fastened so that they are not shielded by specimens and so that no drops of solution from specimens or other sources will be collected. The specific gravity and quantity of the solution collected shall be checked following each salt-spay test. Suitable atomization has been obtained in boxes having a volume of less than 12 cubic feet with the following conditions:

a. Nozzle pressure of from 12 to 18 pounds per square inch.

b. Orifices of from .02 to .03 inch in (0.508 to 0.762 mm) diameter.

c. Atomization of approximately 3 quarts of the salt solution per 10 cubic feet of box volume per 24 hours.

When using large-size boxes having a volume considerably in excess of 12 cubic feet, the above conditions may have to be modified in order to meet the requirements for operating conditions.

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3.3 Length of test. The length of the salt-spray test shall be that indicated in one of the following test conditions, as specified:

Test condition		Length of test
A	- - - - - - - -	96 hours
B	- - - - - - - -	48 hours

Unless otherwise specified, the test shall be run continuously for the time indicated or until definite indication of failure is observed, with no interruption except for adjustment of the apparatus and inspection of the specimen.

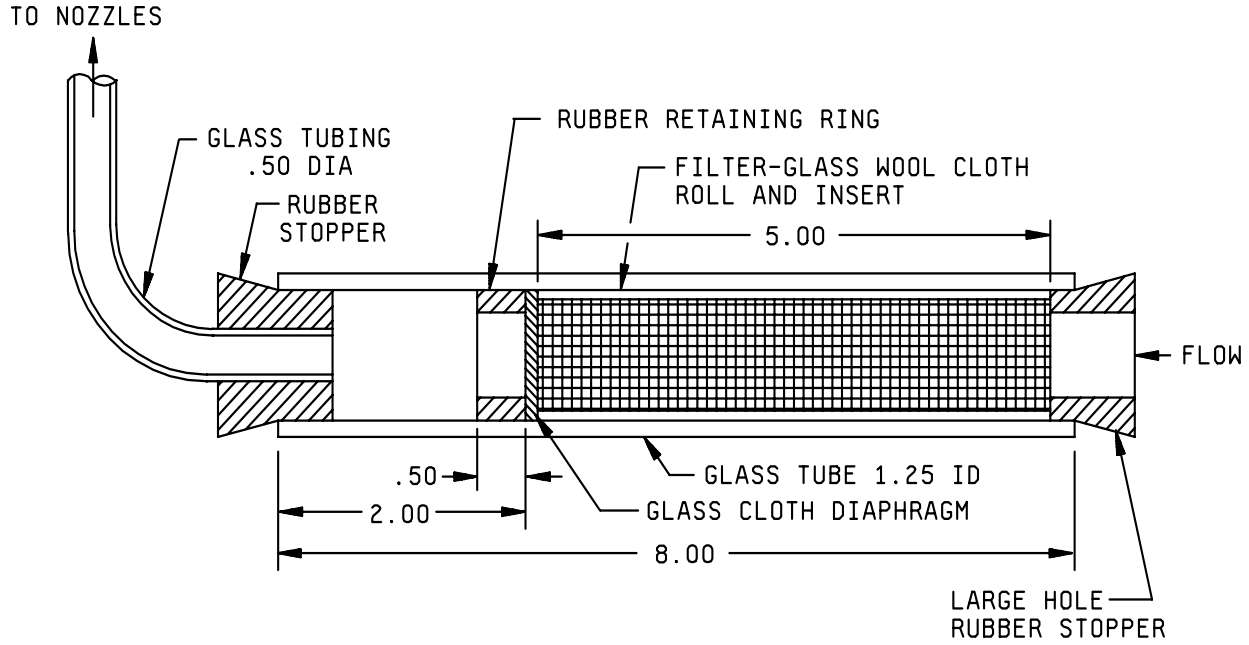
4. Measurements. At the completion of the exposure period, measurements shall be made as specified. To aid in examination, specimens shall be prepared in the following manner, unless otherwise specified: Salt deposits shall be removed by a gentle wash or dip in running water not warmer than +100°F (+37.8°C) and a light brushing, using a soft-hair brush or plastic-bristle brush.

5. Summary. The following details are to be specified in the individual performance specification:

a. Special mounting and details, if applicable (see 3.1).

b. Test condition letter (see 3.3).

c. Measurements after exposure (see 4).



Inches	Millimeters
.50	12.70
1.25	31.75
2.00	50.80
5.00	127.00
8.00	203.20

FIGURE 1046-1. Salt solution filter.

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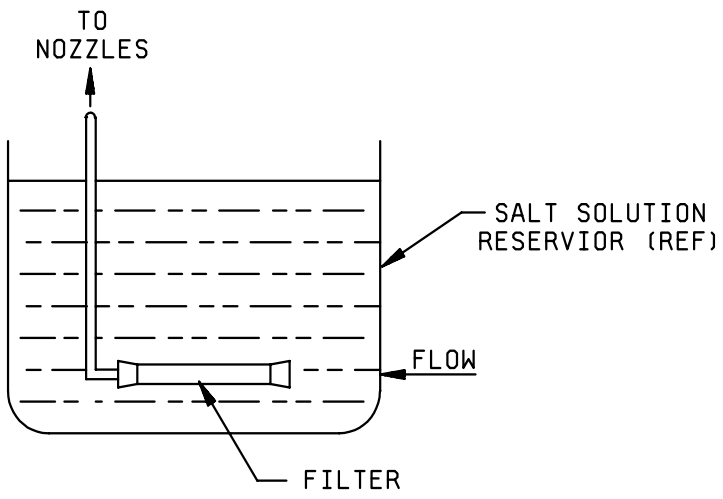

FIGURE 1046-2. Location of salt solution filter.

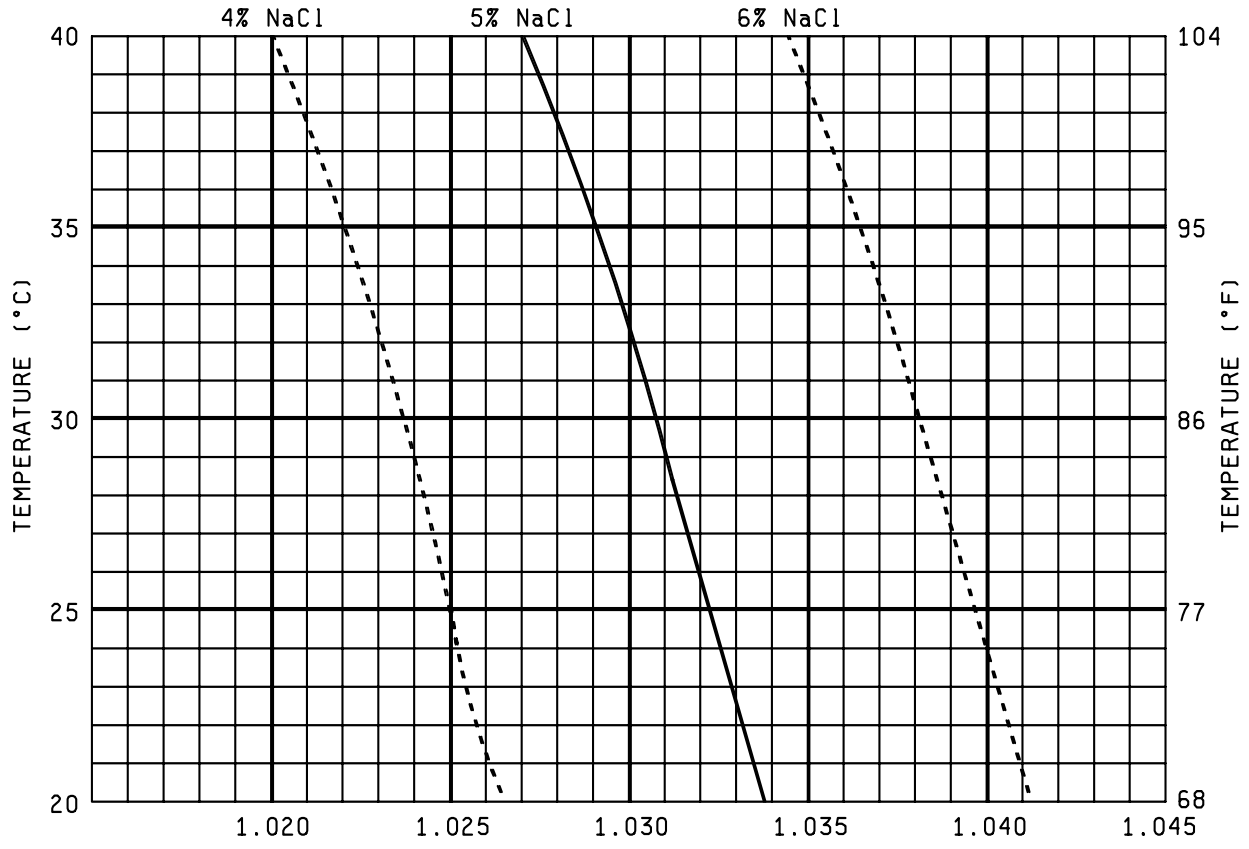

FIGURE 1046-3. Variations of specific gravity of salt (NaCl) solution with temperature.

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METHOD 1048

BLOCKING LIFE

1. Purpose. The purpose of this test is to determine compliance with the specified lambda (λ) for devices subjected to the specified conditions.

2. Mounting. The method of mounting is usually optional for blocking life tests since little power is dissipated in the device. (Devices with normally high reverse leakage current may be mounted to heat sinks to prevent thermal run-away conditions.)

3. Procedure. Blocking life is performed with the primary blocking junction, or insulation, reverse biased at an artificially elevated temperature for the time period in accordance with the life test requirements of MIL-PRF-19500 and herein; at the temperature specified (normally +150°C and at 80 to 85 percent of the rated voltage relevant to the device (V_R, V_Z(min), V_{CB}, V_{AG}, V_{DG}, and V_{GS}).

At the end of the high-temperature test time, as specified, the ambient temperature shall be lowered. The test voltage shall be maintained on the devices until a case temperature of +30°C ±5°C is attained. After this ambient temperature has been established, the bias voltage shall be maintained until testing is performed; testing shall be completed within 24 hours after the removal of power. After removal of the bias voltage, no other voltage shall be applied to the device before taking the post-test leakage current measurement. Post-test measurements shall be taken as specified.

4. Summary. The following details shall be specified in the applicable performance specification:

   a. Test temperature (see 3.).

   b. Test conditions: Voltage and terminals to be biased (see 2. and 3.).

   c. Test time (see 3.).

   d. Pre- and post-test measurements (see 3.).

   e. Time for completion of post-test measurements, if other than 24 hours (see 3.).

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METHOD 1049

BLOCKING LIFE (SAMPLE PLAN)

1. Purpose. The purpose of this test is to determine compliance with the specified sample plan for devices subjected to the specified conditions.

2. Mounting. The method of mounting is usually optional for blocking life tests since little power is dissipated in the device. (Devices with normally high reverse leakage current may be mounted to heat sinks to prevent thermal run-away conditions.)

3. Procedure. Unless otherwise specified, blocking life is performed with the primary blocking junction, or insulation, reverse biased at an artificially elevated temperature for 340 hours, at the temperature specified (normally +150°C and at 80 to 85 percent of the rated voltage relevant to the device (V_R, V_Z (min), V_{CB}, V_{AG}, V_{DG}, and V_{GS}).

At the end of the high-temperature test time, as specified, the ambient temperature shall be lowered. The test voltage shall be maintained on the devices until a case temperature of +30°C ±5°C is attained. After this ambient temperature has been established, the bias voltage shall be maintained until testing is performed; testing shall be completed within 24 hours after the removal of power. After removal of the bias voltage, no other voltage shall be applied to the device before taking the post-test leakage current measurement. Post-test measurements shall be taken as specified.

4. Summary. The following details shall be specified in the applicable performance specification:

   a. Test temperature (see 3.).

   b. Test conditions: Voltage and terminals to be biased (see 2. and 3.).

   c. Test time (see 3.).

   d. Pre- and post-test measurements (see 3).

   e. Time for completion of post test measurements, if other than 24 hours (see 3.1).

   f. Criteria for failure (see 3.).

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METHOD 1051.6

TEMPERATURE CYCLING (AIR TO AIR)

1. Purpose. This test is conducted to determine the resistance of a part to extremes of high and low temperatures, and to the effect of alternate exposures to these extremes.

1.1 Terms and definitions.

1.1.1 Load. The specimens under test and the fixtures holding those specimens during the test. Maximum load shall be determined by using the worst case load temperature with specific specimen loading. Monolithic loads used to simulate loading may not be appropriate when air circulation is reduced by load configuration. The maximum loading must meet the specified conditions.

1.1.2 Monitoring sensor. The temperature sensor that is located and calibrated so as to indicate the same temperature as at the worst case indicator specimen location. The worst case indicator specimen location is identified during the periodic characterization of the worst case load temperature.

1.1.3 Worst case load temperature. The worst case load temperature is the temperature of a specific area in the chamber when measured by thermocouples located at the center and at each corner of the load. The worst case load temperature shall be determined at periodic intervals.

1.1.4 Working zone. The volume in the chamber(s) in which the temperature of the load is controlled within the limits specified in table 1051-I.

1.1.5 Specimen. The device or individual piece being tested.

1.1.6 Transfer time. The elapsed time between specimen removal from one temperature extreme and introduction into the other.

1.1.7 Maximum load. The largest load for which the worst case load temperature meets the timing requirements (see 3.1).

1.1.8 Soak time. The elapsed time that occurs after the load has reached the temperature specified in table 1051-I.

NOTE: During chamber profiling and characterization, a device temperature sensitive parameter should be used to ensure that for various load conditions, the specified soak time shall be guaranteed.

1.1.9 Ramp time. The time allowed for reaching a given temperature. This timing starts when the load is introduced to the chamber and ends when the load reaches the temperature specified in table 1051-I.

CAUTION: Due to the ramp capability of test equipment available today, if care is not taken when profiling and characterizing various load conditions or setting up the equipment, thermal shock can be induced. The ramp rate should be controlled as defined in 3.1 or one can create a thermal shock instead of temperature cycling.

2. Apparatus. The chamber(s) used shall be capable of providing and controlling the specified temperatures in the working zone(s) when the chamber is loaded with a maximum load. The thermal capacity and air circulation shall enable the working zone and loads to meet the specified conditions and timing (see 3.1). Worst case load temperature shall be continually monitored during test by indicators or recorders reading the monitoring sensor. Direct heat conduction to specimens shall be minimized.

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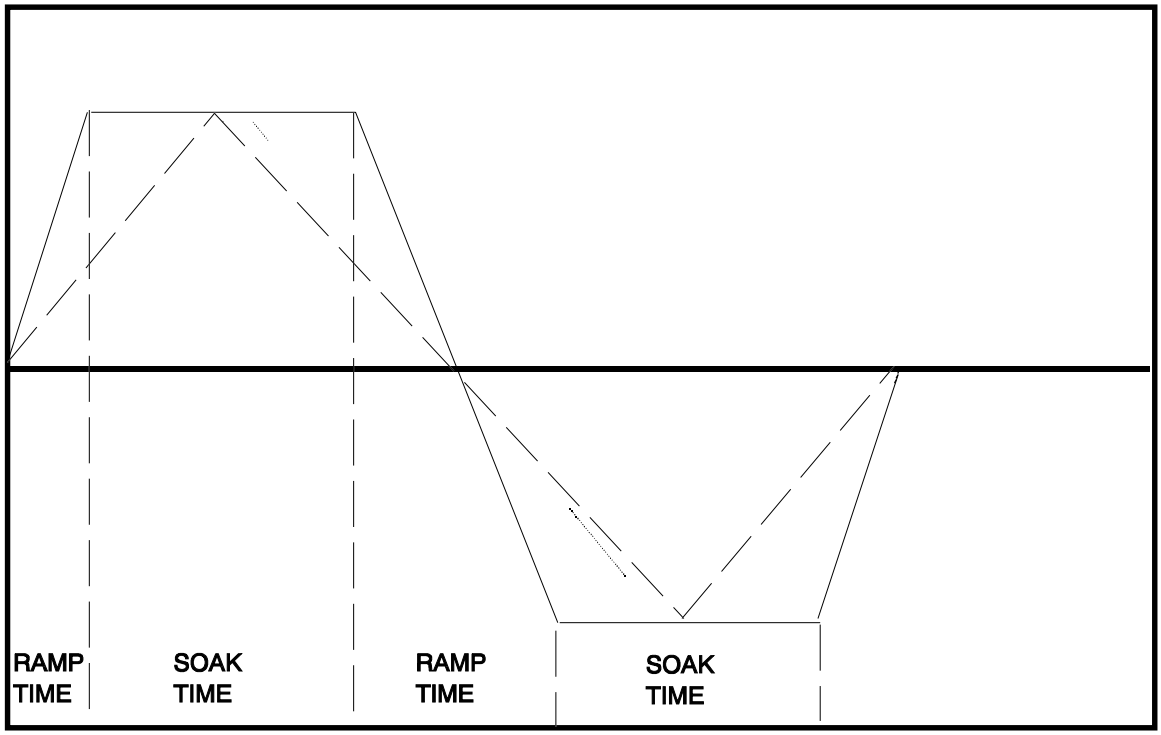
3. Procedure. Specimens shall be placed in such a position with respect to the air stream that there is substantially no obstruction to the flow of air across and around the specimen. When special mounting is required, it shall be specified. The specimen shall then be subjected to the specified condition for the specified number of cycles performed continuously. This test shall be conducted for a minimum of 20 cycles using test condition C. One cycle consists of steps 1 and 2 or the applicable test condition to be counted as a cycle. Completion of the total number of cycles specified for the test may be interrupted for the purpose of test chamber loading or unloading of device lots or as the result of power or equipment failure. However, if for any reason the number of incomplete cycles exceed 10 percent of the total number of cycles specified, one cycle must be added for each incomplete cycle. See Figure 1051-I herein.



Graph depicting two possible scenarios based on current interpretations of wording in specification.

———— Temperature profile with soak at temperature extremes

- - - - - - - - - - - - Temperature profile with no soak time

FIGURE 1051-I. Ramp and soak time scenarios.

* 3.1 Timing. The total transfer time from hot to cold or cold to hot shall not exceed 1 minute. The load may be transferred after a soak of 1 minute minimum. However the ramp time shall not exceed 15 minutes. The ramp rate for DUT shall operate within the following temperature change rates: 15°C/minute minimum and 50°C/minute maximum independent of load size.

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TABLE 1051-I. Temperature-cycling test conditions.

Step	Minutes	Test condition temperature (°C)						
		A	B	C	D	E	F	G
1 Cold	≥ 10	-55 +0 -10	-55 +0 -10	-55 +0 -10	-65 +0 -10	-65 +0 -10	-65 +0 -10	-55 +0 -10
2 Hot	≥ 10	85 +10 -0	125 +15 -0	175 +15 -0	200 +15 -0	300 +15 -0	150 +15 -0	150 +15 -0

NOTE: Steps 1 and 2 may be interchanged. The load temperature may exceed the + or - zero (0) tolerance during the recovery time. Other tolerances shall not be exceeded.

4. Summary. The following details shall be specified in the applicable performance specification:

   a. Special mounting, if applicable (see 3.).

   b. Test condition letter, if other than test condition C herein (see 3.).

   c. Number of test cycles, if other than 20 cycles (see 3.).

   d. End-point measurements and examinations, e.g., end-point electrical measurements, seal test (method 1071 of this general specification), or other acceptance criteria.

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METHOD 1054.1

POTTED ENVIRONMENT STRESS TEST

1. Purpose. The purpose of this test is to determine device design susceptibility to intermittent open failures in conformally coated circuit boards environments while under thermal cycle. The destructive effects of tension and compression are magnified in the potted condition allowing for early detection of design weakness.

2. Equipment.

   a. Container of 3 cubic inches minimum with rigid walls of .125 inch (3.18 mm) minimum.

   b. Devices for testing corrected to a common bussbar arranged in a common cathode or common anode configuration (see figure 1054-1).

   c. Thermal cycling chamber.

   d. Hot plate capable of maintaining +70°C.

   e. Curve tracer, Tektronix 576 or equivalent.

   f. Potting medium, Emerson and Cuming Stycast 2851 MT or equivalent.

3. Procedure:

   a. Place devices in a common connection configuration into the container with provisions made to ensure device clearance of .125 inch (3.18 mm) minimum from the container walls.

   b. Pour stycast potting compound into shell and allow to cure while following all manufacturer's recommendations.

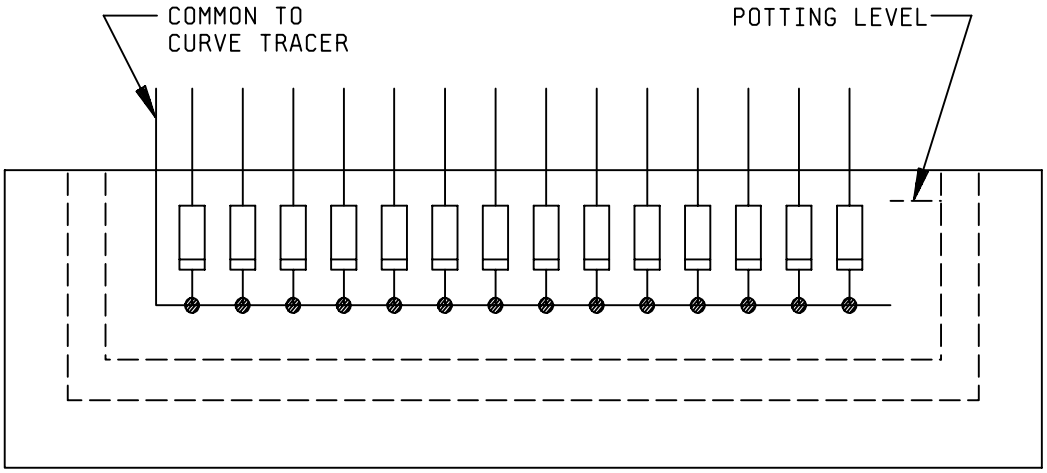

FIGURE 1054-1. Potted diodes.

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c. Place cured assembly on a hot plate and allow the assembly to reach thermal equilibrium of +70°C. Unless otherwise specified, observe the forward voltage trace of each device at a current level of 100 mA. Forward voltage trace should show no incidence of instability or open condition. Record all failures by serial number.

d. Allow assembly to cool at room temperature and place into a thermal shock chamber to perform 20 shocks in accordance with method 1051 of this general specification. Remove assembly and allow to reach room temperature.

e. Repeat 3.c. and record failures.

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METHOD 1055.1

MONITORED MISSION TEMPERATURE CYCLE

1. Purpose. This test is to determine the ability of devices to withstand the effect of thermal stress and rapid dimensional change on internal structural elements caused by the application of power in rapidly changing temperature environments as in mission profile system testing.

2. Apparatus. The equipment required shall consist of that listed below and shall have the stated capabilities.

   a. A chamber of sufficient temperature range and change rate capability with cabling exiting through insulated barriers to external bias and monitoring electronics. Cabling for all monitoring equipment shall provide Kelvin connections.

   b. Electronic regulated power supply(s) capable of maintaining the stated bias tolerances.

   c. Electronic voltage monitoring device with capability of indicating an open circuit of 20 ms or more in duration.

3. Procedure.

   a. Devices conforming to all electrical and mechanical parameter requirements shall be first subjected to high temperature stabilization bake of method 1032 of this general specification. They shall then be subjected to temperature cycling non-operational thermal shock of method 1051 of this general specification, except that no dwell time is required at +25°C. Test condition C shall be +175°C, +5°C, -0°C. Temperature shall remain at the stabilized extremes for 10 minutes minimum.

   b. Electrical measurements shall be performed to ensure that, proceeding to the monitored thermal cycle portion of this test, all devices have remained within specification.

   c. Unless otherwise specified, the temperature extremes shall be as stated below (from worse case mission profile requirements of MIL-HDBK-781.

   d. The temperature and operating profile shall be specified on figure 1055-1. Temperature change rate shall average not less than 5°C per minute, but not greater than 10°C per minute.

   e. The device(s) shall be placed individually, or in series connection, within the chamber. The device(s) shall be connected to a constant current power supply capable of supplying current to raise the device junction(s) to +125°C minimum, +150°C maximum temperature during the high temperature portion of each cycle.

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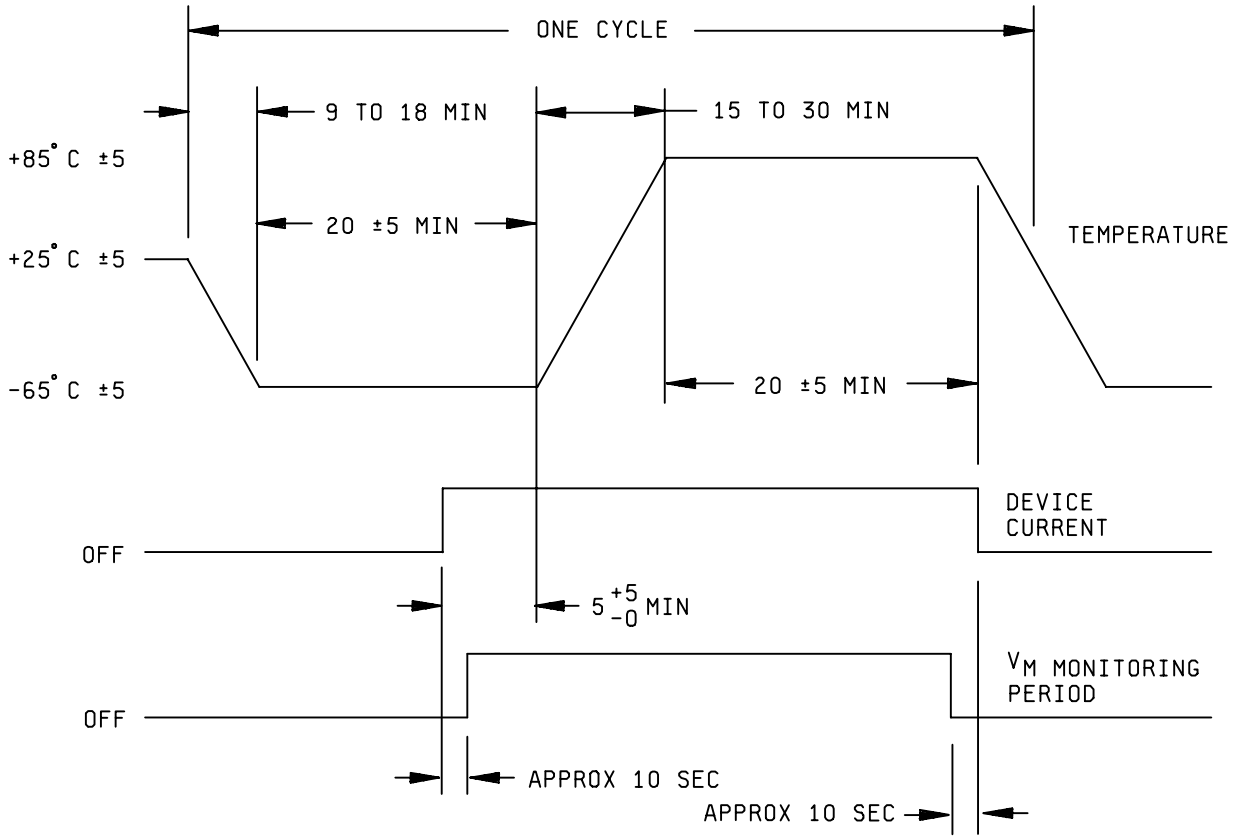

FIGURE 1055-1. Monitored mission cycle.

3.1 Electrical monitoring. Connect electrical monitoring volt meter leads to the extremes of the device(s) and series resistor (see figure 1055-2). Apply the current to raise each junction temperature approximately +50°C. The value of R shall be chosen to cause a 10 ±3 percent increase in monitoring voltage, V_M, if open circuit occurs. Open switch S1 and verify an increase in V_M to verify circuit operation. Remove power.

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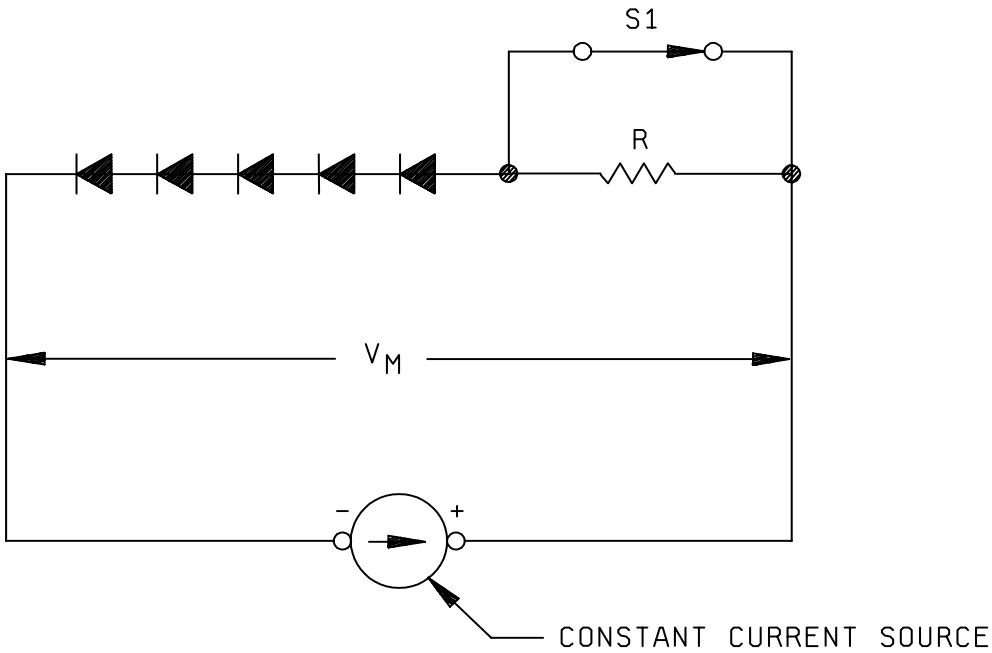

FIGURE 1055-2. Monitored mission cycle.

3.2 Monitoring voltage increase. Close S1 and perform six cycles of figure 1055-1 while monitoring for increases in voltage level above the highest (cold temperature) value.

3.3 Failures. Failures in the first two cycles may be considered non-chargeable de-bug events, if analysis finds fault with test circuitry. The last four cycles shall be failure free.

NOTE: Unless otherwise specified, a momentary, or continuous, open circuit (indicated by an increase in the monitored voltage) in any of the last four cycles, shall be considered failure.

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METHOD 1056.7

THERMAL SHOCK (LIQUID TO LIQUID)

1. Purpose. This test is conducted to determine the resistance of the part to sudden exposure to extreme changes in temperature and to the effect of alternate exposures to these extremes.

1.1 Terms and definitions.

1.1.1 Cycle. A cycle consists of starting at ambient room temperature, proceeding to step 1, then to step 2, or alternately proceeding to step 2, then to step 1 of table 1056.I and 1056.II, and then back to ambient room temperature without interruption.

1.1.2 Dwell time. The total time the load is immersed in the bath.

1.1.3 Load. The DUTs and the fixtures holding those devices.

1.1.4 Maximum load. The maximum mass of devices and fixtures that can be placed in the bath while maintaining specified temperatures and times.

1.1.5 Specimen. The device or individual piece being tested.

1.1.6 Transfer time. The elapsed time measured from removal of the load from one bath until insertion in the other bath.

1.1.7 Worst case load temperature. The body temperature of a specific device located at the center of the load.

2. Apparatus. The baths used shall be capable of providing and controlling the specified temperatures in the working zone(s) when the bath is loaded with a maximum load. The thermal capacity and liquid circulation must enable the working zone and loads to meet the specified conditions and timing (see 3.1). Worst case load temperature shall be continually monitored during test by indicators or recorders reading the monitoring sensor(s). The worst case load temperature under maximum load conditions and configuration shall be verified as needed to validate bath performance. Perfluorocarbons that meet the physical property requirements of table 1056.II shall be used for conditions B and C.

3. Procedure. Specimens shall be placed in the bath in a position so that the flow of liquid across and around them is substantially unobstructed. The load shall then be subjected to condition A or as otherwise specified (see 4.b) of table 1056.I for a duration of 15 cycles. Completion of the total number of cycles specified for the test may be interrupted for the purpose of loading or unloading of device lots or as the result of power or equipment failure. However, if the number of interruptions for any given test exceeds 10 percent of the total number of cycles specified, the test must be restarted from the beginning.

3.1 Timing. The total transfer time from hot to cold or from cold to hot shall not exceed 10 seconds. The load may be transferred when the worst case load temperature is within the limits specified in table 1056.II. However, the dwell time shall not be less than 2 minutes and the load shall reach the specified temperature within 5 minutes.

4. Summary. The following details shall be specified in the applicable performance specification.

a. Special mounting, if applicable.

b. Test condition, if other than test condition B (see 3.).

c. Number of test cycles, if other than 15 cycles (see 3.).

d. End-point measurements and examinations such as end-point electrical measurements, seal test (method 1071 of this general specification), or other acceptance criteria.

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TABLE 1056.I. Physical property requirements of perfluorocarbon fluids. 1/

Test condition		B	C	ASTM test method
Step 1	Boiling point, °C	>125	>150	D1120
	Density at 25°C gm/ml	>1.6		D941
	Dielectric strength volts/mil	>300		D877
	Residue, microgram/gram	<50		D2109
	Appearance	Clear, colorless liquid		Not applicable
Step 2	Density at 25°C gm/ml	>1.6		D941
	Dielectric strength volts/mil	>300		D877
	Residue, microgram/gram	<50		D2109
	Appearance	Clear, colorless liquid		Not applicable

1/ The perfluorocarbon used shall have a viscosity less than or equal to the thermal shock equipment manufacturer's recommended viscosity at the minimum temperature.

TABLE 1056.II. Thermal shock temperature tolerances and suggested fluids. 1/

Test condition		A and B	C	D
		Temperature	Temperature	Temperature
Step 1	Temperature tolerance, °C	100 +10 -2	125 +10 -0	150 +10 -0
	Recommended fluid	Water 2/ or perfluorocarbon 3/	Perfluorocarbon 3/	Perfluorocarbon 3/
Step 2	Temperature tolerance, °C	-0 +2 -10	-55 +0 -10	-65 +0 -10
	Recommended fluid	Water 2/ or perfluorocarbon 3/	Perfluorocarbon 3/	Perfluorocarbon 3/

1/ Ethylene glycol shall not be used as a thermal shock test fluid.
2/ Water is indicated as an acceptable fluid for this temperature range. Its suitability chemically shall be established prior to use. When water is used as the fluid for condition A and the specified temperature tolerances are insufficient due to altitude considerations, the following alternate test conditions may be used.
a. Temperature: +100°C -6°C, 0°C +6°C.
b. Cycles shall be increased to 20.
3/ Perfluorocarbons contain no chlorine or hydrogen.

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METHOD 1057.1

RESISTANCE TO GLASS CRACKING

1. Purpose. This method provides a means of judging the relative resistance of glass encapsulated electronic components to cracking under conditions of thermal stress. It employs immersion in a hot liquid and then water to simulate the thermal stresses associated with both device manufacturing processes and end user assembly procedures.

2. Apparatus. Liquid baths shall be used which are capable of providing and maintaining the specified temperatures in the working zone when loaded with a maximum load. Bath temperatures under maximum load conditions shall be verified, as needed, to validate bath performance. Liquid composition shall be as specified herein.

3. Procedure. Remove any paint or other surface coatings. Clean test specimens using a general purpose cleaner/degreaser, rinse in water, and then acetone. Subsequent to cleaning, specimens shall be placed into the baths defined in table 1057.I for the applicable test condition using a dipping tool that will not significantly heat sink the body of the device under test (DUT). Specimens shall be fully immersed in the first bath for the specified period of time then transferred to, and fully immersed in, the second bath. Unless otherwise specified, the test shall be considered complete upon removal of the specimen from the second bath.

3.1 Timing. Specimens shall be immersed into, and removed from, the first (hot) bath at a rate of 1.0 ±.5 inch (25.4 ±12.7 mm) per second. The maximum preheat dwell time above the hot bath prior to immersion shall be in accordance with table 1057.1. Immersion dwell time in the hot bath shall be in accordance with table 1057.1. Specimens shall be released completely into the cold bath after their removal from the hot bath in accordance with the dwell time specified in table 1057.1.

4. Failure criteria. Specimens that fail to meet the glass crack criteria of method 2074 of MIL-STD-750 shall be considered rejects. If flux was used for condition B, it shall be removed prior to any visual examination.

5. Summary. The following shall be specified in the applicable performance specification.

a. Sample size and acceptance number.

b. Test condition.

c. Special fixturing as applicable.

d. Number of test cycles if other than one cycle.

TABLE 1057.I. Conditions and temperatures.

Step		Test condition and temperatures	
		Condition A	Condition B
0	Pre-immersion conditions or preparations.	Samples at room temperature	Flux dip in accordance with TM2026 is recommended 1/
1	Recommended hot bath fluid Temperature and tolerance Maximum preheat dwell above hot bath Immersion dwell time in hot bath	Water 100°C ±5°C 7.0 seconds 6 ±1.0 seconds	Molten Solder 235°C ±5°C 7.0 seconds 6 ±1.0 seconds
2	Recommended cold bath fluid Temperature and tolerance Dwell time between hot and cold bath Immersion dwell time in cold bath	Water 0°C ±5°C 3.0 seconds max 5.0 seconds min	Water 25°C ±5°C 10 to 15 seconds 5.0 seconds min

1/ Use of flux is optional but recommended to prevent solder irregularities and “blobs”.

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METHOD 1061.1

TEMPERATURE MEASUREMENT, CASE AND STUD

1. Purpose. This proposal covers a method of measuring case temperature of hex-base devices.

2. Test equipment.

2.1 Type of thermocouple. The thermocouple material shall be copper-constantan, as recommended by the "Standard Handbook for Electrical Engineers", for the range of -190°C to +350°C. The wire size shall be no larger than AWG size 30. The junction of the thermocouple shall be welded together to form a bead rather than soldered or twisted.

2.2 Accuracy. The thermocouple shall have an accuracy of ±.5°C. Under load conditions, slight variations in the temperature of different points on the case may reduce this accuracy to ±1.0°C for convection cooling, and ±2.0°C for forced air ventilation.

3. Procedure.

3.1 Method of mounting. A small hole, just large enough to insert the thermocouple, shall be drilled approximately .031 inch (0.79 mm) deep into the flat of the case hex at a point chosen by the manufacturer. The edge of the hole should then be peened with a small center punch to force a rigid mechanical contact with the welded bead of the thermocouple. If forced air ventilation is used, the thermocouple shall be mounted away from the air stream and the thermocouple leads close to the junction shall be shielded.

3.2 Other methods of mounting. Other methods of mounting thermocouple, with the possible exception of the thermocouple welded directly to the case, will result in temperature readings lower than the actual temperature. These deviations will result from:

a. Inadequate contact with the case using cemented thermocouples.

b. External heat sink in contact with the thermocouple using pressure contacts.

4. Summary. The following conditions shall be specified in the performance specification:

a. Method of mounting (see 3.).

b. Test equipment, if required.

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METHOD 1066.1

DEW POINT

1. Purpose. The purpose of this test is to monitor the device parameter for a discontinuity under the specified conditions.

2. Apparatus. The apparatus used in this test shall be capable of varying the temperature from the specified high temperature to -65°C and return to the specified high temperature while the parameter is being measured.

3. Procedure. The voltage and current specified in the performance specification shall be applied to the terminals and the parameter monitored from the specified high temperature to -65°C and return to the specified high temperature. The dew point temperature is indicated by a sharp discontinuity in the parameter being measured with respect to temperature. If no discontinuity is observed, it shall be assumed that the dew point is at a temperature lower than -65°C and the DUT is acceptable.

4. Summary. The following conditions shall be specified in the detail specification:

   a. Test temperature (high) (see 2.).

   b. Test voltage and current (see 3.).

   c. Test parameter (see 3.).

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METHOD 1071.8

HERMETIC SEAL

1. Purpose. The purpose of this test is to determine the hermeticity of semiconductor devices with designed internal cavities.

2. Terms and definitions.

2.1 Standard leak rate. Standard leak rate is defined as that quantity of dry air at +25°C in atmospheric cubic centimeters flowing through a leak, or multiple leak, paths per second when the high-pressure side is at 15 psi (101 kPa) and the low-pressure side is at a pressure of not greater than .0193 psi (133 pA). Standard leak rate shall be expressed in units of atmospheric cubic centimeters per second (atm cm^3/s air).

2.2 Measured leak rate. Measured leak rate (R_1) is defined as the leak rate of a given package as measured under specified conditions and employing a specified test medium. Measured leak rate shall be expressed in units of atmospheric cubic centimeters per second (atm cm^3/s of the gas medium used for the test). For purposes of comparison with rates determined by other methods of testing, the measured leak rates must be converted to the equivalent standard leak rates, (converted to air equivalents).

2.3 Equivalent standard leak rate. The equivalent standard leak rate (L) of a given package, with a measured leak rate (R_1), is defined as the leak rate of the same package with the same leak geometry that would exist under the standard leak rate. The equivalent standard leak rate shall be expressed in units of atmospheric cubic centimeters per second (atm cm^3/s) (air).

NOTE: The leak rate measurements are not necessarily performed with a one atmosphere differential, as implied by the standard leak rate. The equivalent conversion represents gas medium only.

3. Test conditions.

a. Gross leaks. Test conditions A, B, C, D, E, G_2, J, K, or L should be specified for gross leaks.

(1) Test condition A: Radioisotope wet gross leak test (see 4.).

(2) Test condition B: Radioisotope dry gross leak test (see 5.).

(3) Test condition C: Liquid (fluorocarbon) gross leak (see 6.).

(4) Test condition D: Bubble test (see 3.b).

(5) Test condition E: Penetrant dye gross leak (see 8.).

(6) Test condition J: Weight gain gross leak (see 11.).

(7) Test condition K: Fluorocarbon vapor detection gross leak (see 12.).

(8) Test condition L_1: Optical gross leak (see 13.).

(9) Test condition G2: Radioisotope gross/fine combination (see 9.6)

(10) Test condition CH1 and CH2: Cumulative helium gross/fine combination (see 10.).

b. Gross leaks. Test condition D may be specified when a sensitivity of 1 x 10^{-3} atm cm^3/s or greater will satisfy reliability requirements. This condition shall not be used for devices that have internal free volumes of less than 1 cm^3.

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c. Fine leak. Test condition G_1, G_2, H, CH, or L should be specified for the fine leak test.

(1) Test condition G_1, radioisotope fine or G_2, gross/fine combination leak test (see 9.).

(2) Test conditions H_1 and H_2: Tracer gas leak test (helium) (see 10.).

(3) Test condition CH1 and CH2: Cumulative helium gross/fine combination (see 10.).

d. Obsolete.

e. Fine and gross leak test procedure. Unless otherwise specified by applicable performance specification, tests shall be conducted in accordance with table 1071-I. When specified (see 15 herein) measurements after test shall be conducted following the leak test procedures. Where bomb pressure specified exceeds the device package capability, alternate pressure, exposure time, and dwell time conditions shall be used provided they satisfy the leak rate, pressure, and time relationships which apply and provided no less than 30 psi (207 kPa) bomb pressure is applied in any case, or for condition L_1, a minimum 10 psi differential test pressure is applied.

Fine and gross leak tests shall be conducted in accordance with the requirements and procedures of the specified test condition. Testing order shall utilize only the all-dry gas tests first, followed by any liquid immersion gross leak test (i.e.; the option to use the radioisotope gross, fine, or gross/fine combination leak test conditions B, G_1, and G_2 (respectively), may be used together, or in succession, as long as the minimum test requirements are met). The radioisotope dry gas gross leak test B or G_2 may be used for gross leak testing prior to any dry gas fine test. Optical gross leak test (L_1) is an all-dry gas test and can be used before any fine leak test. If any other gross leak test is used, (condition A, C, D, E, F, J, or K), the sequence of testing shall use the dry gas fine leak test first, followed by the gross leak test, except in accordance with 14, note 1. When batch testing (more than one device in the leak detector at one time) is used in performing test condition H_1, H_2, CH, and a reject condition occurs, it shall be noted as a batch failure. Each device with a cavity greater than 0.5 cm3 may then be tested individually one time for acceptance if all devices in the batch are retested within 1 hour after removal from the tracer gas pressurization chamber. Devices with cavity < 0.5 cm3 shall be measured within ten minutes or re-pressurized and then re-read. For condition G_1 only, devices may be batch tested for acceptance provided, if a reject occurs, all remeasuring of parts individually is completed within 30 minutes after removal from the tracer gas pressurization chamber. For condition G_2 only, devices may be batch tested for acceptance provided, if a reject occurs, all remeasuring of parts individually is completed within 10 minutes after removal from the tracer gas pressurization chamber. For condition K only, devices that are batch tested, and indicate a reject condition, may be retested individually one time using the procedure of 12.2 herein, except that repressurization is not required if the devices are immersed in detector fluid within 20 seconds after completion of the first test, and they remain in the bath until retest. For condition CH only, devices that are batch tested, and indicate a reject condition, may be retested individually if they are placed in a bag or container with at least 50 percent helium at atmospheric pressure and then individually removed and tested within 1 hour after removal from the initial helium pressurization chamber.

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TABLE 1071-I. Required test sequence.

Volume (cm^3)	Fine leak condition	Gross leak condition
≤0.4	G_1, G_2 H_1, H_2, CH, L_2	CH,A, B, C, E, G_2 J 1/, K ,L_1
>0.4	G_1, G_2, H_1, H_2, CH, L_2	CH,A, B, C, D 2/, E, K, L_1
>0.4	CH, J 3/	CH,J 3/

1/ Condition J cannot be used for packages whose internal volume is <0.001 cm^3.
2/ Condition D cannot be used for packages whose internal volume is ≤ 1 cm^3.
3/ Condition J may be used as a single test for devices with an internal cavity volume of >0.4 cm^3 provided the specified requirements can be satisfied by a leak rate of 1 x 10^{-6} atm cm^3/s.
4/ Condition B and G_2 may be used for small cavity devices that contain approved getting material.

4. Test condition A, radioisotope wet gross leak test.

4.1 Apparatus. The apparatus required for the seal test shall be as follows:

a. Radioactive tracer gas pressurization console.

b. Counting station equipment consisting of a scintillation crystal, photomultiplier tube, preamplifier, ratemeter, and krypton-85 reference standards. The counting station shall be of sufficient sensitivity to determine through the device wall, the radiation level of any krypton-85 tracer gas present within the device. The counting station detector shall have a minimum detectability of 500 c/m of krypton-85 above ambient background, and shall be calibrated at least once every working shift using krypton-85 reference standards and following the equipment manufacturer's instruction.

c. A container of sufficient volume to allow the devices to be covered with oil and to be degreased with a suitable solvent.

d. Solutions:

(1) Hydrocarbon vacuum pump oil. The solution shall be kept clean and free of contaminants.

(2) Solvent capable of degreasing the devices.

e. A tracer gas consisting of a mixture of krypton-85 and air. The concentration of krypton-85 in air shall be no less than 100 microcuries per atmospheric cubic centimeter. This value shall be determined at least once each 30 days, following manufacturer's procedure, and recorded in accordance with the calibration requirements of this standard.

4.2 Procedure. The devices shall be immersed in the oil and evacuated to a pressure of 10 torr or less for 10 minutes and then pressurized with air for 1 hour at 310 kPa (45 psi) minimum. The devices shall be removed from the oil and flushed with solvent to remove all of the surface oil. The devices shall then be placed in the radioisotope pressurization tank, and the tank evacuated to a pressure of 0.5 torr. The devices shall then be pressurized to a minimum of three atmospheres absolute pressure of krypton-85/*air* mixture for twelve (12) minutes minimum. The gas mixture shall then be transferred to storage until a pressure of 2.0 torr maximum exists in the tank. This transfer shall be completed in 2 minutes maximum. The tank shall then be filled with air, and the devices immediately removed from the tank and leak tested within 10 minutes after gas exposure, with a scintillation crystal equipped counting station. Any device indicating 1,000 c/m or greater above the ambient background of the counting station shall be considered a gross leak.

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5. Test condition B, radioisotope dry gross leak. This test shall be used to test devices that internally contain some krypton-85 absorbing or adsorbing medium, such as electrical insulation, organic, or molecular sieve, or approved gettering material. If the device does not contain any adsorbing medium this can only be used on parts with 0.02 cc internal free volume or larger, or that can demonstrate that the following requirements are met:

a. A 5 mil diameter hole shall be made in a representative unit of the devices to be tested.

b. The device shall be subjected to this test condition and removed from the pressurization tank immediately after the tank is vented to atmosphere, and measured in the counting station. A net reading indicating 1,000 cpm or greater is considered a reject. The device must remain a reject for a minimum of 10 minutes after removal from the pressurization tank. If the device does not fail, this test may not be used.

5.1 Apparatus. Apparatus for this test shall consist of the following:

a. Radioactive tracer gas pressurization console containing krypton-85/air mixture.

b. Counting station with a minimum sensitivity of 10,000, counts per minute per microcurie of krypton-85 tracer gas and a minimum detectable count rate of 500 counts per minute above background level.

c. A tracer gas consisting of a mixture of krypton-85 and air. The concentration of krypton-85 in air shall be no less than 100 microcuries per atmospheric cubic centimeter. This value shall be determined at least once each 30 days, following manufacturer's procedure, and recorded in accordance with the calibration requirements of this standard.

5.2 Procedure. The devices shall be placed in a radioactive tracer gas pressurization tank and the tank shall be evacuated to a pressure not to exceed 0.5 torr. The devices shall then be subjected to a minimum of 45 psia of krypton-85/air gas mixture for 2 minutes. The gas mixture shall then be transferred to storage until a pressure of 2.0 torr maximum exists in the pressurization tank. This gas transfer shall be complete in 3 minutes maximum. The tank shall then be backfilled with air. The devices shall then be removed from the tank and measured within 10 minutes after gas exposure, with a scintillation-crystal-equipped counting station. Any device indicating 1,000 counts per minute, or greater, above the ambient background of the counting station shall be considered a gross leak failure.

6. Test condition C, liquid (fluorocarbon) gross leak. Packages with less than 0.01 cm3 internal free volume shall be tested with extremely careful observation. The number of test samples, configuration, and all critical test criteria shall be included in the manufacturer’s test procedure.

6.1 Apparatus. Apparatus for this test shall consist of the following:

a. A vacuum/pressure chamber for the evacuation and subsequent pressure bombing of devices up to 90 psi (618 kPa) for a maximum of 24 hours.

b. A suitable observation container with provisions to maintain the indicator fluid at a temperature of +125°C ±5°C (+100°C for Germanium transistors with temperature rating of +100°C maximum) and a filtration system capable of removing particles greater than one micrometer in size from the fluid.

c. A magnifier capable of magnifying an object 1.5 to 30 times its normal size (4 to 120 diopters) for observation of bubbles emanating from devices when immersed in the indicator fluid.

d. Sources of type I detector fluids and type II indicator fluids as specified in table 1071-II.

e. A lighting source capable of producing a collimated beam of at least 161,000 luxes (15,000 foot candles) in air at a distance equal to that which the most distant device in the bath will be from the source. The lighting source shall not require calibration, but shall be placed for best detection of bubbles, without excessive incident or reflective glare being directed toward observer.

f. Suitable calibrated instruments to indicate that test temperatures, pressures, and times are as specified.

g. Suitable fixtures to hold the device(s) in the indicator fluid.

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TABLE 1071-II. Physical property requirements of perfluorocarbon fluids. 1/

Property	Type I	Type II	Type III	ASTM test method
Boiling point (°C)	50-95	140-200	50-110	D-1120
Surface tension (dyness/cm) at +25°C		< 20		D-971, D-1331
Density at +25°C (gm/ml)	> 1.6	> 1.6	> 1.6	D-941
Density at +125°C (gm/ml)		> 1.5		D-941
Dielectric strength (volts/mil)	> 300	> 300	> 300	877
Residue (Tgm/gm)	< 50	< 50	< 50	D-2109
Appearance	Clear colorless			N/A

1/ Perfluorocarbons contain no chlorine or hydrogen.

6.2 Procedure. The devices shall be placed in a vacuum/pressure chamber and the pressure reduced to 0.0972 psia(670 Pa) or less and maintained for 30 minutes minimum, except for devices with an internal volume ≥ 0.1 cm^3 this vacuum cycle may be omitted. A sufficient amount of type I detector fluid shall be admitted to cover the devices. When the vacuum cycle is performed, the fluid will be admitted after the minimum 30 minute period but before breaking the vacuum. The devices shall then be pressurized in accordance with table 1071-III. When the pressurization period is complete, the pressure shall be released and the devices removed from the chamber without being removed from a bath of detector fluid for greater than 20 seconds. A holding bath may be another vessel or storage tank. When the devices are removed from the bath, they shall be dried for 2 minutes ±1 minute in air prior to immersion in type II indicator fluid, which shall be maintained at +125°C ±5°C. The devices shall be immersed with the uppermost portion at a minimum depth of 2 inches (50.80 mm) below the surface of the indicator fluid, one at a time or in such a configuration that a single bubble from a single device out of a group under observation may be clearly observed as to its occurrence and source. Unless rejected earlier, the device shall be observed against a dull, nonreflective black background through the magnifier, while illuminated by the lighting source, from the instant of immersion until expiration of a 30 second minimum observation period.

TABLE 1071-III. Condition C and K pressurization conditions.

Pressure psia (minimum)	Minimum pressurization time (hour)	
	Condition C	Condition K
30	23.5	12
45	8	4
60	4	2
75	2	1
90	1	0.5
105	0.5	N/A

6.2.1 Failure criteria. A definite stream of bubbles, or two or more bubbles originating from the same point, shall be cause for rejection.

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6.2.2 Precautions. The following precautions shall be observed in conducting the fluorocarbon gross leak test:

a. Perfluorocarbons fluids shall be filtered through a filter system capable of removing particles greater than one micrometer prior to use. Bulk filtering and storage is permissible. Liquid which has accumulated observable quantities of particulate matter during use shall be discarded or reclaimed by filtration for re-use. Precaution should be taken to prevent contamination.

b. Observation container shall be filled to assure coverage of the device to a minimum of 2 inches (50.80 mm).

c. Devices to be tested shall be free of foreign materials on the surface, including conformal coatings, and any markings which may contribute to erroneous test results.

d. Precaution should be taken to prevent operator injury due to package rupture or violent evolution of bomb fluid when testing large packages.

e. Packages with less than 0.01 cm3 internal free volume shall be tested, with extremely careful observation.

7. Test condition D, bubble test (type II indicator fluid as specified in table 1071-II.) (NOTE: These fluids replace ethylene glycol as a medium for the gross leak bubble test.) Packages with less than 0.01 cm3 internal free volume shall be tested with extremely careful observation.

7.1 Apparatus. Apparatus for this test shall consist of the following:

a. A device internal free volume of greater than 1 cm^3.

b. Container of sufficient volume to allow the devices to be covered with solution to a minimum depth of 2 inches (50.80 mm). The container shall have flat sides to minimize reflections and distortions (example of an acceptable container is a battery jar).

c. Liquid of sufficient volume maintained at no less than +125°C ±5°C for the duration of the test.

d. A light source capable of producing a collimated beam of at least 161,000 luxes (15,000 foot candles) in air at a distance equal to that which the most distant device in the bath will be from the source. The lighting source shall not require calibration.

7.2 Procedure. The devices shall be placed in the container of liquid at +125°C, immersed to a minimum depth of 2 inches (50.80 mm) for a minimum of 1 minute, and observed during the entire immersion period for bubbles or bubbling. Side lighting (see 7.1.d) shall be used to facilitate viewing the bubbles, and the devices shall be observed against a black nonreflective background.

7.2.1 Failure criteria. Any device that shows one or more nonreflective attached growing bubbles, one continuous stream, or a succession of two or more from the same point shall be considered a failure.

8. Test condition E, penetrant dye gross leak.

8.1 Apparatus. Apparatus for this test shall consist of the following:

a. Ultraviolet light source with peak radiation at approximately the frequency causing maximum reflection of the dye (3650Å for Zyglo; 4935Å for Flurosecein; 5560 Å for Rhodamine B).

b. Pressure chamber capable of maintaining 104 psi (719 kPa).

c. Solution of fluorescent dye, (such as Rhodamine B, Fluorescein, Dye-check, Zyglo, FL-50 or equivalent), mixed in accordance with the manufacturer's specification.

d. A magnifier capable of magnifying an object 1.5 to 30 times its nominal size (4 to 120 diopters).

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8.2 Procedure. This test shall be permitted only on transparent glass encased devices or for destructive verification of opaque devices. The pressure chamber shall be filled with the dye solution to a depth sufficient to completely cover all the devices. The devices shall be placed in the solution and the chamber pressurized at 104 psia (719 kPa) minimum for 3 hour minimum. For device packages which will not withstand 105 psia (724 kPa), 60 psia (414 kPa) minimum for 10 hours may be used. The devices shall then be removed and carefully washed, using a suitable solvent for the dye used, followed by an air jet dry. Transparent devices may be examined under magnification capable of magnifying an object up to 1.5 times its normal size (4 diopters) using ultraviolet light source of appropriate frequency for evidence of the dye penetration. For the destructive examination of opaque devices, the devices shall be delidded and examined internally under the magnifier using an ultraviolet light source of appropriate frequency.

8.2.1 Failure criteria. Any evidence of dye in the cavity of the device shall constitute a failure.

8.2.1.1 Opaque devices. After de-lidding or separation of the device (as applicable), any evidence of dye penetration shall be cause for rejection. Area of examination shall be as shown on figures 1071-1 and 1071-2.

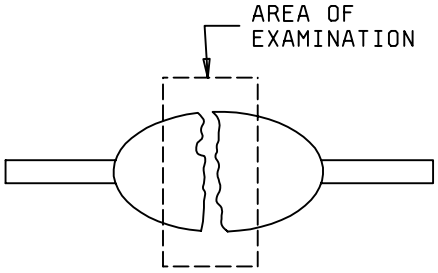

FIGURE 1071-1. Opaque construction.

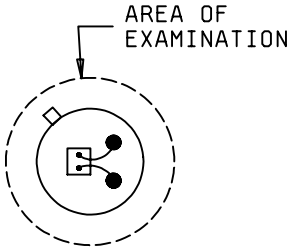

FIGURE 1071-2. Metal can construction.

8.2.1.2 Transparent glass, with large cavity (i.e. S-Bend, C-Bend, or straight-through constructions). Any evidence of dye penetration in the device cavity shall be cause for rejection. Area of examination shall be as shown on figure 1071-3.

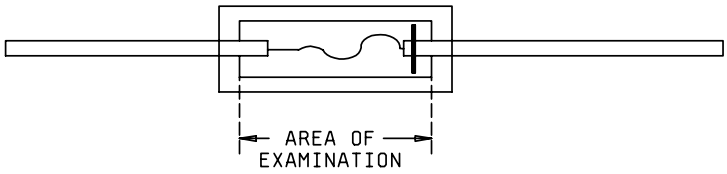

FIGURE 1071-3. Transparent glass or straight through construction.

8.2.1.3 Transparent glass, double plug construction (-1 and tungsten). Any evidence of dye penetration in the die area shall be cause for rejection. In addition, evidence of dye penetration into a crack, fracture, void, which is closer to the die than 50 percent of the designed seal length shall be rejected. Area of examination shall be as shown on figure 1071-4.

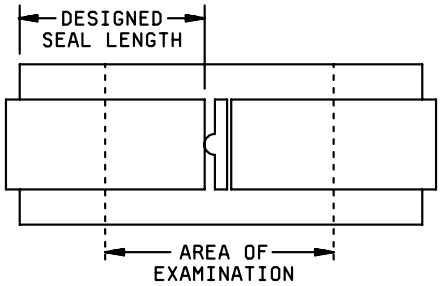

FIGURE 1071-4. Transparent glass double plug construction.

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9. Test condition G_1. Radioisotope fine leak.

9.1 Apparatus. Apparatus for this test shall be as in 5.1.

9.2 Testing parameters. The bombing pressure and soak time shall be determined in accordance with the following equation:

Equation (1): $$Q_S = \frac{R}{SKT\overline{P}t}$$

The parameters of equation (1) are defined as follows:

Q_S = The maximum leak rate allowable, in atm cc/s Kr, for the devices to be tested.

R = Counts per minute above the ambient background after pressurization if the device leak rate were exactly equal to Q_S. This is the reject count above the background of both the counting equipment and the component, if it has been through prior radioactive leak tests.

S = The specific activity, in microcuries per atmospheric cubic centimeter, of the krypton-85 tracer gas in the pressurization system.

K = The overall counting efficiency of the scintillation crystal in counts per minute per microcurie of krypton-85 in the internal void of the specific component being evaluated. This factor depends upon component configuration and dimensions of the scintillation crystal. The counting efficiency shall be determined in accordance with 9.3.

T = Soak time, in hours, that the devices are to be pressurized.

P = $P_e2 - P_i2$, where P_e is the pressure in atmospheres absolute, and P_i is the original internal pressure of the devices in atmospheres absolute. The bombing pressure (P_e) may be established by specification or, if a convenient soak time (T) has been established, the pressure (P_e) can be adjusted to satisfy equation (1).

t = Conversion of hours to seconds and is equal to 3,600 seconds per hour.

NOTE: The complete version of equation (1) contains a factor $(P_O{}^2 - (\Delta P)^2)$ in the numerator which is a correction factor for elevation above sea level. P_O is sea level pressure in atmospheres absolute and ΔP is the difference in pressure, in atmospheres between the actual pressure at the test station and sea level pressure. For the purpose of this test method, this factor has been dropped.

9.3 Determination of counting efficiency (K). The counting efficiency (K) of equation (1) shall be determined as follows:

a. A representative unit of the device type being tested shall have a known microcurie content of krypton-85 placed in the internal void of the device.

b. The counts per minute from the representative unit shall be measured in the shielded scintillation crystal of the counting station in exactly the same position as the actual samples will be measured. From this value, the counting efficiency, in counts per minute per microcurie, shall be calculated.

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9.4 Evaluation of surface sorption. All device encapsulations consisting of glass, metal, substrate and chip coatings, and ceramic or combinations thereof, that also include external coatings and external sealants or labels, shall be evaluated for surface sorption of krypton-85 before establishing the leak test parameters. Representative samples with the questionable surface material shall be subjected to the predetermined pressure and time conditions established for the device configuration as specified by 9.2. The samples shall then be measured at the counting station every 10 minutes, with count rates noted, until the count rate becomes asymptotic with time. (This is the point in time at which surface sorption is no longer a problem.) This time lapse shall be noted and shall determine the "wait time" specified in 9.5.

9.5 Procedure. The devices shall be placed in the radioactive tracer gas pressurization tank. The tank may be partially filled with inert material (aluminum filler blocks), to reduce machine cycle time and increase the efficiency of the system. The tank shall be evacuated to 0.5 torr. The devices shall be subjected to a minimum of 45 psi absolute pressure of krypton-85/nitrogen mixture for a minimum of 12 minutes. Actual pressure and soak time shall be determined in accordance with 9.2. The R value in counts per minute shall not be less than 500 above background. The krypton-85/nitrogen gas mixture shall be transferred to storage until 0.5 torr pressure exists in the pressurization tank. The storage cycle shall be completed in 3 minutes maximum as measured from the end of the bombing cycle or from the time the tank pressure reaches 60 psia (414 kPa) if a higher bombing pressure is used. The tank shall then immediately be backfilled with air. The devices shall then be removed from the tank and measured within one-half hour after gas exposure with a scintillation-crystal-equipped counting station. Device encapsulations that come under the requirements of 9.4 shall be exposed to ambient air for a time not less than the "wait time" determined by 9.4. In no case will the time between removal from the pressurization chamber and test exceed 1 hour. This air exposure shall be performed after gas exposure but before determining leak rate with the counting station. Device encapsulations that do not come under the requirements of 9.4 may be tested without a "wait time". (The number of devices removed from pressurization for measurement shall be limited such that the test of the last device can be completed within one half hour.)

The actual leak rate of the component shall be calculated with the following equation:

Equation (2):

$$Q = \frac{(Actual\ readout\ in\ net\ counts\ per\ minute) \times Q_S}{R}$$

Where Q = actual leak rate in atm cc/s, and Q_S and R are defined in 9.2.

9.5.1 Failure criteria. Unless otherwise specified, devices that exhibit a leak rate equal to or greater than the test limits of table 1071-IV shall be considered as failures.

TABLE 1071-IV. Test limits for radioisotope fine leak method.

Volume of package (cc)	Q_S
<0.05	5×10^{-9}
>0.05 < 0.5	1×10^{-8}
>0.5 <10.0	5×10^{-8}
> 10.0 < 20.0	5×10^{-8}

9.6 Test condition G_1/G_2 radioisotope gross/fine combination:

9.6.1 Apparatus: Apparatus for this test shall be as in 5.1.

9.6.2 Testing parameters. The bombing pressure and soak time shall be as in 9.2.

9.6.3 Determination of counting efficiency (K), shall be as in 9.3.

9.6.4 Evaluation of surface sorption shall be as in 9.4.

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9.6.5 Procedure G_1/G_2 combination gross/fine test. The devices shall be placed in a radioactive gas pressurization chamber. The pressurization chamber must be filled with inert material (aluminum filler blocks), to reduce cycle time and make the test more efficient. The chamber shall be evacuated to 0.5 torr. The devices shall be subjected to a minimum of 45 psia of krypton-85/air mixture for a minimum of 12 minutes. Actual pressure and soak time for G1 shall be in accordance with 9.5. The R value in counts per minute shall not be less than 500 c/m above background. When the soak time is completed the krypton-85/air mixture shall be transferred to storage until 2.0 torr pressure exists in the pressurization chamber. The storage cycle shall be completed in 3 minutes as measured from the end of the pressurization cycle or from the time the tank pressure reaches 60 psia, (if a higher pressure was used). The tank shall then be backfilled with air. The devices shall immediately be removed from the tank and measured at the counting station within 10 minutes after removal from the tank. Devices that come under the conditions of 9.6.4 and require a “wait time”, cannot be subjected to the gross/fine combination test. Those devices must be subjected to G_1 and G_2 separately.

10. Test condition H_1 or H_2 tracer gas (H_e) fine leak and CH1 or CH2 combined fine/gross leak. Test condition H_1 is a "fixed" method with specified conditions in accordance with table 1071-V that will ensure the test sensitivity necessary to detect the required measured leak rate (R_1). Test condition H_2 is a "flexible" method that allows the variance of test conditions in accordance with the formula of 10.2.1.2 to detect the specified equivalent standard leak rate (L) at a predetermined leak rate (R_1). Test conditions CH1 and CH2 expand the range of H1 and H2 to include the gross leak range and require the same test conditions using specialized apparatus.

10.1 Apparatus. Apparatus required for test conditions H_1, H_2, CH1, and CH2 shall consist of suitable pressure and vacuum chambers and a mass spectrometer-type leak detector properly calibrated for a helium leak rate sensitivity sufficient to read measured helium leak rates of 1×10^{-9} atm cm^3/s and greater. The volume of the chamber used for leak rate measurement should be held to the minimum practical, since this chamber volume has an adverse effect on sensitivity limits. The leak detector indicator shall be calibrated using a diffusion-type calibrated standard leak at least once every working shift. In addition, the test apparatus for CH1 and CH2 shall utilize a specialized pumping system which enables the volume of helium released to be measured as well as the rate of change or “slope” of the helium such that the leak rate is determined from the slope measurement for fine leaks and the volume for gross leaks.

10.2 Procedure applicable to "fixed" and "flexible" methods. The completed devices(s) shall be placed in a sealed chamber which is then pressurized with a tracer gas of 100 +0, -5 percent helium for the required time and pressure. The pressure shall then be relieved (an optional air nitrogen wash may be applied except for CH1 and CH2) and each specimen transferred to another chamber, or chambers, which are connected to the evacuating system and a mass-spectrometer-type leak detector. When the chamber(s) is evacuated, any tracer gas which was previously forced into the specimen will thus be drawn out and indicated by the leak detector as a measured leak rate (R_1). (The number of devices removed from pressurization for leak testing shall be limited such that the test of the last device can be completed within 60 minutes for test condition H_1 or CH1 or within the chosen value of dwell time t_2 for test condition H_2 or CH2).

10.2.1 Evaluation of surface sorption. All device encapsulations consisting of glass, metal, and ceramic, or combinations thereof, including coatings and external sealants, shall be evaluated for surface sorption of helium before establishing the leak test parameters. Representative specimens of the questionable devices should be opened and all parts of each device as a unit shall be subjected to the predetermined pressure and time conditions established for the device configuration as specified in table 1071-V and 10.2.1.2. The measured leak rate for each device shall be monitored and the lapsed time shall be determined for the indicated leak rate to fall to $\leq 0.5\ R_1$ as specified in table 1071-V for test condition H_1 or as predetermined for test condition H_2. The average of the lapsed time following the release of pressure will determine the minimum usable dwell time. Note that the sensitivity of measurement increases as this background indicated leak rate decreases relative to the R_1 reject level. Alternately, whole (unopened) specimens of the questionable devices shall be subjected to the same process; then, the shorted value of lapsed time so obtained will determine the minimum dwell time. The fixed method will not be used if the consequent dwell time exceeds the value specified in table 1071-V. It is noted that sorption may vary with pressure and time of exposure so that some trial may be required before satisfactory exposure values are obtained. The test conditions CH1 and CH2 require the same dwell times be established before the slope is determined and, in addition, a volume determination must be made to eliminate the potential for a false gross leak.

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10.2.1.1 Test condition H_1 and CH1 fixed method. The device(s) shall be tested using the appropriate conditions specified in table 1071-V for the internal cavity volumes of the package under test. The t_1 is the time under pressure and time t_2 is the maximum time allowed after the release of pressure before the device shall be read. The fixed method shall not be used if the maximum standard leak rate limit given in the performance specification is less than the limits specified herein for the flexible method.

TABLE 1071-V. Fixed conditions for test condition H_1.

Volume of package (cm^3)	Bomb condition			R_1 reject limit (atm cm^3/s)
	kPa ±15 (psia) ±2	Minimum Exposure time in hours (t_1) (+1.0 - 0.0)	Maximum dwell time (hour)	
< 0.01	517 (75)	2	1	5×10^{-9}
> 0.01 ≤ 0.05	517 (75)	3	1	1×10^{-8}
> 0.05 ≤ 0.5	517 (75)	4	1	1×10^{-8}
> 0.5 ≤ 1.0	517 (75)	2	1	1×10^{-8}
> 1.0 ≤ 10.0	413 (60)	5	1	5×10^{-8}
> 10.0 ≤ 20.0	310 (45)	10	1	5×10^{-8}

10.2.1.2 Test condition H_2 and CH2 flexible method. Values for bomb pressure, exposure time, and dwell time shall be chosen such that actual measured tracer gas leak rate (R_1) readings obtained for the DUTs (if defective) will be greater than the minimum detectable leak rate capability of a mass spectrometer. The devices shall be subjected to a minimum of 29 psi (203 kPa) of helium atmosphere. The chosen values of pressurization and time of pressurization, in conjunction with the value of the internal volume of the device package to be tested, and the maximum equivalent standard leak rate (L) limit as specified in 10.2.2, shall be used to calculate the measured leak rate (R_1) limit using the following formula:

Equation (3):

$$R_1 \frac{2.69\,L\,P_e}{P_o}\left[1 - \exp - \left(\frac{2.69\,L}{P_o V} \bullet t_1\right)\right] \exp - \left(\frac{2.69\,L}{P_o V} \bullet t_2\right)$$

Where: R_1 = The resultant measured leak rate of tracer gas (H_e) through the leak in atm cm^3/s.
L = The equivalent standard leak rate in atm cm^3/s.
P_e = The pressure of exposure in atmospheres absolute.
P_o = 1 standard atmosphere.
t_1 = The time of exposure to P_e in seconds.
t_2 = The dwell time between release of pressure and leak detection in seconds.
V = The internal volume of the device package cavity in cubic centimeters.

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The minimum detectable leak rate shall be determined as in 10.2.1 and shall be taken as the indicated value corresponding to a lapsed time $t_0 < t_2$. The lapsed time t_0 shall be taken as the minimum usable dwell time, and leak testing shall be accomplished in the interval between t_0 and t_2. Alternately, pressurization parameters may be chosen from the fine leak approximate solution of equation (3) for $L < 1 \times 10^{-5}$ as:

Equation (4):

$$L = \frac{P_o}{2.69}\left(\frac{R_1 V}{P_e t_1}\right)^{1/2}$$

with a graphical representation given on figure 1071-5. If chosen dwell time t_2 is greater than 60 minutes, equation (2) shall be used to determine an R_1 value which will assure a maximum detectable standard leak rate large enough to overlap with the selected gross leak test condition. Alternately, the largest detectable leak rate (L) as a function of dwell time may be obtained from the approximate solution:

Equation (5):

$$L\max = \frac{P_o V}{2.69\, t_2}\; 1n\left(\frac{2.69\, L\, P_e}{P_o\, R_1}\right)$$

with graphical representation given on figure 1071-6. In each case (equations (4) and (5)) R_1 shall be taken large compared to the minimum detectable value. 1/

10.2.1.3 Package volume and leak rate limits for CH1 and CH2. For test methods CH1, the minimum size package is determined by the ability of the apparatus to effectively detect a gross leak one hour after the device has been removed from the trace gas pressurization chamber with a signal to noise (background) ratio of at least five to one. It may be necessary to use a shorter test interval if the apparatus has a high background level of helium or the surface absorption of the device is high. A reasonable lower limit would be 0.0005 scc. The only limit on maximum size is the size of the test chamber to accommodate the DUT. A gross leak is defined as a hole in the package at least .010 inches (0.254 mm) in diameter. Very small packages may be stored in an atmosphere containing at least 10 percent helium after bombing to insure adequate signal to noise ratio for the gross leak test over the one hour test interval. Please note that for the CH2 test method, the dwell time chosen should be less than 60 minutes or a 10 percent helium storage container must be used to store the device from the time it is removed from the pressurization chamber to when it is inserted into the test apparatus. The demonstrated minimum detectable leak rate for this test method is 3E-13 atm-cc/sec; however, the design of the apparatus can increase or decrease this limit.

1/ From "Standard Recommended Practices for Determining Hermeticity of Electron Devices with a Helium Mass Spectrometer Leak Detector," ASTM Designation F134, Pt. 43.

10.2.2 Failure criteria. Unless otherwise specified, devices with an internal cavity volume of 0.01 cm^3 or less shall not be accepted if the equivalent standard leak rate (L) exceeds 1×10^{-9} atm cm^3/s. Devices with an internal cavity volume greater than 0.01 cm^3, and equal to or less than 0.5 cm^3, shall not be accepted if the equivalent standard leak rate (L) exceeds 5×10^{-9} atm cm^3/s. Devices with an internal cavity volume greater than 0.5 cm^3 shall not be accepted if the equivalent standard leak rate (L) exceeds 1×10^{-8} atm cm^3/s.

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11. Test condition J, weight gain gross leak.

11.1 Apparatus. Apparatus for this test shall consist of the following:

a. A vacuum/pressure chamber for the evacuation and subsequent pressure bombing of devices up to 90 psia (618 kPa) for up to 10 hours.

b. An analytical balance capable of weighing the devices accurately to 0.1 milligram.

c. A source of type III detector fluid as specified in table 1071-II.

d. A filtration system capable of removing particles greater than one micrometer in size from the fluid.

e. Suitable calibrated instruments to measure test pressures and time.

f. A suitable solvent.

11.2 Procedure. The devices shall be cleaned by placing them in a container of a suitable solvent at +25°C and allowed then to soak for 2 minutes minimum. The devices shall then be removed and placed in an oven at +125°C ±5°C for 1 hour minimum, after which they shall be allowed to cool to room ambient temperature. Each device shall be weighed and the initial weight recorded, or the devices may be categorized into cells as follows: Devices having a volume of ≤0.01 cm^3 shall be categorized in cells of 0.5 milligram increments and devices with volumes >0.01 cm^3 shall be categorized in cells of 1.0 milligram increments. The devices shall be placed in a vacuum/pressure chamber and the pressure reduced to 0.0967 psia (667 Pa) and maintained for 1 hour except that for devices with an internal cavity volume ≥0.1 cm^3, this vacuum cycle may be omitted. A sufficient amount of type III detector fluorocarbon fluid shall be admitted to the pressure chamber to cover the devices. When the vacuum cycle is performed, the fluid shall be admitted after the 1 hour period but before breaking the vacuum. The devices shall then be pressurized to 75 psia (517 kPa) except that 618 kPa (90 psia) shall be used when the vacuum has been omitted. The pressure shall be maintained for two hours minimum. If the devices will not withstand the 75 psia (517 kPa) test pressure, the pressure may be lowered to 45 psia (310 kPa) with the vacuum cycle and pressure maintained for 10 hours minimum. Upon completion of the pressurization period, the pressure shall be released and the devices removed from the pressure chamber and retained in a bath of the fluorocarbon fluid. When the devices are removed from the fluid they shall be air dried for 2 minutes ±1 minute prior to weighing. The devices shall be transferred singly to the balance and the weight, or weight category, of each device determined. All devices shall be tested within 4 minutes following removal from the fluid. The delta weight shall be calculated from the record of the initial weight and the post weight of the device. Devices which were categorized shall be separated into two groups, one of which shall be the devices which shifted one cell or less, and the other devices which shifted more than one cell.

11.3 Failure criteria. A device shall be rejected if it gains 1.0 milligram or more and has an internal volume of ≤0.01 cm^3, and 2.0 milligrams or more if the volume is >0.01 cm^3. If the devices are categorized, any device which gains enough weight to cause the device to shift by more than one cell shall be considered a reject. A device which loses weight of an amount which, if gained, would cause the device to be rejected may be retested after it is baked at +125°C ±5°C for a period of 8 hours minimum.

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12. Test condition K, fluorocarbon vapor detection.

12.1 Apparatus. Apparatus for this test shall consist of:

a. A vacuum/pressure chamber for the evacuation and subsequent pressure bombing of devices up to 90 psia (620 kPa) for up to 12 hours.

b. A fluorocarbon vapor detection system capable of detecting vapor quantities equivalent to 0.28 milligram of type I fluid.

c. A source of type I detector fluid specified in table 1071-II.

d. Suitable calibrated instruments to indicate that test, purge times, and temperatures are as specified. The detection system shall be calibrated at least once each shift when production occurs by introducing 1 microliter of type I detector fluid into the test chamber. The resulting reading shall be adjusted in accordance with the manufacturer's instructions.

e. The vapor detector used for condition K shall be calibrated at least once each working shift using a type I fluid calibration source, and following the manufacturer's instructions.

12.2 Procedure. The devices shall be placed in a vacuum/pressure chamber and the pressure reduced to 5 torr or less and maintained for 30 minutes minimum. A sufficient amount of type I detector fluid shall be admitted to the pressure chamber to cover the devices. The fluid shall be admitted after the 30 minute vacuum period but before breaking the vacuum. The devices shall then be pressurized and maintained in accordance with table 1071-III. Upon completion of the pressurization period, the pressure shall be released, the devices removed from the pressure chamber without being removed from the detector fluid for more than 20 seconds, and then retained in a bath of fluorocarbon fluid. When the devices are removed from the fluid they shall be air dried for a minimum of 20 seconds and a maximum of 5 minutes prior to the test cycle. If the type I detector fluid has a boiling point of less than +80°C, the maximum drying time shall be 3 minutes. The devices shall then be tested with a fluorocarbon vapor detection system that is calibrated in accordance with 12.1. "Purge" time shall be in accordance with table 1071-VI. Test time shall be a minimum of 3.5 seconds unless the device is rejected earlier. The system's purge and test chambers shall be at a temperature of +125°C ±5°C. Test time shall be 2.5 seconds minimum with the purge and test chambers at a temperature of +150°C ±5°C.

NOTE: Test temperature shall be measured at the chamber surface that is in contact with the DUT.

12.3 Failure criteria. A device shall be rejected if the detector instrumentation indicates more than the equivalent of 0.28 milligrams of type I detector fluid in accordance with table 1071-II.

TABLE 1071-VI. Purge time.

Package with internal free volume (cm^3)	Purge time at +125°C ±5°C (seconds)
≤0.01	≤5
≥0.01 ≤0.10	≤9
≥0.1	≤13

NOTE: Purge time shall be defined as the total time the device is heated prior to entering the test mode. Maximum purge time can be determined by cycling a device with a .02 inch to .05 inch (0.51 mm to 1.27 mm) hole and measuring the maximum purge time that can be used without permitting the device to escape detection.

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13. Test condition L_1 or L_2 - optical gross leak.

13.1 Apparatus:

a. An optical inspection station capable of evacuation and pressurization, and subsequent detection of package lid deformation.

b. Suitable calibration instrumention to indicate test results, times, and pressures are as specified.

13.2 Lid stiffness. Test condition L_1 and L_2 are valid only for packages with thin lids (thickness < 0.025 typically for metallic lids). The test sensitivity is related to the extent of deformation of the lid due to the specific pressure change and the test time used. For a specific lid material ad size the following formula must be met:

For condition L_1: $R^4 / E\,T^3 > 1.0 \times 10^{-4}$ (1).

For condition L_2: $R^4 / E\,T^3 > 1.0 \times 10^{-3}$ (2).

Where: R = The minimum width of free lid (inside braze or cavity dimension in inches).
E = The modulus of elasticity of the lid material.
Aluminum: $E = 10 \times 10^6$ lb/in^2.
Kovar: $E = 20 \times 10^6$ lb/in^2.
Ceramic: $E = 60 \times 10^6$ lb/in^2.
T = The thickness of the lid (inches).

13.3 Leak sensitivity. The optical leak test shall be performed with a test pressure (P_o) and time (t), which will provide the leak rate sensitivity required. The leak rate sensitivity is provided by the following equation:

$$L = (-V_o / k_2\, t)\, \ln(1 - dY_t / P_o\, L_o).$$

Where: L = The leak rate sensitivity of the test (atm-cc/sec).
V_o = The volume of the package cavity (in^3).
k_2 = The leak test gas constant (air = 1.0, He = 2.67).
t = The test duration time (seconds).
dY_t = The measured deformation of the package lid (inches).
P_o = The chamber pressure during the test (psig).
L_o = The lid stiffness constant calculated from the package dimensions (inch/psi).

13.4 Test condition L_1 - optical gross leak. The completed device(s) shall be placed in the sealed test chamber. The optical interferometer shall be set to observe the package lid. The chamber shall then be evacuated while the deformation of the lid is being observed with the optical interferometer. The deformation of the lid with pressure change, and the lack of continued deformation of the lid with reduced pressure held for time t_1 (or equivalent procedure), will be observed for each package in the field of view simultaneously.

13.4.1 Failure criteria. A device shall be rejected if the optical interferometer did not detect deformation of the lid as the chamber pressure was initially changed, or if the interferometer detects the lid deforming as the chamber pressure is held constant (or equivalent procedure).

13.5 Test condition L_2 - optical gross/fine leak. The completed device(s) shall be placed in the sealed test chamber. The optical interferometer shall be set to observe the package lid. The chamber shall then be evacuated while the deformation of the lid is being observed with the optical interferometer. The deformation of the lid with pressure change, and the lack of continued deformation of the lid with reduced pressure held for time t_1 (or equivalent procedure), will be observed for each package in the field of view simultaneously. The sealed test chamber is then pressurized with helium gas to no more than 2 atmospheres. The lack of deformation of the lid is then observed with an optical interferometer to time t_2 (or equivalent procedure).

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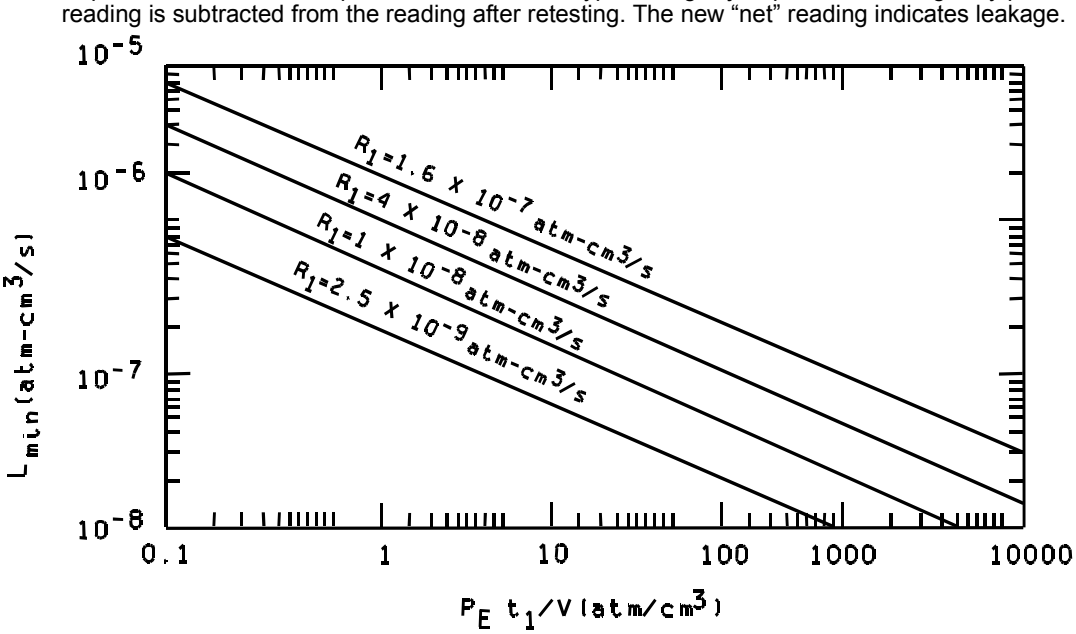
13.5.1 Failure criteria. A device shall be rejected for any of the three following criteria: (1) If the interferometer did not detect deformation of the lid as the chamber pressure was initially changed; or, (2) if the interferometer detects the lid deforming form the package leaking its entrapped internal pressure during time t_1 as the pressure is held constant (or equivalent procedure); or, (3) if the interferometer detects the lid deforming from the package leaking in the pressurized helium gas during time t_2 as the pressure is held constant (or equivalent procedure).

14. Notes.

1. The fine leak test shall be performed first if condition A or E is used for gross leak. Gross leak may be performed prior to fine leak if condition C, D, J, K, or L is used for gross leak and provided that the vapor pressure of the fluorocarbon material used in condition C, J, and K (which may be inside the device) is greater than 59 psia (406 kPa), T_A = +125°C. The devices shall be subjected to a bake at this temperature for a minimum of 1 hour prior to performing the fine leak test. This sequence should be true regardless of whether the leak tests are part of a screening sequence or are included as group B or group C requirements.

2. For test conditions A through E, K, and L_1, the maximum allowable leak rate should not be specified because these tests are "go"/"no-go" type tests that do not provide an indication of actual leak rate. (Although test conditions A, B, K, and L_1 have a definite quantitative measurement to be met, they are still considered "go"/"no-go" tests.)

3. When retesting devices to test condition H, the history of device exposure to helium including dates, backfilling performed, tracer gas concentrations, pressure, and time exposed, should be known in order to ensure reliable results. When retesting devices to conditions G1 or G2, the history of the prior testing is not required. The devices are pre-read for residual krypton-85 gas just prior to retesting. Any prior krypton-85 reading is subtracted from the reading after retesting. The new “net” reading indicates leakage.



4. Reject value of equivalent standard leak rate as a function of pressurization conditions and indicated leak rate as computed from the approximate solution, for small leaks where dwell time t_2 is not a significant factor. The reject level R_2 shall be taken larger relative to the minimum detectable R value.

FIGURE 1071-5. Smallest detectable leak.

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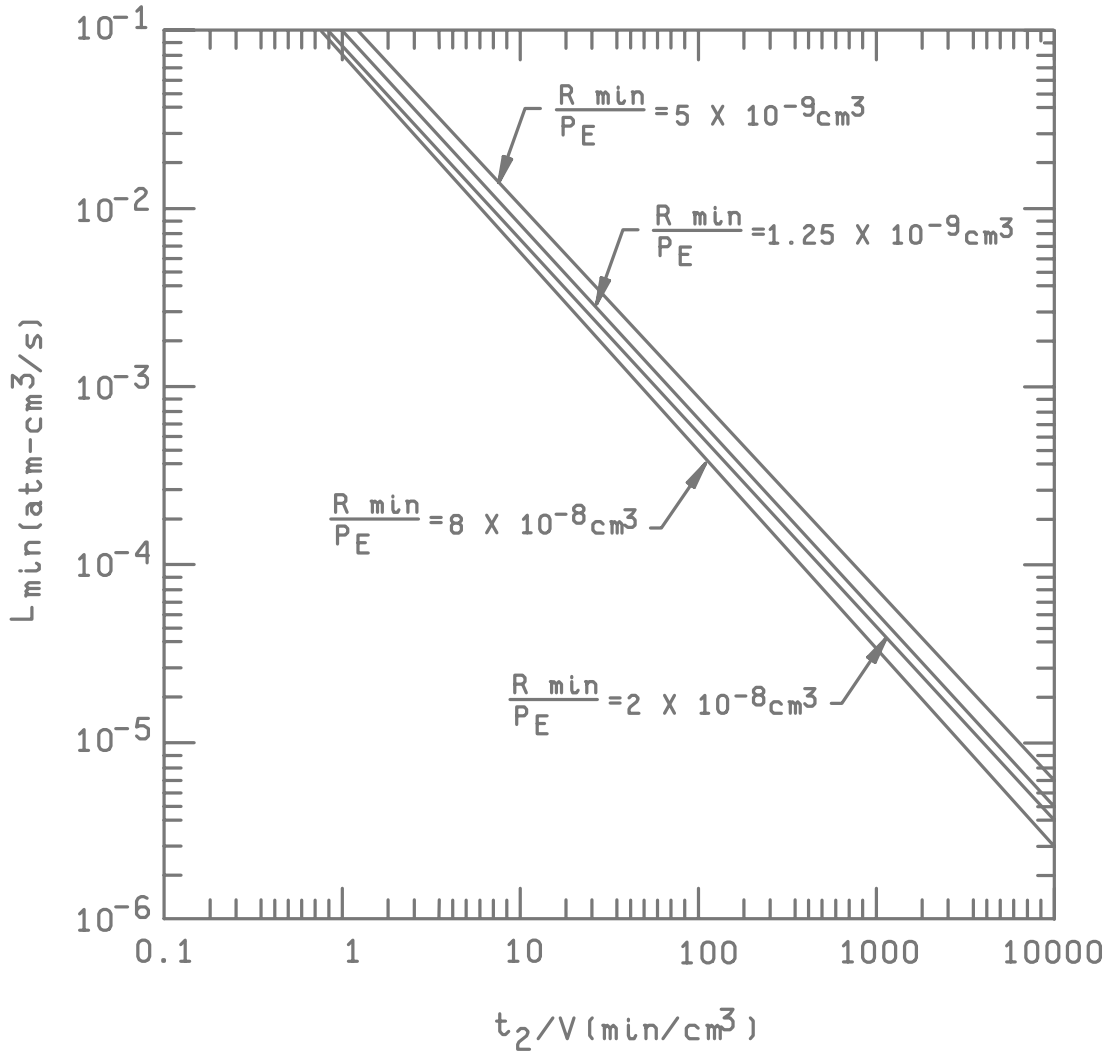

NOTE:

Upper test limit of equivalent standard leak rate as a function of dwell time, pressurization, and indicated leak rate as computed from the approximate solution, (e.g., for larger leaks where internal pressurization is complete).

FIGURE 1071-6. Largest detectable leak.

15. Summary. The following conditions shall be specified in the applicable performance specification:

    a. Test condition letter when a specific test is to be applied (see 3.).

    b. Accept or reject leak rate for test conditions G, H_1, or H_2 when other than the accept or reject leak rate specified herein applies (see 9.5.1, 10.2.1.1, and 10.2.2).

    c. Where applicable, measurements after test (see 3.).

    d. Retest acceptability for test conditions G and H (see 9.). For K (see 3.e.).

    e. Order of performance of fine and gross if other than fine followed by gross (see 3.).

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METHOD 1080

SINGLE-EVENT BURNOUT AND SINGLE-EVENT GATE RUPTURE

1. Purpose. The purpose of this test method is to describe the procedure for conducting heavy ion irradiation of power MOSFETs. This test method establishes a procedure for characterization and for verification (acceptance or qualification) of discrete power MOSFETs for single-event burnout (SEB) and single-event gate rupture (SEGR). In principle, this test method may be applicable to testing where neutrons, protons, or other light particles are used.

1.1 Terms and definitions. The following symbols and terms shall apply for the purpose of this test method:

a. Cross-sectional area: Calculated as the number of events per unit fluence.

b. DUT: Device under test.

c. Fluence: The ion flux integrated over the time required for the run, expressed as ions/cm^2.

d. Flux: The number of ions passing through a one cm^2 area perpendicular to the ion beam per unit of time, expressed as ions/cm^2•s.

e. I_{DS}: The measured drain-to-source current (amps).

f. I_{GS}: The measured gate-to-source current (amps).

g. Linear energy transfer (LET): The amount of energy transferred per unit length as the ion travels through a material, expressed as MeV/(mg/cm^2) in this test method.

h. Single-event burnout (SEB): A single-ion-induced condition that causes a localized high-current state resulting in a catastrophic device failure characterized by an increase in drain current that exceeds the manufacturer's rated leakage current at the drain electrode.

i. Single-event gate rupture (SEGR): A single-ion-induced condition that causes a localized defect in the gate dielectric resulting in a catastrophic device failure, characterized by an increase in gate current that exceeds the manufacturer's rated leakage current at the gate electrode.

j. SEB circumvention: A technique used to prevent the device from catastrophically failing during an SEB event.

k. SEB cross-sectional area: Calculated as the number of SEB events per unit fluence.

l. SEGR cross-sectional area: Calculated as the reciprocal of the fluence required to induce the SEGR event.

m. SEGR post gate-stress test: After the heavy ion irradiation, a test is conducted to verify the gate integrity by applying the maximum specified V_{GS}.

n. Threshold LET: The minimum LET required to cause a single-ion-induced failure under the specified bias conditions.

o. V_{DS}: The applied drain-to-source voltage (volts).

p. V_{GS}: The applied gate-to-source voltage (volts).

q. V_{TH}: The value of V_{GS} where the inversion layer is formed and the device turns on.

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1.2 Applicable documents. The following documents form part of this test method. The most current revision of these documents shall take precedence over those cited.

EIA/JESD57 - Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation.

ASTM F-1192 - Standard Guide for the Measurement of Single-Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

1.3 Device handling. Special care shall be taken to ensure that the devices are not damaged before testing. Since the lids are removed before irradiation, extra precautions shall be taken to protect the exposed die. Otherwise, devices shall be handled in accordance with standard operating procedures to protect against damage and electrostatic discharge. Use of anti-static foams, grounding straps, and other precautions is recommended.

NOTE: Some power MOSFETs may require voltages that exceed 500 volts and voltages in excess of 32 volts can present a safety hazard. Safety precautions shall be taken to ensure safe operation of all equipment and personnel. Note that conformal coatings may interfere with the test, changing the penetration depth of the ion as well as degrading the ion energy. The effect of conformal coatings shall be evaluated. Conformal coatings, such as polyamide, shall be chemically removed before testing.

2. Apparatus. The apparatus required for SEB/SEGR testing consists of a heavy ion source, a vacuum chamber system, DUT test instrumentation, test circuit board(s), cabling, switching system (if required), an x-y-z stage system (if required), and dosimetry measurement instrumentation. Precautions shall be taken to obtain an electrical measurement system with sufficient insulation, shielding, and grounding to measure a gate current, I_{GS}, of 10 nA or less (measurement resolution).

2.1 Heavy ion source. The heavy ion source shall be a cyclotron, Van de Graaff accelerator, or other suitable source. The heavy ion source shall be capable of providing an average ion flux up to 100,000 ions/cm^2•s. The average beam uniformity should be maintained within ±15 percent over the die area unless otherwise specified. The ion beam energy shall provide sufficient ion penetration depth to induce the SEGR response or as agreed to by both parties to the test. Note that the accelerator design determines the maximum ion beam energy; and, therefore, some accelerators may be inadequate to perform a worst-case test condition. Also, note that some accelerators are rf-type machines (e.g. cyclotrons) and may have higher instantaneous fluxes.

2.2 Vacuum chamber system. The chamber shall have a test circuit board mounting frame and cable feed-through. The vacuum chamber system should be capable of accepting an x-y-z stage mechanism. The pumping system shall be capable of evacuating the vacuum chamber below1.3 x 10^{-1} Pa (10^{-3} torr). Precautions shall be taken to ensure that any component placed in the vacuum chamber does not interfere with the vacuum system. Note that certain materials can out-gas, affecting the vacuum quality. Also note that some capacitors (e.g., electrolytic capacitors) can explode, fail, or out-gas when placed in a vacuum.

2.3 Test instrumentation. Standard electrical test instruments capable of establishing the required test conditions and measuring the required electrical parameters shall be used. Note that many power MOSFETs may require operating voltages in excess of 32 volts and safety precautions shall be followed to ensure safe operation of all equipment and personnel.

2.3.1 SEB instrumentation. Test instrumentation to bias and monitor the DUT may consist of one or more of the following types of instruments:

a. Power supply.

b. Ammeter.

c. Voltmeter.

d. Counter.

e. Oscilloscope.

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2.3.2 SEGR instrumentation. Test instrumentation to bias and monitor the DUT may consist of one or more of the following types of instruments:

a. Power supply.

b. Ammeter.

c. Voltmeter.

2.4 Test circuit board. The test circuit board contains the test socket, delidded DUT, any additional wiring, and any auxiliary components. The test board provides a mounting surface and interface between the test instrumentation and the DUT, applying V_{GS} and V_{DS}, while monitoring I_{GS} and I_{DS}. Figure 1080-1 shows a representative test circuit and figure 1080-2 shows a typical SEB circumvention and monitoring technique. Any auxiliary components, such as the resistors, capacitors, or current probes, shall be included in the final test circuit. Any accepted SEB circumvention and monitoring technique is acceptable. The test board can have multiple test sockets to minimize the time required to vent and evacuate the vacuum chamber. The test socket, in which the DUT is inserted, is mounted in such a way that the DUT surface shall be perpendicular (nominally within ±5°C) to the heavy ion beam. The DUT is delidded prior to testing, and the entire die shall be irradiated.

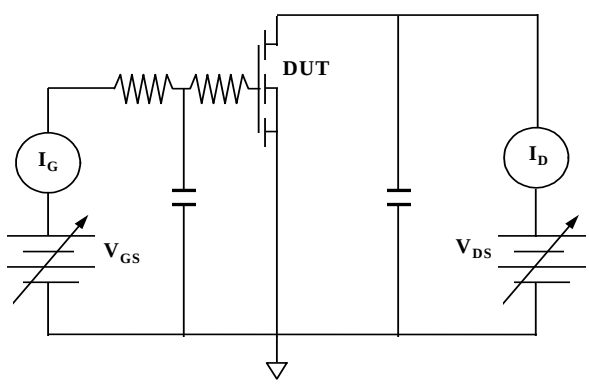

FIGURE 1080-1. Basic SEB/SEGR test circuit.

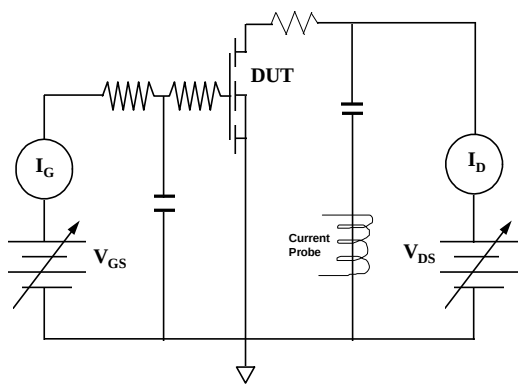

FIGURE 1080-2. SEB circumvention and monitoring circuit.

2.5 Cabling. Cables are typically used to connect the test circuit board, located in the vacuum chamber, to the test instrumentation, normally placed outside the vacuum chamber. The cable length shall be minimized to prevent interference with the desired measurement. However, the actual cable length is dictated by the size of the vacuum chamber, the spatial location of the test board with respect to the cabling feed-throughs, and the minimum distance from the cabling feed-throughs to the DUT test instrumentation. Observation of SEB pulses shall be performed using properly terminated shielded cables to minimize reflections and other signal/noise interference.

2.6 Switching system. A switching system can be used when multiple devices are placed on the test board. The switching system shall provide electrical isolation between the gate and drain electrodes of the various test devices on the test board. Inclusion of a switching system shall not interfere with the electrical measurement system, as specified in 2.

2.7 X-Y-Z stage system. If multiple devices are placed on the test board, an x-y-z stage system can be used to provide a mechanical mechanism to move the device into and out of the heavy ion beam.

2.8 Dosimetry system. The dosimetry system shall be used to determine the ion beam energy, LET, average ion beam flux, fluence, and average ion beam uniformity. Note that many facilities provide this dosimetry system.

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3. SEB/SEGR prediction. To assist in the preparation of the test plan and the selection of initial bias conditions, an appropriate SEB/SEGR prediction method may be utilized to predict the SEB/SEGR failure thresholds. The preferred prediction method is to use previous measurements on similar device types. Test personnel should use these predicted failure thresholds to help verify that the SEGR and SEB test measurements are valid. If a significant difference (nominally greater than a ±30 percent deviation from the predicted response) is observed, the test personnel should verify the test setup including the ion specie, ion energy, bias conditions, and device type. These predictions can help to develop the overall test plan.

3.1 SEB prediction. Currently, there are not any accurate prediction models available for SEB. Predictions based upon previously obtained SEB data are helpful, but, due to the nature of the failure mechanism, cannot be used to accurately predict SEB.

3.2 SEGR prediction. Predictions of SEGR can be made from previous SEGR data or calculated using currently accepted models. If previous test results are unavailable or the device layout, design, or process has been modified, then SEGR failure thresholds can be predicted using an empirical prediction method or an analytical prediction method.

3.2.1 SEGR empirical prediction. The empirical prediction method uses an empirically derived equation to predict the SEGR failure threshold of the oxide capacitor when V_{DS} = 0 volts, as expressed by equation (1).

$$V_{GS}=\frac{(E_{OX_BR})(T_{OX})}{\left(1+\frac{LET}{53}\right)}$$

Where: E_{OX_BR} is the breakdown field strength of the oxide (V/cm), T_{OX} is the thickness of the gate oxide dielectric (cm), and LET_PEAK is the maximum LET value of the given ion species in MeV/mg/cm2.

An approximation of the substrate response for the case when V_{DS} is biased can be obtained by using an expanded form of equation (1). This expanded equation is expressed by equation (2).

$$V_{GS}=(0.84)(1-e^{-\frac{LET}{17}})(V_{DS})\frac{(E_{OX_BR})(T_{OX})}{\left(1+\frac{LET}{53}\right)}$$

Where: E_{OX_BR} is the breakdown field strength of the oxide (V/cm), T_{OX} is the thickness of the gate oxide dielectric (cm), and LET is the linear energy transfer in (MeV/mg/cm2). LET PEAK is the maximum LET value of the given ion species in MeV/mg/cm2

3.2.2 SEGR analytical prediction. Analytical predictions can be obtained using sophisticated numerical simulations to predict the SEGR failure threshold response. Additional information concerning these predictions can be found in the literature.

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4. Characterization tests. Characterization testing is that testing required to obtain an SEB cross-sectional area curve, an SEGR cross-sectional area curve, or an SEGR failure threshold curve. Data points are taken to describe the response of the discrete MOSFET as a function of V_{GS} and/or V_{DS} over the operating range of the device and/or over a range of LET values. Characterization testing should be conducted initially to define the worst-case operating conditions of the device or to identify the sensitive die area. Additional characterization testing may be required after process and/or design changes have been made to the device. Characterization tests are useful for establishing the conditions for subsequent verification tests. Characterization testing does not have to be performed as a part of the verification testing unless fabrication changes have been made that might invalidate the initial technology characterization. Note that angling the die surface away from the plane where the ion beam is perpendicular to the die surface to produce an effective LET is invalid and shall not be used. It has been reported that the ion energy can influence the measured SEGR failure thresholds, suggesting that the ion energy shall be considered when a worst case test condition is specified. The maximum allowable V_{DS} bias increment for a DUT shall be no more than 10 percent of the device's rated drain voltage. The maximum allowable V_{GS} bias increment for a DUT shall be no more than 5 volts. Smaller V_{DS} and V_{GS} bias increments are recommended. Also, note that increasing the DUT's operating temperature has been demonstrated to increase the LET threshold for SEB but not for SEGR, indicating that lower operating temperatures are a worst case test condition.

4.1 SEB characterization**.** Characterization requires that an SEB circumvention method be utilized. SEB characterization produces a cross-sectional area curve as a function of LET for a fixed V_{DS} and V_{GS}. SEB is not sensitive to changes in the gate bias, V_{GS}. The V_{GS} bias shall be sufficient to bias the DUT in an "off" state (a few volts below V_{TH}), allowing for total dose effects that may reduce the V_{TH}. Multiple SEB cross-sectional area curves may be required, expressing different operating conditions for V_{DS}. Note that p-channel devices have not been demonstrated to be sensitive to SEB.

4.1.1 SEB cross-sectional area If specified as a test requirement and if SEB is observed, one of the many reported techniques can be used to circumvent catastrophic SEB failure, such as a current-limiting resistor placed between the drain stiffening capacitor and the drain electrode. Then, to obtain an SEB error count, a current probe (Tektronix CT-2, sense resistor, or other suitable current probe) shall be inserted between the source electrode and ground. Using this setup, an SEB event will produce current pulses. SEB occurrence can be monitored using an electronic oscilloscope to record the shape of the SEB pulse(s), if required, and a pulse counter to record the number of SEB occurrences. A point on the SEB cross-sectional area curve is then obtained by dividing the number of SEB events by the fluence for that given test condition. The SEB cross sectional curve is subsequently found by finding points at several different LET values. After the DUTs have been delidded and the chamber evacuated, apply the specified V_{GS} and V_{DS} bias condition; and irradiate the DUT to the specified fluence level (typical ranges are between 10^5 and 10^7 ions/cm^2). If SEB occurs, record the event by incrementing the counter. The flux shall be adjusted so that the number of SEB events is no more than 100 events per second. When the desired fluence is achieved, the beam is shuttered; and the total number of SEB events are recorded. This process is continued, selecting different ions to obtain the required LET values. Repeat this process for the specified samples and conditions.

4.2 SEGR characterization. SEGR characterization may produce three unique curves: An SEGR cross-sectional area curve as a function of LET for a fixed V_{GS} and V_{DS} bias condition; an SEGR threshold curve of V_{GS} as a function of V_{DS} for a fixed LET value; or an SEGR threshold curve of V_{DS} as a function of LET at a fixed V_{GS}. Multiple SEGR cross sectional area curves may be required to express different V_{DS} and V_{GS} conditions. Multiple SEGR threshold curves may be required to express different V_{GS}, V_{DS}, or LET conditions. SEGR characterization may be performed in conjunction with SEGR verification.

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4.2.1 SEGR cross-sectional area. If specified in the test requirements and if SEGR occurs, an SEGR cross-sectional area curve can be obtained. However, SEGR cannot be circumvented. Hence, to obtain an SEGR cross-sectional area curve requires the destruction of numerous devices. For a given device, the ion irradiation would be terminated upon detection of SEGR. One point on the SEGR cross-sectional area curve can be obtained by dividing one SEGR event by the measured fluence to induce that event. After the DUTs have been delidded and the chamber evacuated, apply the specified V_{GS} and V_{DS} bias condition; and irradiate the DUT to the specified fluence level. If SEGR occurs, immediately terminate the exposure; and record the accumulated fluence. Note that the ion flux can be lowered to obtain a more accurate fluence. If the maximum fluence is achieved and the DUT passes the post gate-stress test, a new test condition or a new DUT is selected. If SEGR occurs, a new DUT is selected. Apply the new test condition (incrementing V_{GS}, V_{DS}, or changing the ion specie). This process is repeated until the desired curve is obtained. Repeat this process to obtain the required curves. Note that characterization results in device failure and only represents a single data point for that device. For the special case where the applied dc field across the gate dielectric is less than 1 MV/cm, the procedure to obtain a cross-sectional area curve should be modified as follows:

a. An incremental fluence should be set at one-third of the die area or less;

b. After each irradiation step, a post gate-stress test shall be performed to verify device functionality;

c. If SEGR is not detected, continue irradiation steps until SEGR occurs or until the maximum accumulated fluence is obtained; and

d. Select new device and bias condition and repeat test procedure until the desired curve is obtained.

4.2.2 SEGR post gate-stress test. If the gate bias is small (typically V_{GS} < 10 volts) during irradiation, SEGR may or may not produce a catastrophic failure until sufficient gate bias is applied. If an insufficient gate bias is applied, SEGR may only produce a latent defect site. Therefore, after the irradiation, a post gate-stress test shall be performed on each test device. The post gate-stress test shall apply a gate bias equal to the maximum operating gate voltage (nominally ±10 percent) or as specified.

5. Verification tests. Verification testing requires the irradiation of the DUT to specified test conditions (e.g. gate bias, drain bias, ion species, ion energy, ion LET, ion range, ion flux, and ion fluence). Verification testing is useful for hardness assurance and qualification testing of discrete power MOSFETs to determine their suitability at the specified test conditions. These tests use a "pass"/"no pass" criterion and can be destructive. Note that angling the die surface away from the plane where the ion beam is perpendicular to that surface to produce an effective LET is invalid and shall not be used to conduct these tests. It has been reported that the ion energy can influence the measured SEGR failure thresholds, suggesting that the ion energy should be considered to achieve a worst case test condition. Also, note that increasing the DUT's operating temperature has been demonstrated to increase the LET threshold for SEB but not for SEGR, indicating that lower operating temperatures are a worst case test condition.

5.1 SEB verification tests. For SEB verification, a sufficiently large capacitance is placed at the drain electrode to produce catastrophic failure. Note that no circumvention techniques are used in this test. After the DUTs have been delidded and the chamber evacuated, apply the specified V_{GS} and V_{DS} bias condition and irradiate the DUT to the specified fluence level. If failure occurs, the exposure can be terminated. Record SEB results. Repeat for the specified samples and conditions.

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5.2 SEGR verification tests. For SEGR verification, this test is a two-step process. After DUTs have been delidded and the chamber evacuated, apply the specified V_{GS} and V_{DS} bias condition and irradiate the DUT to the specified fluence. If failure occurs, the exposure can be terminated. The second step requires a post gate-stress test to be performed after irradiation, if the gate bias during irradiation was less than the maximum operating gate voltage. Record SEGR result. Repeat for the specified samples and conditions.

6. SEB/SEGR test procedure. The test plan should document the proper steps to be followed before, during, and after heavy ion irradiation. Sufficient samples shall be obtained to conduct the test. Samples with conformal coatings, such as polyamide, should be chemically removed before testing. SEB and SEGR both can result in catastrophic failure that produces large leakage currents, destroying the device. In SEB testing, a capacitance sufficient to hold the bias voltage within ±10 percent may be required to induce damage during an SEB event. For characterization testing, SEB can be circumvented and recorded producing an SEB event count, which then can be used to produce a point on the cross-sectional area curve. To help select the proper biases, an SEB/SEGR prediction shall be made. The required ion specie is selected and the ion beam energy shall be tuned and verified using the dosimetry system. The test circuit board, cabling, and instrumentation shall be connected and its operation verified. Before irradiation, test devices shall be delidded and inserted into the test board. The drain and gate currents, I_{GS} and I_{DS}, shall be monitored before, during, and after the irradiation(s), as well as during the post gate-stress test, to verify the condition of the DUT. After completion of the test run, the results of the test shall be recorded and documented.

6.1 Test plan. A test plan shall be devised that supports each test. The test plan shall be used as a guide for the procedures and decisions during irradiation. The test plan shall be developed, and the following conditions shall be outlined.

6.1.1 Ion specie and energy. The test plan shall identify the ion specie and an appropriate energy to perform the test. Selection of a specific ion specie and its energy determines the LET value. Obtaining a range of LET values requires using different ion species at different energies. Note that using angles to modulate the LET value is unacceptable. Selection of a different ion specie and energy by test personnel requires verification that the ion LET and its range meet the test requirements. Verification can be made using the TRIM code or other suitable simulation codes for the given device material. Also, note that the energy of the ion beam has been shown to influence the SEGR failure thresholds. Therefore, determination of the worst case test condition can require multiple irradiations with the same ion at different energies.

6.1.2 Device information. The test plan shall provide a description of the devices to be tested and the number of test samples required for each test. The test plan shall identify the device type, acceptance lot, and other critical information. Devices shall be marked for traceability so that lids can be removed. Identification markers should be placed on the flange and not on the lid. Only devices that have passed the pre-electrical tests shall undergo heavy ion testing. Test samples shall be randomly selected from the parent population. The number of samples shall be specified to meet the test requirements. For the purposes of verification testing, a representative sample should be selected from the lot.

6.1.3 Electrical parameters. The test plan shall specify the electrical parameters to be measured before and after irradiation.

6.1.4 Test configuration. The test plan shall specify the bias and exposure conditions for each test sample. The test plan shall specify the case temperature of the DUT if it is required to be set at other than the room ambient temperature.

6.1.5 Test sequence. The test plan should specify a test sequence similar to figure 1080-3. For characterization testing, the test plan shall define an initial bias condition and the bias increment. The V_{DS} bias increment shall not exceed 10 percent of the device's rated drain breakdown voltage. For verification testing, the test plan shall define the specified biases, the minimum number of samples that shall be tested at each bias, and the handling of the devices after testing. Any additional electrical tests shall be specified and any special handling requirements shall be specified.

6.1.6 SEB/SEGR detection. The test plan shall specify the procedure to monitor the drain and gate currents, I_{GS} and I_{DS}, before, during, and after the irradiation(s). In addition, the gate and drain currents shall be monitored during the post gate-stress test to verify that the DUT was not damaged during the previous irradiation.

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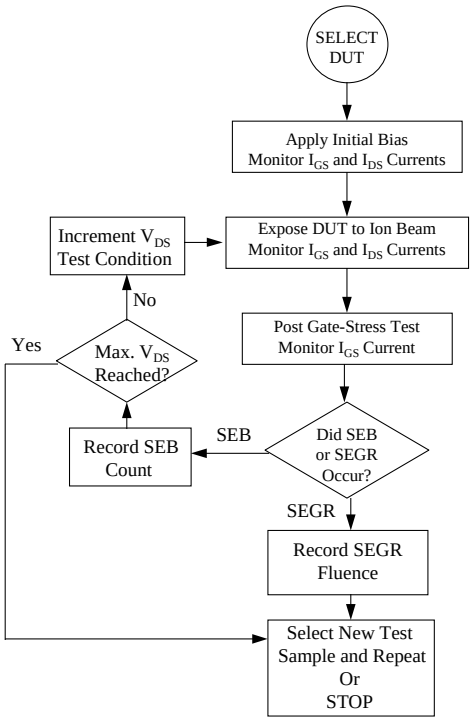
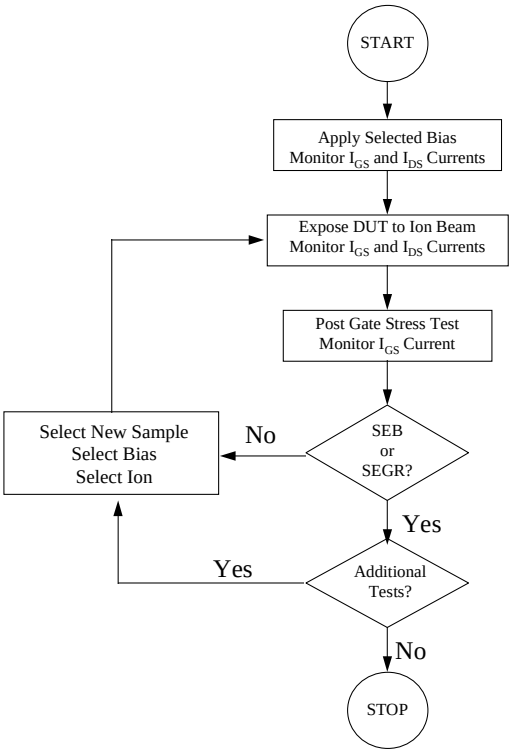


Characterization flowchart sample.



Verification flowchart sample.

FIGURE 1080-3. Test plan flowcharts.

6.1.7 Data recording. The test plan shall specify the necessary parameters that shall be recorded during the test.

6.1.8 Reporting requirements. The test plan shall specify the test documentation as required by 7 herein.

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6.2 Radiation test procedure. The test plan shall be used as a guide to perform the radiation test. A typical SEB/SEGR test procedure is given here as an example.

a. Test personnel shall specify the selected ion specie and energy to the facility operators as defined in the SEGR/SEB test plan specifying the desired flux, fluence, LET, range, and beam uniformity. Dosimetry shall be performed to verify that the ion beam characteristics are as specified.

b. The SEGR/SEB test board shall be mounted in the test fixture mounting frame. All necessary test cables shall be connected to the test board and vacuum feed-through inside the vacuum chamber.

c. The test instrumentation shall be set up as close as possible to the vacuum chamber. All necessary test cables shall be connected to the test hardware and vacuum feed-through outside the vacuum chamber.

d. When the test system is set up, the operation of the test system shall be verified for continuity and operation. Note that a quick check can be performed by applying a V_{GS} and V_{DS} and verifying the presence of these voltages with a voltmeter.

e. After test system verification is completed, ground all electrodes, and insert the devices for test. Handling of devices shall be in accordance with normal ESD practices. If lids were not removed before placement on the test board, remove the device lids. To verify that the devices were not damaged during the delidding process or insertion into the test board, a simple electrical check of I_{GS} and I_{DS} should be performed.

f. After device verification is completed, the device to be tested shall be aligned to the ion beam. With the beam shuttered and the DUT biases set at 0 volts, perform an alignment of the DUT to the ion beam. Note that some facilities provide a laser alignment system for this task.

g. When positional alignment is complete, turn off any lighting systems and laser systems in the vacuum chamber. Apply the selected bias conditions to the DUT, and begin monitoring the gate and drain leakage currents, I_{GS} and I_{DS}. Note that excitation by lights or laser may produce photocurrents which may interfere with the measurements.

h. When ready, open the ion beam shutter, exposing the DUT to the heavy ion beam. Note that most facilities include instrumentation to monitor the ion beam characteristics monitoring the average flux, fluence, and beam uniformity which should be recorded. When the desired fluence level is achieved, shutter the ion beam, terminating the irradiation.

(1) If performing an SEB characterization test, the test circuit shall include an appropriate circumvention technique and a current-sensing circuit. The number of current pulses for each irradiation shall be recorded (see 4.1).

(2) If performing an SEGR characterization test, the ion beam shall be shuttered immediately following the detection of SEGR-any significant gate current change. The ion fluence at failure shall be recorded. Note that detection of SEGR may require the test personnel to make a judgment concerning the SEGR status of the device.

(3) If performing an SEGR or SEB verification test, the gate and drain leakage currents, I_{GS} and I_{DS}, shall be monitored. If a current change is recorded (typically, a flag can be set, e.g. an $I_{GS} > 10^{-7}$ amps), document the observed conditions.

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i. After the ion beam is shuttered, a post gate-stress test shall be performed. During the post gate-stress test (the rated gate voltage is applied), the gate current shall be monitored. If a current change is detected (typically, a flag can be set, e.g. an $I_{GS} > 10^{-7}$ amps), document any observed conditions.

j. Upon completion of the post gate-stress test, record all pertinent test data. Record run number, ion specie, ion energy, range, LET, average flux, fluence, and test conditions (V_{GS}, V_{DS}). Record any changes in the drain or gate currents (I_{GS} and I_{DS}) before, during, and after the ion irradiation. Record any changes in the drain and gate currents, I_{GS} and I_{DS}, during the post gate-stress test. Determine the status of the test run. If the test is a characterization test, increment the test condition or select new device as required. Repeat test procedure. If the test is a verification, select next device and test conditions. Repeat test procedure.

7. Data formatting reporting. Test data/test reports shall be maintained and shall include the following information:

a. Device type, identification marker, lot identification, and date code.

b. Test date and test personnel names.

c. Facility, accelerator type, identification of ion, energy, average flux, LET, range in device material, and fluence.

d. Schematic of test circuit or test board.

e. Dosimetry output of each ion beam used.

f. Bias condition of each exposure run.

g. Record of observed SEGR or SEB (current changes).

h. Device case temperature (only if required at other than room ambient).

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2000 Series

Mechanical characteristics tests

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METHOD 2005.2

AXIAL LEAD TENSILE TEST

1. Purpose. The purpose of this test method is to establish the capability of axial lead glass body diodes to be free of intermittents or opens when measured in the forward mode under conditions of tensile stress and controlled temperature. This test may be destructive.

2. Equipment or apparatus.

   a. Digital volt meter and constant current source capable of supplying 100 mA of dc current to the DUT. A battery supply is preferred but if a constant current supply is used, a voltage clamp of approximately five volts shall be used.

   b. Load cell with 10 pounds full scale dial (or equivalent) capable of measuring 8 pounds ±10 percent.

   c. Pull test fixture capable of clamping both ends of the diode while applying an 8 pound axial pull. One clamp must be electrically isolated allowing the diode forward voltage to be monitored.

   d. Hot air supply capable of heating the diode ambient to T_A = +150°C ±5°C. (T_J approximately +175°C)

3. Procedure. The diode under test shall be mounted in the pull test fixture. The electrical monitoring equipment shall be connected to the diode leads. A forward current of 100 mA is passed through the diode while noting the forward voltage. The ambient temperature of the diode is then increased to ±150°C. NOTE: The diode junction temperature (T_J) will be approximately +25°C higher than ambient (T_J approximately +175°C) due to the thermal resistance of the diode when testing small (computer) diodes at 100 mA dc in the forward direction. A silicon diode (computer type) also has an approximate negative 1.2 mV/°C temperature coefficient at 100 mA. Therefore a 150 mV decline (100 mV minimum) in voltage should be expected during the ambient temperature increase (from +25°C to +150°C). After stabilizing at this temperature, then the axial lead pull force of eight pounds shall be applied while observing the forward voltage change.

4. Criteria for rejection. An acceptable device shall not exhibit a forward voltage increase of more than 30 mV during the 8 pound pull. Any instability or open is cause for rejection.

5. Summary. The following conditions shall be specified in the specification sheet.

   a. Ambient test temperature, if other than +150°C ±5°C.

   b. Measurement current, if other than 100 mA dc.

   c. Axial tensile stress, if other than 8 pounds.

   d. Allowable change in forward voltage, if other than 30 mV.

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METHOD 2006

CONSTANT ACCELERATION

1. Purpose. The constant acceleration test is used to determine the effect on devices of a centrifugal force. This test is an accelerated test designed to indicate types of structural and mechanical weaknesses not necessarily detected in shock and vibration tests.

2. Apparatus. Constant acceleration tests shall be made on an apparatus capable of meeting the minimum requirements of the individual specification sheets.

3. Procedure. The device shall be restrained by its case, or by normal mountings, and the leads or cables secured. A centrifugal acceleration of the value specified shall then be applied to the device for one minute in each of the orientations X_1, X_2, Y_1, Y_2, Z_1, and Z_2. The acceleration shall be increased gradually, to the value specified, in not less than 20 seconds. The acceleration shall be decreased gradually to zero in not less than 20 seconds.

4. Summary. The following conditions shall be specified in the specification sheet:

   a. Amount of centrifugal force to be applied, in gravity units (g) (see 3.).

   b. Measurements to be made after test.

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METHOD 2016.2

SHOCK

1. Purpose. This test method is intended to determine the ability of the devices to withstand moderately severe shocks such as would be produced by rough handling, transportation, or field operation. Shocks of this type may disturb operating characteristics or cause damage similar to that resulting from excessive vibration, particularly if the shock pulses are repetitive.

2. Apparatus. The shock testing apparatus shall be capable of providing shock pulses of the specified peak acceleration and pulse duration to the body of the device. The acceleration pulse, as determined from the output of a transducer with a natural frequency greater than or equal to five times the frequency of the shock pulse being established, shall be a half-sine waveform with an allowable distortion not greater than ±20 percent of the specified peak acceleration. The pulse duration shall be measured between the points at 10 percent of the peak acceleration during rise time and at 10 percent of the peak acceleration during decay time. Absolute tolerances of the pulse duration shall be the greater of ±0.6 milliseconds (ms) or ±15 percent of the specified duration for specified durations of 2 ms and greater. For specified duration less than 2 ms, absolute tolerances shall be the greater of ±0.1 ms or ±30 percent of the specified duration.

3. Procedure. The shock-testing apparatus shall be mounted on a sturdy laboratory table, or equivalent base, and leveled before use. The device shall be rigidly mounted or restrained by its case with suitable protection for the leads. The device shall be subjected to the specified number of blows in the specified direction. For each blow, the carriage shall be raised to the height necessary for obtaining the specified acceleration and then allowed to fall. Means may be provided to prevent the carriage from striking the anvil a second time. Electrical load conditions and measurements to be taken during the shock test, if applicable, shall be as specified. End-point measurements shall be as specified.

4. Summary. The following conditions shall be as specified in the specification sheet.

   a. Acceleration and duration of pulse (see 2.).

   b. Number and direction of blows (see 3.).

   c. Electrical-load conditions, if applicable (see 3.).

   d. Measurements during shock, if applicable (see 3.).

   e. End-point measurements (see 3.).

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METHOD 2017.2

DIE ATTACH INTEGRITY

1. Purpose. The purpose of this test method is to establish the integrity of the semiconductor die attachment to the package header or other substrate.

2. Apparatus. The test equipment shall consist of a force-applying instrument with an accuracy of ±5 percent of full scale or 50 grams, whichever is less. A circular dynamometer with a lever arm or a linear motion force-applying instrument may be used to apply the force required for testing. The test equipment shall have the following capabilities:

a. A die contact tool which applies a uniform distribution of the force gradually to an edge of the die (see figure 2017-1).

b. Provisions to assure that the face of the die contact tool is perpendicular to the die mounting plane of the header or substrate.

c. A rotational capability, relative to the header/substrate holding fixture and the die contact tool, to facilitate line contact parallel to the edge of the die; the tool applying the force to the die shall contact the die edge from end-to-end (see figure 2017-2).

d. A binocular microscope with a minimum magnification of 10X and sufficient lighting for visual inspection of the die and die contact tool interface during testing.

e. Optional apparatus for devices with a die area less than 25.5×10^{-4} in^2 instead of a calibrated instrument. Any hand held tool may be used. The general requirements of 2.a., 2.b., and 2.d. shall apply. The tool which shall apply a uniform perpendicular force to the edge of the die (see figures 2017-1, 2017-2, and 2017-3) and a microscope with a minimum magnification of 10X shall be used.

f. Apparatus for test condition C: A hammer, chisel, or spring loaded punch are suitable.

3. Test condition A die shear. For die directly bonded to a header or substrate.

3.1 Procedure. The test shall be conducted as defined herein or to the test conditions specified in the applicable specification sheet consistent with the particular part construction. All die strength tests shall be counted and the specific sampling, acceptance, and added sample provisions shall be observed, as applicable. (This test shall be considered destructive.)

3.1.1 Shear strength. A force sufficient to shear the die from its mounting, or equal to twice the minimum specified shear strength (see figure 2017-4), whichever occurs first, shall be applied to the die using the apparatus of 2 above.

a. When a linear motion force-applying instrument is used, the direction of the applied force shall be parallel with the plane of the header or substrate and perpendicular to the edge of the die being tested.

b. When a circular dynamometer with a lever arm is employed to apply the force required for testing, it shall be pivoted about the lever arm axis and the motion shall be parallel with the plane of the header or substrate and perpendicular to the edge of the die being tested. The contact tool attached to the lever arm shall be at a proper distance to assure an accurate value of applied force.

c. The die contact tool shall apply a force gradually from zero to a specified value against an edge of the die which most closely approximates a 90° degree angle with the base of the header or substrate to which it is bonded (see figure 2017-3). For rectangular die, the force shall be applied perpendicular to the longer side of the die. When constrained by package configurations, any available side of the die may be tested if the above options are not available.

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d. After initial contact with the die edge and during the application of force, the relative position of the contact tool shall not move vertically such that contact is made with the header/substrate or die attach material. If the tool rides over the die, a new die may be substituted or the die may be repositioned, provided that the requirements of 3.1.3 are met.

3.1.2 Criteria for device acceptability.

3.1.2.1 Failure criteria. A device will be considered a failure if the die bond shears as follows:

a. With a force less than the minimum shear strength requirements specified on figure 2017-4 (1.0 X line).

b. With a force less than 1.25 times (1.25 X line) the minimum shear strength requirements (1.0 X line) specified on figure 2017-4 and evidence of adhesion, of the die attach material, less than 50 percent of the die attach area.

c. With a force less than 1.5 times (1.5 X line) the minimum shear strength requirements (1.0 X line) specified on figure 2017-4 and evidence of adhesion, of the die attach material, less than 25 percent of the die attach area.

d. With a force less than 2.0 times (2.0 X line) the minimum shear strength requirements (1.0 X line) specified on figure 2017-4 and evidence of less than 10 percent adhesion of the die attach material.

3.1.2.2 Acceptance criteria. A device will be considered acceptable if the die bond:

a. Does not shear with a force equal to or greater than 2.0 times (2.0 X line) the minimum shear strength requirements (1.0 X line) specified on figure 2017-4.

b. Shears with evidence of remaining semiconductor material equal to or greater than 50 percent of the die attach area regardless of the shearing force applied. (This criteria applicable only for devices with die area less than 25.5×10^{-4} in^2 (1.645 mm^2)).

NOTE: Residual semiconductor material attached in discrete areas of the die attach medium shall be considered as evidence of such adhesion.

3.1.2.3 Separation categories. When specified, the force required to achieve separation and the category of the separation shall be defined as:

a. Shearing of the die with residual silicon remaining.

b. Separation of die from die attach material.

c. Separation of die and die attach material from package.

3.1.3 Summary. The following details shall be specified in the specification sheet.

a. The minimum die attach strength if other that shown on figure 2017-4.

b. Test condition letter.

c. Sample size and accept number.

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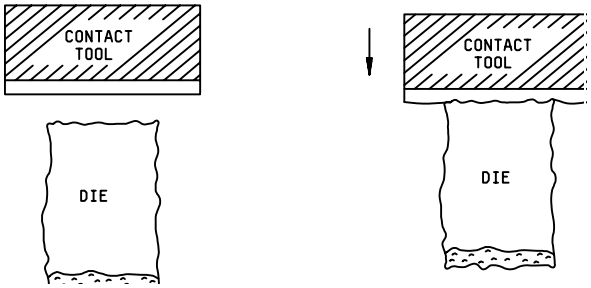

FIGURE 2017-1. Uniform force distribution.

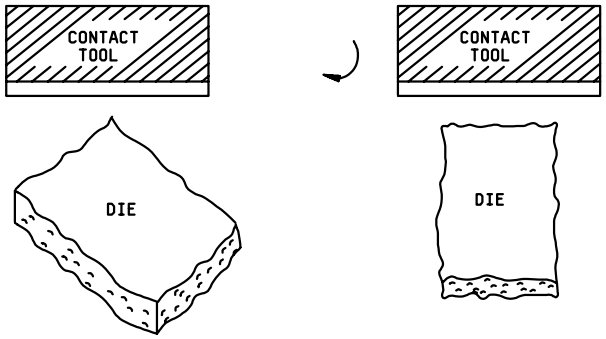

FIGURE 2017-2. Rotational capability.

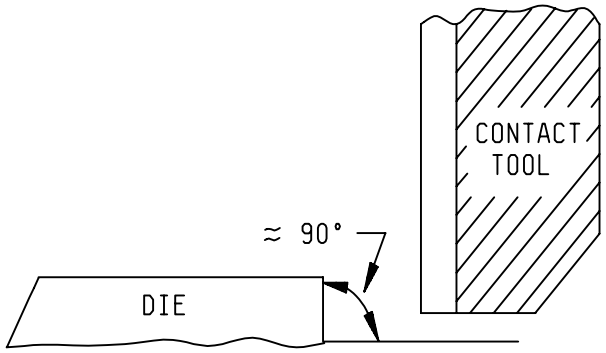

FIGURE 2017-3. Perpendicular force application.

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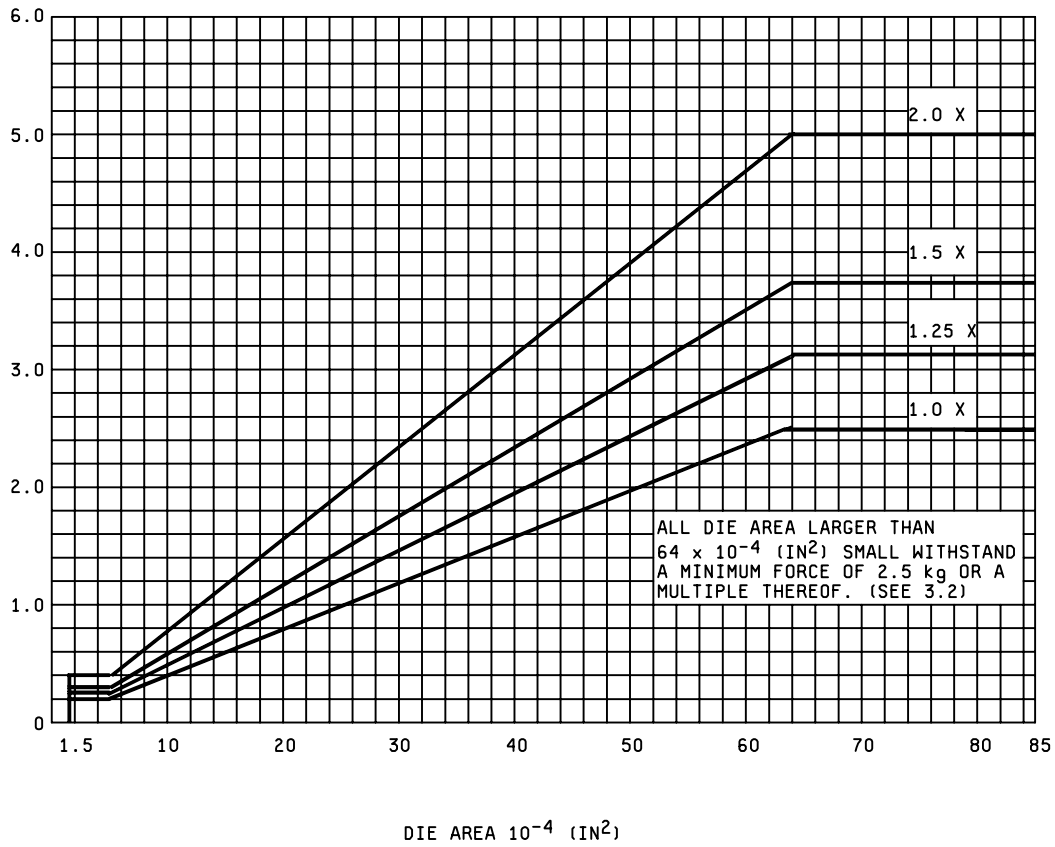

FIGURE 2017-4. Die shear strength criteria (minimum force versus die attach area).

4. Test condition B, mechanical impact. Test condition B may be used on devices which have a metallurgical bond between a header or contact plate and the silicon die on only one side of the die and is to be used for those devices with a contact plate bonded to both sides of the die or to one side of the die with the other side bonded to a header. This method shall not be used for die with area less than .25 square inch (6.35 mm).

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5. Procedure. The die assemblies are placed on a suitable anvil. For die with a contact plate or header on only one side, the die is struck with a ball peen hammer such that the silicon is shattered. The silicon will not be adhered to those areas of the bond where solder, braze, or alloy voids exist and the voids will thus be visible. The contact plate or header can now be visually examined to determine the size and density of any voids. The size and density of the voids are compared to the established visual standards for acceptable die attachment. For die with both sides die attached (a contact plate on both sides or a header on one side and contact plate on the other) the die can be struck with a hammer on one contact plate or cleaved by striking with a chisel on the edge. If cleaved with a chisel, each side should be struck with a hammer to break free any voided silicon. Visual comparison to the standards is then done as above.

5.1 Precautions. The following precautions shall be observed during test:

a. Use of a chisel or hammer can result in flying debris. Eye protection and protective clothing must be worn.

b. Breaking of the silicon can result in the exposure of sharp edges. Care in handling must be taken to avoid injury.

5.2 Failure criteria. A device will be considered a failure if:

a. Any single void has an area greater than 3 percent of the total die area.

b. The sum total of all void areas exceeds 6 percent of the total die area.

6. Summary. The following details shall be specified in the specification sheet.

a. A test condition letter.

b. Sample size for each batch or run.

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METHOD 2026.11

SOLDERABILITY

1. PURPOSE. The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to .125 inch in diameter) that will be assembled using tin lead eutectic solder. This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method which degrades the termination finish to provide a guardband against marginal finishes.

2. PROCEDURE. The solderability test shall be performed in accordance with IPC/EIA J-STD-002 (current revision) Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires" and herein. The following details and exceptions shall apply:

2.1 Contractual Agreements. The contractual agreements statement in J-STD-002 shall not apply. Any exceptions to the requirements specified in J-STD-002 current revision and this test method shall be documented in the individual military procurement document or approved by the procuring military activity.

2.2 Coating Durability. The coating durability category (from J-STD-002 current revision) shall be as follows:

a. Category 2 - For stranded wire (1 hour +/- 5 minutes steam preconditioning with insulation removed).
b. Category 3 - For all other components (8 hours +/- 15 minutes steam preconditioning).

2.3 Test Method. The test method from J-STD-002 (current revision) shall be used as follows:

Test A - For through hole mount and surface mount leaded components, solid wire less than 0.045 inch diameter and stranded wire 18 AWG or smaller. If not otherwise specified in the procurement document, angle of immersion for surface mount leaded components shall be 90 degrees.

Test B - For surface mount leadless components.

Test C - For lugs, tabs, terminals, solid wire greater than 0.045 inch diameter and stranded wire greater than 18 AWG.

3. SUMMARY. The following details shall be specified in the applicable procurement document.

a. Depth of immersion if other than specified.
b. Angle of immersion for surface mount leaded components, if other than 90 degrees.
c. Measurements after test, where applicable.

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METHOD 2031.3

RESISTANCE TO SOLDERING HEAT

1. Purpose. This test method is performed to determine whether wire and other component parts can withstand the effects of the heat to which they will be subjected during the soldering process (solder iron, solder dip, solder wave, or solder reflow). The heat can be either conducted heat through the termination into the component part or radiant heat from the solder bath when in close proximity to the body of the component part, or both. The solder dip method is used as a reasonably close simulation of the conditions encountered in wave soldering, in regard to radiated and conducted heat. This test also is intended to evaluate the impact of reflow techniques to which components may be exposed. The heat of soldering can cause solder reflow which may affect the electrical characteristics of the component part and may cause mechanical damage to the materials making up the part, such as loosening of terminations or windings, softening of insulation, opening of solder seals, and weakening of mechanical joints.

1.1 Scope. This test method is intended to confirm that semiconductor components are capable of withstanding the elevated temperatures and thermal shocks associated with hot solder attachment. It is not intended to evaluate conformal coating, printed circuit designs, poor thermal expansion matching, and mistreatment due to improper pre-heat or automation tools.

This test method does not require the supplier to buy the same processing equipment as employed by the user. The equipment and procedures listed herein are to serve as a guide with the supplier having the option, with DSCC approval, of substituting soldering heat tests using equivalent equipment that is capable of meeting the intent of this method with techniques that apply equal or better soldering tests.

Semiconductors will be tested to the solder attach procedures that are applicable to the package design. For example, many surface mount packages have their solder pads hidden when mounted so the soldering iron test is not appropriate. In addition, a soldering iron shall never be applied to the top of a surface mount package in an attempt to achieve a “sweat” solder bond. Permanent damage will result.

2. Apparatus.

2.1 Solder pot. A static solder pot, of sufficient size to accommodate the mounting board (see 2.4) and to immerse the terminations to the depth specified for the solder dip (without touching the bottom of the pot), shall be used. This apparatus shall be capable of maintaining the solder at the temperature specified. The solder bath temperature shall be measured in the center of the pot at a depth of at least .500 inch (12.7 mm), but no deeper than 1 inch (25.4 mm) below the surface of the solder.

2.2 Heat sinks or shielding. The use of heat sinks or shielding is prohibited except when it is a part of the component. When applicable, heat sinks or shielding shall be specified in the individual specification, including all of the details, such as materials, dimensions, method of attachment, and location of the necessary protection.

2.3 Fixtures. Fixtures, when required, shall be made of a non-solderable material designed so that they will make minimum contact (i.e., minimum heat sink) with the component. Further, they shall not place undue stress on the component when fixtured.

2.4 Mounting board. A mounting board, in accordance with NEMA grade FR-4 of IPC-4101, 9 square inches (i.e., 3 x 3, 1 x 9.), minimum area, .062 inch ±.0075 inch (1.57 mm ±.191 mm) thick, shall be used, unless otherwise specified. Component lead holes shall be drilled such that the diametrical clearance between the hole and component terminals shall not exceed .015 inch (0.38 mm). Metal eyelets or feed-throughs shall not be used. Surface mount boards, when specified in the individual specification, shall have pads of sufficient size and number to accommodate the component being tested.

2.5 Solder iron. A solder iron, capable of maintaining a temperature of 350°C ±10°C, shall be used.

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2.6 Reflow chambers. The reflow chambers or equivalent (vapor phase reflow (VPR) chamber, infrared reflow (IRR) oven, air circulating oven.) shall be of sufficient size to accommodate the mounting board and components to be tested. The chamber shall be capable of generating the specified heating rate, temperatures, and environments.

2.7 Temperature measurement. Low mass thermocouples that do not affect the heating rate of the sample shall be used. A temperature recording device is recommended. The equipment shall be capable of maintaining an accuracy of ±1°C at the temperature range of interest.

3. Materials.

3.1 Solder. The solder or solder paste shall be tin-lead alloy with a nominal tin content of 50 percent to 70 percent in accordance with ANSI/J-STD-006, “Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications” or ANSI/J-STD-005, “Requirements for Soldering Pastes”. When specified in the individual specification, other solders can be used provided they are molten at the specified temperature.

3.2 Flux. When flux is used, it shall conform to type A of ANSI/J-STD-004, “Requirements for Soldering Fluxes”, or as specified in the individual specification.

3.3 VPR fluid. A perfluorocarbon fluid that has a boiling point of 215°C shall be used.

4. Procedure.

4.1 Special preparation of specimens. Any special preparation of specimens prior to testing shall be as specified in the individual specification. This could include specific instructions such as bending or any other relocation of terminations, cleaning, application of flux, pretinning, or attachment of heat sinks or protective shielding (see 2.2), prior to the solder immersion.

4.2 Preparation of solder bath. The molten solder shall be agitated to assure that the temperature is uniform. The surface of the solder shall be kept clean and bright.

4.3 Application of flux. When flux is used, the terminations to be tested shall be immersed in the flux (see 3.2), which is at room ambient temperature, to the depth specified for the solder dip. The duration of the immersion shall be from 5 seconds to 10 seconds.

4.4 Test conditions. Unless otherwise specified in the individual specification, the test shall be performed on all solder terminations attached to the component part. There are six types of soldering techniques covered by these test conditions. The test conditions are outlined below and in table 2031-I.

Test condition A:	Solder iron - Hand soldering of solder cups, through hole components, tab and post terminations, solder eyelet terminations.
Test condition B:	Solder dip - Simulates hot solder dipping (tinning) of leaded components.
Test condition C:	Wave solder - Simulates wave solder of topside board mount product.
Test condition D:	Wave solder - Simulates wave solder of bottom side board mount product.
Test condition H:	VPR - VPR environment without preheat.
Test conditions I, J, K:	Infrared/convection reflow - Simulates IRR, natural convection, and forced air convection reflow environments.

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4.4.1 Test condition A: Solder iron.

a. When testing a solder cup, tab and post termination, or solder eyelet termination, the applicable wire size, properly prepared for the solder termination, shall be attached in the appropriate manner.

When testing a board mount component, the component shall be placed on a mounting board (see 2.4).

b. When specified, the components shall be fluxed (see 4.3).

c. Unless otherwise specified, a solder iron in accordance with 2.5 shall be used.

d. The solder iron shall be heated to 350°C ±10°C and applied to the termination for a duration of 4 seconds to 5 seconds as specified in table 2031-I. The solder and iron shall be applied to the area of the assembly closest to the component body that the product is likely to experience. For surface mount components, the iron shall be placed on the pad only.

e. Remove the iron and allow the component to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

The component shall be visually examined under 10X magnification.

4.4.2 Test condition B: Solder dip.

a. Place the component in an appropriate fixture (see 2.3).

b. When specified, the leads shall be fluxed (see 4.3).

c. The specific combination of temperature, immersion and emersion rate, immersion duration, and number of heats shall be as specified in table 2031-I. Unless otherwise specified, terminations shall be immersed to within .050 inch (1.27 mm) of the component body. Terminations shall be immersed simultaneously, if the geometry of the component permits.

d. After the solder dip, the component shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

e. The component shall be visually examined under 10X magnification.

4.4.3 Test condition C: Wave solder - topside board mount component.

a. The component under test shall be mounted on a mounting board (see 2.4).

Wire leads: Wire leads shall be brought through the board holes and bent at least 30 degrees from a line perpendicular to the board. Leads shall extend from .050 inch to .100 inch (1.27 mm to 2.54 mm) from the bottom of the board. Axial leads shall be bent at a 90 degree angle at a point between .06 inch and .08 inch (1.5 mm and 2.1 mm) from the body, eyelet fillet, or weld unless otherwise specified.

Pin leads: Where the component is designed with rigid pin leads, the full length of the termination shall be retained. Pin leads shall not be cut or bent.

b. When specified, the leads shall be fluxed (see 4.3).

c. The specific combination of temperature, duration, and number of heats shall be as specified in table 2031-I.

d. The components, mounted on the board, shall be immersed in the solder pot so that the bottom of the board floats on the molten solder.

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e. After the float, the components shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the components shall be cleaned using an appropriate cleaning solution.

f. The components shall be visually examined under 10X magnification.

4.4.4 Test condition D: Wave solder – bottom side board mount product.

a. Place the component in an appropriate fixture (see 2.3).

b. When specified, the terminations shall be fluxed (see 4.3).

c. The specific combination of temperature, preheat conditions, immersion and emersion rates, immersion duration, and number of heats shall be as specified in table 2031-I.

d. The component shall be preheated and fully immersed in the solder bath in accordance with 4.4.4c.

e. After the immersion, the component shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

f. The component shall be visually examined under 10X magnification.

4.4.5 Test condition H: Vapor phase reflow soldering.

a. Components shall be mounted on a mounting board (see 2.4). Through-hole mounted components shall have their terminals inserted into the termination holes. Surface mount components shall be placed on top of the board.

b. A test chamber (see 2.6) shall be used which is large enough to suspend the mounting board without touching the sides or the solution. The VPR fluid shall be placed in the test chamber and shall be heated until it is boiling. The solution shall be allowed to boil for 5 minutes prior to suspending the mounting board.

c. The specific combination of temperature, duration of exposure, and number of heats shall be as specified in table 2031-I.

d. After chamber equalization, the mounting board shall be suspended into the vapor in a horizontal plane. The mounting board shall not touch the solution.

e. After the heat, the components shall be allowed to cool and stabilize at room ambient conditions. If a solder paste was used, the component shall be cleaned using an appropriate solution.

f. The components shall be visually examined under 10X magnification.

4.4.6 Test conditions I, J, K: Infared/convection reflow soldering.

a. Components shall be mounted on a mounting board (see 2.4). Through-hole mounted components shall have their terminals inserted into the termination holes. Surface mount components shall be placed on top of the board.

b. A test chamber as specified in 2.6 shall be used.

c. A low mass thermocouple shall be attached tightly to the component at an appropriate position away from the edges.

d. The specific combination of temperature, preheat, duration, and number of heats shall be as specified by test condition I, J, or K in table 2031-I and the individual procurement document.

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e. The board shall be placed into the test chamber and the temperature of the component ramped at a rate of 1°C/s to 4°C/s as measured by the thermocouple. The assembly shall be above 183°C for 90 seconds to 120 seconds and held at the final temperature and time designated by the test condition. The assembly shall then be allowed to cool to room ambient temperature. This constitutes one heat cycle. The assembly shall be exposed to three heat cycles.

f. The components shall be visually examined under 10X magnification.

5. Examinations and measurements. Examinations and measurements to be made before and after the test, as applicable, shall be as specified in the individual specification. After the procedure, the specimens shall be allowed to cool and stabilize at room ambient conditions, for the time specified in the individual specification.

5.1 Internal examination. When specified, internal examination of the part shall be made after the test to check for solder reflow or heat damage.

6. Summary. The following details are to be specified in the performance specification sheet:

a. The use of heat sinks or shielding is prohibited except when they are part of the component (see 2.2).

b. Mounting board, if different from that specified (see 2.4).

c. Solder, if different from that specified (see 3.1).

d. Flux, if applicable and if different from that specified (see 3.2, 4.1, and 4.3).

e. Solder terminations that are not to be tested, if applicable (see 4.4).

f. Special preparation of specimens if applicable (see 4.1).

g. Depth of immersion in the molten solder, if different from that specified (see 4.4.2).

h. Test condition letter (see 4.4).

i. Cooling time prior to final examinations and measurements (see 4.4 and 5.).

j. Examinations and measurements before and after test, as applicable (see 5.).

k. Method of internal inspection, if required (see 5.1).

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TABLE 2031-I. Test conditions.

Solder technique simulation	Test condition	Temperature (°C)	Time (s)	Temperature ramp/ immersion and emersion rate	Number of heat cycles
Solder iron	A	350 ±10 (solder iron temp)	4 - 5		1
Dip	B	260 ±5 (solder temp)	10 ±1	25mm/s ±6 mm/s	1
Wave: Topside board-mount product	C	260 ±5 (solder temp)	20 ±1		1
Wave: Bottomside board-mount product	D	260 ±5 (solder temp)	10 ±1	Preheat 1°C/s-4°C/s to within 100°C of solder temp. 25 mm/s ± 6 mm/s	1
Vapor phase reflow	H	215 ±5 (vapor temp)	60 ±5		1
IR/convection reflow	I	215 ±5 (component temp)	30 ±5	1°C/s-4°C/s; time above 183°C, 90 s - 120 s	3
	J	235 ±5 (component temp)	30 ±5	1°C/s-4°C/s; time above 183°C, 90 s - 120 s	3
	K	250 ±5 (component temp)	30 ±5	1°C/s-4°C/s; time above 183°C, 90 s - 120 s	3

Test condition codes E, F, and G have not been used in this method.

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METHOD 2036.4

TERMINAL STRENGTH

1. Test condition A, tension.

1.1. Purpose. This test method is designed to check the capabilities of the device leads, welds and seals to withstand a straight pull.

1.2. Apparatus. The tension test requires suitable clamps, vise, and hand vise for securing the device and for securing the specified weight to the device lead without lead restriction.

1.3. Procedure. The specified weight shall be applied, without shock, to each lead or terminal. The case of the device shall be held in a fixed position. When testing axial lead devices, the device shall be supported, with the leads in a vertical position, by securing one lead to a clamp or vise. With a hand vise or equivalent, the specified weight, including the attaching device, shall be fastened to the lower lead for the time specified. Each lead shall be fastened as close to its end as practicable. When examined using 10X magnification after removal of the stress, any evidence of breakage (other than meniscus), loosening, or relative motion between the terminal lead and the device body shall be considered a device failure.

1.4. Summary. The following shall be specified in the performance specification sheet

a. Weight to be attached to lead (see 1.3).

b. Length of time weight is to be attached (see 1.3).

c. Measurements to be made after this test.

2. Test condition D1, lead or terminal torque.

2.1. Purpose. This test is designed to check device leads and seals for their resistance to twisting motions.

2.2. Apparatus. The torque test requires suitable clamps and fixtures and a torsion wrench or other suitable method of applying the specified torque without lead restriction.

2.3. Procedure. The body of the device shall be securely clamped, with a suitable fixture, and the specified torque shall be applied to the portion of the terminal nearest the seal for the specified time. The specified torque shall be applied, without shock, about the device axis. The torque shall be applied between the lead or terminal and the case in a direction which tends to cause loosening of the lead or terminal.

2.3.1 UHF and microwave diodes. Unless otherwise specified, a torque of 1.5 pound-inches (.17 newton-meter) about the diode axis shall be applied for the specified time, without shock, between the terminals, and in a direction which tends to cause loosening of the terminals. The manufacturer's recommendation shall be allowed in the method clamping.

2.3.2 Examination under magnification. When examined using 10X magnification after removal of the stress, any evidence of breakage (other than meniscus), loosening, or relative motion between the terminal lead and the device body shall be considered a device failure.

2.4. Summary. The following conditions shall be specified in the performance specification sheet

a. The amount of torque to be applied (see 2.3.1).

b. Length of time torque is to be applied (see 2.3.1).

c. Measurements to be made after test.

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3. Test condition D2, stud torque.

3.1. Purpose. This test is designed to check the resistance of the device with threaded mounting stud to the stress caused by tightening the device when mounting.

3.2. Apparatus. The torque test requires suitable clamps and fixtures and a torsion wrench or suitable method of applying the specified torque.

3.3. Procedure. The device shall be clamped by its body or flange. A flat steel washer of a thickness equal to 6-thread pitches of the stud being tested and a class 2 fit steel nut shall be assembled in that order on the stud, with all parts clean and dry. The specified torque shall be applied for the specified length of time without shock to the nut. The nut and washer shall then be disassembled from the device, and the device then examined for compliance with the requirements.

3.3.1 Failure. The device shall be considered a failure if:

a. The stud breaks.

b. The stud exhibits elongation greater than one-half of one-thread pitch.

c. The device exhibits obvious visual mechanical deformations, such as:

(1) stripping of threads,

(2) deformation of mounting seat, and

(3) bending of stud.

d. It fails the specified post-test and point measurements.

3.4. Summary. The following conditions shall be specified in the performance specification sheet

a. The amount of torque to be applied (see 3.3).

b. Length of time torque is to be applied (see 3.3).

c. Measurements to be made after test.

4. TEST CONDITION E, LEAD FATIGUE

4.1. Purpose. This test is to check the resistance of the device leads to metal fatigue.

4.2. Apparatus. The lead-fatigue test shall be made using the specified weight and with suitable clamping or attaching devices.

4.3. Procedure. Where applicable, two leads on each device shall be tested. The leads shall be selected in a cyclical manner (regular recurring), when applicable; that is, leads number 1 and 2 on the first device, number 2 and 3 on the second device. Unless otherwise specified, a weight of 8 ±0.5 ounces (225 ±15 grams) shall be applied to each lead for three 90 ±5 degrees arcs of the case. An arc is defined as the movement of the case, without torsion, to a position perpendicular to the pull axis and return to normal. All arcs on a single lead shall be made in the same direction and in the same plane without lead restriction. One bending cycle shall be completed in from 2 to 5 seconds. Any glass fracture (other than meniscus) or broken lead shall be considered a failure.

4.4. Summary. The following conditions shall be specified in the performance specification sheet

a. Weight to be attached to the lead, if other than 8 ±0.5 ounces (225 ±15 grams) (see 4.3.).

b. Number of arcs, if other than three (see 4.3.).

c. Measurements to be made after this test.

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5. TEST CONDITION F, BENDING STRESS.

5.1. Purpose. This test is made to check the quality of the leads, lead welds, and glass-to-metal seals of the devices.

5.2. Apparatus. Bending-stress tests shall be made using attaching devices, such as suitable clamps or other supports for stud-mounted devices.

5.3. Procedure.

5.3.1 Method A (for cylindrical devices). With one contact of the device held in a suitable clamp, the specified force shall be applied, without shock, at right angles to the reference axis of the device, as near the top of the opposite contact or tubulation as practicable.

5.3.2 Method B (for stud-mounted devices). The device shall be securely fastened, with its reference axis in a horizontal position, by screwing the stud into a suitable support. With a hand vise, or equivalent, the specified weight shall be suspended from the hold in the lug for the length of time specified.

5.3.3 Failure criteria. When examined using 10X magnification after removal of the stress, any evidence of breakage (other than meniscus), loosening, or relative motion between the terminal lead and the device body shall be considered a failure.

5.4. Summary. The following conditions shall be specified in the performance specification sheet

a. Special preparations or conditions, if required.

b. Weight to be attached to lead (see 5.3.).

c. Test method (see 5.3.1 and 5.3.2).

d. Length of time weight is applied.

e. Measurements to be made after test.

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METHOD 2037.1

BOND STRENGTH (DESTRUCTIVE BOND PULL TEST)

1. Purpose. The purpose of this test method is to measure bond strengths, evaluate bond strength distributions, or determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermocompression, ultrasonic, or related techniques. It may also be applied to bonds external to the device such as those from device terminals-to-substrate or wiring board or to internal bonds between die and substrate in non-wire-bonded device configurations such as beam lead or flip chip devices.

2. Apparatus. The apparatus for this test shall consist of suitable equipment for applying the specified stress to the bond, lead wire, or terminal as required in the specified test condition. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ±5 percent or ±0.25 gf, whichever is the greater tolerance.

3. Procedure. The test shall be conducted using the test condition specified in the applicable acquisition document consistent with the particular device construction. All bond pulls shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. Unless otherwise specified, for conditions A, C, and D of table 2037 - I, the sample size number specified for the bond strength test shall determine the minimum sample size in terms of the minimum number of bond pulls to be accomplished rather than the number of complete devices in the sample, except that the required number of bond pulls shall be randomly selected from a minimum of 4 devices. Bond pulls in accordance with test conditions D, F, G, and H of table 2037 - I, while involving two or more bonds, shall count as a single pull for bond strength and sample size number purposes. Unless otherwise specified, for conditions F, G, and H, the sample size number specified shall determine the number of die to be tested (not bonds). For multichip devices (all conditions), a minimum of 4, die or use all die if four are not available, on a minimum of 2 completed devices shall be used. Where there is any adhesive, encapsulant, or other material under, on, or surrounding the die such as to increase the apparent bond strength, the bond strength test shall be performed prior to application.

When flip chip or beam-lead chips are bonded to substrates other than those in completed devices, the following conditions shall apply:

a. The sample of chips for this test shall be taken at random from the same chip population as that used in the completed devices that they are intended to represent.

b. The chips for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.

c. The test chip substrates shall be processed, metallized, and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1 Test conditions.

3.1.1 Test condition A - bond peel. This test is normally employed for bonds external to the device package. The lead or terminal and the device package shall be gripped or clamped in such a manner that a peeling stress is exerted with the specified angle between the lead or terminal and the board or substrate. Unless otherwise specified, an angle of 90 degrees shall be used. When a failure occurs, the force causing the failure and the failure category shall be recorded.

3.1.2 Test condition C - wire pull (single bond). This test is normally employed for internal bonds at the die or substrate and the lead frame of microelectronic devices. The wire connecting the die or substrate shall be cut so as to provide two ends accessible for pull test. In the case of short wire runs, it may be necessary to cut the wire close to one termination in order to allow pull test at the opposite termination. The wire shall be gripped in a suitable device and simple pulling action applied to the wire or to the device (with the wire clamped) in such a manner that the force is applied approximately normal to the surface of the die or substrate. When a failure occurs, the force causing the failure and the failure category shall be recorded.

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3.1.3 Test condition D - wire pull (double bond). This procedure is identical to that of test condition C, except that the pull is applied by inserting a hook under the lead wire (attached to die, substrate or header or both ends) with the device clamped and the pulling force applied approximately in the center of the wire in a direction approximately normal to the die or substrate surface or approximately normal to a straight line between the bonds. When a failure occurs, the force causing the failure, and the failure category, shall be recorded. The minimum bond strength shall be taken from table 2037 - I. Figure 20371 - 1 may be used for wire diameters not specified in table 2037 -I. For wire diameter or equivalent cross section >0.005 inch (0.127 mm), where a hook will not fit under the wire, a suitable clamp can be used in lieu of a hook.

3.1.4 Test condition F - bond shear (flip chip). This test is normally employed for internal bonds between a semiconductor die and a substrate to which it is attached in a face-bonded configuration. It may also be used to test the bonds between a substrate and an intermediate carrier or secondary substrate to which the die is mounted. A suitable tool or wedge shall be brought in contact with the die (or carrier) at a point just above the primary substrate and a force applied perpendicular to one edge of the die (or carrier) and parallel to the primary substrate, to cause bond failure by shear. When a failure occurs, the force at the time of failure, and the failure category, shall be recorded.

3.1.5 Test condition G - push-off test (beam lead). This test is normally employed for process control and is used on a sample of semiconductor die bonded to a specially prepared substrate. Therefore, it shall not be used for random sampling of production or inspection lots. A metallized substrate containing a hole shall be employed. The hole appropriately centered, shall be sufficiently large to provide clearance for a push tool, but not large enough to interfere with the bonding areas. The push tool shall be sufficiently large to minimize device cracking during testing, but not large enough to contact the beam leads in the anchor bond area. Proceed with push-off tests as follows: The substrate shall be rigidly held and the push tool inserted through the hole. The contact of the push tool to the silicon device shall be made without appreciable impact (less than 0.01 inch/minute (0.254 mm/minute) and forced against the underside of the bonded device at a constant rate. When failure occurs, the force at the time of failure, and the failure category, shall be recorded.

3.1.6 Test condition H - pull-off test (beam lead). This test is normally employed on a sample basis on beam lead devices which have been bonded down on a ceramic or other suitable substrate. The calibrated pull-off apparatus (see 2) shall include a pull-off rod (i.e., a current loop of nichrome or Kovar wire) to make connection with a hard setting adhesive material (i.e., heat sensitive polyvinyl acetate resin glue) on the back (top side) of the beam lead die. The substrate shall be rigidly installed in the pull-off fixture and the pull-off rod shall make firm mechanical connection to the adhesive material. The device shall be pulled within 5 degrees of the normal to at least the calculated force (see 3.2), or until the die is at .10 inch(2.54 mm) above the substrate. When a failure occurs, the force at the time of failure, the calculated force limit, and the failure category shall be recorded.

3.2 Failure criteria. Any bond pull which results in separation under an applied stress less than that indicated in table 2037 -I as the required minimum bond strength for the indicated test condition, composition, and construction shall constitute a failure.

3.2.1 Failure category. Failure categories are as follows: When specified, the stress required to achieve separation and the category of separation or failure shall be recorded.

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a. For internal wire bonds:

(a-1) Wire break at neckdown point (reduction of cross section due to bonding process).

(a-2) Wire break at point other than neckdown.

(a-3) Failure in bond (interface between wire and metallization) at die.

(a-4) Failure in bond (interface between wire and metallization) at substrate, package post, or other than die.

(a-5) Lifted metallization from die.

(a-6) Lifted metallization from substrate or package post.

(a-7) Fracture of die.

(a-8) Fracture of substrate.

b. For external bonds connecting device to wiring board or substrate:

(b-1) Lead or terminal break at deformation point (weld affected region).

(b-2) Lead or terminal break at point not affected by bonding process.

(b-3) Failure in bond interface (in solder or at point of weld interface between lead or terminal and the board or substrate conductor to which the bond was made).

(b-4) Conductor lifted from board or substrate.

(b-5) Fracture within board or substrate.

c. For flip-chip configurations:

(c-1) Failure in the bond material or pedestal, if applicable.

(c-2) Fracture of die (or carrier) or substrate (removal of portion of die or substrate immediately under the bond).

(c-3) Lifted metallization (separation of metallization or bonding pedestal from die (or carrier) or substrate.

d. For beam lead devices:

(d-1) Silicon broken.

(d-2) Beam lifting on silicon.

(d-3) Beam broken at bond.

(d-4) Beam broken at edge of silicon.

(d-5) Beam broken between bond and edge of silicon.

(d-6) Bond lifted.

(d-7) Lifted metallization (separation of metallization) from die, separation of bonding pad.

(d-8) Lifted metallization.

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NOTE: RF/microwave that require extremely flat loops, which may cause erroneous wire pull data, may use the following formula to determine the proper wire pull value.

$$V_1 = V_2 \sin \theta$$

Where: V_1 = New value to pull test.
V_2 = Table I value for size wire tested.
θ = Greatest calculated wire loop angle (figure 2037-2).

Also, RF/microwave that contain wires that cannot be accessed with a pull hook must be duplicated on a test coupon in such a way to allow hook access for purposes of pull testing. These wires are to be bonded at the same time the production devices are bonded using the same setup, operator, and schedule. The test wires are to be pull tested in lieu of the tuning or inaccessible wires on the production devices. Failures on the test coupon shall be considered as failures to production units and appropriate action is to be taken in accordance with the applicable specification (figure 2037-3).

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TABLE 2037 - I. Minimum bond strength.

Test condition	Wire composition and diameter 1/	Construction 2/	Minimum bond strength (grams force)	
			Pre-seal	Post-seal and any other processing and screening when applicable
A	---	---	Given in applicable document	Given in applicable document
C or D	AL .0007 inch (0.0178 mm) AU .0007 inch (0.0178 mm)	Wire	1.5 2.0	1.0 1.5
C or D	AL .0010 inch (0.0254 mm) AU .0010 inch (0.0254 mm)	Wire	2.5 3.0	1.5 2.5
C or D	AL .00125 inch (0.0318 mm) AU .00125 inch (0.0318 mm)	Wire	Same bond strength limits as the .0013 inch (0.033 mm) wire	
C or D	AL .0013 inch (0.033 mm) AU .0013 inch (0.033 mm)	Wire	3.0 4.0	2.0 3.0
C or D	AL .0015 inch (0.0381 mm) AU .0015 inch (0.0381 mm)	Wire	4.0 5.0	2.5 4.0
C or D	AL .0030 inch (0.0762 mm) AU .0030 inch (0.0762 mm)	Wire	12.0 15.0	8.0 12.0
F	Any	Flip-clip	5 grams-force x number of bonds (bumps)	
G or H	Any	Beam lead	30 grams force in accordance with linear millimeter of nominal undeformed (before bonding) beam width. 3/	

1/ For wire diameters not specified, use the curve of figure 2037-1 to determine the bond pull limit.
2/ For ribbon wire, use the equivalent round wire diameter which gives the same cross-sectional area as the ribbon wire being tested.
3/ For condition G or H, the bond strength shall be determined by dividing the breaking force by the total of the nominal beam widths before bonding.

4. Summary. The following details shall be specified in the applicable specification sheet:

a. Test condition letter (see 3).

b. Minimum bond strength if other than specified in 3.2 or details of required strength distributions if applicable.

c. Sample size number and accept number or number, and selection of bond pulls, to be tested on each device, and number of devices, if other than 4.

d. For test condition A, angle of bond peel if other than 90 degrees, and bond strength limit (see 3.2).

e. Requirement for reporting of separation forces and failure categories, when applicable (see 3.2.1).

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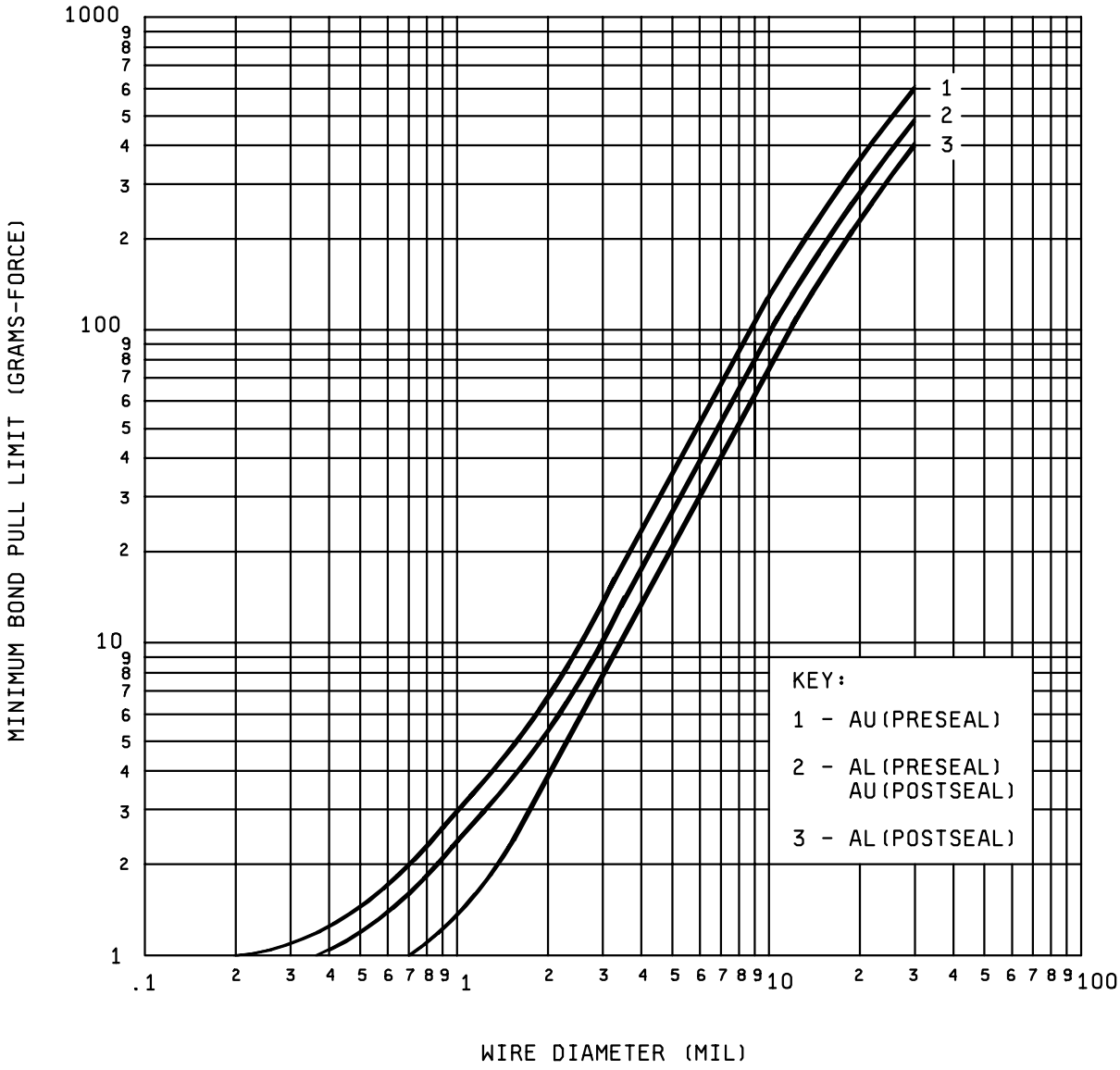

NOTE: The minimum bond strength should be taken from table 2037 - I. Figure 2037 – 1 may be used for wire diameters not specified in table 2037 - I.

FIGURE 2037 - 1 Minimum bond pull limits.

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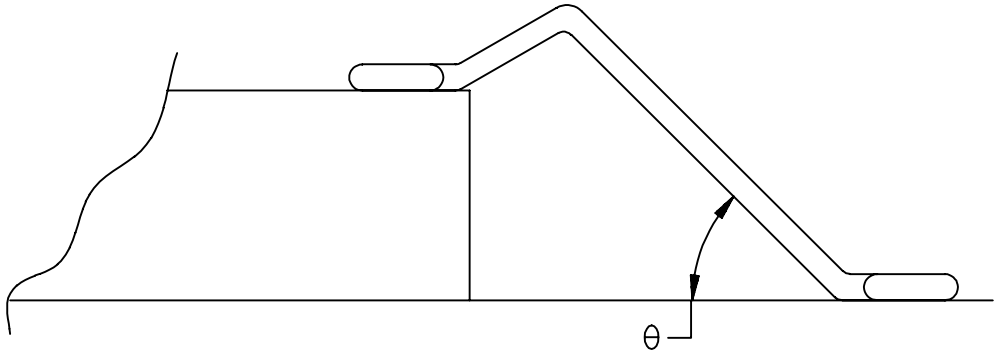

FIGURE 2037-2 Wire loop angle.

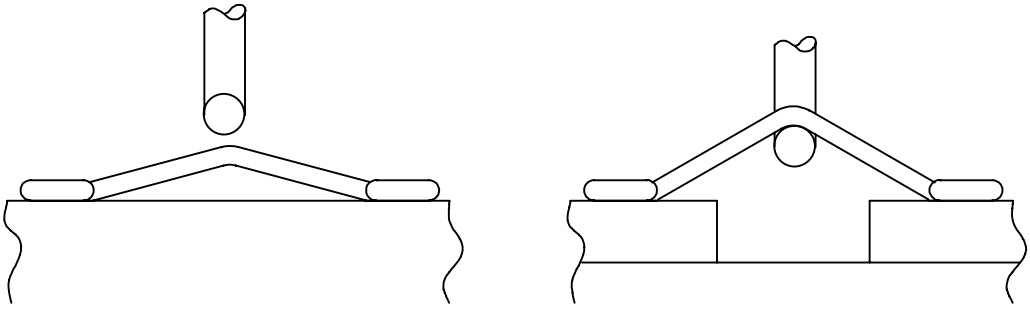

FIGURE 2037-3 Flat loop wire pull testing.

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METHOD 2046.2

VIBRATION FATIGUE

1. Purpose. The purpose of this test method is to determine the effect on the device of vibration in the frequency range specified.

2. Procedure. The device shall be rigidly fastened on the vibration platform and the leads or cables adequately secured. The device shall then be subjected to a sample harmonic motion in the range of 60 ±20 Hz, with a constant peak acceleration of 20 g minimum. The vibration shall be applied for 32 ±8 hours, minimum, in each of the orientations X, Y, and Z for a total of 96 hours, minimum.

3. Summary. The measurements after test shall be specified in the specification sheet.

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METHOD 2051.1

VIBRATION NOISE

1. Purpose. The purpose of this test method is to measure the amount of electrical noise produced by the device under vibration.

2. Procedure. The device and its leads shall be rigidly fastened on the vibration platform and the leads or cables adequately secured. The device shall be vibrated with simple harmonic motion with a constant peak acceleration of 20 g minimum. The vibration frequency shall be varied approximately logarithmically between 100 and 2,000 Hz. The entire frequency range shall be traversed is not less than four minutes for each cycle. This cycle shall be performed once in each of the orientations X_1, Y_1, and Z_1 (total of 3 times), so that the motion shall be applied for a total period of approximately 12 minutes. The specified voltages and currents shall be applied in the test circuit. The maximum noise-output voltage across the specified load resistance during traverse shall be measured with an average-responding root-means-square (rms) calibrated high impedance voltmeter. The meter shall measure, with an error of not more than 3 percent, the rms value of a sine-wave voltage at 2,000 Hz. The characteristic of the meter over a bandwidth of 20 to 20,000 Hz shall be ±1 decibel (dB) of the value at 2,000 Hz, with an attenuation rate below 20 and above 20,000 Hz of 6 ±2 dB per octave. The maximum inherent noise in the circuit shall be at least 10 dB, below the specified noise-output voltage.

3. Summary. The following conditions shall be specified in the specification sheet:

   a. Test voltages and currents (see 2.).

   b. Load resistance (see 2.).

   c. Post-test measurements.

   d. Noise-output voltage limit.

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METHOD 2052.4

PARTICLE IMPACT NOISE DETECTION (PIND) TEST

1. Purpose. The purpose of this test method is to detect loose particles inside a device cavity. The test provides a nondestructive means of identifying those devices containing particles of sufficient mass that, upon impact with the case, excite the transducer.

2. Apparatus. The equipment required for the PIND test shall consist of the following (or equivalent):

a. A threshold detector to detect particle noise voltage exceeding a preset threshold of the absolute value of 15 ±1 mV peak reference to system ground.

b. A vibration shaker and driver assembly capable of providing essentially sinusoidal motion to the device under test (DUT) at:

(1) Condition A: 20 g's peak at 40 to 250 Hz.

(2) Condition B: 10 g's peak at 60 Hz minimum.

c. PIND transducer, calibrated to a peak sensitivity of -77.5 ±3 dB in regards to one volt per microbar at a point within the frequency of 150 to 160 kHz.

d. A sensitivity test unit (STU) (see figure 2052-1) for periodic assessment of the PIND system performance. The STU shall consist of a transducer with the same tolerances as the PIND transducer and a circuit to excite the transducer with a 250 microvolt ±20 percent pulse. The STU shall produce a pulse of about 20 mV peak on the oscilloscope when the transducer is coupled to the PIND transducer with attachment medium.

e. PIND electronics, consisting of an amplifier with a gain of 60 ±2 dB centered at the frequency of peak sensitivity of the PIND transducer. The noise at the output of the amplifier shall not exceed 10 mV peak.

f. Attachment medium. The attachment medium used to attach the DUT to the PIND transducer shall be the same attachment medium as used for the STU test.

g. Shock mechanism or tool capable of imparting shock pulses of 1,000 ±200 g's peak to the DUT. The duration of the main shock shall not exceed 100 μs. If an integral co-test shock system is used, the shaker vibration may be interrupted or perturbed for period of time not to exceed 250 ms from initiation of the last shock pulse in the sequence. The co-test duration shall be measured at the 50 ±5 percent point.

3. Procedures.

3.1 Test equipment setup. Shaker drive frequency and amplitude shall be adjusted to the specified conditions. The shock pulse shall be adjusted to provide 1,000 ±200 g's peak to the DUT.

3.2 Test equipment checkout. The test equipment checkout shall be performed a minimum of one time per operation shift. Failure of the system to meet checkout requirements shall require retest of all devices tested subsequent to the last successful system checkout.

3.2.1 Shaker drive system checkout. The drive system shall achieve the shaker frequency and the shaker amplitude specified. The drive system shall be calibrated so that the frequency settings are within ±8 percent and the amplitude vibration settings are within ±10 percent of the nominal values. If a visual displacement monitor is affixed to the transducer, it may be used for amplitudes between .04 and .12 inch (1.02 and 3.05 mm). An accelerometer may be used over the entire range of amplitudes and shall be used below amplitudes of .040 inch (1.02 mm).

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3.2.2 Detection system checkout. With the shaker de-energized, the STU transducer shall be mounted face-to-face and coaxial with the PIND transducer using the attachment medium used for testing the devices, prior to attaching any special fixtures. The STU shall be activated several times to verify low level signal pulse visual and threshold detection on the oscilloscope. Not every application of the STU will produce the required amplitude. All pulses which are greater than 20 mV shall activate the detector.

3.2.3 System noise verification. System noise will appear as a fairly constant band and shall not exceed 20 mV peak to peak when observed for a period of 30 to 60 seconds.

3.3 Test sequence. The following sequence of operations (3.3.a through 3.3.i) constitute one test cycle or run.

a. Three pre-test shocks.

b. Vibration 3 ±1 seconds.

c. Three co-test shocks.

d. Vibration 3 ±1 seconds.

e. Three co-test shocks.

f. Vibration 3 ±1 seconds.

g. Three co-test shocks.

h. Vibration 3 ±1 seconds.

i. Accept or reject.

3.3.1 Mounting requirements. Special precautions (e.g., in mounting, grounding of DUT leads, or grounding of test operator) shall be taken as necessary to prevent electrostatic damage to the DUT. Batch or bulk testing is prohibited.

Most part types will mount directly to the transducer via the attachment medium. Parts shall be mounted with the largest flat surface against the transducer at the center or axis of the transducer for maximum sensitivity. The DUT shall placed directly over the transducer detection crystal or crystals. In the case of a single crystal transducer, the geometric center of the DUT shall be aligned to the center of the transducer within .078 inch (2 mm). In the case of multiple crystal transducers, the geometric center of the DUT should be arranged to have the maximum sensitivity utilizing as many crystals as possible. Where more than one large surface exists, the one that is the thinnest in section or has the most uniform thickness shall be mounted toward the transducer, e.g., flat packs are mounted top down against the transducer. Small axial-lead, right circular cylindrical parts are mounted with their axis horizontal and the side of the cylinder against the transducer. Parts with unusual shapes may require special fixtures. Such fixtures shall have the following properties:

a. Low mass.

b High acoustic transmission (aluminum alloy 7075 works well).

c. Full transducer surface contact, especially at the center.

d. Maximum practical surface contact with test part.

e. No moving parts.

f. Suitable for attachment medium mounting.

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3.3.2 Test monitoring. Each test cycle (see 3.3) shall be continuously monitored, except for the period during co-test shocks and 250 ms maximum after the shocks. Particle indications can occur in one, or any combination, of the three detection systems as follows:

a. Visual indication of high frequency spikes which exceed the normal constant background white noise level.

b. Audio indication of clicks, pops, or rattling which is different from the constant background noise present with no DUT on the transducer.

c. Threshold detection shall be indicated by the lighting of a lamp or by deflection of the secondary oscilloscope trace.

3.4 Failure criteria. Any noise bursts, as detected by any of the three detection systems exclusive of background noise, except those caused by the shock blows, during the monitoring periods, shall be cause for rejection of the device. Rejects shall not be retested except for retest of all devices in the event of test system failure. If additional cycles of testing on a lot are specified, the entire test procedure (equipment setup and checkout mounting, vibration, and co-shocking) shall be repeated for each retest cycle. Reject devices from each test cycle shall be removed from the lot and shall not be retested in subsequent lot testing.

3.5 Screening lot acceptance. Unless otherwise specified, the inspection lot (or sub lot) to be screened for lot acceptance shall be submitted to 100 percent PIND testing a maximum of five times in accordance with condition A herein. PIND prescreening shall not be performed. The lot may be accepted on any of the five runs if the percentage of defective devices in that run is less than 1 percent and the cumulative number of defective devices does not exceed 25 percent. All defective devices shall be removed after each run. Resubmission is not allowed.

NOTE: The shaker drive test frequency (F) for condition A (see 3.1) is determined by the package internal cavity height using the following formula:

$$F = \sqrt{20 / \left[(D) X (0.0511) \right]}$$

Where: D = Average internal package height (in inches).
20 is a constant in this application and is equal to sinusoidal acceleration of 20g.
F is the shaker drive test frequency (in Hz).

NOTE: The use of this formula is to be limited to frequencies in the range of 40 – 130 Hz and should not be used for package heights outside this range unless a frequency outside this range is approved by the acquiring activity.

Based on the formula above, the following table is generated:

TABLE I. Package Height vs. Test Frequency for 20 g Acceleration (condition A).

Average Internal Cavity Height			Test Frequency
Mils	mm	Inches	Hz
23	0.58	.023	130
30	0.76	.030	114
40	1.02	.040	99
50	1.27	.050	88
60	1.52	.060	81
70	1.78	.070	75
80	2.13	.080	70
90	2.29	.090	66
100	2.54	.100	63
110	2.79	.110	60
250	6.35	.250	40

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Example calculation: Assume an average internal cavity height of 70 mils.

$$F = \sqrt{20/[(D)X(0.0511)]}$$

D = 70 mils converted to inches = .070 inch.

$$F = \sqrt{20/[(D)X(0.0511)]} = \sqrt{20/[.00358]} = \sqrt{5586} = 75 \text{ Hz}$$

NOTE: The approximate average internal package height shall be measured from the floor of the package cavity or the top of the major substrate for hybrid or multichip assemblies and shall exclude the thickness of the die mounted inside the package.

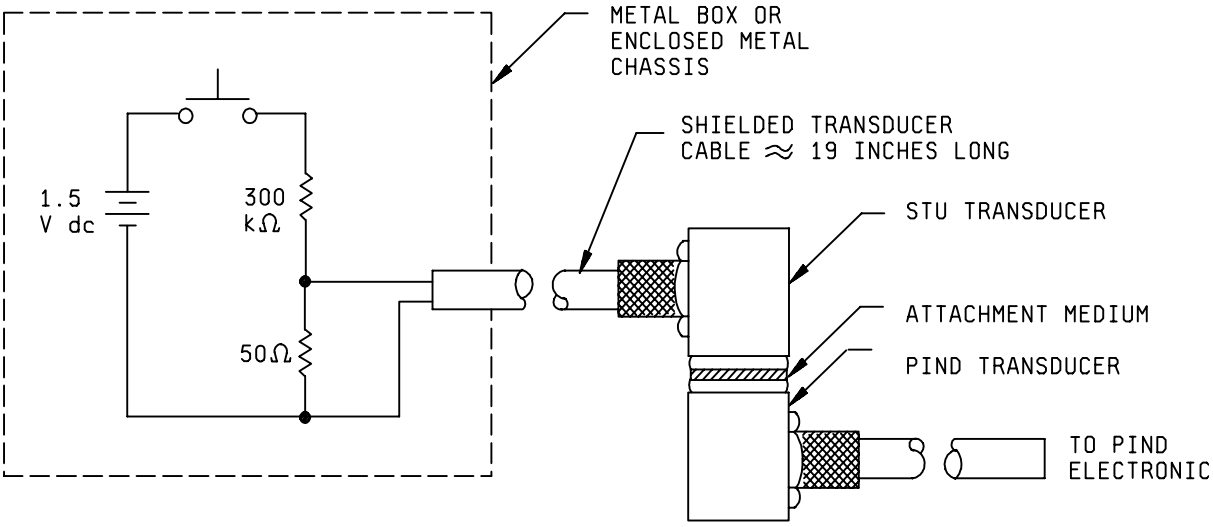
4. Summary. The following details shall be specified in the applicable performance specification sheets:

   a. Test condition letter A or B.

   b. Lot acceptance/rejection criteria (if applicable).

   c. The number of test cycles, if other than one.

   d. Pre-test shock level and co-test shock level, if other than specified.



NOTES:
1. Pushbutton switch: Mechanically quiet, fast make, gold contacts (e.g. T2 SM4 microswitch).
2. Resistance tolerance five percent noninductive.
3. Voltage source can be a standard dry cell.
4. The coupled transducers must be coaxial during test.
5. Voltage output to STU transducer 250 microvolts, ±20 percent.

FIGURE 2052-1. Typical STU.

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METHOD 2056

VIBRATION, VARIABLE FREQUENCY

1. Purpose. The variable-frequency-vibration test method is performed for the purpose of determining the effect on component parts of vibration in the specified frequency range.

2. Procedure.

2.1 Mounting. The device shall be rigidly fastened on the vibration platform and the leads or cables adequately secured.

2.2 Amplitude. The device shall be subjected to a constant peak acceleration of 20 g minimum.

2.2.1 Frequency range. The vibration frequency shall be varied approximately logarithmically between 100 and 2,000 Hz.

2.2.2 Sweep time and duration. The entire frequency range of 100 to 2,000 Hz and return to 100 Hz shall be traversed in not less than four minutes. This cycle shall be performed 4 times in each of the orientations X, Y, and Z (a total of 12 times), so that the motion shall be applied for a total period of approximately 48 minutes.

3. Summary. The measurements after test shall be specified in the performance specification sheets.

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METHOD 2057.2

VIBRATION, VARIABLE FREQUENCY (MONITORED)

1. Purpose. This test method is performed for the purpose of detecting malfunctions of semiconductor devices during vibration in the specified frequency range at the specified acceleration.

2. Procedure.

2.1 Mounting. The device shall be rigidly fastened on the vibration platform. Special care is required to ensure the position of the electrical connection to the device leads to prevent intermittent contacts during vibration. Care must also be exercised to avoid magnetic fields in the area of the device being vibrated.

2.2 Amplitude. The device shall be vibrated with a simple harmonic motion with a constant peak acceleration of 20 g minimum. The acceleration shall be monitored at a point where the g level is equivalent to that of the support point for the device(s).

2.3 Frequency range. The vibration shall be varied logarithmically between 100 and 2,000 Hz.

2.4 Sweep time and duration. The entire frequency range of 100 to 2,000 Hz and return to 100 Hz shall be traversed in not less than 8 minutes. This frequency range shall be executed at one time in each of the orientations X, Y, and Z (total of 3 times) so that the motion shall be applied for a total of 24 minutes minimum. Interruptions are permitted provided the requirements for rate of change and test duration are met. Completion of vibration within any separate frequency band is permissible before going on to the next band.

3. Measurements. With the specified dc voltages and currents applied, the semiconductor device shall be monitored continuously, during the vibration period, for intermittent opens and shorts. The monitoring equipment shall be capable of detecting voltage or current changes of the duration and magnitude specified on the performance specification sheet. In addition, the equipment shall utilize a positive-indication "go-no go" technique or a recorded trace. Equipment requiring continuous visual monitoring, such as an oscilloscope, shall not be used.

4. Summary. The following conditions shall be specified in the performance specification sheet:

a. Electrical test conditions.

b. The duration and magnitude of the voltage or current change.

c. Post-test measurements.

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METHOD 2066

PHYSICAL DIMENSIONS

1. Purpose. The purpose of this test method is to check the physical dimensions of the device.

2. Apparatus. Equipment used in this examination shall be capable of demonstrating conformance to the requirements of the performance specification sheet.

3. Procedure. The semiconductor device shall be examined to verify that the physical dimensions are as specified in the performance specification sheet.

4. Summary. The dimensions which are capable of physically describing the device shall be specified in the performance specification sheet.

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METHOD 2068

EXTERNAL VISUAL FOR NONTRANSPARENT GLASS-ENCASED, DOUBLE PLUG, NONCAVITY AXIAL LEADED DIODES

1. Purpose. The purpose of this test method is to visually inspect glass-encased, double plug, noncavity, axial leaded devices for cracks which may affect the integrity of the hermetic seal.

2. Apparatus. A binocular microscope with a magnification of 10X to 20X and sufficient lighting for visual inspection of the glass body.

3. Procedure. The examination shall be performed prior to any body coating. The devices shall be examined under a magnification of 10X to 20X for evidence of glass body cracks.

3.1 Failure criteria. Any device exhibiting cracks in the body glass shall be rejected. Cracks or chipouts in the meniscus area at either end of the body are not cause for rejection.

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METHOD 2069.2

PRE-CAP VISUAL, POWER MOSFET'S

1. Purpose. The purpose of this test method is to verify the construction and quality of workmanship in the assembly process to the point of pre-cap inspection. These various inspections and tests are intended to verify compliance with the requirements of the applicable specification sheet.

2. Apparatus. The apparatus for this inspection shall consist of the following:

a. Optical equipment capable of the specified magnification(s).

b. Adequate fixturing for handling the devices being inspected without causing damage.

c. Adequate covered storage and transportation containers to protect devices from mechanical damage and environmental contamination.

d. Any visual standards (e.g., drawings, photographs) necessary to enable the inspector to make objective decisions as to the acceptability of devices being inspected.

3. Procedure.

3.1 General. The devices shall be examined in a suitable sequence of observations with the specified magnification range to determine compliance with the requirements of this test method and the applicable specification sheet.

a. Sequence of inspection. The order in which criteria are presented is not a required order of inspection and may be varied at the discretion of the manufacturer.

b. Inspection control. Within the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment (i.e., an environment in which air-borne particles and relative humidity are controlled). The use of a positive pressure inert gas environment, such as dry nitrogen, shall satisfy the requirement of storing in a controlled environment. Unless a cleaning operation is performed prior to sealing, devices inspected in accordance with this test method shall be inspected in a class 100,000 environment in accordance with FED-STD-209. The maximum allowable relative humidity shall not exceed 65 percent. Devices shall be in clean covered containers when transferred through any uncontrolled environment.

c. Magnification. Inspection shall be performed with either a monocular, binocular, or stereo microscope and the inspection performed with any appropriate angle, with the device under suitable illumination. Magnification shall be performed within the range of 3X to 100X. All criteria of this test method shall be met for the full range of magnification.

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3.2 Bonding inspection (low magnification). This inspection and criteria shall be the required inspection for the bond type(s) and location(s) to which they are applicable when viewed from above (see figures 2069-1 and 2069-2). (Wire tail is not considered part of the bond when determining physical bond dimensions.) No device shall be acceptable which exhibits any of the following defects.

3.2.1 Gold ball bonds.

a. Gold ball bonds where the ball bond diameter is less than 2 times or greater than 5 times the bonding wire diameter.

b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.

c. Gold ball bonds where the exiting wire is not within boundaries of the bonding pad.

d. Any visible intermetallic formation at the periphery of any gold ball bond.

3.2.2 Wedge bonds.

a. Ultrasonic/thermasonic wedge bonds that are less than 1.2 times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 3.0 times the wire diameter in length, before cutoff, as viewed from above.

b. Thermocompression wedge bonds that are less than 1.2 times or greater than 3.0 times the wire diameter in width or are less than 1.5 times or greater than 3.0 times the wire diameter in length.

3.2.3 Tailless bonds (crescent).

a. Tailless bonds that are less than 1.2 times or greater than 5.0 times the wire diameter in width, or are less than 0.5 times or greater than 3.0 times the wire diameter in length.

b. Tailless bonds where the bond impression does not cover the entire width of the wire.

3.2.4 General (gold ball, wedge, and tailless). As viewed from above, no device shall be acceptable which exhibits any of the following defects:

a. Bonds on the die where less than 75 percent of the bond is within the unglassivated bonding pad area (except where due to geometry, the bonding pad is smaller than the bond, the criteria shall be 50 percent).

b. Wire bond tails that extend over and make contact with any metallization not covered by glassivation and not connected to the wire.

c. Wire bond tails that exceed two wire diameters in length at the die bonding pad or four wire diameters in length at the package or post.

d. Bonds on the package post that are not bonded entirely on the flat surface of the post top.

e. A bond on top of another bond, bond wire tail, or residual segment of lead wire. An ultrasonic wedge bond alongside a previous bond where the observable width of the first bond is reduced less than 0.25 mil is considered acceptable.

f. Bonds placed so that the separation between bond and adjacent unglassivated die metallization not connected to it, is less than 1.0 mil.

g. Rebonding.

h. Gold bonds where less than 50 percent of the bond is located within an area that is free of eutectic melt.

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3.2.5 Internal lead wires. This inspection and criteria shall be required inspection for the location(s) to which they are applicable when viewed from above. No device shall be acceptable that exhibits any of the following defects:

a. Any wire that comes closer than one wire diameter to unglassivated operating metallization, another wire (common wires excluded), package post, unpassivated die area of opposite polarity, or any portion of the package of opposite polarity including the plane of the lid to be attached (except by design, but in no case should the separation be less than 0.25 mil). (Within a 5.0 mil spherical radial distance from the perimeter of the bond on the die surface, the separation shall be greater than 1.0 mil.)

b. Nicks, tears, bends, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent, except in bond deformation area.

c. Missing or extra lead wires.

d. Bond lifting or tearing at interface of pad and wire.

e. Any wire which runs from die bonding pad to package post and has no arc or stress relief.

f. Wires which cross other wires, except common connectors, except by design, in which case the clearance shall be 1.0 mil minimum.

g. Wire(s) not in accordance with bonding diagram (unless allowed in design documentation, for tuning purposes).

h. Kinked wires (an unintended sharp bend) with an interior angle of less than 90 degrees or twisted wires to an extent that stress marks appear.

i. Wire (ball bonded devices) not within 10 degrees of the perpendicular to the surface of the chip for a distance of greater than 0.5 mil before bending toward the package post or other termination point.

3.3 Package conditions (low magnification). No device shall be acceptable which exhibits any of the following defects.

3.3.1 Foreign material on die surface. All foreign material or particles may be blown off with a nominal gas blow (approximately 20 psig) or removed with a soft camel hair brush. The device shall then be inspected for the following criteria:

a. Loosely attached conductive particles (conductive particles which are attached by less than one-half of their largest dimension) that are large enough to bridge the narrowest unglassivated active metal spacing (silicon chips or any opaque material shall be included as conductive particles).

b. Liquid droplets, chemical stains, or photoresist on the die surface that bridge any combination of unglassivated metallization or bare silicon areas, except for unused cells.

c. Ink on the surface of the die that covers more than 25 percent of a bonding pad area (or interferes with bonding) or that bridges any combination of unglassivated metallization or bare silicon areas, except for unused cells.

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3.3.2 Die mounting.

a. Die to header mounting material which is not visible around at least three sides or 75 percent of the die perimeter. Wetting criteria is not required if the devices pass an approved die attached evaluation test.

b. Any balling of the die mounting material which does not exhibit a fillet when viewed from above.

c. Any flaking of the die mounting material.

d. Any die mounting material which extends onto the die surface or extends vertically above the top surface of the die and interferes with bonding.

3.3.3 Die orientation.

a. A die which is not oriented or located in accordance with the applicable assembly drawing of the device.

b. Die is visibly tipped or tilted (more than 10 degrees) with respect to the die attach surface.

3.3.4 Internal package defects (low magnification inspection) (applicable to headers, bases, caps, and lids). As an alternative to 100 percent visual inspection of lids and caps in accordance with the criteria of 3.3.1.a, the lids or caps may be subjected to a suitable cleaning process and quality verification procedure approved by the qualifying activity, provided the lids or caps are subsequently held in a controlled environment until capping or preparation for seal.

a. Any header or post plating which is blistered, flaked, cracked, or any combination thereof.

b. Any conductive particle which is attached by less than one-half of the longest dimension.

c. A bubble or a series of interconnecting bubbles in the glass surrounding the pins which are more than one-half the distance between the pin and body or pin-to-pin.

d. Header posts which are severely bent.

e. Any glass, die, or other material greater than 1.0 mil in its major dimension which adheres to the flange or side of the header and would impair sealing.

f. Any stain, varnish, or header discoloration which appears to extend under a die bond or wire bond.

g. For isolated stud packages:

(1) Any defect or abnormality causing the designed isolating paths between the metal island to be reduced to less than 50 percent of the design separation.

(2) A crack or chip-out in the substrate.

3.3.5 Carrier defects (substrate (e.g., BeO, alumina)).

a. Any chip-out in the carrier material.

b. Carrier metallization which is smeared or is obviously not uniform in metallization design pattern to the extent that there is less than 50 percent of the original design separation, or 0.5 mil, whichever is less, between operating pads, paths, lid mounting metallization, edges, or any combination thereof.

c. Any crack in the BeO or operating metallization that would affect hermetic seal or die mounting metallization. (Tooling marks or cold form interface lines are not cracks and are not cause for rejection.)

d. Any metallization lifting, peeling, or blistering (on the carrier surface).

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e. Any attached conductive foreign material which bridges any combination of metallization paths, leads, or active circuit elements.

f. A scratch or void in the metallization which exposes the substrate anywhere along its length and leaves less than 75 percent of the original metal width undisturbed.

NOTE: Occasionally package metallization is intentionally burnished or scratched, in areas which require wire bond attachment, to improve surface bondability; such conditions are not cause for rejection. Burnished or scratched areas must satisfy the criteria of 3.3.4.b.

g. Excessive scratches in carrier metallization due to abuse in handling or processing.

h. Any staple, bridge, or clip with solder joint which exhibits less than 50 percent wetting around the section that is attached to the package.

i. Any header post(s) which are not perpendicular within 10 degrees of the horizontal plane of the header.

j. Any lead attach eutectic or solder which extends across greater than 50 percent of the design separation gap between metallization pads.

3.3.6 Presence of extraneous matter. Extraneous matter (foreign particles) shall include, but not be limited to:

a. Any foreign particle, loose or attached, greater than .003 inch (0.08 mm) or of any lesser size which is sufficient to bridge nonconnected conducting elements of the device.

b. Any wire tail extending beyond its normal end by more than two diameters at the semiconductor die pad or by more than four wire diameters at the package post (see figure 2069-3).

c. Any burr on a post (header lead) greater than .003 inch (0.08 mm) in its major dimension or of such configuration that it may break away.

d. Excessive semiconductor die bonding material buildup. A semiconductor die shall be mounted and bonded so that it is not tilted more than 10 degrees from mounting surface. The bonding agent that accumulates around the perimeter of the semiconductor die and touches the side of the semiconductor die shall not accumulate to a thickness greater than that of the semiconductor die (see figures 2069-4 and 2069-5). Where the bonding agent is built up but is not touching the semiconductor die, the build up shall not be greater than twice the thickness of the semiconductor die. There shall be no excess semiconductor die bonding material in contact with the active surface of the semiconductor die or any lead or post, or separated from the main bonding material area (see figure 2069-6).

e. Flaking on the header or posts or anywhere inside the case.

f. Extraneous ball bonds anywhere inside case, except for attached bond residue when rebonding is allowed.

3.4 Semiconductor conditions. No device shall be acceptable which exhibits any of the following defects.

3.4.1 Metallization, scratches, and voids exposing underlying material.

a. A scratch or void that severs the innermost guard ring.

b. Any die containing a void in the metallization at the bonding pad covering more that 25 percent of the pad area.

c. For devices with non-expanded contacts and all power devices. Any scratch or void which isolates more than 25 percent of the total metallization of an active region from the bonding pad.

d. For all devices with expanded contacts. A scratch or void, whether or not underlying material is exposed, which leaves less than 50 percent undisturbed metal width in the metal connecting the pad and the contact regions.

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e. For expanded contacts with less than or equal to 10 contact regions. A scratch or void extending across more than 50 percent of the first half of any contact region (beginning at the bonding area) in more than 10 percent of the contact regions.

f. For expanded contacts with less than or equal to 10 contact regions. A scratch or void in the contact area which isolates more then 10 percent of the metallized area form the bonding area.

3.4.2 Metallization corrosion. Any metallization which shows evidence of corrosion.

3.4.3 Metallization adherence. Any metallization which has lifted, peeled, or blistered.

3.4.4 Metallization probe marks. Criteria found in 3.4.1 shall apply as limitations for probing damage.

3.4.5 Metallization bridging. Metallization bridging between two normally unconnected metallization paths which reduces the separation, such that a line of oxide is not visible (no less than 0.1 mil) when viewed at the prescribed magnification.

3.4.6 Metallization alignment.

a. Except by design, contact window that has less than 50 percent of its area covered by continuous metallization.

b. A metallization path not intended to cover a contact window which is separated from the window by less than 0.1 mil.

3.4.7 Passivation faults.

a. Any passivation fault including pinholes not covered by glassivation that exposes semiconductor material and allows bridging between any two diffused areas, any two metallization strips, or any such combination not intended by design.

b. Except by design, an absence of passivation visible at the edge and continuing under the metallization causing an apparent short between the metal and the underlying material (closely spaced double or triple lines on the edges of the defect indicate that it may have sufficient depth to penetrate down to the silicon).

c. Except by design, any active junction not covered by passivation or glassivation.

3.4.8 Scribing and other die defects.

a. Except by design, less than 0.1 mil passivation visible between active metallization or bond pad periphery and the edge of the die.

b. Any chip-out or crack in the active area.

c. Except by design, die having attached portions of the active area on another die, and which exceeds 10 percent of the area of the second die.

d. Any crack which extends 2.0 mils in length inside the scribe grid or scribe line that points toward active metallization or active area and extends into the oxide area.

e. Any chip-out that extends to within 1.0 mil of a junction.

f. Any crack or chip-out that extends under any active metallization area.

g. Any chip-out which extends completely through the guard ring.

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3.4.9 Glassivation defects.

a. Glass crazing that prohibits the detection of visual criteria contained herein.

b. Any glassivation which has delaminated. (Lifting or peeling of the glassivation may be excluded from the criteria above, when it does not extend more than 1.0 mil from the designed periphery of the glassivation, provided that the only exposure of metal is adjacent to bond pads or of metallization leading from those pads.)

c. Except by design, two or more adjacent active metallization paths which are not covered by glassivation.

d. Unglassivated areas at the edge of bonding pad which expose silicon.

e. Glassivation which covers more than 25 percent of the design bonding pad area.

3.5 Post protective coating visual inspection. If devices are to be coated with a protective coating, the devices shall be visually examined in accordance with the criteria specified in 3 herein, prior to the application of the coating. After the application and cure of the protective coating, the devices shall be visually examined under a minimum of 10X magnification. No device shall be acceptable which exhibits any of the following defects:

a. Except by design, any unglassivated or passivated areas or insulating substrate which has incomplete age.

b. Open bubbles, cracks, or voids in the protective coating.

c. A bubble, or a chain of bubbles, which covers two adjacent metallized surfaces.

d. Protective coating which has flaked or peeled.

e. Protective coating which is not fully cured.

f. Conductive particles which are embedded in the coating and are large enough to bridge the narrowest unglassivated active metal spacing (silicon chips shall be included as conductive particles).

g. Except by design, a web of protective coating that connects the wire with the header.

4. Summary. The following details shall be specified in the specification sheet:

a. Exceptions or additions to the inspection method.

b. Where applicable, any conflicts with approved circuit design topology or construction.

c. Where applicable, gauges, drawings, and photographs that are to be used as standards for operator comparison.

d. When applicable, specific magnification.

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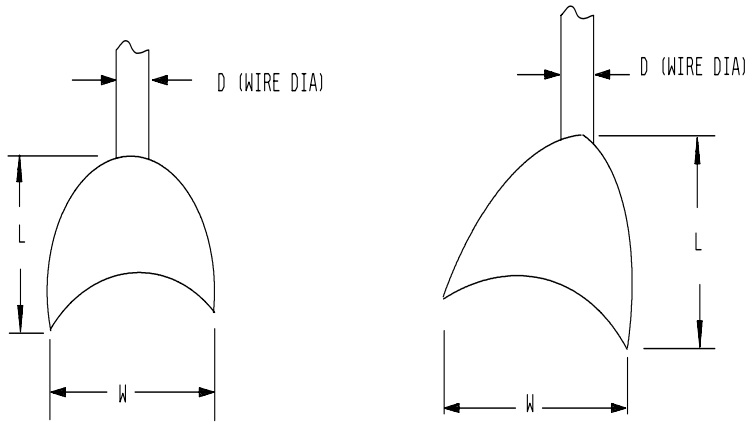
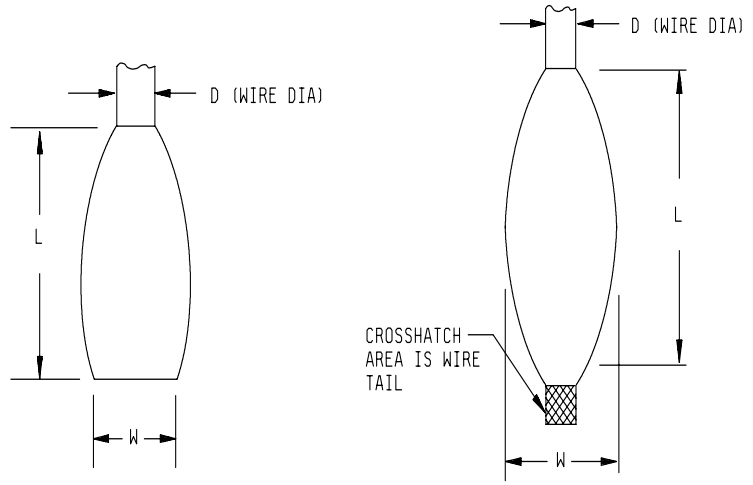


A. Tailless or crescent.

NOTES:
1. 1.2 D ≤ W ≤ 5.0 D (width).
2. 0.5 D ≤ L ≤ 3.0 D (length).



B. Wedge.

Ultrasonic

NOTES:
1. 1.0 D ≤ W ≤ 3.0 D (width).
2. 1.5 D ≤ L ≤ 3.0 D (length).

Thermocompression

NOTES:
1. 1.2 D ≤ W ≤ 3.0 D (width).
2. 1.5 D ≤ L ≤ 3.0 D (length).

FIGURE 2069-1. Bond dimensions.

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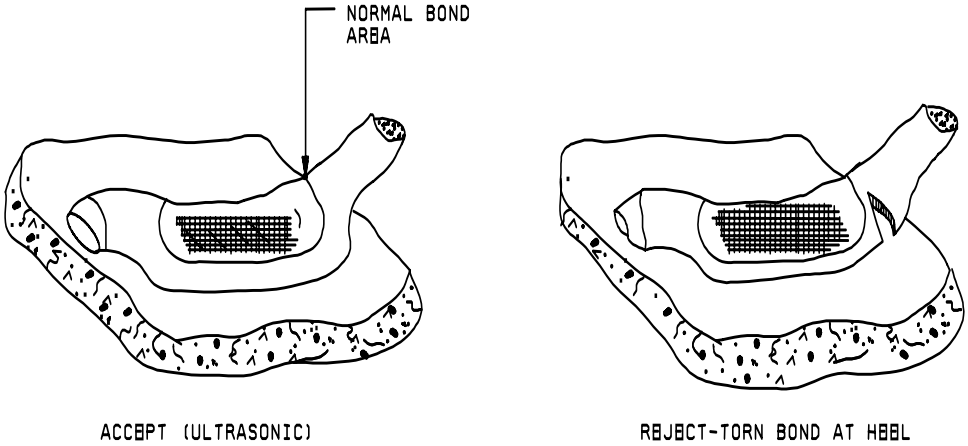

FIGURE 2069-2. Lifted/torn bonds.

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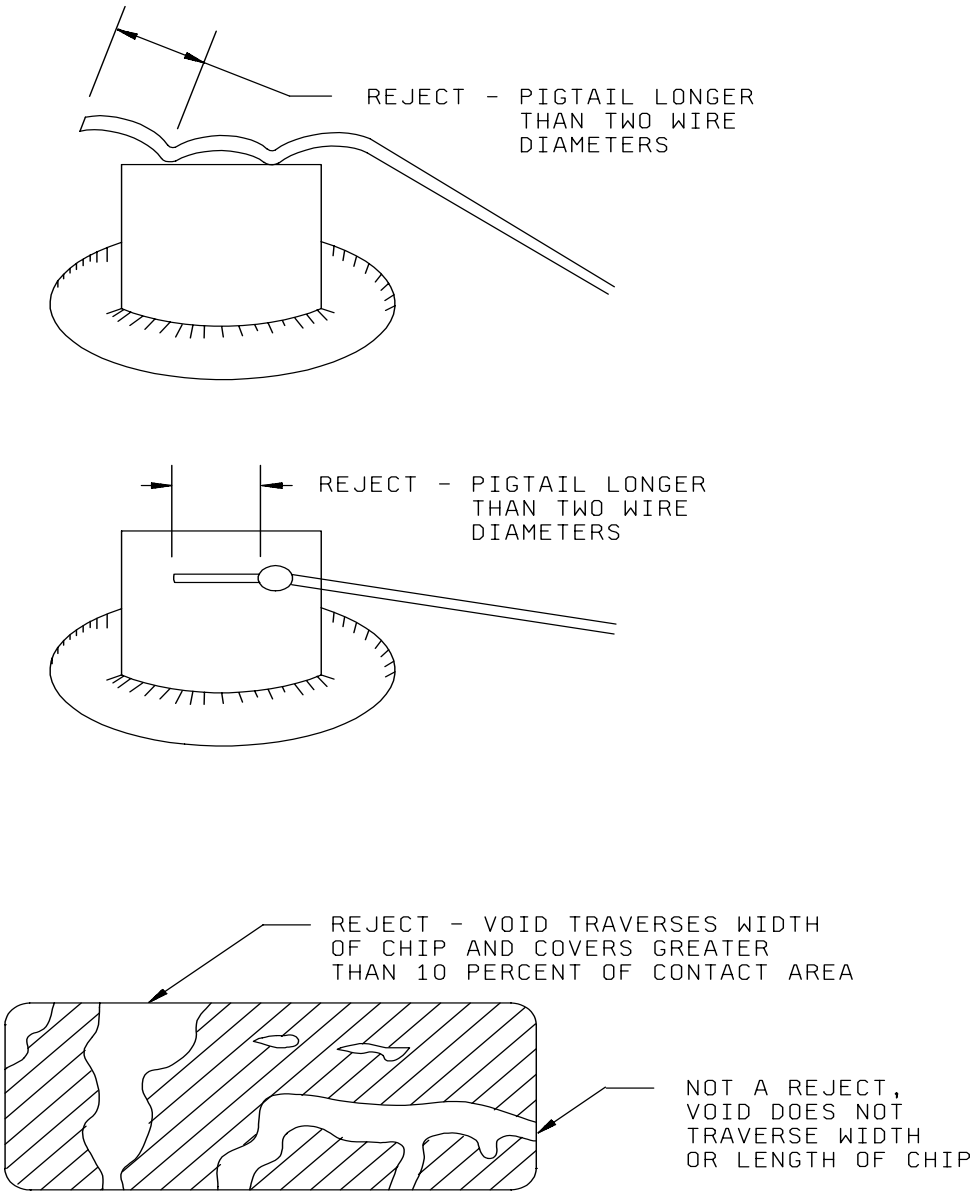

FIGURE 2069-3. Acceptable and unacceptable voids and excessive pigtails.

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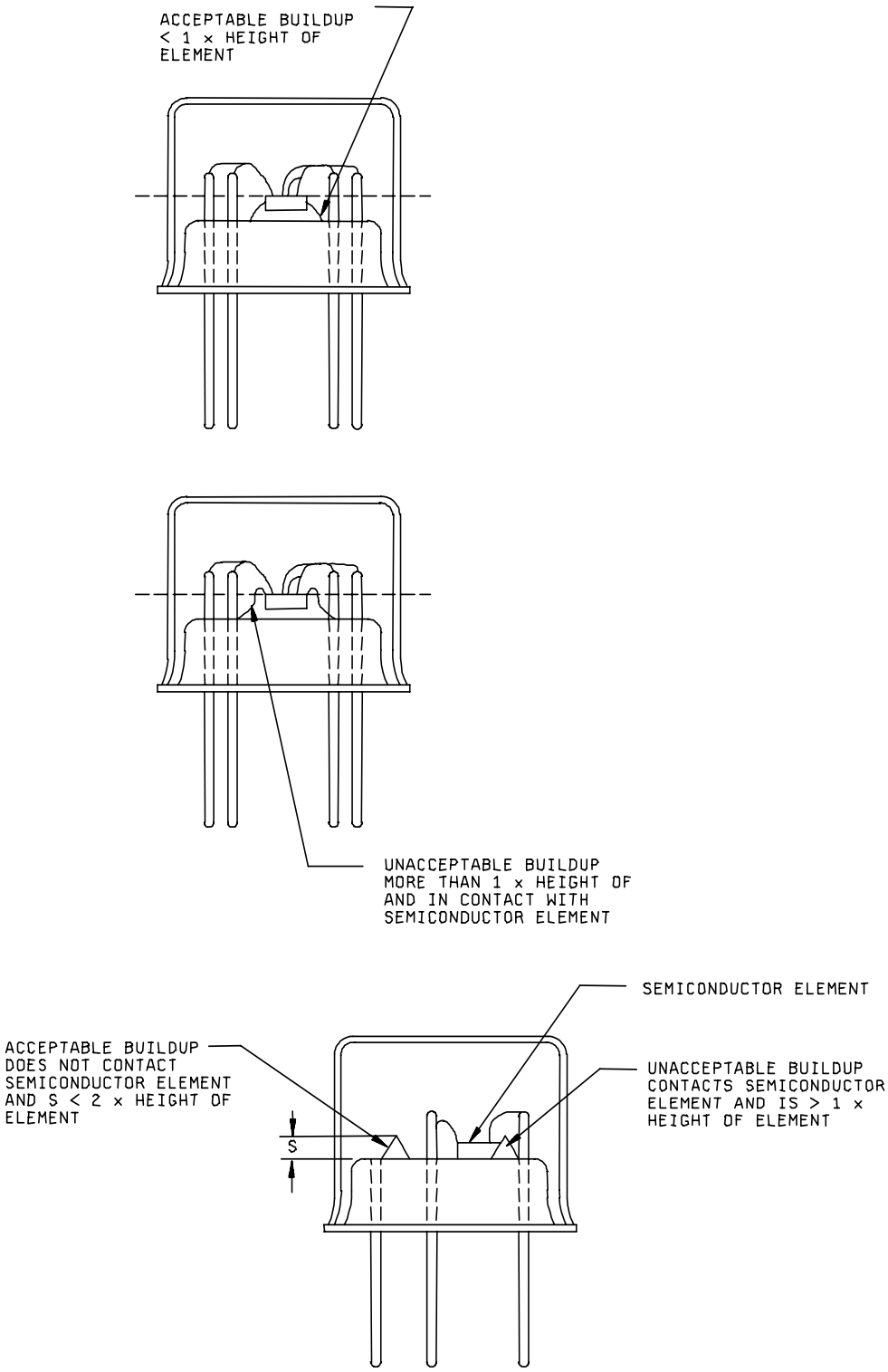

FIGURE 2069-4. Acceptable and unacceptable bonding material build-up.

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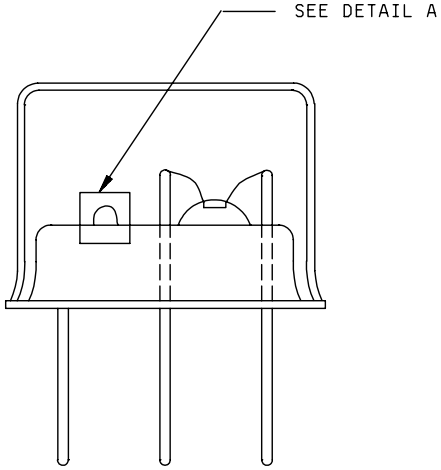

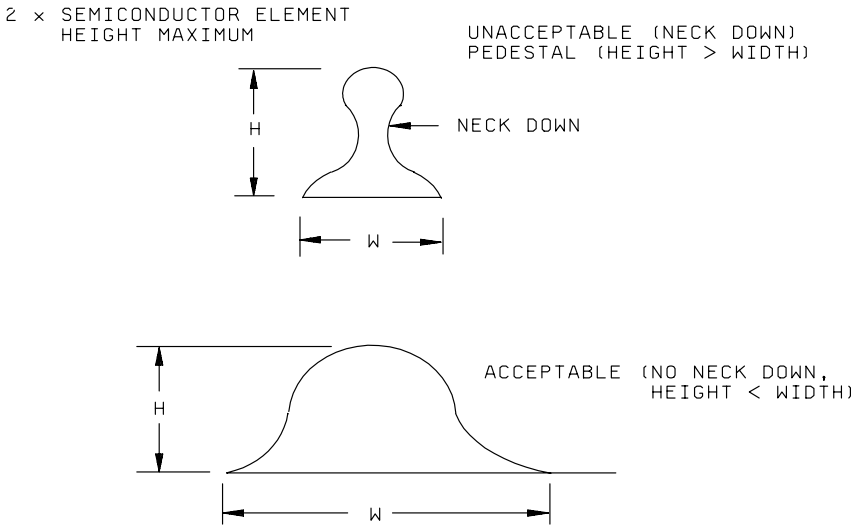

FIGURE 2069-5. Extraneous bonding material build-up.

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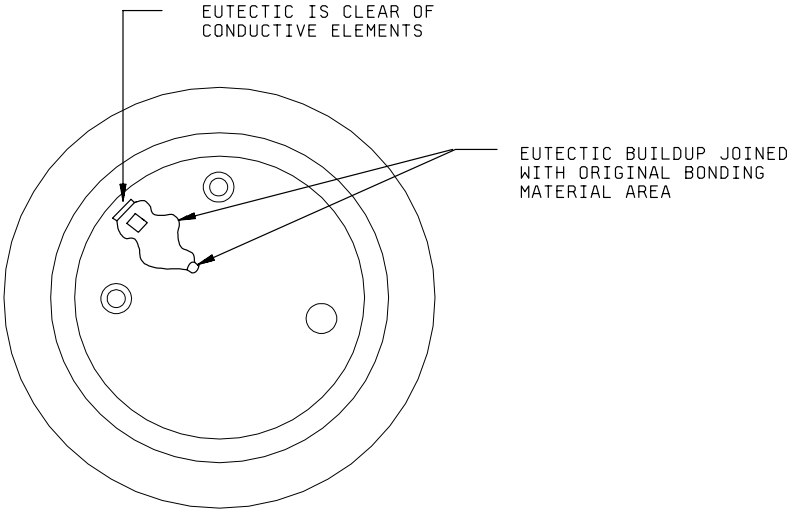
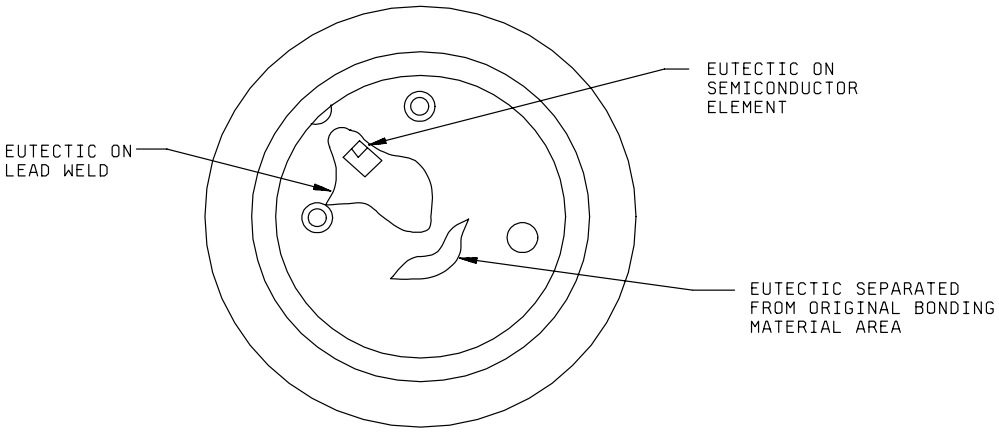


ACCEPTABLE



UNACCEPTABLE

FIGURE 2069-6. Acceptable and unacceptable excess material.

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METHOD 2070.2

PRE-CAP VISUAL
MICROWAVE DISCRETE AND MULTICHIP TRANSISTORS

1. Purpose. The purpose of this test is to verify the construction and quality of workmanship in wafer, wafer dc testing, die inspection, and assembly processes to the point of pre-cap inspection. These various inspections and tests are intended to detect and remove transistor die with defects that could lead to device failure during application and to verify compliance with the requirements of the applicable specification sheet.

2. Apparatus. The apparatus for this inspection shall consist of the following:

a. Optical equipment capable of the specified magnifications, and both normal incident and darkfield lighting.

b. Adequate fixturing for handling the devices being inspected without causing damage.

c. Adequate covered storage and transportation containers to protect devices from mechanical damage and environmental contamination.

d. Any visual standards (e.g., drawings, photographs) necessary to enable the inspector to make objective decisions as to the acceptability of devices being inspected.

2.1 Microwave Devices. GaAs devices shall be inspected to all applicable criteria as listed herein. GaAs microwave devices shall also have additional specific criteria as listed and the applicable high power magnification for individual features of GaAs microwave devices shall be selected from the following table.

TABLE 2071-I GaAs microwave device high magnification requirements.

Feature dimensions	Magnification range
> 5 microns	75 - 150X
1 - 5 microns	150 - 400X
< 1 micron	400 - 1000X

3. Procedure.

3.1 General. The devices shall be examined in a suitable sequence of observations with the specified magnification range to determine compliance with the requirements of this document and the applicable specification sheet.

a. Sequence of inspection. The order in which criteria are presented is not a required order of inspection and may be varied at the discretion of the manufacturer.

b. Inspection control. Within the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment (an environment in which air-borne particles and relative humidity are controlled). The use of a positive pressure inert gas environment, such as dry nitrogen, shall satisfy the requirement of storing in a controlled environment. Unless a cleaning operation is performed prior to sealing, devices inspected in accordance with this specification shall be inspected in a class 100,000 environment in accordance with FED-STD-209. The maximum allowable relative humidity shall not exceed 05 percent. Devices shall be in clean covered containers when transferred through any uncontrolled environment.

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c. Magnification. High magnification inspection shall be performed perpendicular to the die surface with normal incident or darkfield illumination as required. Low magnification inspection shall be performed with either a monocular, binocular, or stereo microscope and the inspection performed with any appropriate angle, with the device under suitable illumination. High magnification may be used to verify a discrepancy which has first been noted at low magnification.

(1) High magnification inspection shall be performed within the range of 00X to 200X.

(2) Low magnification shall be performed within the range of 30X to 00X.

d. General reject criteria. Unless otherwise specified, reject if the defect is present in 25 percent of any one cell or in 10 percent of the entire die. Figures 2070-1 through 2070-4 illustrate accept and reject criteria for die and bonds.

e. Figures 2070-5 through 2070-7 illustrate different geometries used in fabricating microwave discrete transistors.

3.2 Wafer inspection. Not applicable.

3.2.1 Metallization inspection. Unless otherwise specified, the 25 percent of a cell and 10 percent of a die reject conditions apply. No die shall be acceptable which exhibits any of the following defects:

a. Metallization misalignment so that there is less than 75 percent coverage of the ohmic contact windows.

b. Contact window that has less than a continuous 50 percent of its perimeter covered by metallization. NOTE: Metal coverage is not required at the far dielectric steps of the end base contacts under base metal finger tips.

c. Metal must cover 50 percent of the contact that lies over the enhancement area.

d. Metallization bridging, between two normally unconnected metallization paths, which reduces the design separation to less than 50 percent or 0.1 mil whichever is less.

e. Metallization corrosion. Any metallization which shows evidence of corrosion.

f. Metallization adherence. Any metallization which has lifted, peeled, or blistered.

g. Exception: Do not reject for missing or defective run around metal (run around metal is non active metal used for probing purposes with multicell devices).

3.2.2 Glassivation and silicon nitride defects. (Unless otherwise specified, the 25 percent of a cell and 10 percent of a die reject conditions apply). No die shall be acceptable which exhibits any of the following defects:

a. Glass crazing that prohibits the detection of voids or scratches during subsequent inspection or that covers more than 25 percent of the die area.

b. Any glassivation which has delaminated.

c. Two or more adjacent active metallization paths which are not covered by glassivation, except by design.

d. Unglassivated areas at the edge of bonding pads which expose silicon.

e. Glassivation which covers more than 25 percent of the designed bonding pad area.

f. Glass crazing covering more than 25 percent of the die area.

g. Glass cracks which form closed loops over adjacent metallization paths.

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3.3 Die metallization defects (high magnification). No die shall be acceptable which exhibits any of the following defects.

3.3.1 Metallization scratches and voids exposing underlying material (see figure 2070-1). Unless otherwise specified, the 25 percent of a cell and 10 percent of a die conditions apply.

a. A scratch or void that severs the innermost metallized guard ring.

b. Any die containing a void in the metallization at the bonding pad covering more than 25 percent of the pad area (see figure 2070-1).

c. For all devices with expanded contacts. A scratch, whether or not underlying material is exposed; or a void, which leaves less than 50 percent undisturbed metal width in the metal connecting the pad and the contact regions.

d. For expanded contacts with more than 10 contact regions. A scratch or void extending across more than 50 percent of the first half of any contact region (beginning at the bonding area) in more than 10 percent of the contact regions.

e. For expanded contacts with less than 10 contact regions. A scratch or void in the contact area which isolates more than 10 percent of the contact regions.

f. Metallization probing. Criteria contained in 3.3.1.b shall apply as limitation on probing damage.

3.4 Scribing and die defects (high magnification). No device shall be acceptable which exhibits any of the following defects (see figure 2070-2).

a. Unless by design, less than 0.1 mil passivation visible between active metallization or bond pad periphery and the edge of the die.

b. Any chip-out or crack in the active area.

c. Any crack which exceeds 2.0 mils in length beyond the scribe grid or line that points toward active metallization or an active area.

d. Any chip-out that extends to within 1.0 mil of an active area or to within 50 percent of the design spacing, whichever is less.

e. Any crack or chip-out that extends under any active metallization.

f. Reject if more than 25 percent of a depletion ring is missing. A depletion ring encompasses an individual cell. An annular ring encompasses the entire die. A true annular ring will be the same color as the emitter.

3.5 Bonding inspection (low magnification). This inspection and criteria shall be the required inspection for the bond types and locations to which they are applicable when viewed from above (see figures 2070-3 and 2070-4). (Wire tail is not considered part of the bond when determining physical bond dimensions.) No device shall be acceptable which exhibits any of the following defects.

3.5.1 Gold ball bonds.

a. Gold ball bonds where the ball bond diameter is less than 2.0 times or greater than 5.0 times the bonding wire diameter.

b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.

c. Gold ball bonds where the exiting wire is not within boundaries of the bonding pad.

d. Any visible intermetallic formation at the periphery of any gold ball bond.

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3.5.2 Wedge bonds.

a. Aluminum wire: Ultrasonic/thermasonic wedge bonds that are less than 1.2 times or greater than 3.0 times the wire diameter in width, or less than 1.5 times or greater than 3.0 times the wire diameter in length.

b. Gold wire: Ultrasonic/thermasonic wedge bonds that are less than 1.0 times or greater than 3.0 times the wire diameter in width, or less than 0.5 times or greater than 3.0 times the wire diameter in length.

c. Thermocompression wedge bonds that are less than 1.2 times or greater than 3.0 times the wire diameter in width or are less than 0.5 times or greater than 3.0 times the wire diameter in length.

3.5.3 Tailless bonds (crescent).

a. Tailless bonds that are less than 1.2 times or greater than 5.0 times the wire diameter in width or are less than 0.5 times or greater 3.0 times the wire diameter in length.

b. Tailless bonds where the bond impression does not cover the entire width of the wire.

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3.5.4 General (gold ball, wedge, and tailless). As viewed from above, no device shall be acceptable which exhibits any of the following defects.

a. Bonds on the die where less than 50 percent of the bond is within the unglassivated bonding pad area.

b. Wire bond tails that extend over and make contact with any metallization not covered by glassivation and not connected to the wire.

c. Wire bond tails that exceed two wire diameters in length at the die bonding pad or four wire diameters in length at the package or post.

d. Bonds on the package post that are not bonded entirely on the flat surface of the post top.

e. A bond on top of another bond, bond wire tail, or residual segment of lead wire. An ultrasonic wedge bond alongside a previous bond where the observable width of the first bond is reduced less than 0.25 mil is considered acceptable.

f. Bonds placed so that the separation between bond and adjacent unglassivated die metallization not connected to it is less than 1.0 mil, except if the glass does not exhibit cracking, the separation may be 0.1 mil.

g. Rebonding shall be permitted with the following limitations.

(1) No scratched, open, or discontinuous metallization paths or conductor patterns shall be repaired by bridging with, or addition of, bonding wire or ribbon.

(2) All rebonds shall be placed on at least 50 percent undisturbed metal (excluding probe marks that do not expose oxide) and no more than one rebond attempt at any design bond location shall be permitted at any pad or post and no rebonds shall touch an area of exposed oxide caused by lifting metal.

(3) The total number of rebond attempts shall be limited to a maximum of 10 percent of the total number of bonds in the device. The 10 percent limit on rebonds may be interpreted as the nearest whole number of bonds in the device. A bond shall be defined as a wire to post or wire to bond pad. Bond-offs required to clear the bonder after an unsuccessful first bond attempt need not be considered as rebonds provided they can be identified as bond-offs by being made physically away from normal bond areas. The initial bond attempt need not be visible. A replacement of one wire at one end or an unsuccessful bond attempt at one end of the wire counts as one rebond; a replacement of wire bonded at both ends, or an unsuccessful bond attempt of a wire already bonded at the other end, counts as two rebonds.

h. Gold bonds where less than 50 percent of the bond is located within an area that is free of eutectic melt. The blush area shall not be considered part of the eutectic melt. (The blush area is defined as the area where a color change can be seen but not a change in surface texture.)

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3.5.5 Internal lead wires. This inspection and criteria shall be required inspection for the locations to which they are applicable when viewed from above. No device shall be acceptable that exhibits any of the following defects.

a. Any wire that comes closer than one wire diameter to unglassivated operating metallization, another wire (common wires excluded), package post, unpassivated die area of opposite polarity, or any portion of the package of opposite polarity including the plane of the lid to be attached (except by design, but in no case should the separation be less than 0.25 mil). (Within a 5.0 mil spherical radial distance from the perimeter of the bond on the die surface, the separation shall be greater than 1.0 mil.)

b. Nicks, tears, bends, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent, except in bond deformation area.

c. Missing or extra lead wires.

d. Bond lifting or tearing at interface of pad and wire.

e. Any wire which runs from die bonding pad to package post and has no arc or stress relief.

f. Wires which cross other wires, except common connectors, except by design, in which case the clearance shall be 1.0 mil minimum.

g. Wires not in accordance with bonding diagram (unless allowed in design documentation, for tuning purposes).

h. Kinked wires (an unintended sharp bend) with an interior angle of less than 90 degrees or twisted wires to an extent that stress marks appear.

i. Wire (ball bonded devices) not within 10 degrees of the perpendicular to the surface of the chip for a distance of greater than 0.5 mil before bending toward the package post or other termination point.

3.6 Package conditions (low magnification). No device shall be acceptable which exhibits any of the following defects.

3.6.1 Foreign material on die surface. All foreign material or particles may be blown off with a nominal gas blow (approximately 20 psi (138 kPa)) or removed with a soft camel hair brush. The device shall then be inspected for the following criteria.

a. Loosely attached conductive particles (conductive particles which are attached by less than one-half of their largest dimension) that are large enough to bridge the narrowest unglassivated active metal spacing (silicon chips or any opaque material shall be included as conductive particles).

b. Liquid droplets, chemical stains, or photoresist on the die surface that bridge any combination of unglassivated metallization or bare silicon areas, except for unused cells.

c. Ink on the surface of the die that covers more than 25 percent of a bonding pad area (or interferes with bonding) or that bridges any combination of unglassivated metallization or bare silicon areas, except for unused cells.

d. Any entrapped opaque material which appears to extend over metallization.

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3.6.2 Die mounting.

a. Die to header mounting material which is not visible around at least three sides or 75 percent of the die perimeter. Wetting criteria is not required if the devices pass an approved die attached evaluation test.

b. Any balling of the die mounting material which does not exhibit a fillet when viewed from above.

c. Any flaking of the die mounting material.

d. Any die mounting material which extends onto the die surface beyond the scribe zone and comes closer than 0.5 mil to any active area or metallization, or extends vertically above the top surface of the die and interferes with bonding.

3.6.3 Die orientation.

a. A die which is not oriented or located in accordance with the applicable assembly drawing of the device.

b. Die is visibly tipped or tilted (more than 10 degrees) with respect to the die attach surface.

3.6.4 Internal package defects (applicable to headers, bases, caps, and lids). As an alternative to 100-percent visual inspection, the lids or caps may be subjected to a suitable cleaning process and quality verification procedure approved by the qualifying activity, provided the lids or caps are subsequently held in a controlled environment until capping or preparation for seal.

a. Any header or post plating which is blistered.

b. Any conductive particle which is attached by less than one-half of the longest dimension.

c. For isolated heat sink packages:

(1) Any defect or abnormality causing the designed isolating paths between the metal islands to be reduced to less than 50 percent of the design separation or reduced to 0.2 mil, whichever is less.

(2) A crack in the substrate.

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3.6.5 Carrier defects ((e.g., BeO, alumina) substrate).

a. Any chip-out in the carrier material.

b. Carrier metallization which is smeared or is obviously not uniform in metallization design pattern to the extent that there is less than 50 percent of the original design separation, or 0.5 mil, whichever is less, between operating pads, paths, lid mounting metallization, edges, or any combination thereof.

c. Any crack in the BeO or operating metallization that would affect hermetic seal or die mounting metallization. (Tooling marks or cold form interface lines are not cracks and are not cause for rejection.)

d. Any metallization lifting, peeling, or blistering (on the carrier surface).

e. Any attached conductive foreign material which bridges any combination of metallization paths, leads, or active circuit elements.

f. A scratch or void in the metallization which exposes the substrate anywhere along its length and leaves less than 75 percent of the original metal width undisturbed.

NOTE: Occasionally package metallization is intentionally burnished or scratched, in areas which require wire bond attachment, to improve surface bondability; such conditions are not cause for rejection. Burnished or scratched areas must satisfy the criteria of 3.0.4.b.

g. Excessive scratches in carrier metallization due to abuse in handling or processing.

h. Any staple, bridge, or clip with solder joint which exhibits less than 50 percent wetting around the section that is attached to the package.

i. Any header posts which are not perpendicular within 10 degrees of the horizontal plane of the header.

j. Any lead attach eutectic or solder which extends across greater than 50 percent of the design separation gap between metallization pads.

3.7 Capacitor defects (high magnification).

a. Scratches through the metal that extend the length of the metal and expose underlying oxide.

b. Any metallization peeling (except due to bond tail pull).

c. Any metallization which shows evidence of corrosion.

d. Cracks in the silicon that point toward the metal and are within 1.0 mil of the metal (except for ground bar portion).

e. Chip-outs within 0.5 mil of the metal (except for ground bar portion).

f. Metal that has been gouged or probed over 20 percent of a bonding pad area and exposes underlying oxide.

g. Mounting material which is not visible around at least three sides or 75 percent of the capacitor perimeter. Wetting criteria is not required if the devices pass an approved capacitor attach evaluation test. (This inspection is to be performed at low magnification.)

NOTE: Multiple bonding is allowable for tuning purposes, however initial bond wire shall be completely removed before rebonding and must be in accordance with design documentation.

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3.8 Alignment (this applies to 25 percent of any one cell or 10 percent of any die). Reject any diffusion line which touches another diffusion line, except for contact enhancements, which can touch an active area of the same type. Emitter contacts can touch emitter base junction but cannot cross. Base contacts must engage 50 percent or more of the contact enhancement.

NOTE: Contacts are not diffused.

3.9 Resistors (criteria applies to 25 percent of any one cell or 10 percent of any die). (See table 2072-2)

TABLE 2072-2. 1/

Process level	Defect	Reject
Nickel-Chromium (NICR) resistor	Pinched	Resistor is less than 90 percent of its intended design width.
	Undercutting	Resistor is less than 75 percent of its intended design width.
	Bridging or excess NICR	Bridging between discrete resistor pattern.
Diffused resistors	Oxide defects Poor definitions	No visible opening.
	Misalignment	Contacting less than 90 percent of its intended design width.
	Undercutting	Resistor less than 75 percent of its intended design width.
	Over etched	Resistor is greater than 125 percent of its intended design width.
Poly SI resistor	Pinched	Resistor is less than 90 percent of its intended design width.
Poly SI resistor	Undercut	Resistor is less than 75 percent of its intended design width.
	Bridging or excess poly SI	Bridging between discrete resistor pattern.
	Misalignment	Contacting less than 75 percent of the design separation.

1/ Reject if 25 percent of any one cell or 10 percent of any die exhibits burned or missing resistors.

3.9.1 NICR resistor. Thin film deposited and patterned usually connecting emitter fingers to emitter feed metal to control current. It can also be used as a passive element in RF IC's.

3.9.2 Poly SI resistors (bevel). Thin film of poly SI is deposited, doped, and patterned usually connecting emitter fingers to emitter feed metal to control current. It can also be used as passive elements in RF IC's.

3.9.3 Diffused resistors (contact appearance). A diffused area connecting emitter fingers to emitter feed metal used to control current.

3.9.4 Contacts and diffusion defects (contacts are not diffused). Reject if contacts are less than 50 percent of design on 10 percent of the die. Reject any die that has a discontinuous implant or diffusion line effecting more than 10 percent of the die. A discontinuous line is a line that wanders but does not close on itself. Reject any die where an implant or diffusion fault bridges between two diffuse areas, any two metallized stripes of any combination not intended by design. This must effect greater than 10 percent of the die. Reject any implant or diffused area that is less than 50 percent of design.

3.9.5 Passivation or oxide defects. This applies to 25 percent of a cell and 10 percent of the die. Reject any active junction not covered by passivation or glassivation. Reject for absence of passivation or oxide visible at the edge and continuing under the metallization causing a short between the metal and the underlying material (unless by design). Reject for passivation or oxide defects that allows bridging between any two metallized stripes.

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4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Exceptions or additions to the inspection method.

b. Where applicable, any conflicts with approved circuit design topology or construction.

c. Where applicable, gauges, drawings, and photographs that are to be used as standards for operator comparison.

d. When applicable, specific magnification.

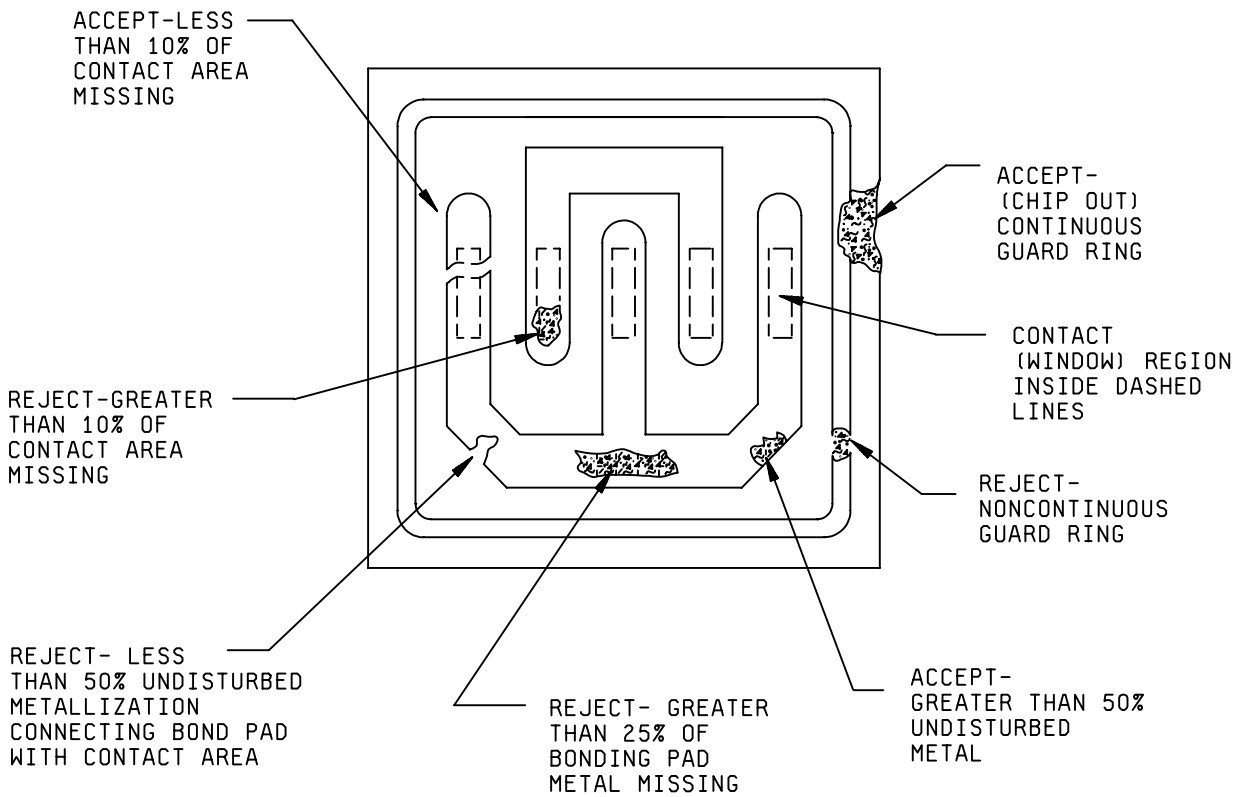

FIGURE 2070-1. Metallization scratches and voids (expanded contact).

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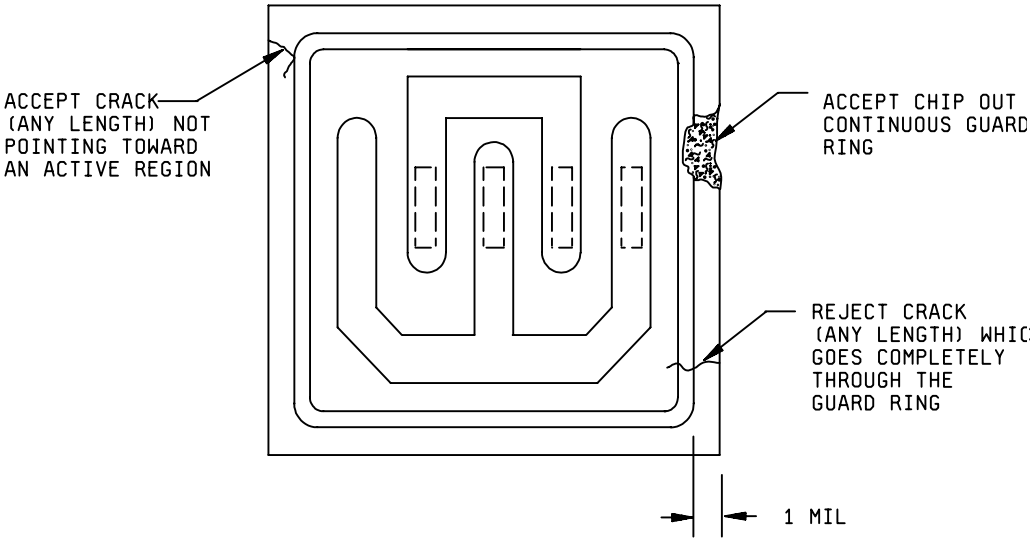
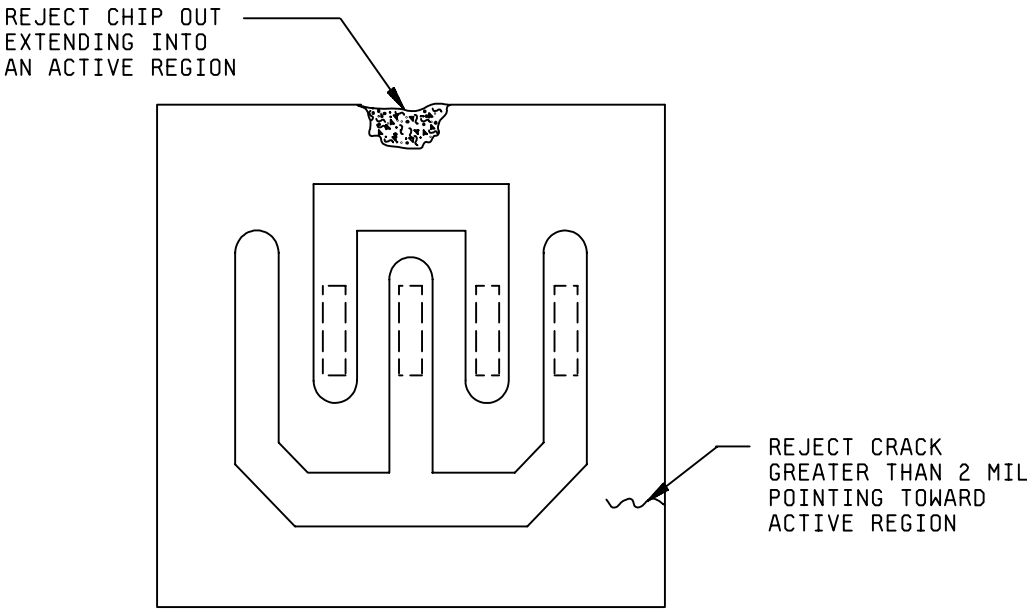


Die with guard ring.



Die without guard ring.

FIGURE 2070-2. Cracks and chips.

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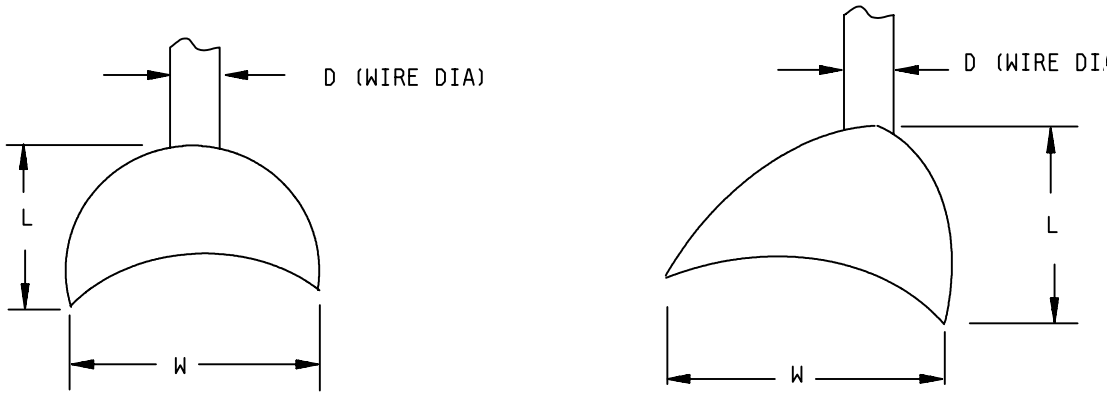
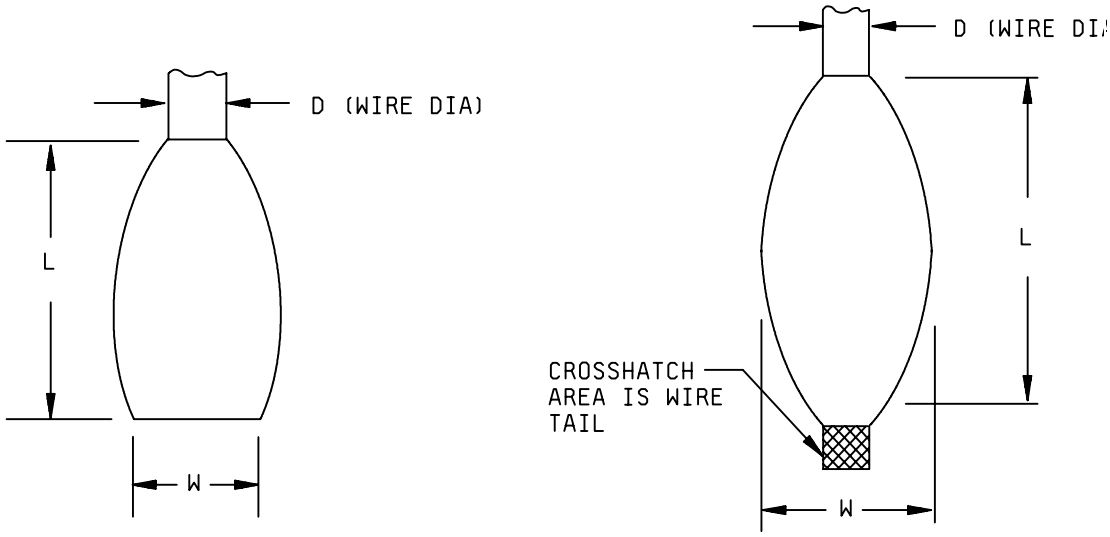


Tailless or crescent.

NOTES:
1.2 D ≤ W ≤ 5.0 D (width)
0.5 D ≤ L ≤ 3.0 D (length)



Wedge.

Ultrasonic

NOTES:
1. 1.0 D ≤ W ≤ 3.0 D (width)
2. 1.5 D ≤ L ≤ 5.0 D (length)

Thermocompression

NOTES:
1. 1.2 D ≤ W ≤ 3.0 D (width)
2. 1.5 D ≤ L ≤ 5.0 D (length)

FIGURE 2070-3. Bond dimensions.

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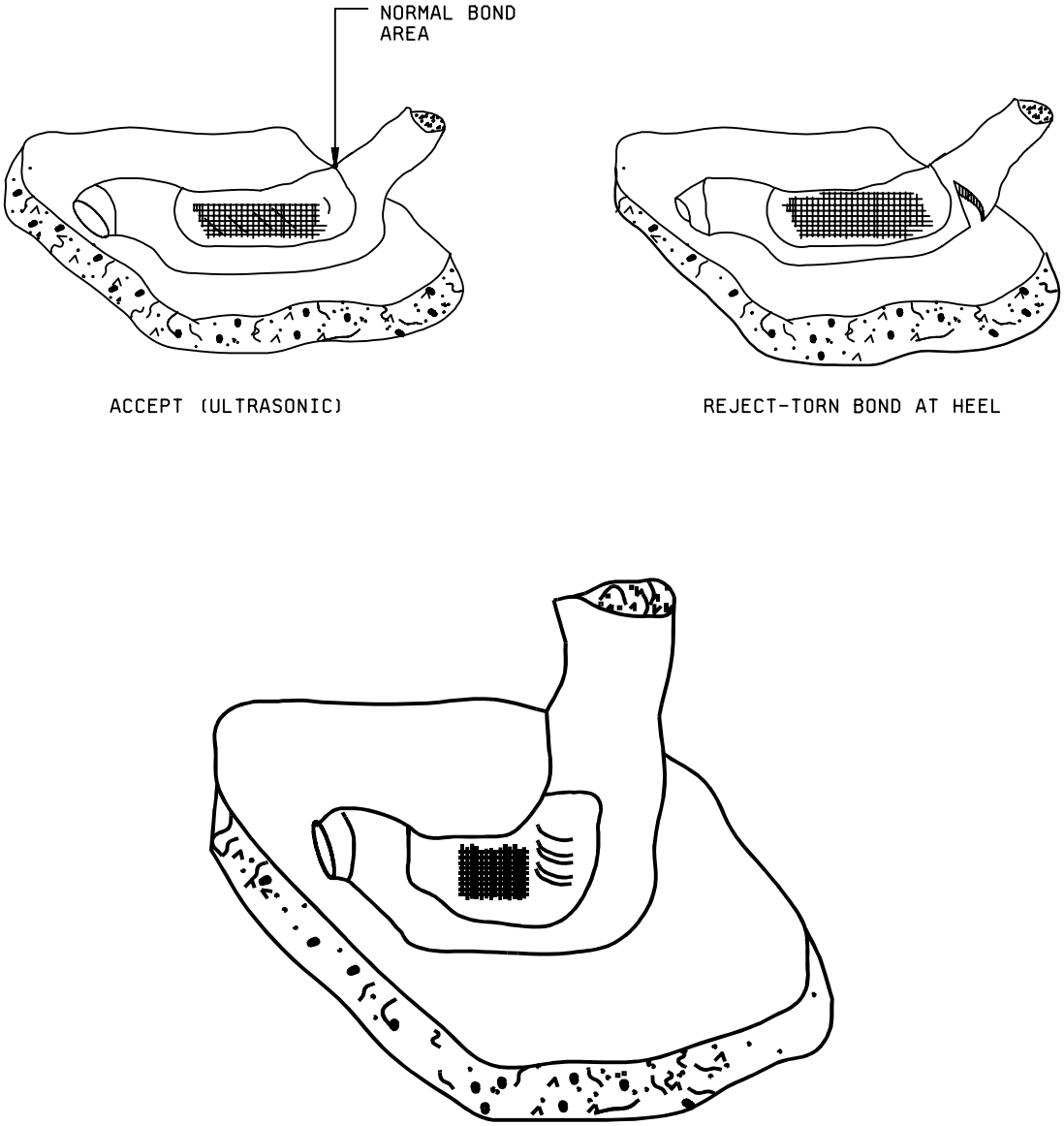

FIGURE 2070-4. Lifted/torn bonds.

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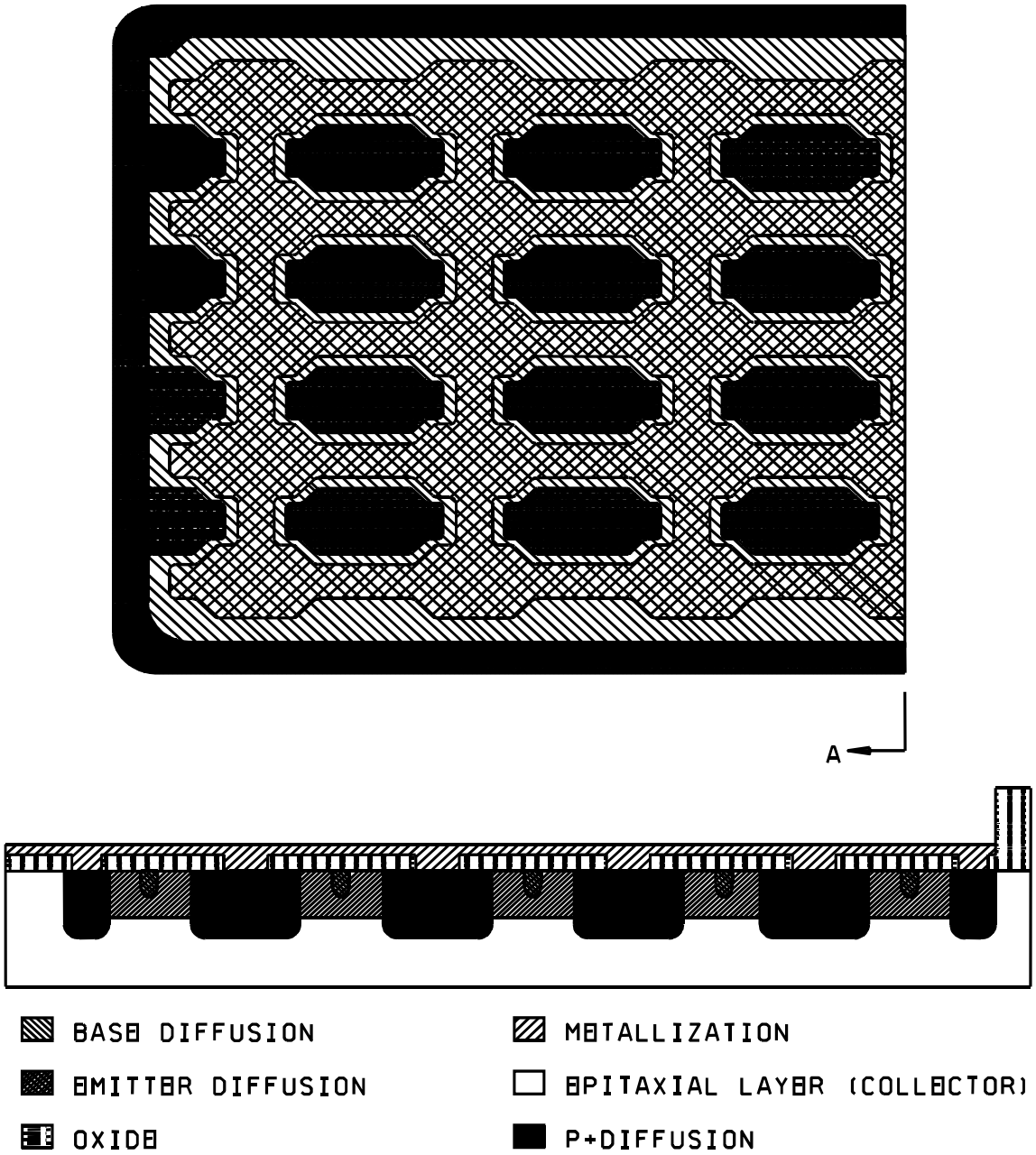

FIGURE 2070-5. Mesh geometry.

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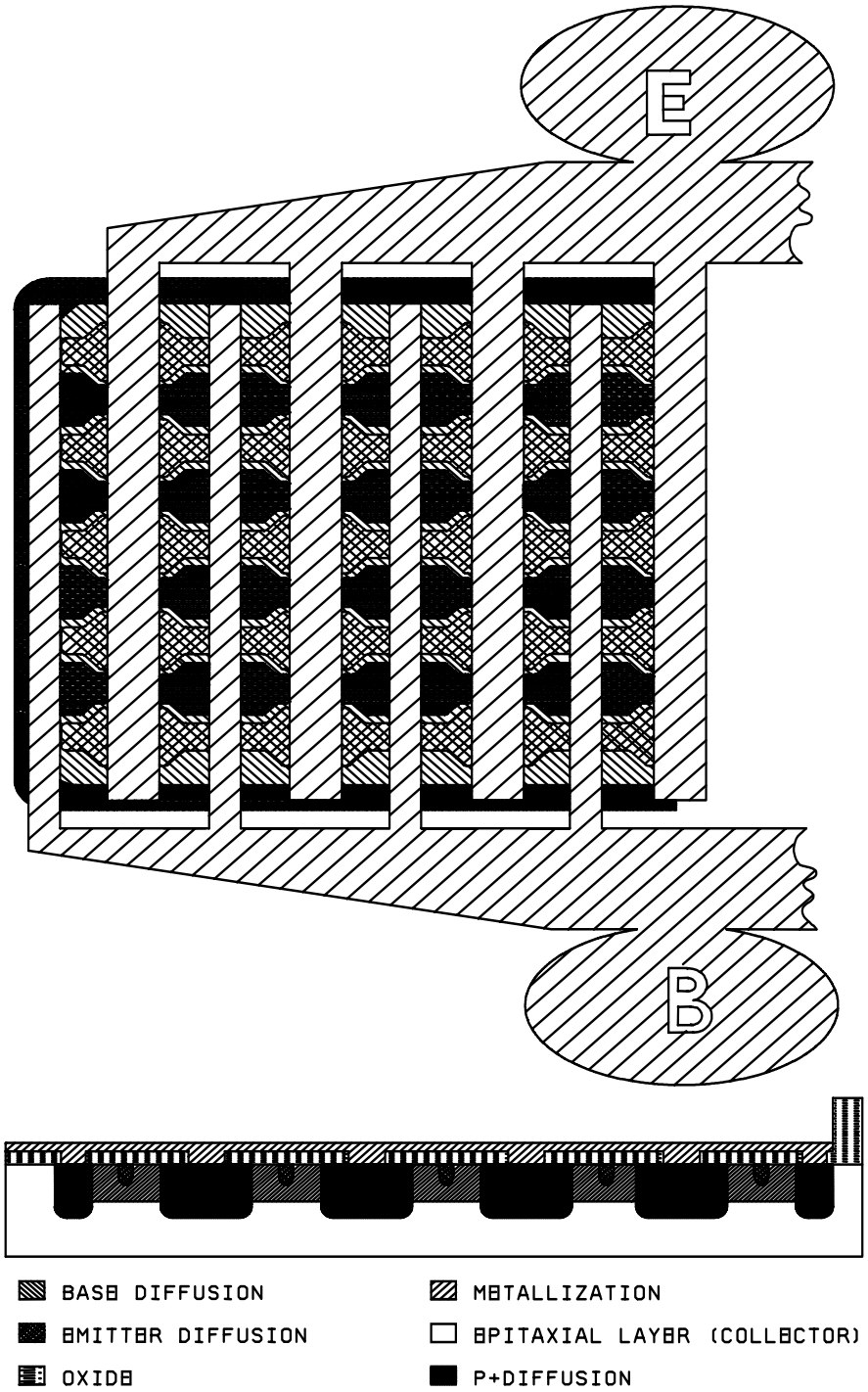

FIGURE 2070-5. Mesh geometry - Continued.

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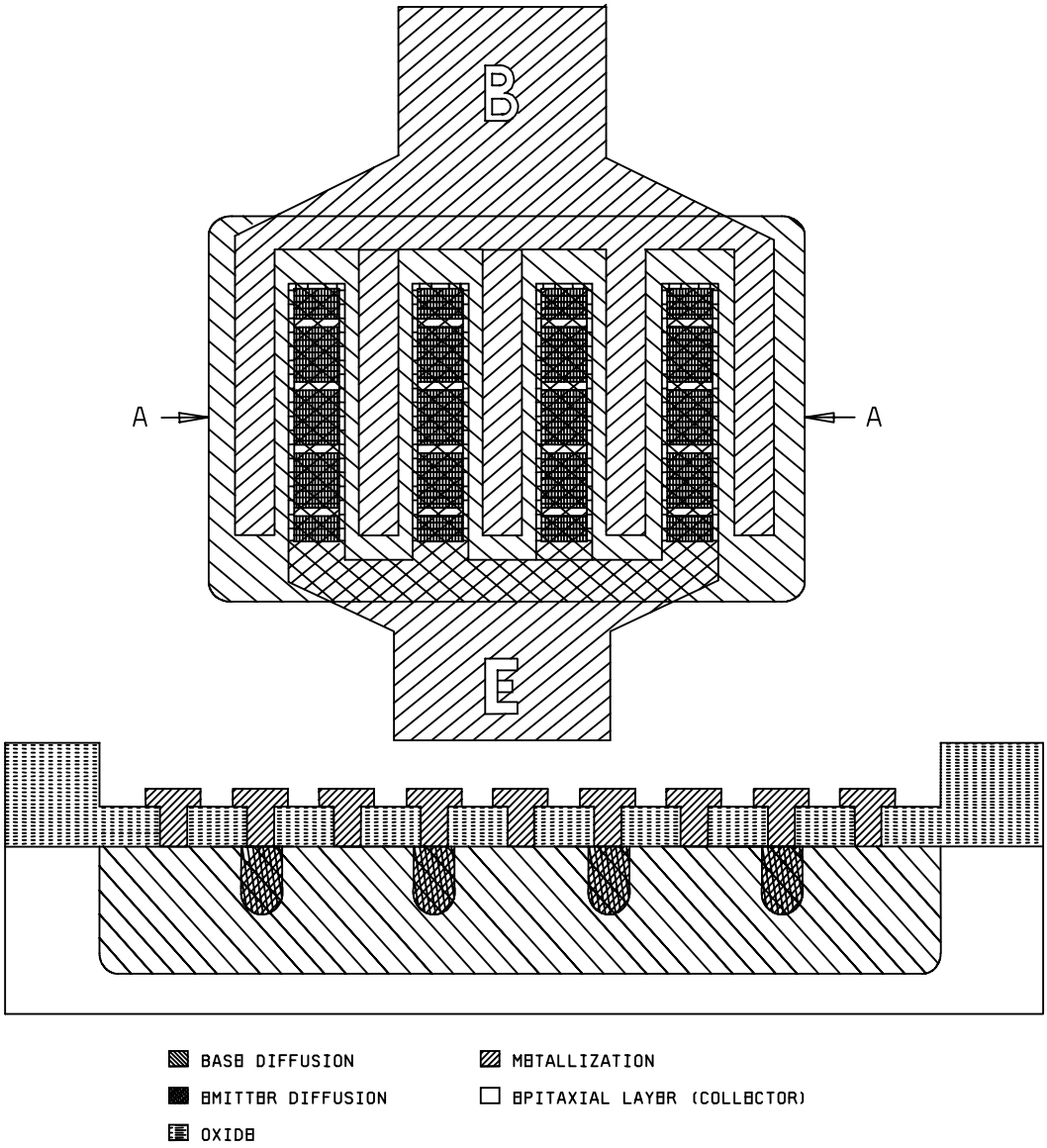

FIGURE 2070-6. Interdigitated geometry.

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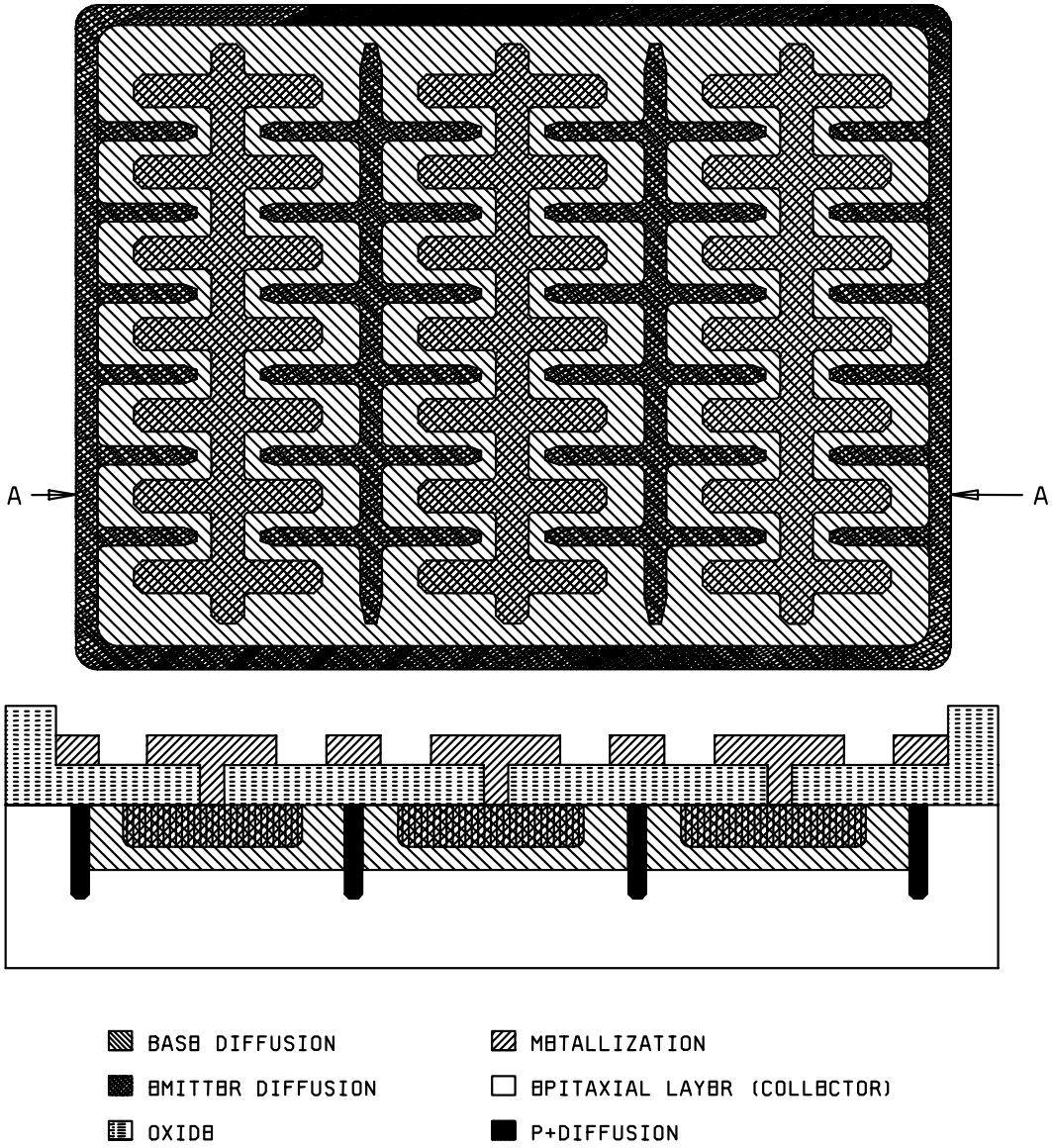

FIGURE 2070-7. Spine geometry.

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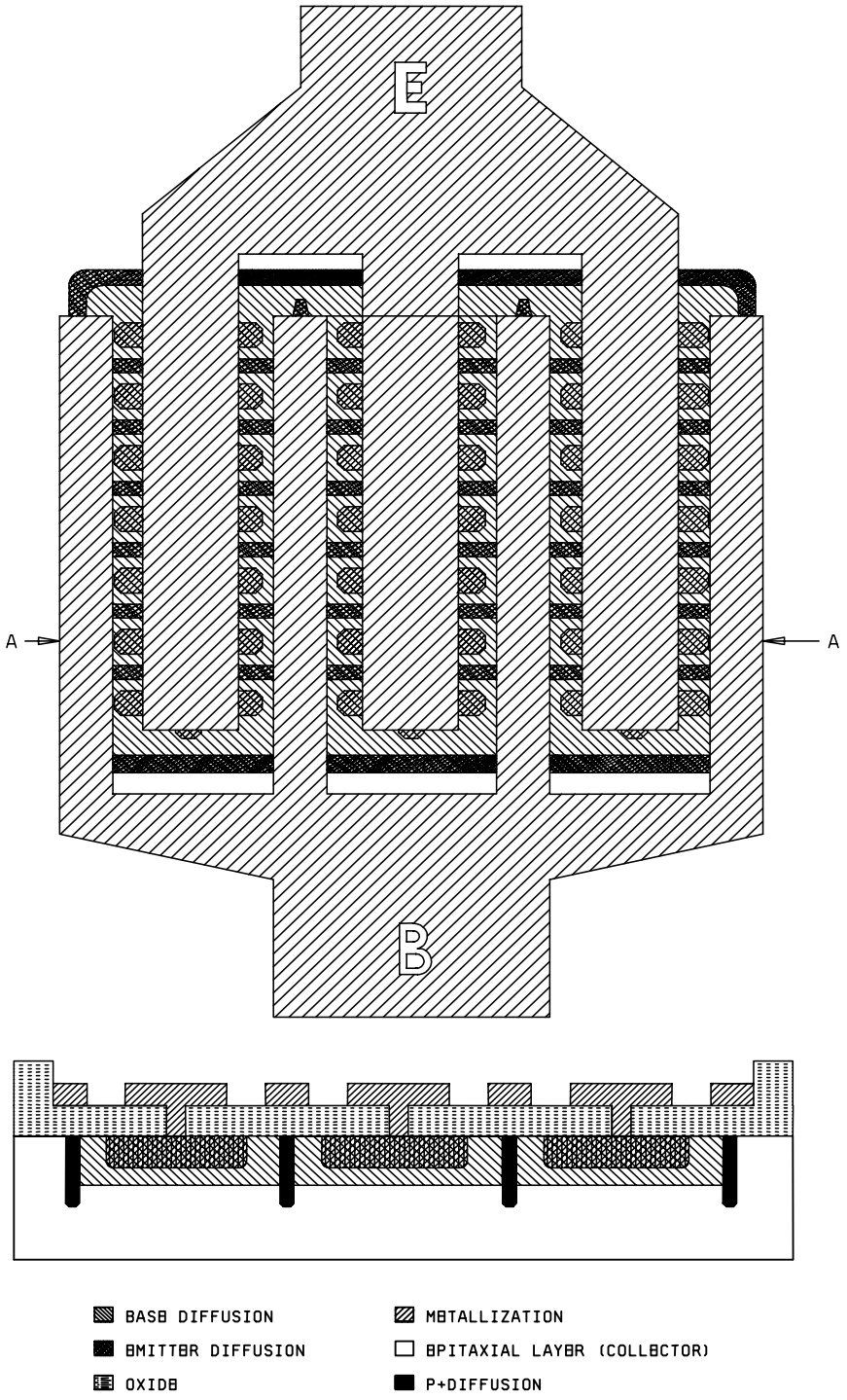

FIGURE 2070-7. Spine geometry - Continued.

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METHOD 2071.6

VISUAL AND MECHANICAL EXAMINATION

1. Purpose. The purpose of this test method is to verify the workmanship of hermetically packaged devices. This method shall also be utilized to inspect for damage due to handling, assembly, and test of the packaged device. This test is normally employed at outgoing inspection within the device manufacturer's facility, or as an incoming inspection of the assembled device.

2. Apparatus. Apparatus used in this test shall be capable of demonstrating device conformance to the applicable requirements of the individual specification sheet. This includes optical equipment capable of magnification of 3X minimum to as specified herein, with a large field of view such as an illuminated ring magnifier.

3. Procedure. Unless otherwise specified, the device shall be examined under a magnification of 3X minimum. The field of view shall be sufficiently large to contain the entire device and allow inspection to the criteria listed in 3.1. Where inspection at a lower magnification reveals an anomaly, then inspection at a higher magnification (10X maximum, unless otherwise specified) may be performed to determine acceptability.

When a disposition is in doubt for any dimensional criteria, that dimension may be measured for verification.

3.1 Failure criteria. Devices which exhibit any of the following shall be considered rejects.

3.1.1 Rejects. Device construction (package outline), lead (terminal), identification, markings (content, placement, and legibility), and workmanship not in accordance with the applicable specification sheet shall be rejected. This includes the following.

a. Any misalignment of component parts to the extent that the package outline drawing dimensions are exceeded.

b. Visual evidence of corrosion or contamination. Discoloration is not sufficient cause for rejection. The presence of lead carbonate formations in the form of a white/yellow crystalline shall be considered evidence of contamination.

c. Damaged or bent leads or terminals which precludes their use in the intended application.

d. Defective finish: Evidence of blistering, or evidence of non-adhesion, peeling, or flaking which exposes underplate or base metal.

e. Burrs that will cause lead or terminal dimensions to be exceeded.

f. Foreign material (including solder or other metallization) bridging leads or otherwise interfering with the normal application of the device. Where adherence of foreign material is in question, devices may be subjected to a clean filtered air stream (suction or expulsion) or an isopropyl alcohol wash and then reinspected.

g. Protrusions beyond seating plane that will interfere with proper seating of the device.

h. Missing welds or crimps.

i. Damage causing distortion of a flange beyond its normal configuration.

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j. Damage to a stud (thread damage or bending) which restricts normal mounting.

k. Dents in metal lids which precludes their use in the intended application or causing a defect in the finish (see 3.1.1.d).

l. Gaps, separations, or other openings that are not part of the normal design configuration.

m. Tubulation weld: Any fracture or split in the tubulation weld.

n. Weld alignment: Base weld mating surfaces not parallel, or that precludes intended use.

3.1.1.1 Failure criteria for lead/terminal seal area of metal can devices.

a. Radial cracks (except meniscus cracks) that extend more than one-half of the distance from the pin to the outer member (see figure 2071-1). Radial cracks that originate from the outer member.

b. Circumferential cracks (except meniscus cracks) that extend more than 90 degrees around the seal center (see figure 2071-2).

c. Open surface bubble(s) in strings or clusters that exceed two-thirds of the distance between the lead and the package wall.

d. Visible subsurface bubbles that exceed the following:

(1) Large bubbles or voids that exceed one-third of the glass sealing area (see figure 2071-3).

(2) Single bubble or void that is larger than two-thirds of the distance between the lead and the package wall at the site of the inclusion and extends more than one-third of the glass seal depth (see figure 2071-4).

(3) Two bubbles in a line totaling more than two-thirds of the distance from pin to case (see figure 2071-5).

(4) Interconnecting bubbles greater than two-thirds of the distance between pin and case (see figure 2071-6).

e. Except as designed, re-entrant seals which exhibit non-uniform wicking or negative wicking.

f. Twenty-five percent or greater of the radius length from the center of the feedthrough to the edge of the glass eyelet.

g. Glass meniscus cracks that are not located within one-half of the distance between the lead to the case (see figure 2071-7). The glass meniscus is defined as that area of glass that wicks up the lead or terminal.

h. Any chip-out of ceramic or sealing glass that penetrates the sealing glass deeper than the glass meniscus plane. Exposed base metal as a result of meniscus chip outs are acceptable if the exposed area is no deeper than .010 inch (0.25 mm) or 50 percent of lead diameter, whichever is greater (see figure 2071-8).

3.1.1.2 Failure criteria for ceramic packages. Failure criteria for ceramic packages (see method 2009 of MIL-STD-883).

3.1.1.3 Failure criteria for opaque glass body devices. Failure criteria for opaque glass body devices (see method 2068 of this general specification).

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3.1.1.4 Transparent glass diodes, double plug construction.

a. Any evidence of a crack, fracture, or a chipout closer to the die than 50 percent of the designed seal length shall be rejected. Area of examination shall be as shown on figure 2071-9.

b. Any crack that terminates in the axial direction is cause for rejection

c. Meniscus cracks are not cause for rejection.

d. Any chip out that exposes base metal shall be rejected.

3.1.1.5 Transparent glass diodes, large cavity (i.e. S-bend, C-bend, or straight-through constructions). Any crack or fracture in the glass over the area of the device cavity shall be rejected.

a. Any crack or fracture in the glass over the area of the device cavity shall be rejected.

b. Any chip out that exposes base metal shall be rejected (this does not apply to chip outs at either end of device where glass joins external lead).

c. Any crack that terminates in the axial direction is cause for rejection.

d. Meniscus cracks are not cause for rejection.

3.1.1.6 Failure criteria for hermetic packages with ceramic eyelet feedthroughs.

a. Any separation or delamination of the braze metallization from the inner diameter (ID) or outer diameter (OD) of the ceramic eyelet (see figures 2071-10 and 2071-11).

b. Any cracks or separation in the braze between the ceramic eyelet ID and the lead or the ceramic eyelet OD and the package. Any voids, depressions, or pinholes the bottom of which cannot be seen at 30X maximum magnification in the braze between the ceramic eyelet ID and the lead or the ceramic eyelet OD and the package.

c. Any discontinuation in the braze from the ceramic eyelet ID to the lead or the ceramic eyelet OD to the package exposing unplated metallization or bare ceramic (see figures 2071-12).

d. Any conductive material attached to the ceramic eyelet that reduces the designed isolation width by more than one-third unless it is demonstrated that the device voltage isolation requirement can be met with less than two-thirds of the width of the ceramic eyelet (see figures 207113 through 14).

e. Any metallization that extends beyond the height of the ceramic that is not adhered to the ceramic.

f. No cracks are allowed. Chipouts greater than .005 inch (0.127 mm) in any direction are not allowed.

4. Summary. The following conditions shall be specified in the applicable acquisition document:

a. Requirements for markings and the lead (terminal) or pin identification.

b. Detailed requirements for materials, design, construction, and workmanship.

c. Magnification requirements, if other than specified.

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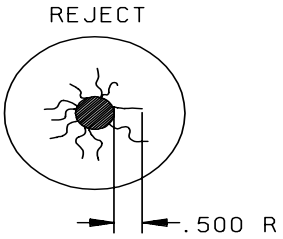

FIGURE 2071-1. Radial cracks extending more than one-half the distance from pin to outer member.

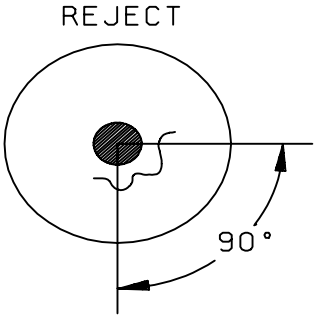

FIGURE 2071-2. Circumferential cracks.

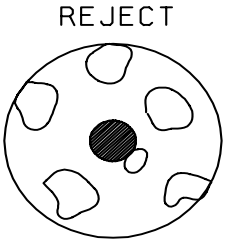

FIGURE 2071-3. Bubbles in glass exceeding one-third of the sealing area.

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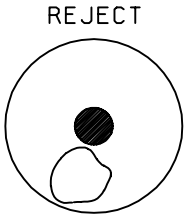

FIGURE 2071-4. Single bubble or void.

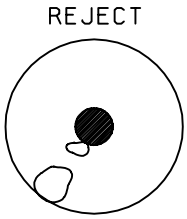

FIGURE 2071-5. Two bubbles in a line.

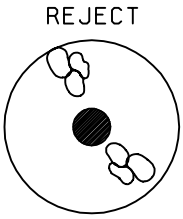

FIGURE 2071-6. Interconnecting bubbles.

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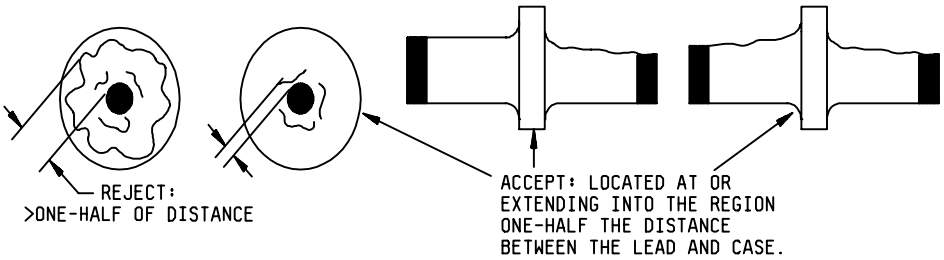

FIGURE 2071-7. Meniscus cracks.

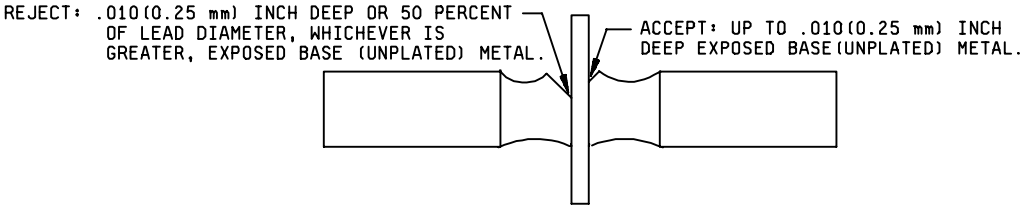

FIGURE 2071-8. Chip outs.

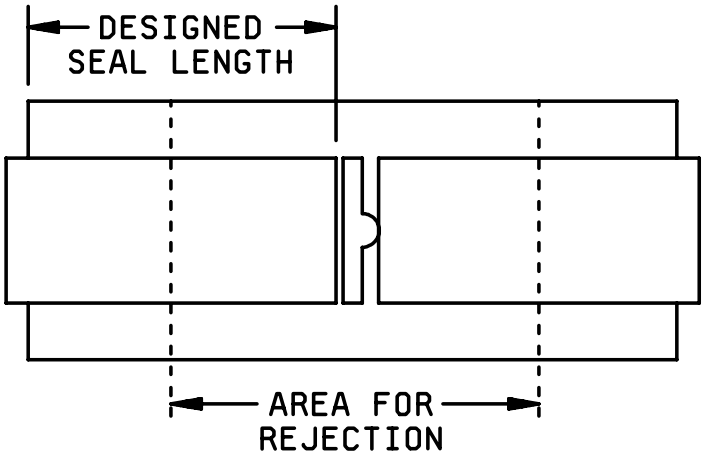

FIGURE 2071-9. Transparent glass diode (double plug construction).

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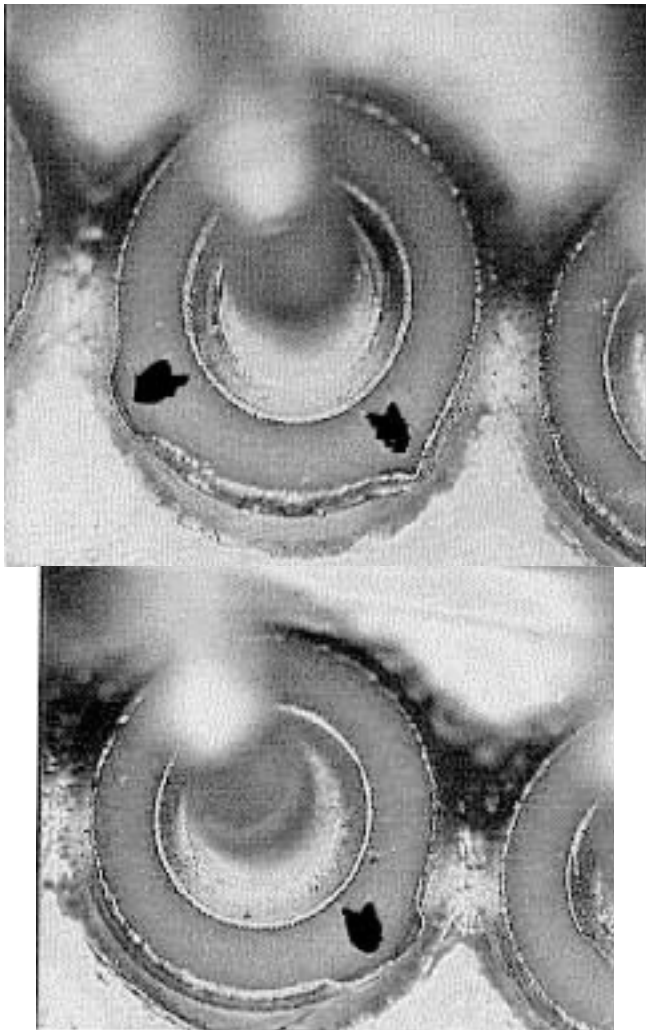

Arrows on both pictures illustrate rejectable conditions of braze separation/delamination.

FIGURE 2071-10. Braze separation/delamination.

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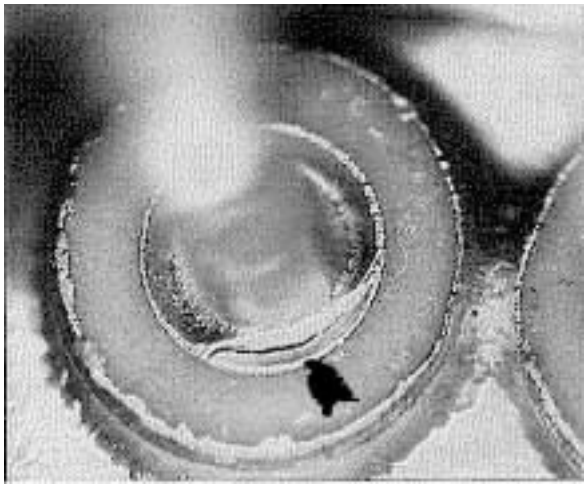

Reject: Arrow indicates a crack on the inner diameter braze metallization of the ceramic eyelet.

FIGURE 2071-11. Crack (braze metallization.

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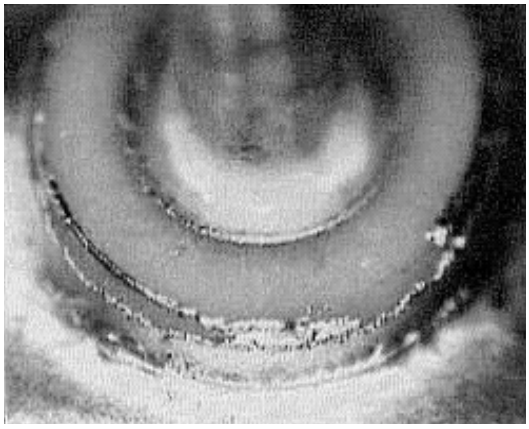

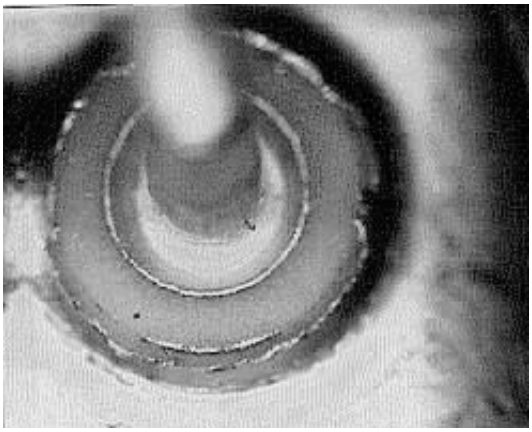

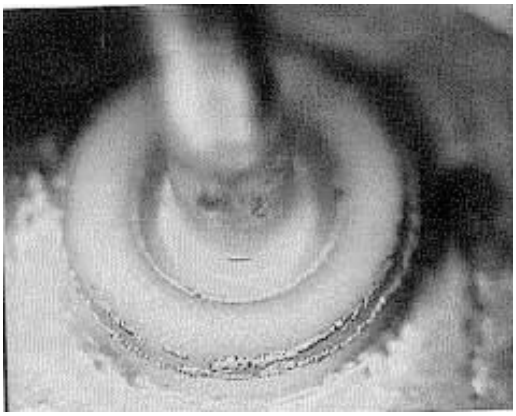

Reject: All three figures illustrate discontinuous braze metallization on the outer diameter of the ceramic eyelet.

FIGURE 2071-12. Discontinuous braze metallization.

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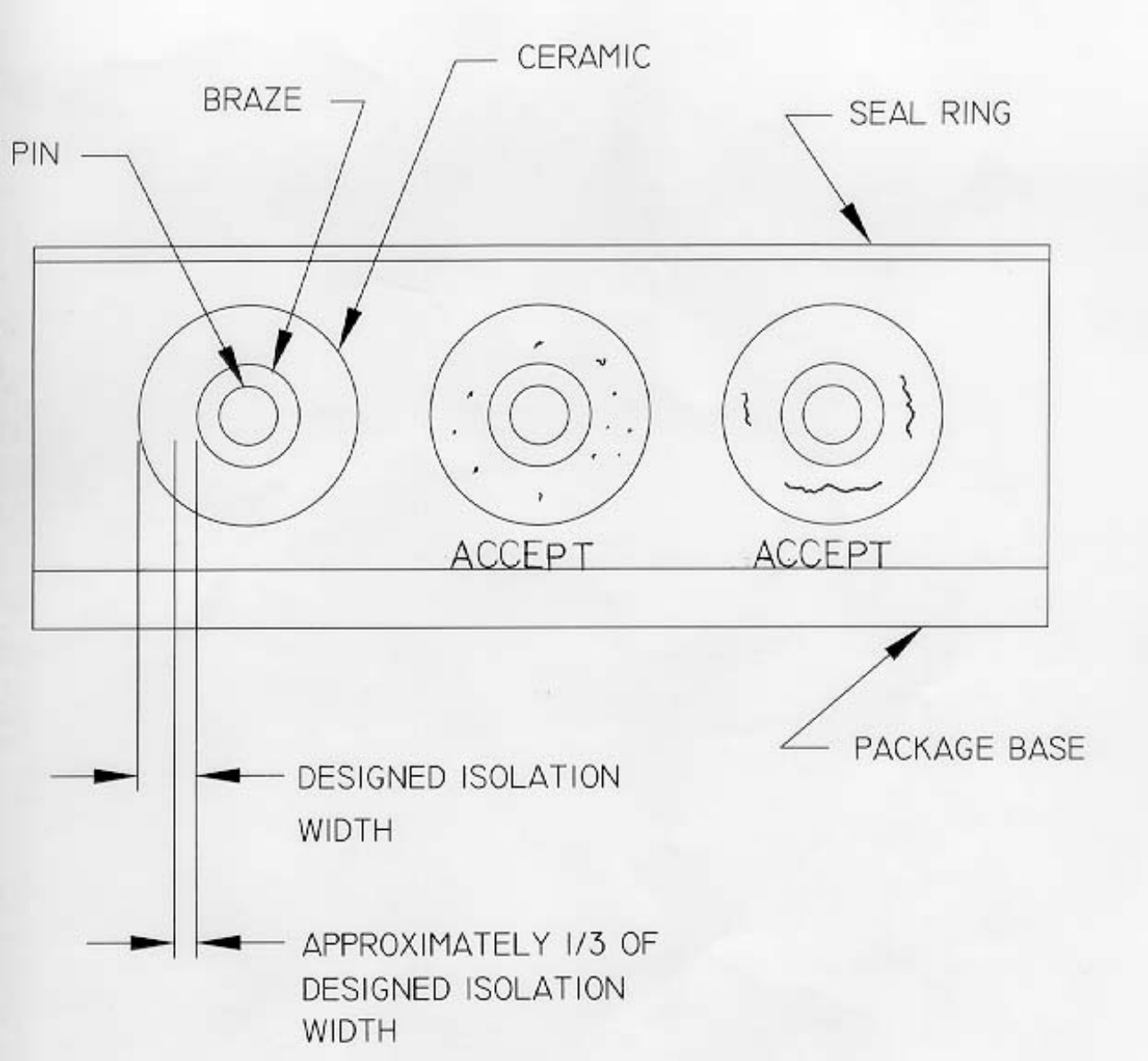

FIGURE 2071-13. Ceramic feedthrough visual inspection criteria.

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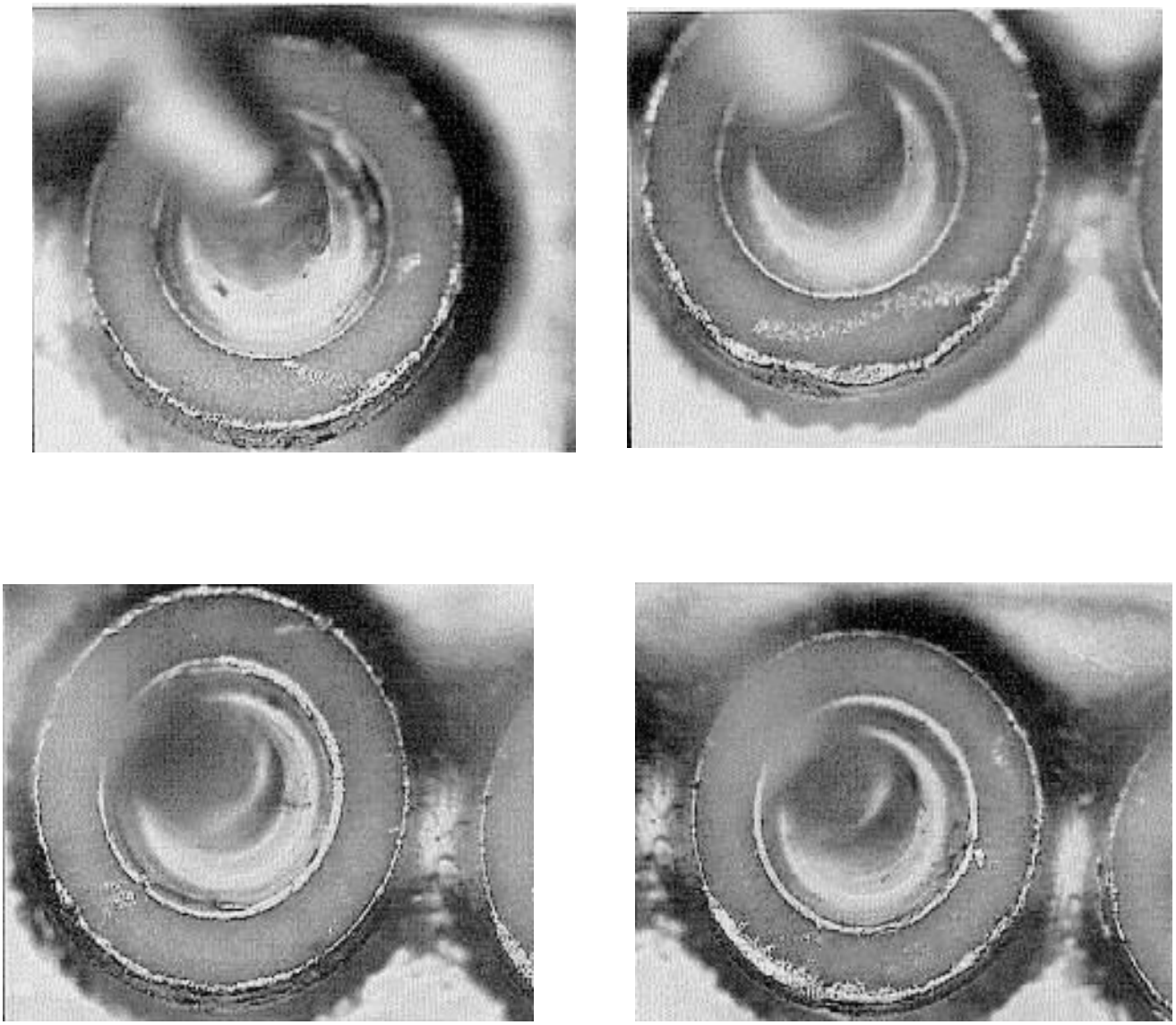

Reject: All figures indicate rejectable foreign material conditions.

FIGURE 2071-14. Rejectable foreign material conditions.

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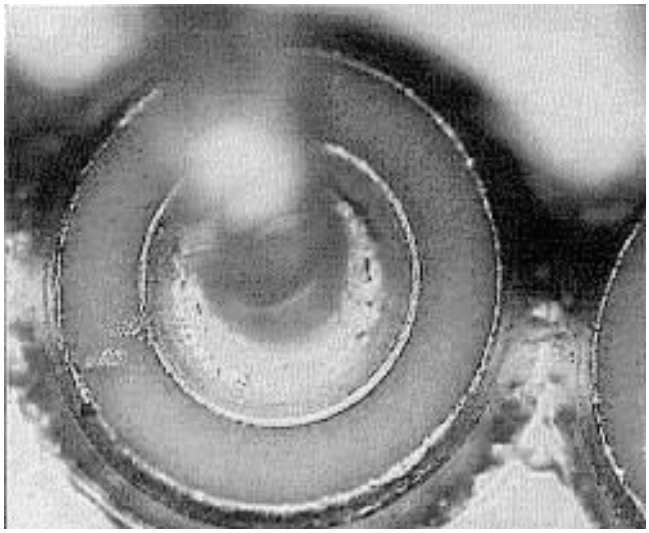

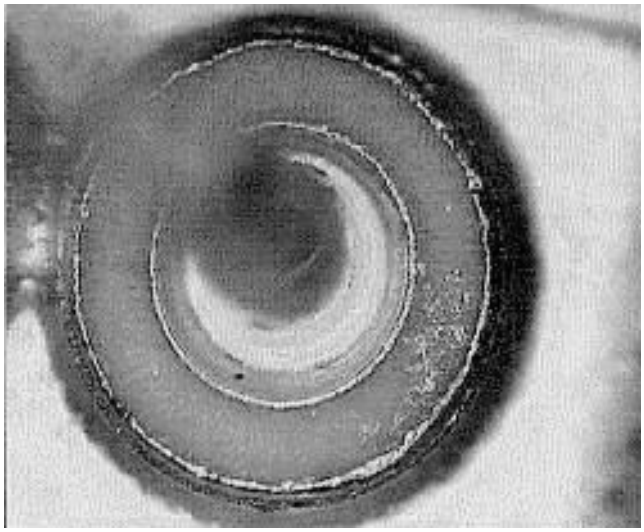

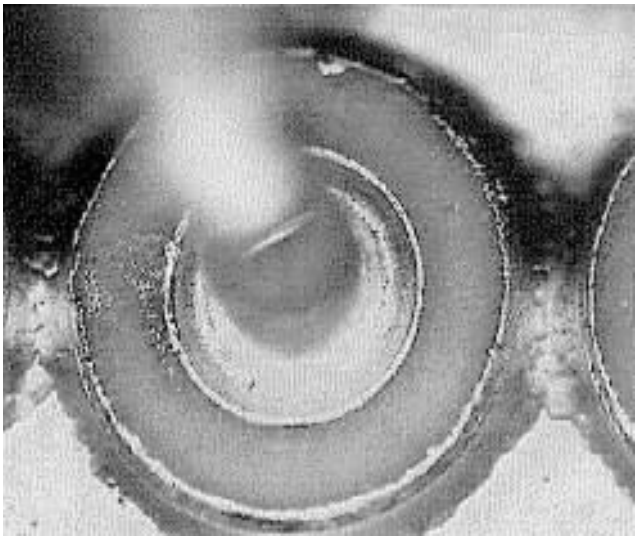

Reject: All figures indicate rejectable foreign material conditions.

FIGURE 2071-14. Rejectable foreign material conditions-continued.

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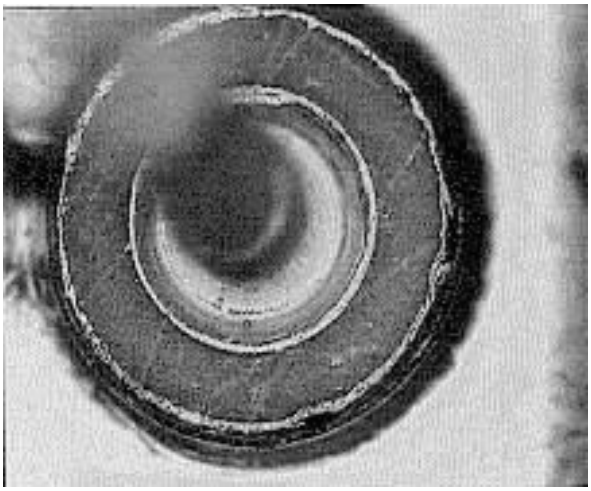

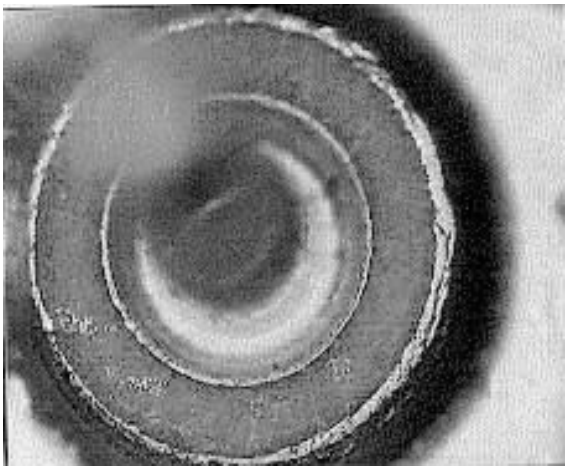

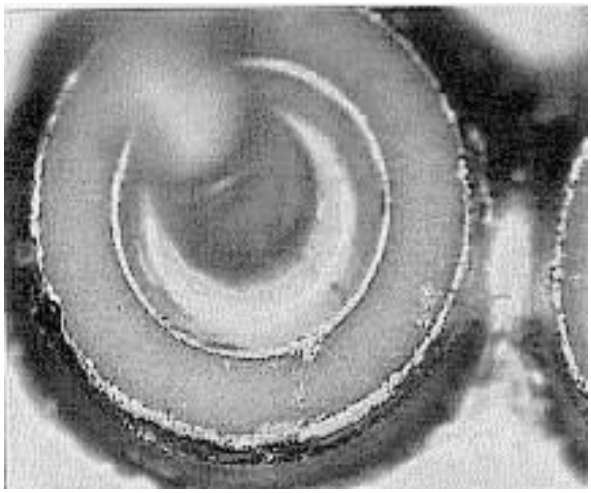

Reject: All figures indicate rejectable foreign material conditions.

FIGURE 2071-14. Rejectable foreign material conditions-continued.

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METHOD 2072.6

INTERNAL VISUAL TRANSISTOR (PRE-CAP) INSPECTION

1. Purpose. The purpose of this test method is to verify the construction and workmanship of bipolar transistors, field effect transistors (FET), discrete monolithic, multichip, and multijunction devices excluding microwave and selected RF devices. This test will be performed prior to capping or encapsulation to detect those devices with internal defects that could lead to failures in normal application and verify compliance with the requirements of the applicable specification sheet.

2. Apparatus. The apparatus for this inspection shall consist of the following.

a. Optical equipment capable of the specified magnifications.

b. Light sources of sufficient intensity to adequately illuminate the devices being inspected.

c. Adequate fixturing for handling the devices being inspected without causing damage.

d. Adequate covered storage and transportation containers to protect devices from mechanical damage and environmental contamination.

e. Any visual standards (drawings and photographs) necessary to enable the inspector to make objective decisions as to the acceptability of the devices being examined.

3. Definitions.

3.1 Glassivation. The top layer of transparent insulating material that covers the active circuit area metallization, but excluding bonding pads.

3.2 Passivation. Silicon oxide, nitride, or other insulating material that is grown or deposited directly on the die prior to the deposition of any metal.

3.3 Wetting. The spreading, and sometimes absorption, of a liquid on or into a surface.

4. Procedure.

4.1 General. The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the requirements of the applicable specification sheet and the criteria of the specified test condition. If a specified visual inspection requirement is in conflict with the topology or construction of a specific device design, alternate inspection criteria may be included in the specification sheet. Any alternate inspection criteria contained in the specification sheet shall take precedence over the criteria of this test method. Any criteria of this test method intended for a specific device process or technology has been indicated. Where applicable, unused cells shall not be subjected to internal visual criteria.

a. Sequence of inspection. The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer. Visual criteria specified in 4.1.1, 4.1.2, 4.1.3, and 4.1.7, may be examined prior to die attachment with reexamination at low or high magnification after die attachment for these criteria. Visual criteria specified in 4.1.6.2 and 4.1.6.3 may be examined prior to lead wire bonding without reexamination after bonding.

b. Inspection control. Within the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment (one which controls airborne particle count and relative humidity). The use of an inert gas environment, such as dry nitrogen shall satisfy the requirements for storing in a controlled environment. Devices examined in accordance with this test method shall be inspected and stored in a class 100,000 environment, in accordance with FED-STD-209, except that the maximum allowable relative humidity shall not exceed 65 percent.

If devices are subjected to a high temperature bake (>+100°C) immediately prior to sealing, the humidity control is not required. Unless a cleaning operation is performed prior to sealing, devices shall be in covered containers when transferred from one controlled environment to another.

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c. Magnification. High magnification inspection shall be performed perpendicular to the die surface with normal incident illumination. Low magnification inspection shall be performed with either a monocular, binocular, or stereo microscope, and the inspection performed within any appropriate angle, with the device under suitable illumination. The inspection criteria of 4.1.4 and 4.1.6.1 may be examined at "high magnification" at the manufacturer's option. High power magnification may be used to verify a discrepancy noted at a low power.

TABLE 2072-1. Die magnification requirements.

Chip size 1/	High magnification	Low magnification
30 mils or less	100X to 200X	30X to 50X
31 to 60 mils	75X to 150X	30X to 50X
61 to 150 mils	35X to 120X	10X to 30X
Greater than 150 mils	25X to 75X	10X to 30X

1/ Length of shortest dimension.

d. Reinspection. Unless a specific magnification is required by the specification sheet, when inspection for product acceptance or quality verification of the visual requirements herein is conducted subsequent to the manufacturer's successful inspection, the additional inspection may be performed at any magnification specified herein. If sampling is used rather than 100 percent reinspection, reevaluation of lot quality in accordance with the Reevaluation of lot quality of MIL-PRF-19500 shall be used.

e. Exclusions. If conditional exclusions have been allowed, specific instruction as to the location and conditions for which the exclusion can be applied shall be documented in the assembly inspection drawing.

4.1.1 Die metallization defects (high magnification). A die which exhibits any of the following defects shall be rejected.

4.1.1.1 Metallization, scratches, and voids exposing underlying material (see figure 2072-1).

a. A scratch or void that severs the innermost metallized guard ring.

b. Any die containing a void in the metallization at the bonding pad covering more than 25 percent of the pad area.

c. For devices with nonexpanded contacts and all power devices. Any scratch or void which isolates more than 25 percent of the total metallization of an active region from the bonding pad.

d. For all devices with expanded contacts. A scratch or void, whether or not underlying material is exposed, which leaves less than 50 percent undisturbed metal width in the metal connecting the pad and contact regions.

e. For expanded contacts with more than 10 contact regions. A scratch or void extending across more than 50 percent of the first half of any contact region (beginning at the bonding area) in more than 10 percent of the contact regions.

f. For expanded contacts with less than 10 contact regions. A scratch or void in the contact area which isolates more than 10 percent of the metallized area from the bonding pad.

4.1.1.2 Metallization corrosion. Any metallization which shows evidence of corrosion.

4.1.1.3 Metallization adherence. Any metallization which has lifted, peeled, or blistered.

4.1.1.4 Metallization probing. Criteria contained in 4.1.1.1 shall apply as limitations on probing damage.

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4.1.1.5 Metallization bridging. Metallization bridging between two normally unconnected metallization paths which reduces the separation, such that a line of oxide is not visible (no less than 0.1 mil) when viewed at the prescribed high magnification.

4.1.1.6 Metallization alignment.

a. Except by design, contact window that has less than 50 percent of its area covered by continuous metallization.

b. A metallization path not intended to cover a contact window which is separated from the window by less than 0.1 mil.

c. Except by design, any misalignment to the extent that continuous passivation color cannot be seen (i.e., metallization crossing passivation).

4.1.2 Passivation and diffusion faults (high magnification). A device which exhibits any of the following defects (see figure 2072-2) shall be rejected:

a. Any diffusion fault that allows bridging between any two diffused areas, any two metallization strips, or any such combination not intended by design.

b. Any passivation fault including pinholes not covered by glassivation that exposes semiconductor material and allows bridging between any two diffused areas, any two metallization strips, or any such combination not intended by design.

c. Unless intended by design, a diffusion area which is discontinuous.

d. Except by design, an absence of passivation visible at the edge and continuing under the metallization causing an apparent short between the metal and the underlying material (closely spaced double or triple lines on the edges of the defect indicate that it may have sufficient depth to penetrate down to the silicon).

e. Except by design, any active junction not covered by passivation or glassivation.

f. Unless by design, a contact window in a diffused area which extends across a junction.

4.1.3 Scribing and die defects (high magnification). A device which exhibits any of the following defects (see figure 2072-3) shall be rejected:

a. Unless by design, less than 0.1 mil passivation visible between active metallization or bond pad periphery and the edge of the die.

b. Any chip-out or crack in the active area.

c. Except by design, die having attached portions of the active area of another die and which exceeds 10 percent of the area of the second die.

d. Any crack which exceeds 2.0 mils in length inside the scribe grid or scribe line that points toward active metallization or active area and extends into the oxide area.

e. Any chip-out that extends to within 1.0 mil of a junction.

f. Any crack or chip-out that extends under any active metallization area.

g. Any chip-out which extends completely through the guard ring.

4.1.4 Bond inspection (low magnification). This inspection and criteria shall be the required inspection for the bond type(s) and location(s) to which they are applicable when viewed from above (see figures 2072-4 and 2072-5). Wire tail is not considered part of the bond when determining physical bond dimensions. A device which exhibits any of the following defects shall be rejected.

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4.1.4.1 Gold ball bonds.

a. Gold ball bonds on the die or package post where the ball bond diameter is less than 2.0 times or greater than 5.0 times the wire diameter.

b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.

c. Gold ball bonds where the existing wire is not within the boundaries of the bonding pad.

d. Any visible intermetallic formation at the periphery of any gold ball bond.

4.1.4.2 Wedge bonds.

a. Ultrasonic wedge bonds on the die or package post that are less than 1.2 times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 5.0 times the wire diameter in length.

b. Thermocompression wedge bonds on the die or package post that are less than 1.2 times or greater than 3.0 times the wire diameter in width or are less than 1.5 or greater than 5.0 times the wire diameter in length.

4.1.4.3 Tailless bonds (crescent).

a. Tailless bonds on the die or package post that are less than 1.2 times or greater than 5.0 times the wire diameter in width or are less than 0.5 times or greater than 3.0 times the wire diameter in length.

b. Tailless bonds where the bond impression does not cover the entire width of the wire.

4.1.4.4 General (gold ball, wedge, and tailless). As viewed from above, a device which exhibits any of the following defects shall be rejected.

a. Bonds on the die where less than 75 percent of the bond is within the unglassivated bonding pad area (except where due to geometry, the bonding pad is smaller than the bond, the criteria shall be 50 percent).

b. Wire bond tails that extend over and make contact with any metallization not covered by glassivation and not connected to the wire.

c. Wire bond tails that exceed two wire diameters in length at the bonding pad or four wire diameters in length at the package post.

d. Bonds on the package post that are not bonded entirely on the flat surface of the post top.

e. A bond on top of another bond.

f. Bonds placed so that the separation between bonds and adjacent unglassivated die metallization is less than 1.0 mil.

g. Bonds placed so that the separation between bonds and adjacent glassivated die metallization is less than 0.25 mil.

h. Bonds placed so that the separation between adjacent bonds is less than 0.25 mil. This criteria does not apply to designs which employ multiple bond wires in place of a single wire.

i. Bonds located where any of the bond is placed on an area containing die preform mounting material.

j. Repair on conductors by bridging or addition of bonding wire or ribbon.

k. For aluminum wires over 2.0 mils diameter, the bond width shall not be less than 1.0 times the wire diameter.

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4.1.5 Internal lead wires (low magnification). This inspection and criteria shall be required inspection for the location(s) to which they are applicable when viewed from above. A device which exhibits any of the following defects shall be rejected.

a. Any wire that comes closer than two wire diameters or 5 mils, whichever is less, to unglassivated operating metallization, another wire (common wires and pigtails excluded) package post, unpassivated die area, or any portion of the package, including the plane of the lid to be attached. (Within a 5.0 mil spherical radial distance from the perimeter of the bond on the die surface, the separation can be 1.0 mil.)

b. Nicks, tears, bonds, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent.

c. Missing or extra lead wires.

d. Bond lifting or tearing at interface of pad and wire (see figure 2072-5).

e. Any wire which runs from die bonding pad to package post and has no arc or stress relief.

f. Except in common connectors, wires which cross other wires.

g. Wire(s) not in accordance with bonding diagram.

h. Wire is kinked (unintended sharp bend) with an interior angle of less than 90 degrees or twisted to an extent that stress marks appear.

i. Wire (ball bonded devices) not within 10 degrees of the perpendicular to the surface of the chip for a distance of greater than 0.5 mil before bending toward the package post or other termination point.

j. Excessive lead burn at lead post weld.

k. Pigtail longer than 50 percent of post diameter.

l. A bow or loop between double bonds at post greater than four times wire diameter.

m. Excessive loops, bows, or sags in any wire such that it could short to another wire, to another pad, to another package post, to the die or touch any portion of the package.

n. When clips are used, solder fillets shall encompass at least 50 percent of the clip-to-die and post-to-clip periphery. There shall be no deformation or plating defects on the clip.

4.1.6 Package conditions (magnification as indicated). A device which exhibits any of the following defects shall be rejected.

4.1.6.1 Conductive foreign material on die surface. All foreign material or particles may be blown off with a nominal gas blow (approximately 20 psi (138 kPa)) or removed with a soft camel hair brush. The device shall then be inspected for the following criteria (low magnification):

a. Loosely attached foreign particles (conductive particles which are attached by less than one-half of their largest dimension) which are present on the surface of the die that are large enough to bridge the narrowest unglassivated active metal spacing (silicon chips shall be included as conductive particles).

b. Embedded foreign particles on the die that bridge two or more metallization paths or semiconductor junctions, or any combination of metallization or junction.

c. Liquid droplets, chemical stains, or photoresist on the die surface that bridge any combinations of unglassivated metal or bare silicon areas.

d. Except for unused cells, ink on the surface of the die that covers more than 25 percent of a bonding pad area or that bridges any combination of unglassivated metallization or bare silicon areas.

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4.1.6.2 Die mounting (low magnification).

a. Die mounting material buildup that extends onto the top surface of the die or extends vertically above the top surface of the die and interferes with bonding.

b. Die to header mounting material (wetting) which is not visible on the mounting surface of the package around at least three complete sides or 75 percent of the die perimeter. Wetting criteria is not required if the devices pass an approved electrical die attach evaluation test.

c. Any flaking of the die mounting material.

d. Any balling of the die mounting material which does not exhibit a fillet when viewed from above.

4.1.6.3 Die orientation.

a. Die is not located or orientated in accordance with the applicable assembly drawing of the device.

b. Die is visibly tipped or tilted (more than 10 degrees) with respect to the die attach surface.

4.1.6.4 Internal package defects (low magnification inspection) (applicable to headers, bases, caps, and lids). As an alternative to 100-percent visual inspection of lids and caps in accordance with the criteria of 4.1.6.1.a, the lids or caps may be subjected to a suitable cleaning process and quality verification procedure approved by the qualifying activity, provided the lids or caps are subsequently held in a controlled environment until capping or preparation for seal.

a. Any header or post-plating which is blistered, flaked, cracked, or any combination thereof.

b. Any conductive particle which is attached by less than one-half of the longest dimension.

c. A bubble, or a series of interconnecting bubbles, in the glass surrounding the pins which are more than one-half the distance between the pin and body or pin-to-pin.

d. Header posts which are severely bent.

e. Any glass, die, or other material greater than 1.0 mil in its major dimension which adheres to the flange or side of the header and would impair sealing.

f. Any stain, varnish, or header discoloration which appears to extend under a die bond or wire bond.

g. For isolated stud packages:

(1) Any defect or abnormality causing the designed isolating paths between the metal island to be reduced to less than 50 percent of the design separation.

(2) A crack or chip-out in the substrate.

4.1.6.5 Presence of extraneous matter. Extraneous matter (foreign particles) shall include, but not be limited to:

a. Any foreign particle, loose or attached, greater than .003 inch (0.08 mm) or of any lesser size which is sufficient to bridge nonconnected conducting elements of the device.

b. Any wire tail extending beyond its normal end by more than two diameters at the semiconductor die pad or by more than four wire diameters at the package post (see figure 2072-6).

c. Any burr on a post (header lead) greater than .003 inch (0.08 mm) in its major dimension or of such configuration that it may break away.

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d. Excessive semiconductor die bonding material buildup. A semiconductor die shall be mounted and bonded so that it is not tilted more than 10 degrees from mounting surface. The bonding agent that accumulates around the perimeter of the semiconductor die and touches the side of the semiconductor die shall not accumulate to a thickness greater than that of the semiconductor die (see figures 2072-7 and 2072-8). Where the bonding agent is built up but is not touching the semiconductor die, the build up shall not be greater than twice the thickness of the semiconductor die. There shall be no excess semiconductor die bonding material in contact with the active surface of the semiconductor die or any lead or post, or separated from the main bonding material area (see figure 2072-9).

e. Flaking on the header or posts or anywhere inside the case.

f. Extraneous ball bonds anywhere inside case, except for attached bond residue when rebonding is allowed.

4.1.7 Glassivation and silicon nitride defects (high magnification). No device shall be acceptable that exhibits any of the following defects.

a. Glass crazing that prohibits the detection of visual criteria contained herein.

b. Any glassivation which has delaminated. (Lifting or peeling of the glassivation may be excluded from the criteria above, when it does not extend more than 1.0 mil distance from the designed periphery of the glassivation, provided that the only exposure of metal is adjacent to bond pads or of metallization leading from those pads.)

c. Except by design, two or more adjacent active metallization paths which are not covered by glassivation.

d. Unglassivated areas at the edge of bonding pad which expose silicon.

e. Glassivation which covers more than 25 percent of the design bonding pad area.

4.2 Post organic protective coating visual inspection. If devices are to be coated with an organic protective coating, the devices shall be visually examined in accordance with the criteria specified in 4.1 prior to application of the coating. After the application and cure of the organic protective coating, the devices shall be visually examined under a minimum of 10X magnification. Devices which exhibit any of the following defects shall be rejected.

a. Except by design, any unglassivated or unpassivated areas or insulating substrate which has incomplete coverage.

b. Open bubbles, cracks, or voids in the organic protective coating.

c. A bubble, or a chain of bubbles, which covers two adjacent metallized surfaces.

d. Organic protective coating which has flaked or peeled.

e. Organic protective coating which is tacky.

f. Conductive particles which are embedded in the coating and are large enough to bridge the narrowest unglassivated active metal spacing (silicon chips shall be included as conductive particles).

g. A web of varnish (organic protective coating) that connects the wire with the header.

5. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test conditions, exceptions, or additions to the test method.

b. Where applicable, any conflicts with approved circuit design topology or construction.

c. Where applicable, gauges, drawings, and photographs that are to be used as standards for operator comparison.

d. When applicable, specific magnification.

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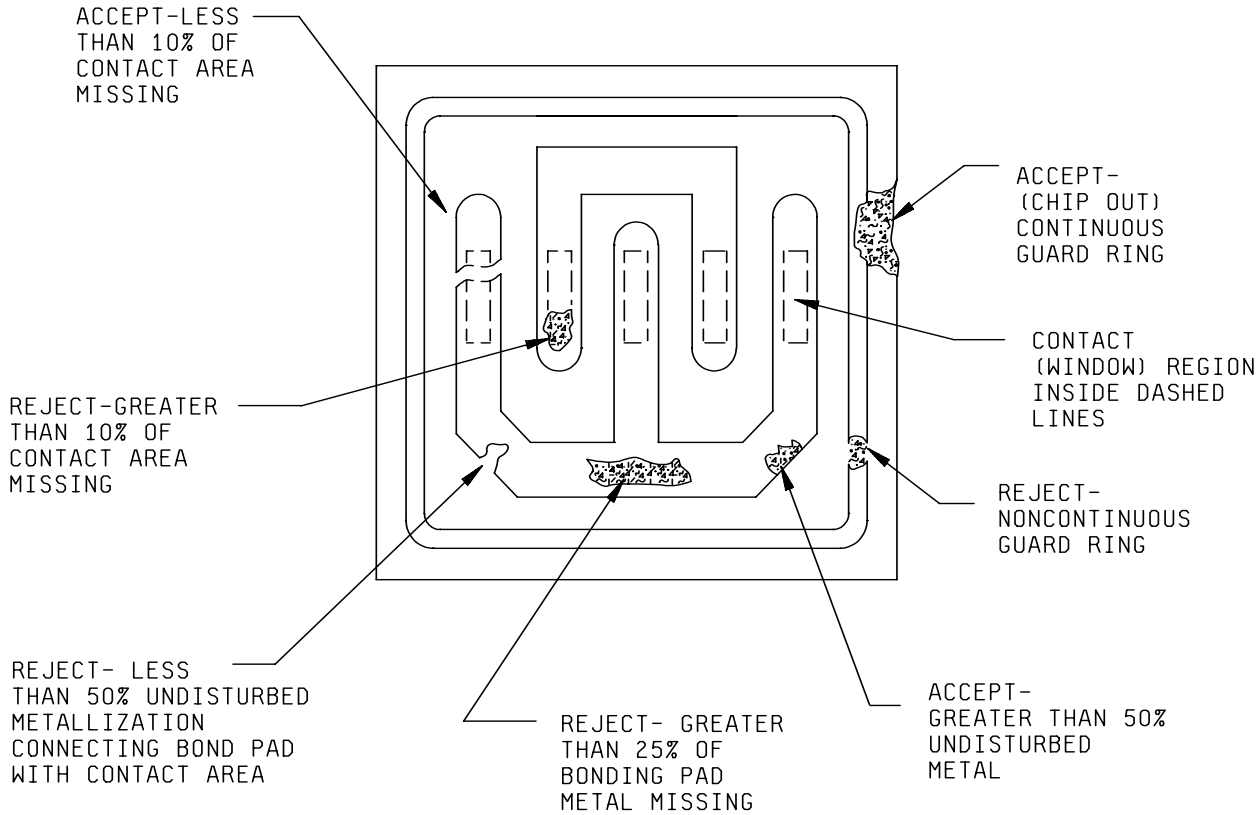

FIGURE 2072-1. Metallization scratches and voids (expanded contact).

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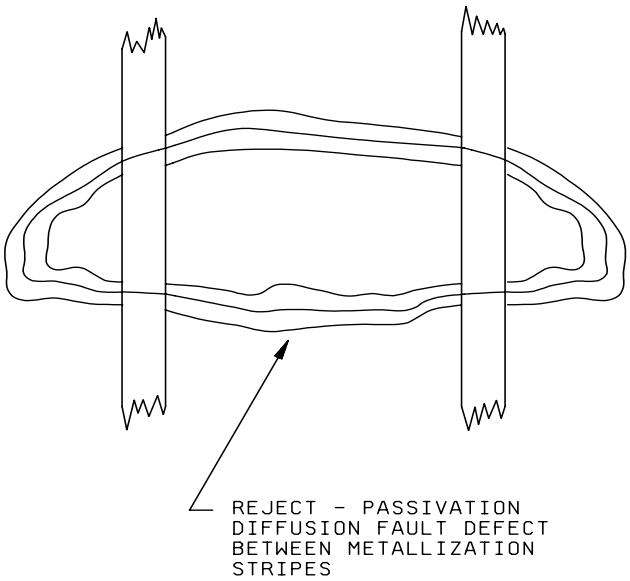

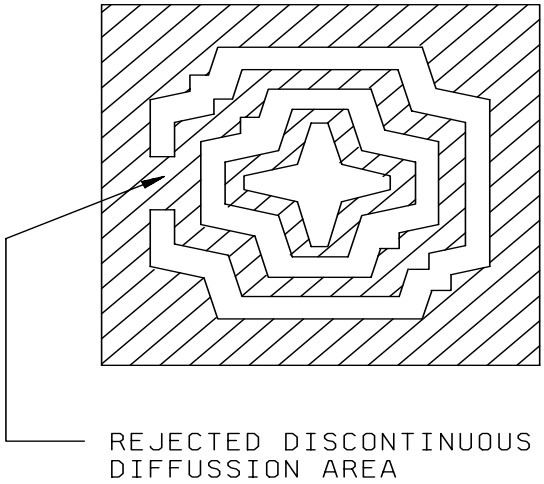

FIGURE 2072-2. Passivation and diffusion faults.

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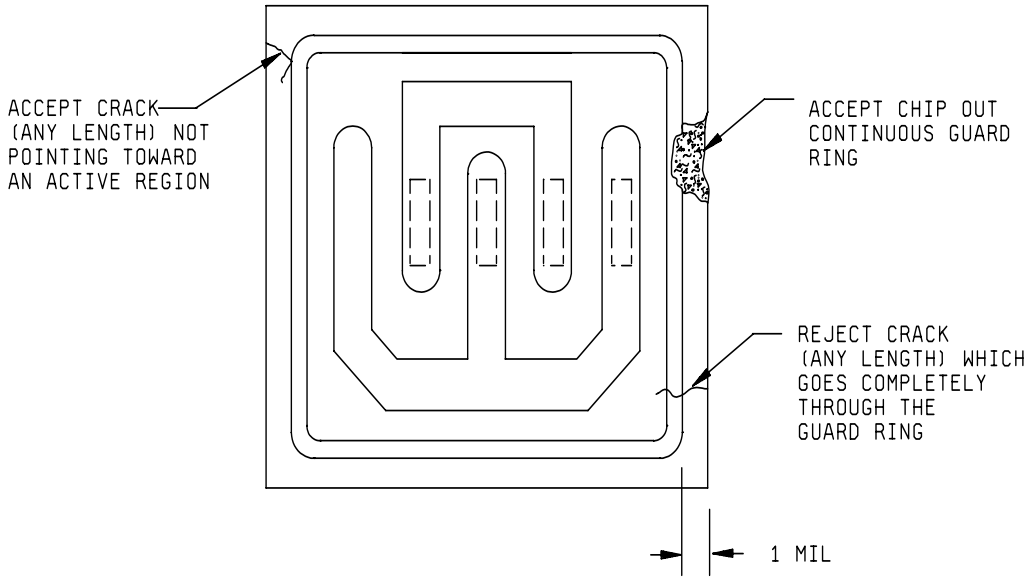
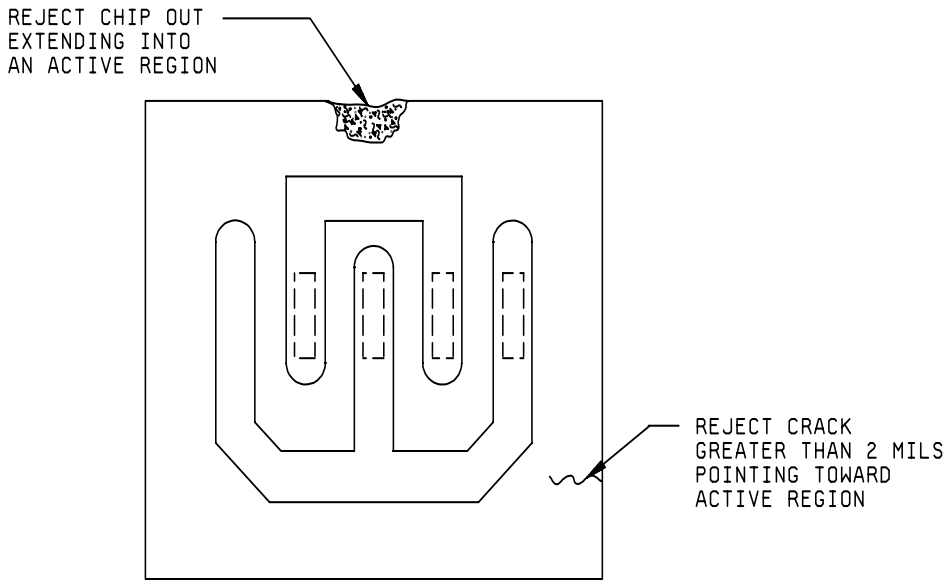


A. Die with guard ring.



B. Die without guard ring.

FIGURE 2072-3. Cracks and chips.

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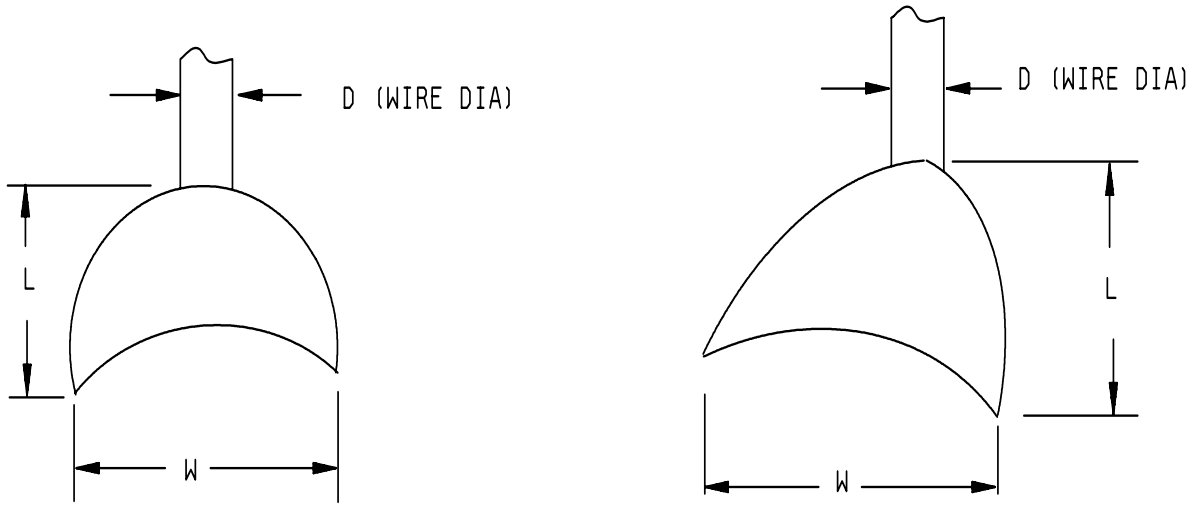
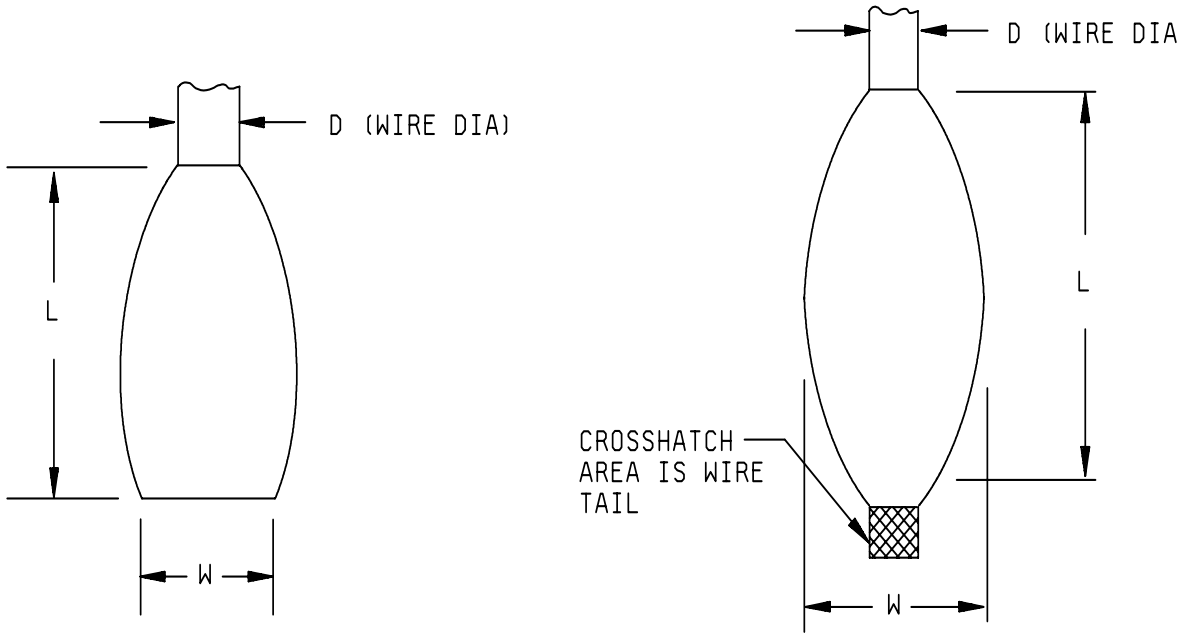


A. Tailless or crescent.

NOTES:
1. 1.2.D ≤ W ≤ 5.0 D (width).
2. 0.5 D ≤ L ≤ 3.0 D (length).



B. Wedge.

Ultrasonic

NOTES:
1. 1.2 D ≤ W ≤ 3.0 D (width).
2. 1.5 D ≤ L ≤ 5.0 D (length).

Thermocompression

NOTES:
1. 1.2 D ≤ W ≤ 3.0 D (width).
2. 1.5 D ≤ L ≤ 5.0 D (length).

FIGURE 2072-4. Bond dimensions.

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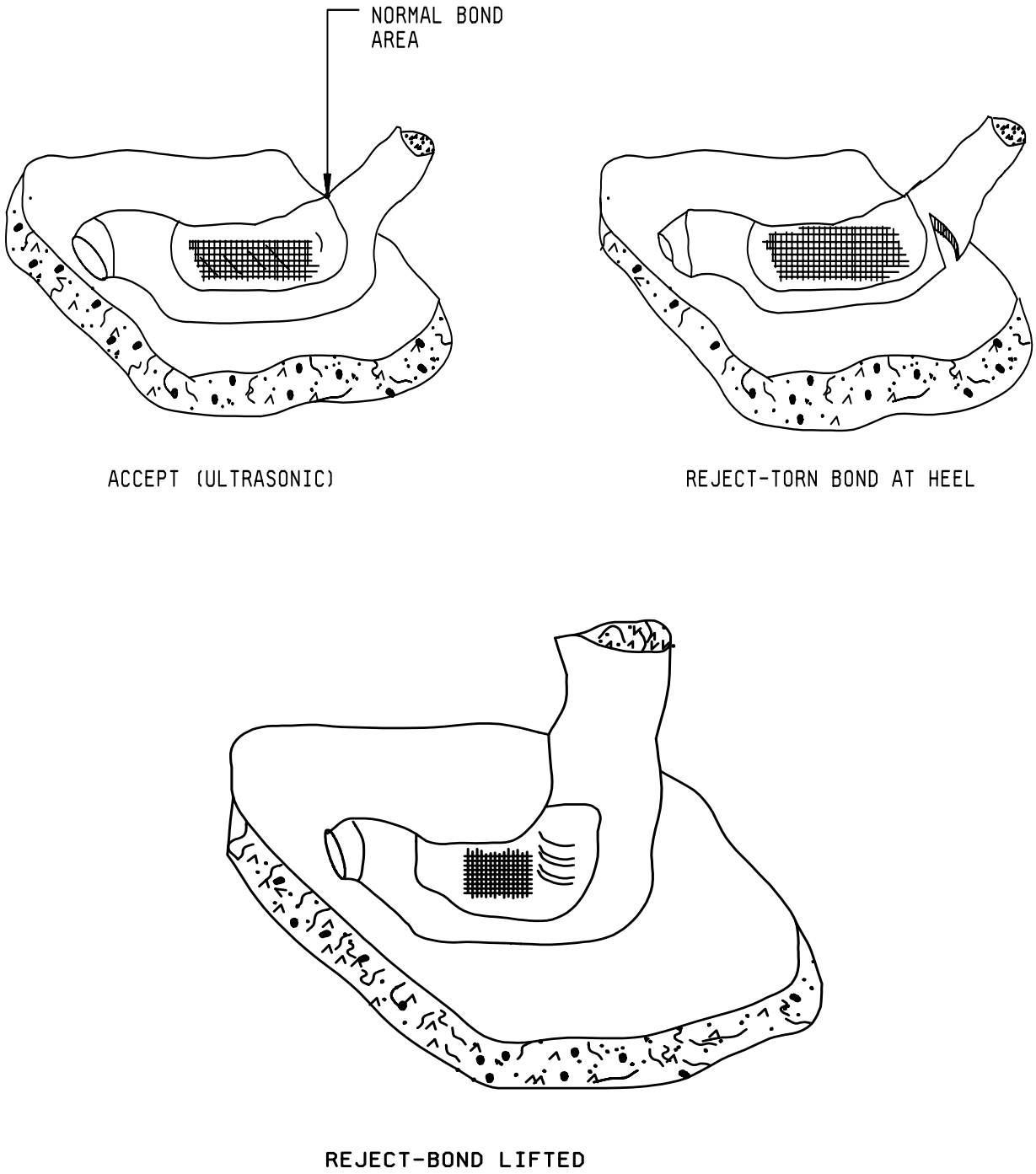

FIGURE 2072-5. Lift/torn bonds.

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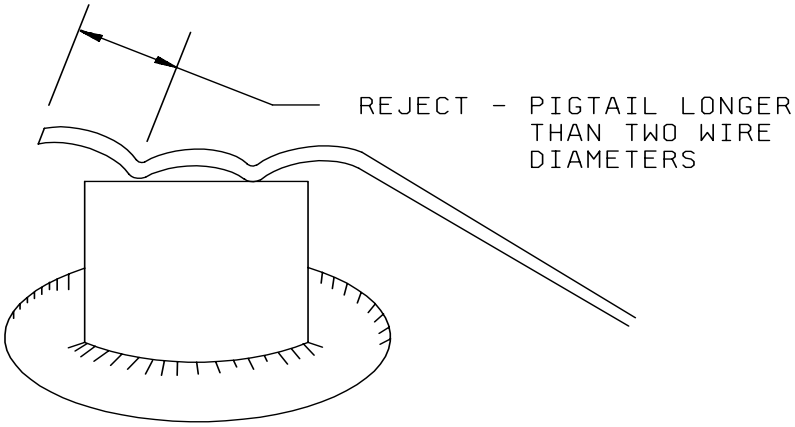

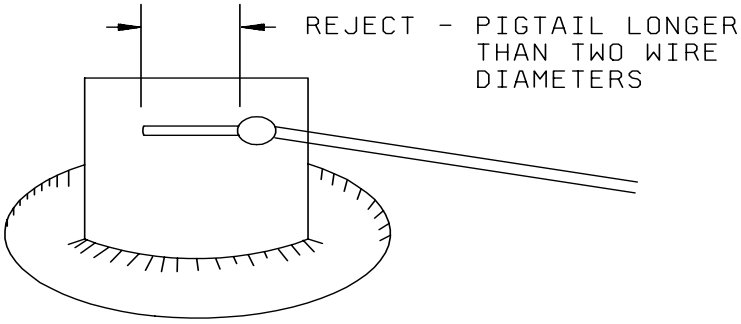

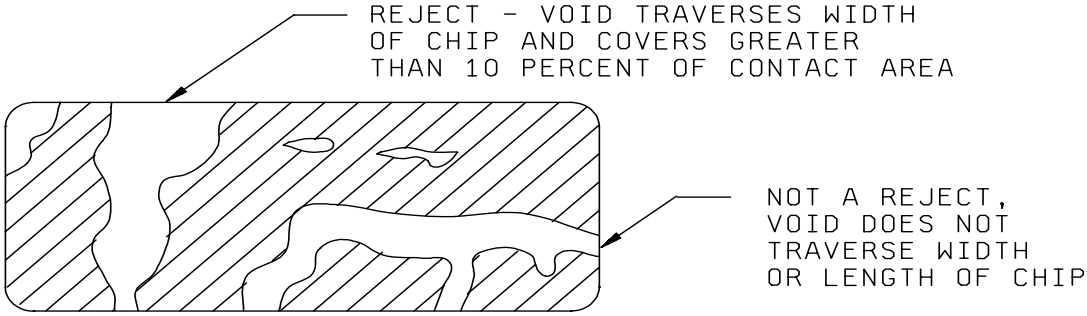

FIGURE 2072-6. Acceptable and unacceptable voids and excessive pigtails.

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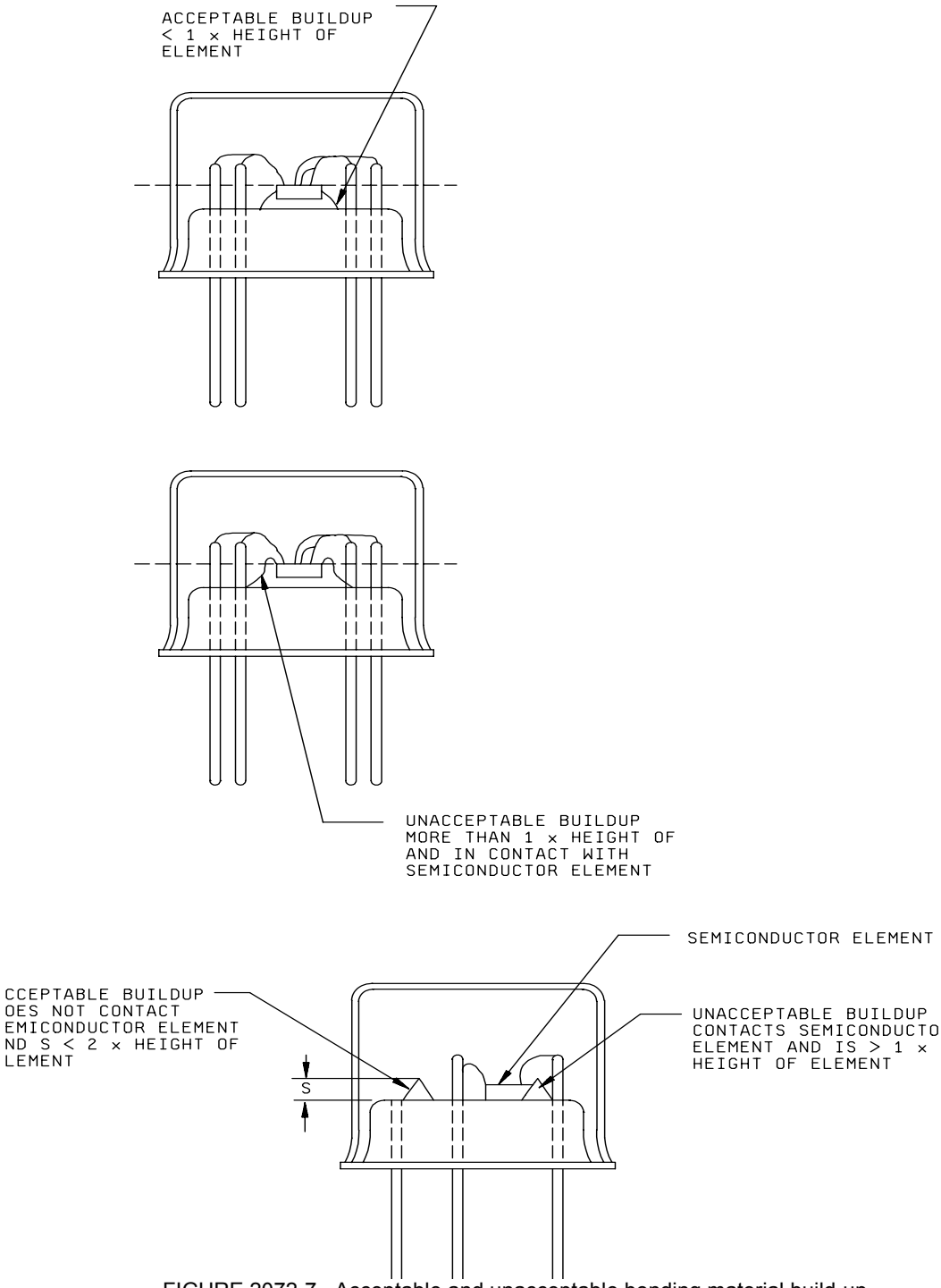

FIGURE 2072-7. Acceptable and unacceptable bonding material build-up.

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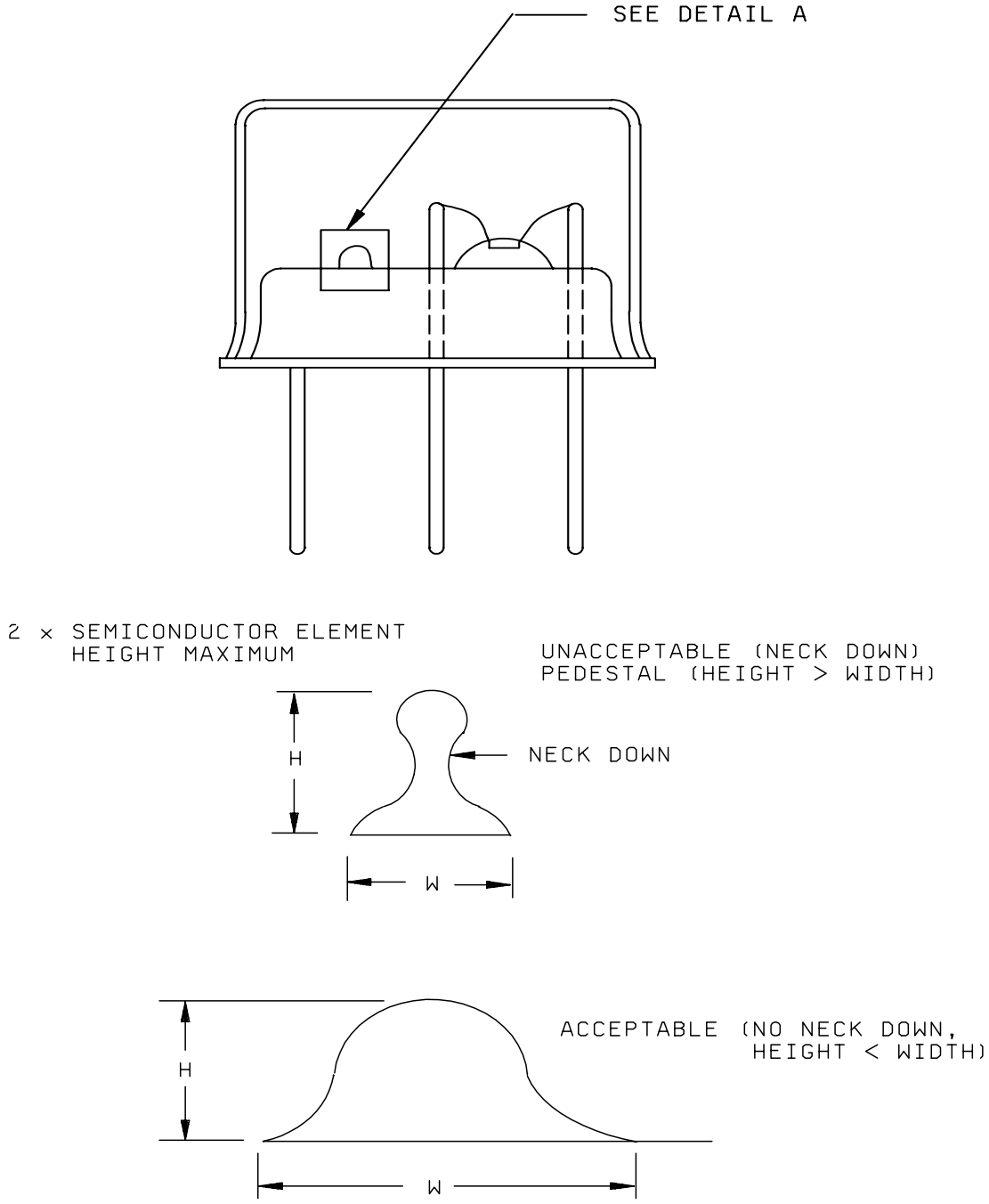

DETAIL A

NOTE: Die and wire are not necessarily visible.

FIGURE 2072-8. Extraneous bonding material build-up.

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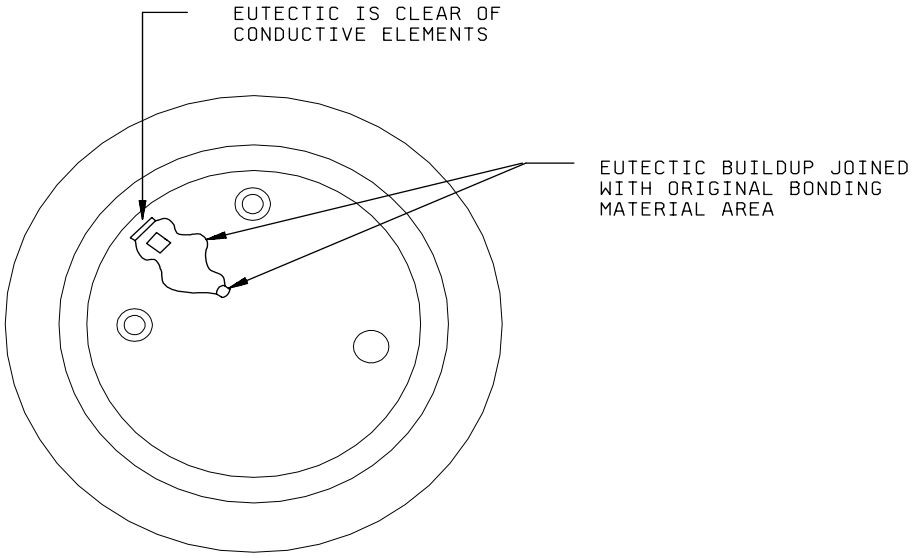
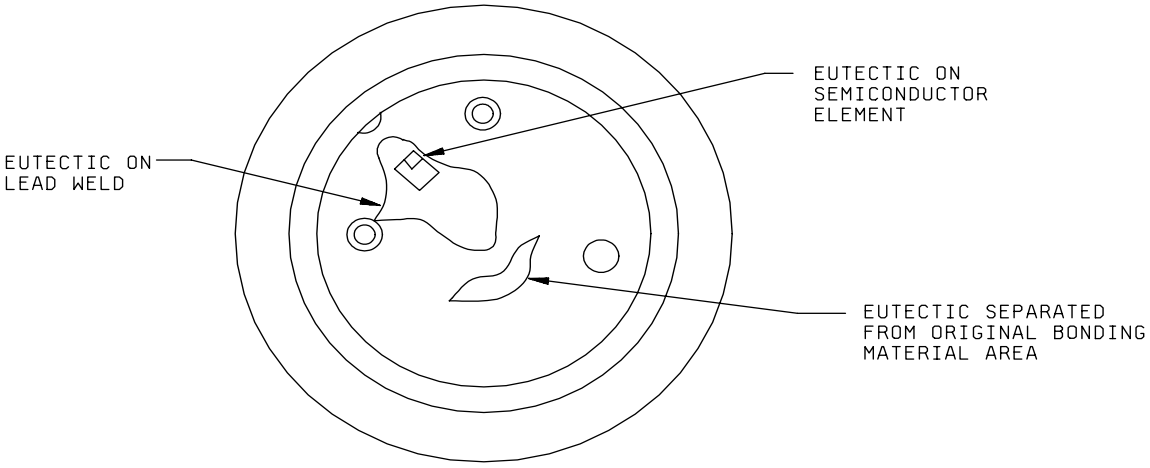


ACCEPTABLE



UNACCEPTABLE

FIGURE 2072-9. Acceptable and unacceptable excess material.

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METHOD 2073.1

VISUAL INSPECTION FOR DIE (SEMICONDUCTOR DIODE)

1. Purpose. The purpose of this test method is to check the quality and workmanship of semiconductor die for compliance with the requirements of the individual specification sheet. All tests shall be performed to detect and eliminate those die with defects that could lead to device failures. This test will normally be used prior to installation on a 100 percent inspection basis. The test may also be employed on a sampling basis prior to encapsulation to determine the effectiveness of the manufacturer's quality control and handling procedures.

2. Definitions. The following definitions shall apply:

a. Active area: Any area where electrical contact may be made on the "N" or "P" regions of the die.

b. Active region: Region covered by passivation that supports electrical activity and junction geometries.

c. Foreign material (attached): Any conductive or nonconductive material that is not part of the die construction. Conductive foreign material is defined as any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspections. Therefore, nonconductive foreign material is defined as any substance that appears transparent

d. Junction: The boundary between "P" and "N" type semiconductor material. (In the case of a Schottky diode, there is no actual junction other than the guard ring. Schottky diodes have a barrier that exists at the metal-silicon contact, however, for the purposes of this test method the barrier will be treated as a junction.)

e. Passivation: Silicon oxide, silicon nitride, or other insulating material that is grown or deposited directly over the "P-N" junction or the Schottky guard ring “P-N” junction.

3. Apparatus.

a. The apparatus for this test shall include optical equipment and any visual standards (e.g., gauges, drawings, photographs) necessary to perform an effective examination and enable the examiner to make objective decisions on the acceptability of the die being examined. Adequate fixturing shall be provided for handling die without contamination during examination.

b. Unless otherwise specified by the individual specification sheet or procuring activity, magnification at 20X and 30X minimum shall be performed with a monocular, binocular, or stereo microscope. The inspection shall be performed under suitable illumination. Binocular and stereo microscopes shall have each eyepiece individually focused for the examiner.

4. Procedure. The die shall be examined in a suitable sequence of operations and at the specified magnifications to determine compliance with the requirements of the individual specification sheet and the criteria of the specified test conditions. The sequence of examinations required may be varied at the discretion of the manufacturer.

4.1 Die inspections. These inspections shall apply to alloy, diffused mesa, epitaxial mesa, planar, and epitaxial planar construction techniques. Unless otherwise specified, inspections shall be made on a random selection of at least one side of each die being inspected. If a lot fails, 100-percent inspection of the total lot shall be performed.

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4.1.1 Type of die examined. Determine type of die being examined by referring to figure 2073-1 through figure 2073-8. An exact match is not necessary, select a representative figure. If a representative figure cannot be discerned, perhaps elements of different figures will apply. Contact the die vendor source for assistance in matching an appropriate figure. NOTE: Hexagonal shaped die will be inspected to the same criteria as square die.

a.	Button contact diodes.	Figure 2073-1.
b.	High voltage planar diode I.	Figure 2073-2.
c.	High voltage planar diodes II.	Figure 2073-3.
d.	Inside moat mesa diodes.	Figure 2073-4.
e.	Low voltage contact overlay diodes.	Figure 2073-5.
f.	Low voltage planar diode.	Figure 2073-6.
g.	Outside moat mesa diodes.	Figure 2073-7.
h.	Schottky barrier diodes.	Figure 2073-8.

4.2 Examination options. Examine die according to the appropriate figure, its' illustrations, and associated textual criteria.

a. Option A: Front side visual inspection with sample size specified by individual specification sheet or procuring activity. If no sample size is specified, 100-percent visual is assumed.

b. Option B: Backside visual in addition to front side visual. Backside inspection is conducted with sample size specified by individual specification sheet or procuring activity. If no sample size is specified, use sample size 22 for class H or sample size 45 for class K and reject on 1.

NOTE: If no option is specified by the individual specification sheet or procuring activity, option A will apply.

4.3 Foreign material. Examine die for attached conductive foreign material. No detailed illustration is provided for this due to the random nature of such material. The examiner is expected to use their own judgment in this matter.

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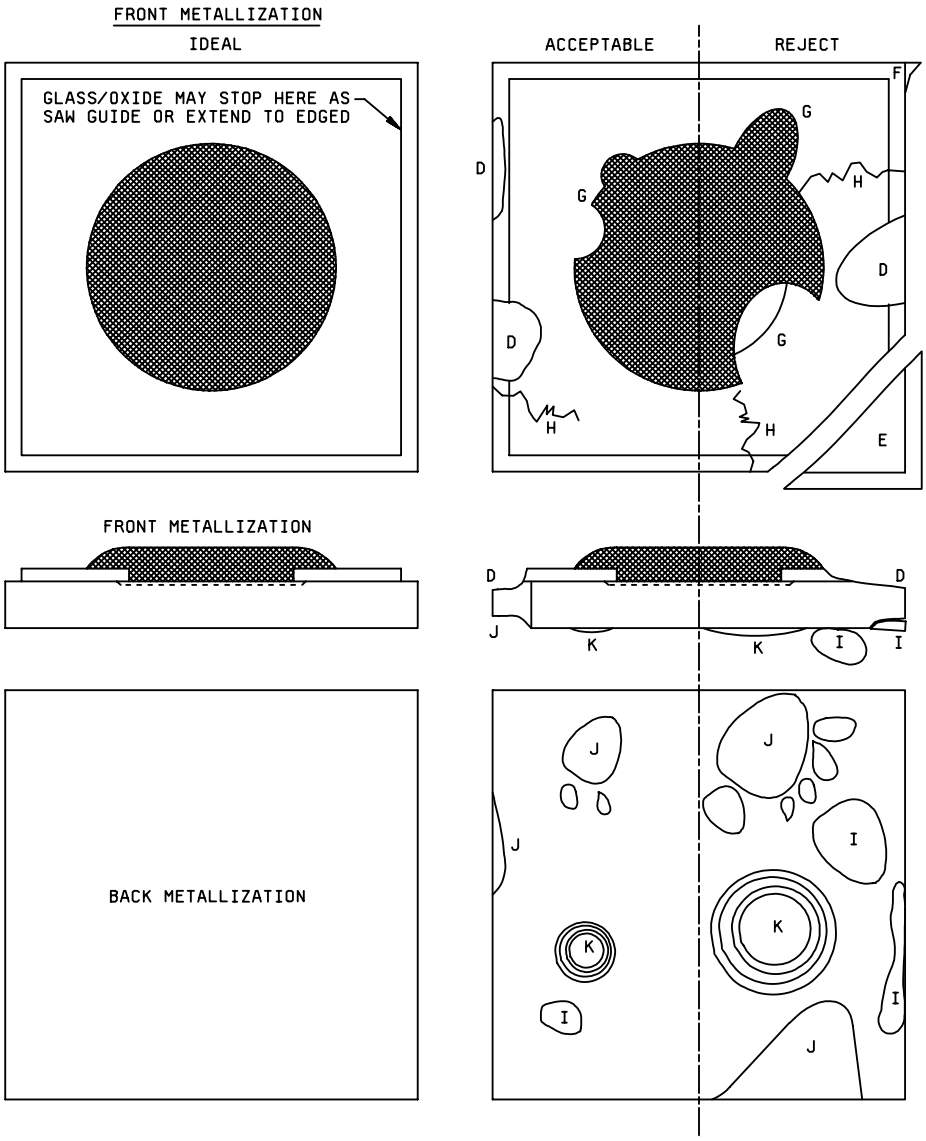

Note: Reject criteria
Edge chipping (D) may not extend more than 50 percent to metallization.

Missing pieces (E) extending beyond 50 percent to junction boundary or additional attached pieces (F) defined by an incomplete cut or scribe line are not permitted.

Additional front metallization extending 50 percent or more to the next geometric boundary (G) or pulled back to reveal contact area or any non-passivated active region.

Cracks (H) must not extend near the metalized button closer than 50 percent and must not be directed toward button such that additional propagation would intersect the button.

Backside
Back contamination and foreign material (I), either firmly or loosely attached, exceeding 10 percent of total area.

Missing backside metal (J) exceeding 20 percent of total area.

Blisters (K) in metalization exceeding 10 percent of total area.

FIGURE 2073-1. Button contact diodes (metal button overlays junction and active area).

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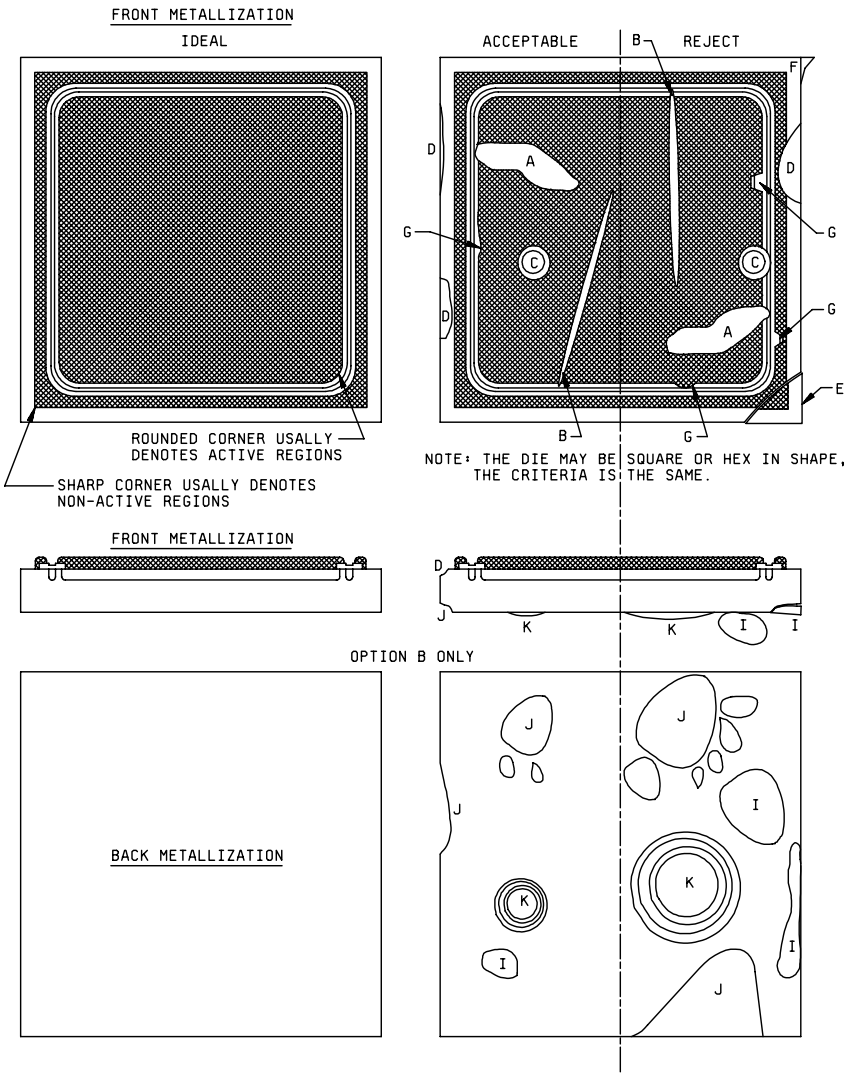

Reject criteria

Smears (A), scratches (B) or probe marks (C) may not extrude metal such that it covers any guard rings.

Edge chipping or cracks (D) may not extend into outside metallization ring (or if absent, 50 percent of distance between chip edge and nearest active ring.)

Missing pieces (E) extending into outside metal ring or additional attached pieces (F) defined by an incomplete cut or scribe line are not permitted.

Additional front metallization extending over nearest ring boundary (G) or pulled back to reveal contact area or any non-passivated region.

Cracks (not illustrated) must not extend under the metalized areas and must not be present inside any of the active regions.

Backside

Backside contamination and foreign material (I), either firmly or loosely attached, exceeding 10 percent of total area.

Missing backside metal (J) exceeding 20 percent of total area.

Blisters (K) in metalization exceeding 10 percent of total area.

FIGURE 2073-2. High voltage planar diode I (guard ring(s) and outside metal oxide edge cover or field plate).

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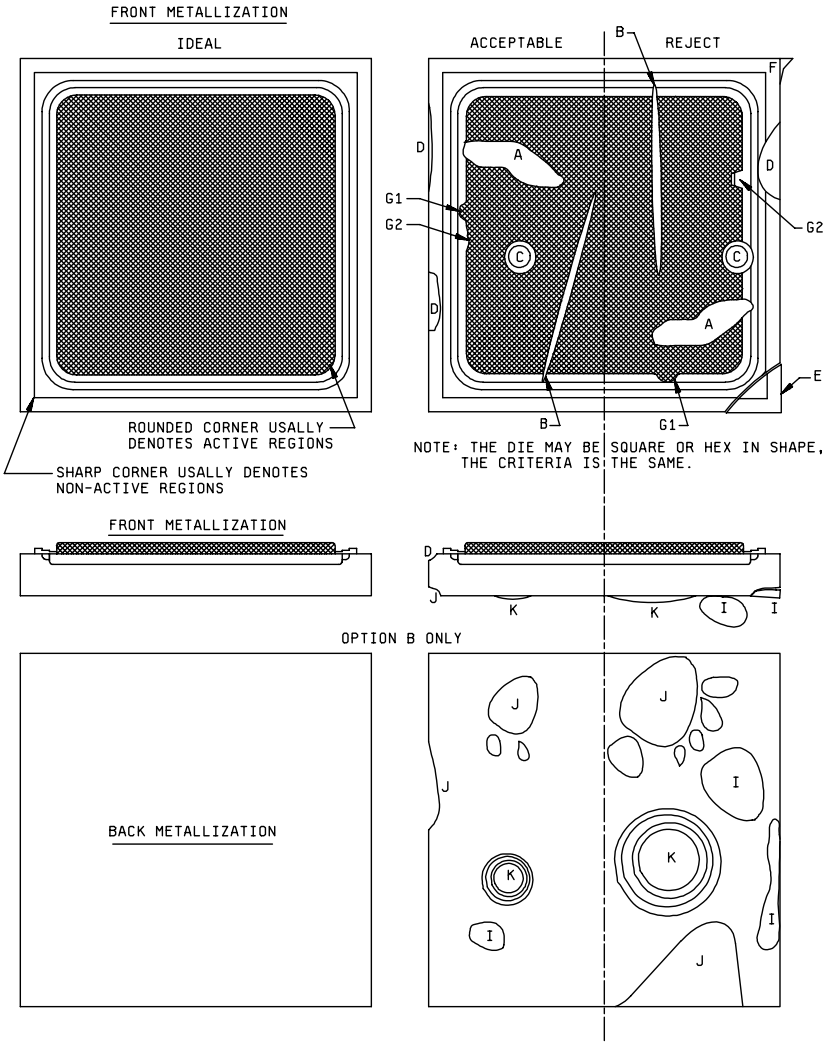

Reject criteria

Smears (A), scratches (B) or probe marks (C) may not extrude metal such that it extends over the next geometric boundary (covers the P-guard ring area).

Edge chipping or cracks (D) may not extend into outside metallization ring (or if absent, 50 percent of distance between chip edge and active ring boundary.)

Missing pieces (E) extending 50 percent of distance between chip edge and nearest ring boundary or additional attached pieces (F) defined by an incomplete cut or scribe line are not permitted.

Additional front islands of metallization crossing any diffusion line (G1) or pulled back to reveal contact area or any non-passivated region (G2). Note that G2 does not apply to chips designed without requiring metal-passivation overlay. In this latter exception, much or all of the oxide window will be exposed as a legal part of the design.

Cracks (not illustrated) must not extend under the metalized areas and must not be present inside any of the active regions.

Backside

Backside contamination and foreign material (I), either firmly or loosely attached, exceeding 10 percent of total area.

Missing backside metal (J) exceeding 20 percent of total area.

Blisters (K) in metalization exceeding 10 percent of total area.

FIGURE 2073-3. High voltage planar diodes II (integrated P-minus guard ring).

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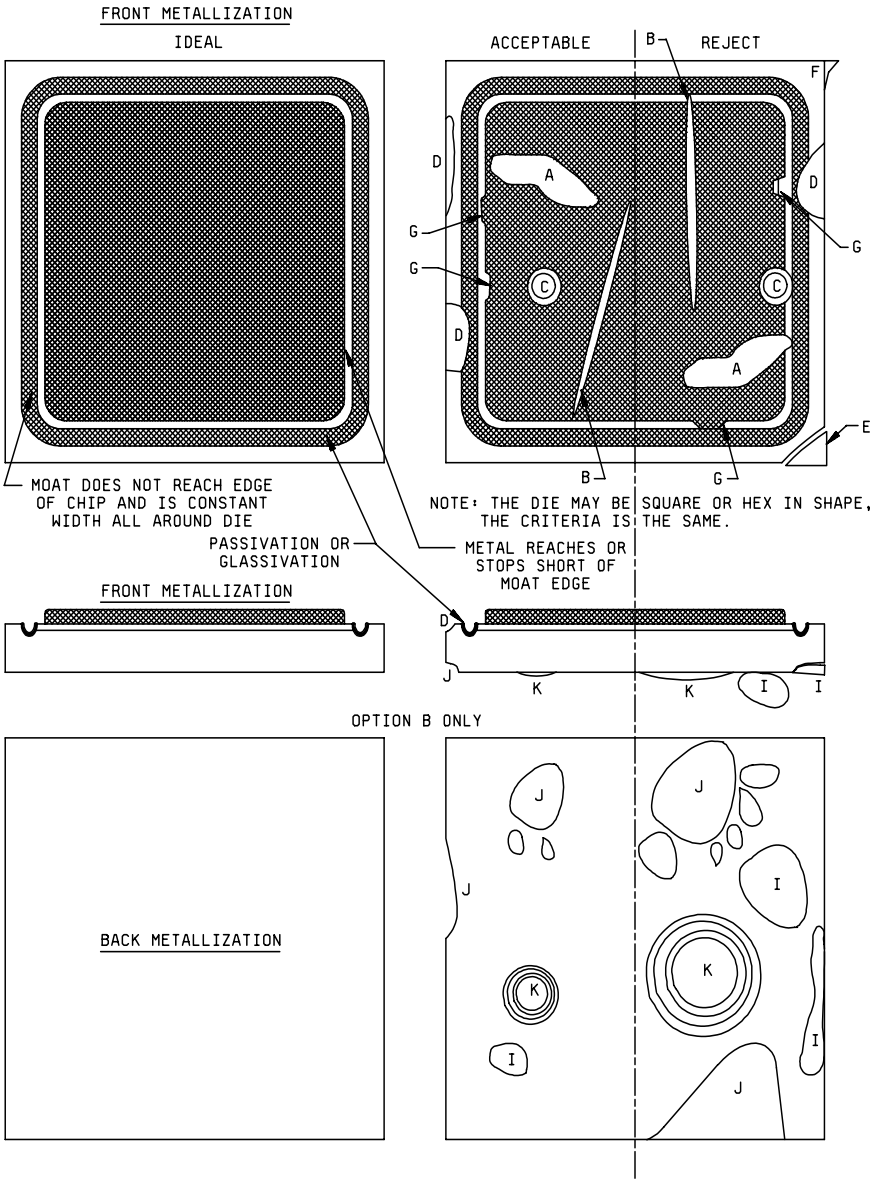

Reject criteria

Smears (A), scratches (B) or probe marks (C) may not extrude metal outside metalized region over moat edge.

Edge chipping or cracks (D) may not extend into moat area.

Missing pieces (E) extending 50 percent of distance between chip edge and the moat or additional attached pieces (F) defined by an incomplete cut or scribe line are not permitted die.

Additional front metallization extending over into the moat (G) or pulled back to reveal contact area or any non-passivated region

Cracks (not illustrated) must not extend under the metalized areas nor more than 50 percent of the way across the moat from the outside.

Backside

Backside contamination and foreign material (I), either firmly or loosely attached, exceeding 10 percent of total area.

Missing backside metal (J) exceeding 20 percent of total area.

Blisters (K) in metalization exceeding 10 percent of total area.

FIGURE 2073-4. Inside moat mesa diodes (passivated moat does not extent to edge of die).

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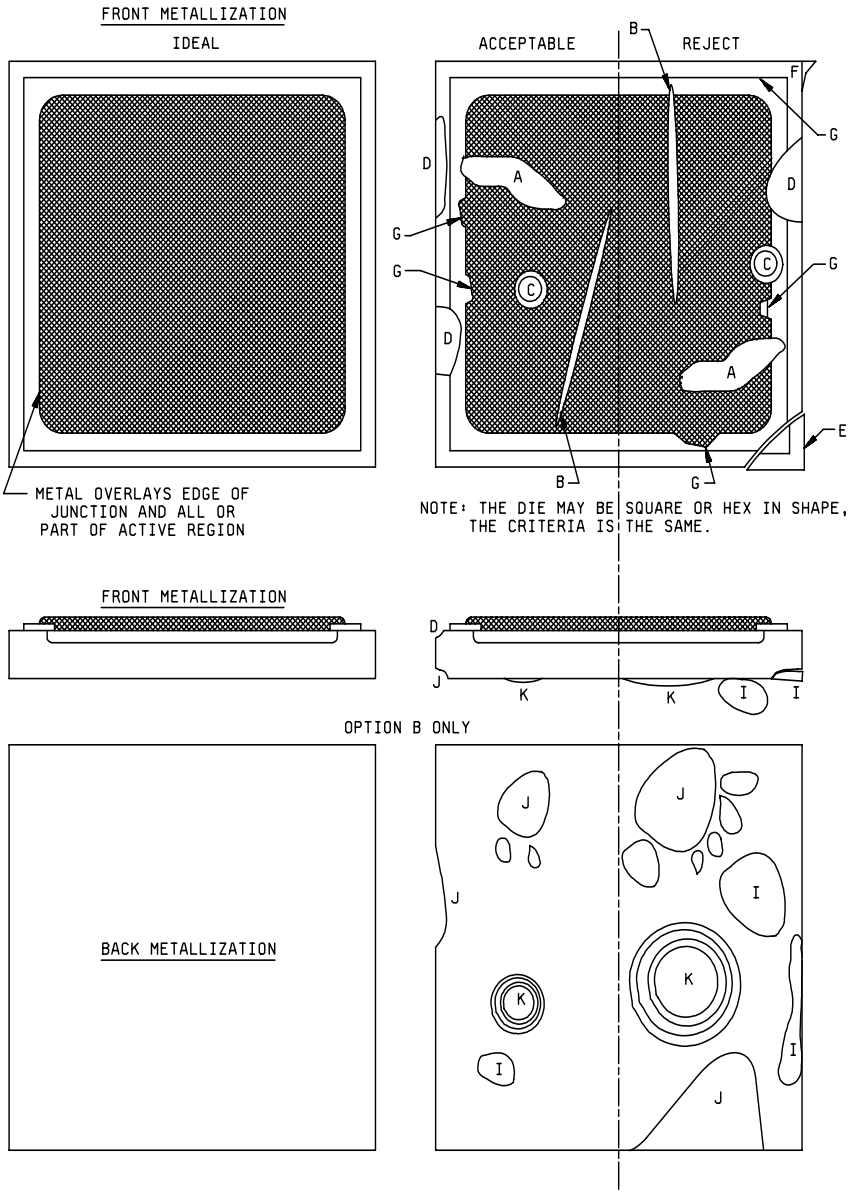

Reject criteria

Smears (A), scratches (B) or probe marks (C) may not extrude metal outside metalized region more than 50 percent of the way to the next boundary.

Edge chipping (D) may not extend into metallization.

Missing pieces (E) extending beyond 50 percent to metal boundary or additional attached pieces (F) defined by an incomplete cut or scribe are not permitted.

Additional front metallization extending 50 percent or more to the next geometric boundary (G) or pulled back to reveal contact area or any non-passivated active region.

Cracks (not illustrated) must not extend under the metalized areas and must not be present inside any of the active regions.

Backside

Backside contamination and foreign material (I), either firmly or loosely attached, exceeding 10 percent of total area.

Missing backside metal (J) exceeding 20 percent of total area.

Blisters (K) in metallization exceeding 10 percent of total area.

FIGURE 2073-5. Low voltage contact overlay diodes (metal overlays junction and active area field plate).

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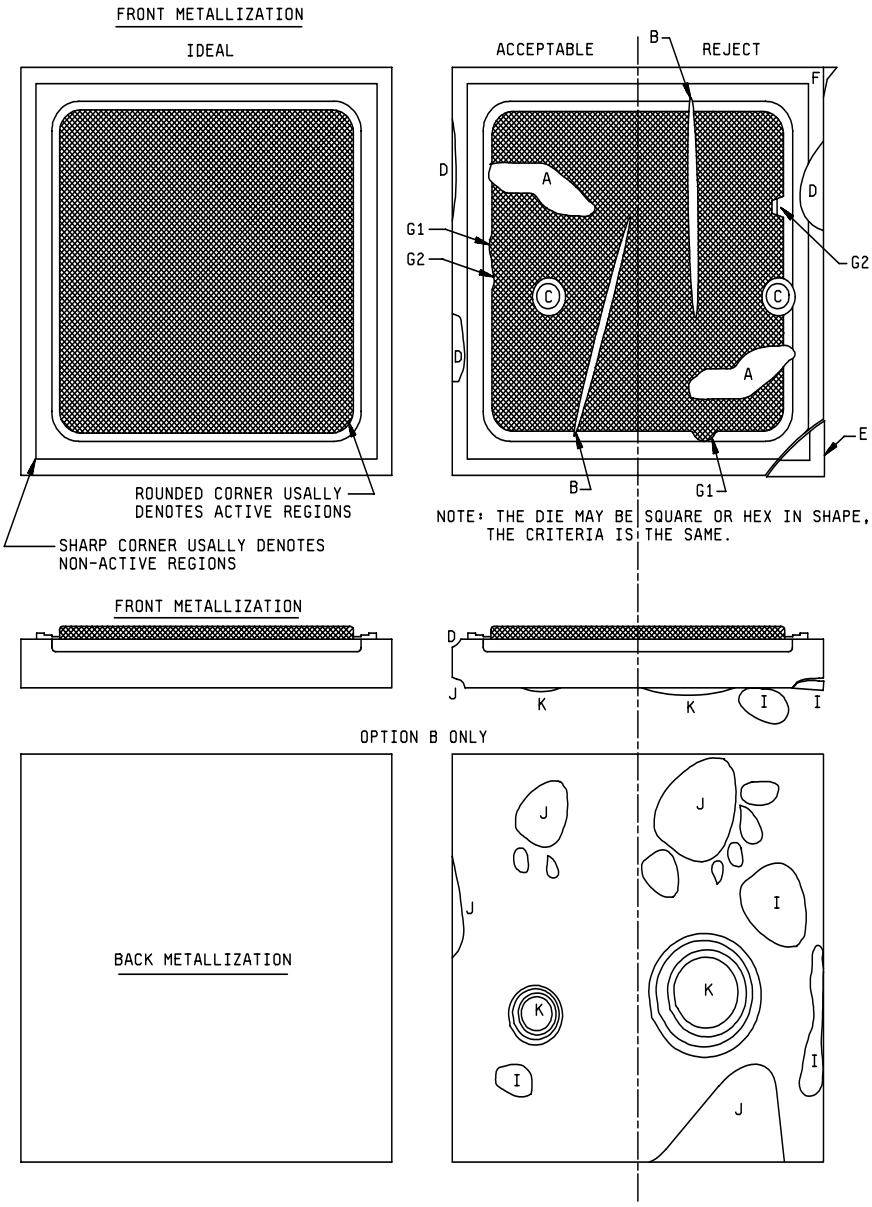

Reject criteria

Smears (A), scratches (B) or probe marks (C) may not extrude metal outside junction boundary region.

Edge chipping or cracks (D) may not extend beyond 50 percent between chip edge and junction boundary.

Missing pieces (E) extending beyond 50 percent to junction boundary or additional attached pieces (F) defined by an incomplete cut or scribe line are not permitted.

Additional front islands of metallization crossing any diffusion line (G1) or pulled back to reveal contact area or any non-passivated region (G2). Note that G2 does not apply to chips designed without requiring metal passivation overlay. In this latter exception, much or all of the oxide window will be exposed as a legal part of the design.

Cracks (not illustrated) must not extend under the metalized areas and must not be present inside any of the active regions. Sharp corner usually denotes non-active regions

Backside

Backside contamination and foreign material (I), either firmly or loosely attached, exceeding 10 percent of total area.

Missing backside metal (J) exceeding 20 percent of total area.

Blisters (K) in metalization exceeding 10 percent of total area.

FIGURE 2073-6. Low voltage planar diode.

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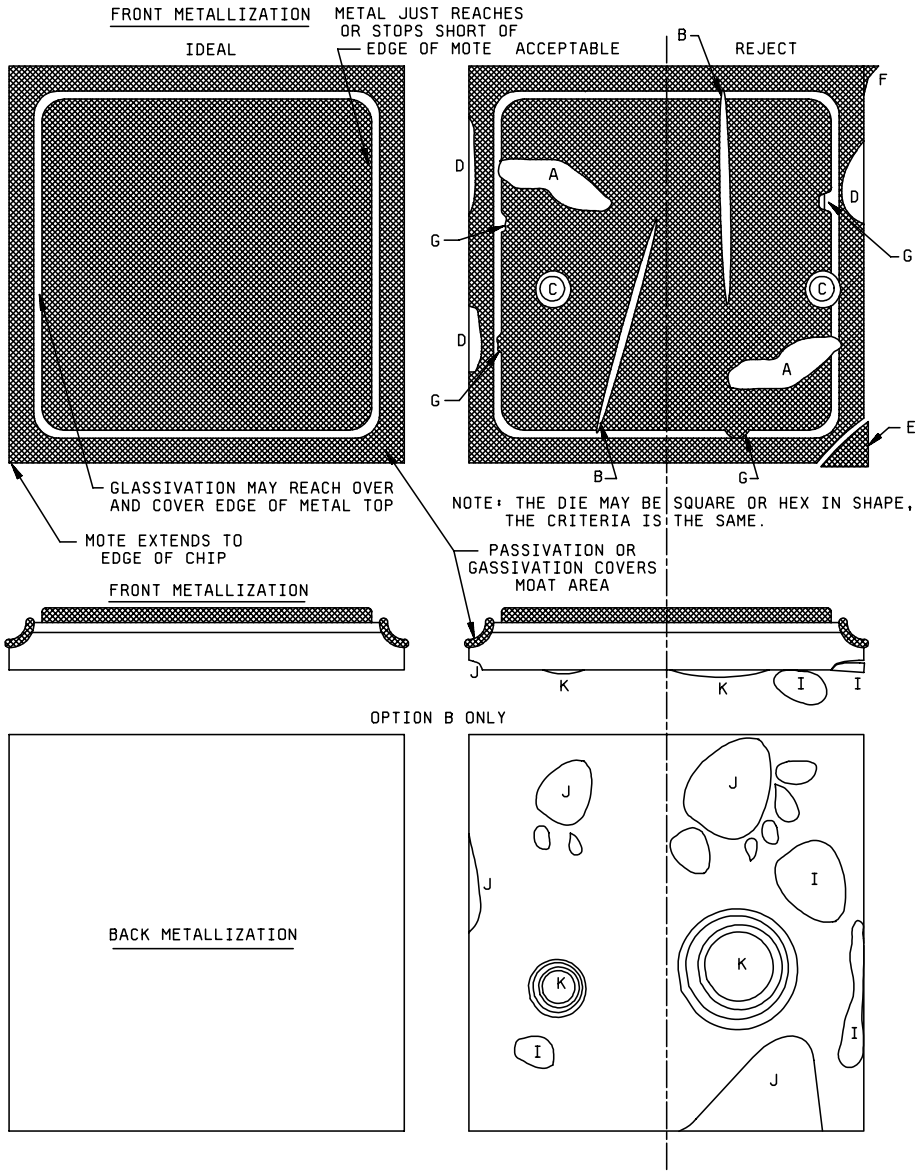

Reject criteria

Smears (A), scratches (B) or probe marks (C) may not extrude metal outside metalized region over moat edge.

Edge chipping (D) may not extend into moat area more than 50 percent.

Missing pieces (E) extending beyond 50 percent across moat or additional attached pieces (F) defined by an incomplete cut or scribe line are not permitted.

Additional front metallization extending over into the moat (G) or pulled back to reveal contact area or any non-passivated active region.

Cracks (not illustrated) must not extend under the metalized area no more than 50 percent of the way across the moat from the outside

Backside

Backside contamination and foreign material (I), either firmly or loosely attached, exceeding 10 percent of total area.

Missing backside metal (J) exceeding 20 percent of total area.

Blisters (K) in metalization exceeding 10 percent of total area.

FIGURE 2073-7. Outside moat mesa diodes (moat extends from mesa to edge of die).

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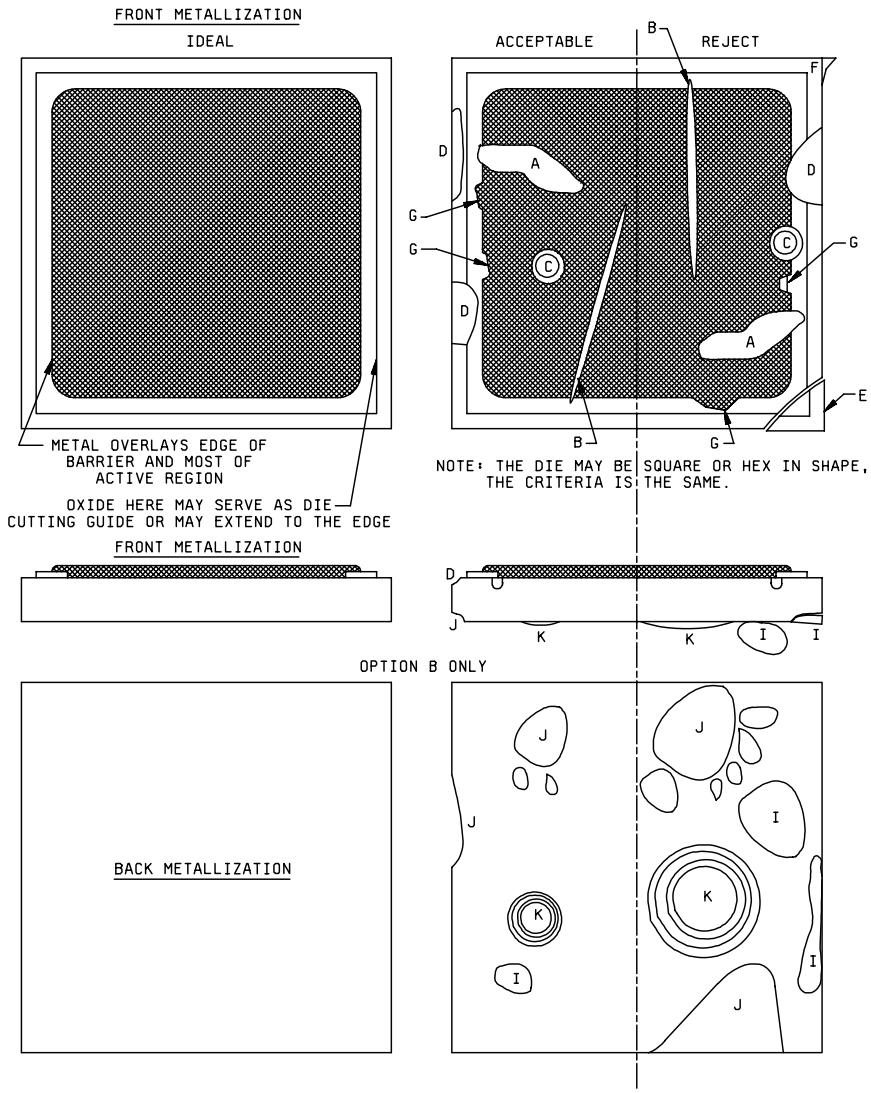

Reject criteria

Smears (A), scratches (B) or probe marks (C) may not extrude metal outside metalized region more than 50 percent to the next geometric boundry.

Edge chipping (D) may not extend into metallization.

Missing pieces (E) extending more than 50 percent of distance from chip edge and metalization or additional attached pieces (F) that exceed chip dimensional specifications are not permitted.

Additional front metallization extending 50 percent or more to the next geometric boundary (G) or pulled back to reveal contact area or any non-passivated barrier region.

Cracks (not illustrated) must not extend under the metalized areas and must not be present inside any of the active regions.

Backside

Backside contamination and foreign material (I), either firmly or loosely attached, exceeding 10 percent of total area.

Missing backside metal (J) exceeding 20 percent of total area.

Blisters (K) in metalization exceeding 10 percent of total area.

FIGURE 2073-8. Schottky barrier diodes (metal overlays barrier edge and active area field plate).

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METHOD 2074.5

INTERNAL VISUAL INSPECTION (DISCRETE SEMICONDUCTOR DIODES)

1. Purpose. The purpose of this test method is to check the materials, design, construction, and workmanship of discrete semiconductor diodes and other two-terminal semiconductor devices described herein. All tests shall be performed to detect and eliminate those devices with defects that could lead to device failures. Opaque glass type constructions shall be examined before encapsulation. (After encapsulation, see method 2068 of this general specification). Metal can devices shall be examined before capping. (After capping or sealing, see method 2071 of this general specification). Clear glass construction shall be examined after encapsulation.

2. Apparatus.

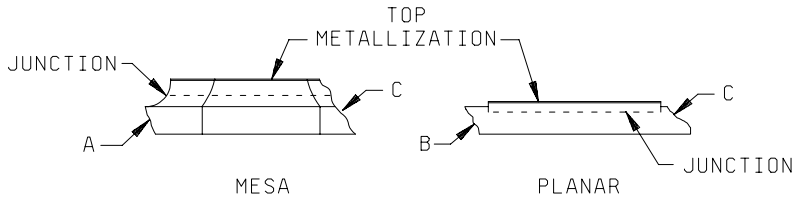
a. The apparatus for these tests shall include optical equipment and any visual standards (e.g., gauges, drawings, photographs) necessary to perform an effective examination and enable the operator to make objective decisions on the acceptability of the device being examined. Any necessary fixturing for handling devices during examination to promote efficient operation without damaging the units shall be provided.

b. A monocular, binocular, or stereo microscope capable of magnification from 20X minimum to 30X maximum, shall be used unless otherwise specified. The inspection shall be performed under suitable illumination.

3. Procedure. The devices shall be examined at the specified magnifications to determine compliance with the requirements of the applicable sections of this test method based on device construction. Examinations for transparent body devices may be performed anytime prior to body coating or painting. Axial construction devices shall be viewed at approximate right angles to their major axis while being rotated through 360 degrees. For the time interval, if any, between visual inspection and package sealing, devices shall be stored, handled, and processed in a manner to avoid contamination and to preserve the integrity of the devices as inspected.

3.1 Die criteria (applicable to all body styles).

a. Chip outs. Reject for chip outs that extend more than 50 percent of the way up the moat area (mesa devices) or that extend to within 2.0 mils of the junction. NOTE: Actual junction location will vary depending on specific device characteristics. (See figure 2074-1.)



Accept: Chipouts ≤ 50 percent up moat and ≥ 2 mils from junction - "A"
Accept: Chipouts ≥ 2 mils from junction - "B"
Reject: Chipouts ≤ 2 mils from junction - "C"

FIGURE 2074-1. Chip outs.

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b. Cracks. Reject for cracks that extend to within 2.0 mils of the junction or propagate in the direction of the junction. NOTE: The junction may be in a different place than shown depending on specific device characteristics. (See figure 2074-2.)

Reject: Cracks ≤ 2 mils from junction or propagating toward junction -"A"
Accept: Cracks ≥ 2 mils from junction and propagating away from junction -"B"

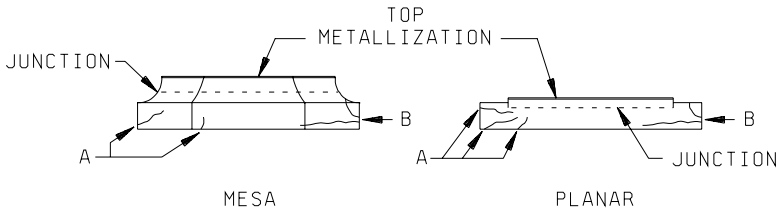

FIGURE 2074-2. Cracks.

3.2 Applicable body styles. The devices shall be examined in accordance with the following appendixes as applicable for the body style involved.

Appendix A: Axial lead, transparent body, pressure contact design.

Appendix B: Axial lead, transparent body, straight through lead to die contact.

Appendix C: Axial lead and surface mount, double plug, transparent body (dumet plug, round end-cap, soft glass).

Appendix D: Axial lead and surface mount, double plug, transparent body (tungsten or molybdenum plug, square end-cap, hard glass).

Appendix E: Axial lead, transparent body, point contact.

Appendix F: Axial lead, double plug, opaque body, power rectifier and regulator.

Appendix G: Metal body, axial lead, solder contact design.

Appendix H: Metal body, stud mounted, solder contact design.

Appendix I: Metal body, diamond base regulators, solder contact design.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Detailed requirements for materials, design, construction, and workmanship.

b. Magnification requirements, if other than specified.

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AXIAL LEAD, TRANSPARENT BODY, PRESSURE CONTACT DESIGN

A.1 Axial lead, transparent body, pressure contact design. The following examinations shall be made after encapsulation (C and S bend whisker). This appendix is a mandatory part of the standard. The information contained herein is intended for compliance.

A.1.1 Glass cracks and chips (see figure 2074-A1). No cracks shall be allowed in the vicinity of the cavity. Any crack originating at either end of the package or crack that extends into the body of the glass toward the cavity more than 25 percent of the glass-to-glass or glass-to-metal seal length shall be cause for rejection. Any glass chip deep enough to expose the plug or lead surface and extending longitudinally into the glass-to-metal seal toward the cavity to reduce the effective seal length to less than one external lead diameter shall be cause for rejection.

A.1.2 Incomplete seal. All devices shall be inspected for glass-to-metal seal or glass-to-glass seal. Both seals shall be a minimum of one external lead diameter over the entire sealed portion (sealed interface).

A.1.3 Bubbles in seal. All devices shall be inspected for bubbles in the glass-to-metal or glass-to-glass seal. A series of bubbles that reduce the effective seal length to less than one external lead diameter shall be cause for rejection. Bubbles in the glass, but not affecting the glass-to-glass or glass-to-metal seal area, are not cause for rejection.

A.1.4 Glass package deformities (see figure 2074-A2). Any glass envelope deformity equal to or greater than 75 percent of the external lead diameter shall be cause for rejection.

A.1.5 Extraneous matter. A device shall be rejected if there are unattached solder balls, semiconductor material, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

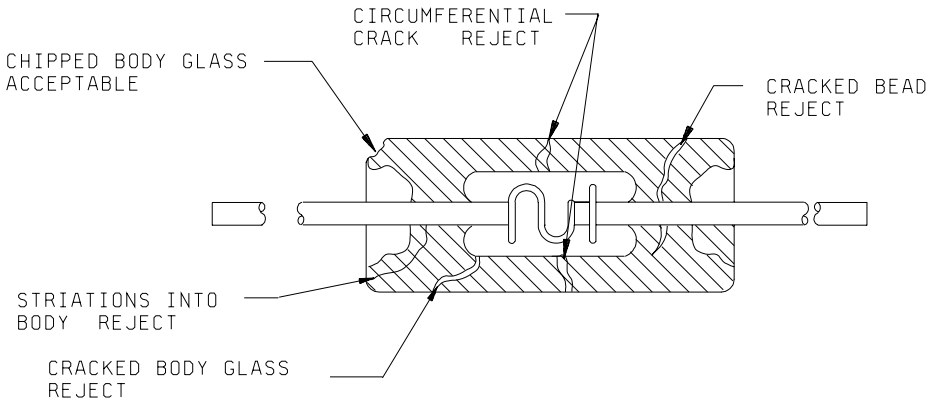

FIGURE 2074-A1. Glass cracks and chips.

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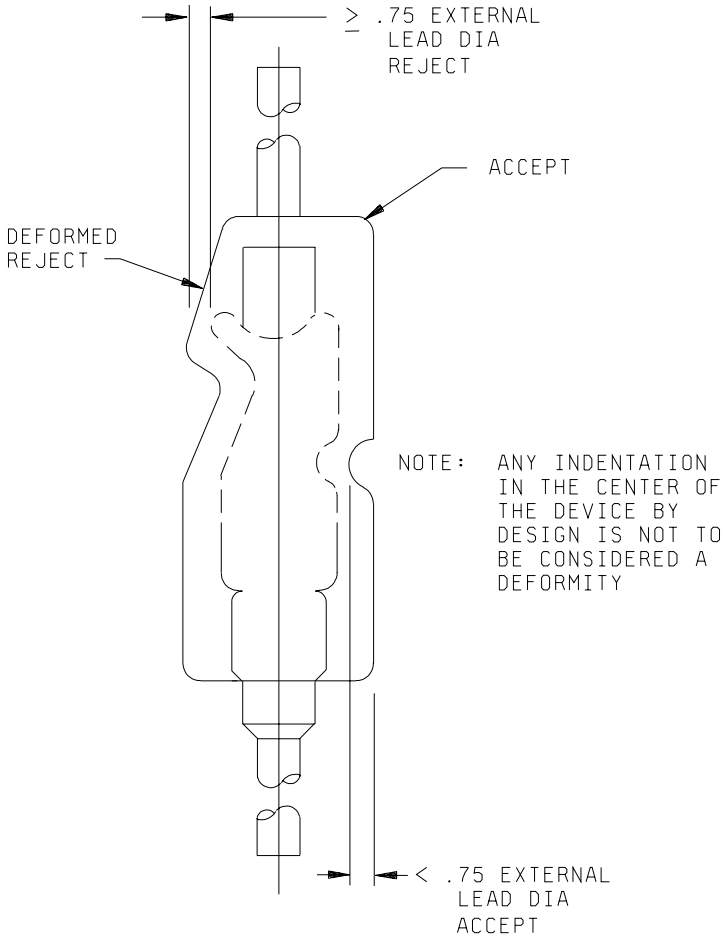

FIGURE 2074-A2. Package deformities.

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A.1.6 Solder protrusions (see figure 2074-A3). All devices shall be inspected for solder protrusions. Any device with a protrusion that extends more than twice the smallest protrusion width shall be rejected.

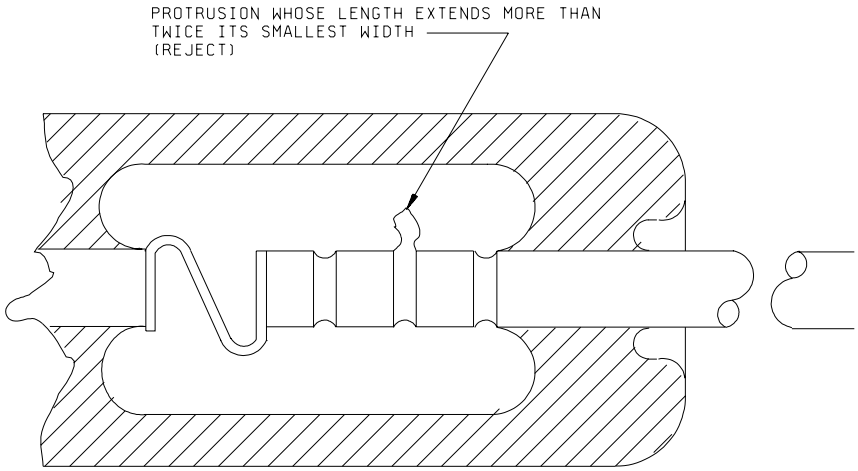

FIGURE 2074-A3. Solder protrusions.

A.1.7 Pressure contact defects. The following misalignments or deformations shall be cause for rejection:

a. Whisker embedded within glass body wall (see figure 2074-A4).

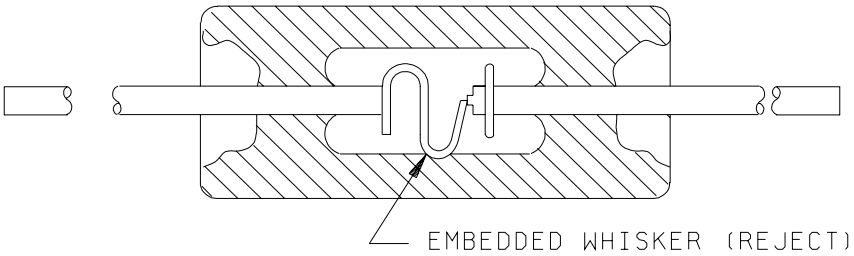

FIGURE 2074-A4. Embedded whisker.

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b. Toe contact between base of S or C spring and top surface of die caused by insufficient loading (see figure 2074-A5).

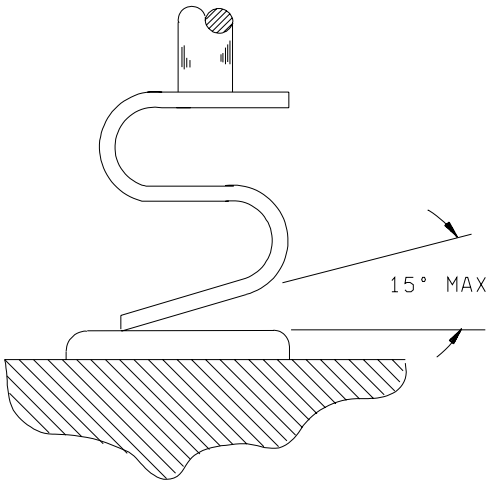

FIGURE 2074-A5. Toe contact.

c. Toe contact on top surface of die (see figure 2074-A6).

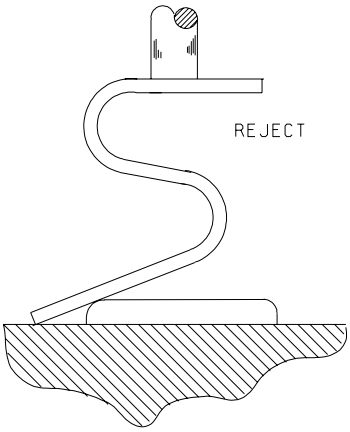

FIGURE 2074-A6. Toe contact on top surface of die.

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d. Heel contact between base of S or C spring and top surface of die (see figure 2074-A7).

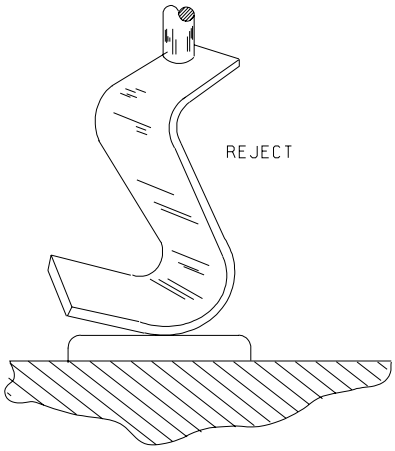

FIGURE 2074-A7. Heel contact.

e. Point contact between base of S or C spring and top surface of die except by design (deformed or twisted whisker) (see figure 2074-A8).

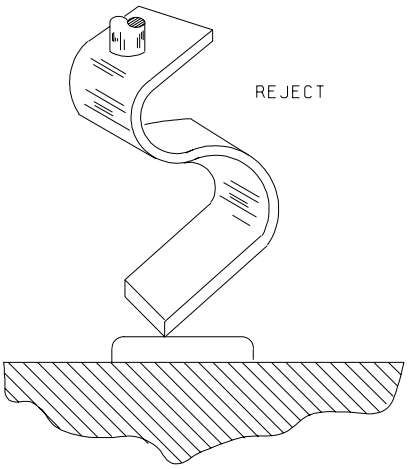

FIGURE 2074-A8. Point contact.

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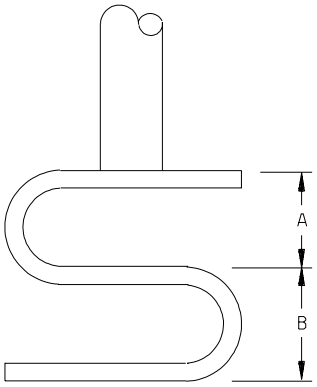
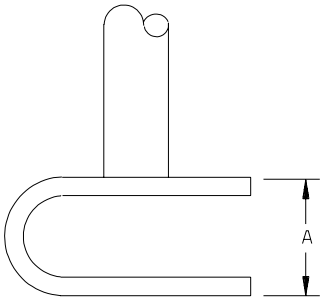
f. Design compressed height (see figures 2074-A9 and 2074-A10). Either half of an S or C bend that is compressed so that any dimension is reduced to less than 50 percent of its design shall be rejected.



REJECT IF EITHER "A" OR "B" IS LESS THAN 50% OF ITS DESIGN COMPRESSED HEIGHT

FIGURE 2074-A9. S whisker compressed height.



REJECT IF EITHER "A" IS LESS THAN 50% OF ITS DESIGN COMPRESSED HEIGHT

FIGURE 2074-A10. C bend compressed height.

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A.1.8 Whisker weld to post. Any device that exhibits weld splash or splatter (teardrop or balled) between whisker and post shall be rejected when it exceeds 25 percent of nominal lead diameter. The profile of the whisker weld to post shall not allow light penetration by more than 50 percent of lead diameter when using back lighting techniques.

A.1.9 Die-to-post or die-to-die contact area. Solder shall not be rough in appearance and shall be fused to a minimum of one-half the available bonding perimeter. Any solder overflow that touches the opposite surface of the die or dice shall be cause for rejection.

A.1.10 Die alignment (see figure 2074-A11). A device shall be rejected if the die surface is not within 15 degrees of being normal to the centerline of the mounting post.

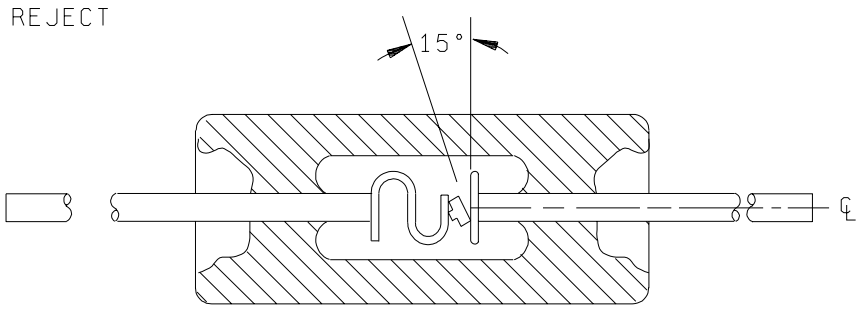

FIGURE 2074-A11. Die alignment.

A.1.11 Lead alignment defects (applicable to that portion of each lead within the glass envelope). A device lead which is either misaligned or bent so that it makes an angle with the principle device axis greater than 10 degrees shall be rejected.

A.1.12 Multiple chip attachment defects. A multiple chip stack that tilts more than 10 degrees from the principle axis of the device shall be cause for rejection.

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AXIAL LEAD, TRANSPARENT BODY, STRAIGHT THROUGH LEAD TO DIE CONTACT

B.1 Axial lead, transparent body, straight through lead to die contact (see figure 2074-B1). The following criteria shall be specified for the straight through construction after encapsulation but before body coating or painting. This appendix is a mandatory part of the standard. The information contained herein is intended for compliance.

B.1.1 Glass cracks and chips (see figure 2074-A1). No cracks shall be allowed in the vicinity of the cavity. Any crack originating at either end of the package or crack that extends into the body of the glass toward the cavity more than 25 percent of the glass-to-glass or glass-to-metal seal length shall be cause for rejection. Any glass chip deep enough to expose the plug or lead surface and extending longitudinally into the glass-to-metal seal toward the cavity to reduce the effective seal length to less than one external lead diameter shall be cause for rejection.

B.1.2 Incomplete seal. All devices shall be inspected for glass-to-metal seal or glass-to-glass seal. Both seals shall be a minimum of one external lead diameter over the entire sealed portion (sealed interface).

B.1.3 Bubbles in seal. All devices shall be inspected for bubbles in the glass-to-metal or glass-to-glass seal. A series of bubbles that reduce the effective seal length to less than one external lead diameter shall be cause for rejection. Bubbles in the glass, but not affecting the glass-to-glass or glass-to-metal seal area, are not cause for rejection.

B.1.4 Glass package deformities (see figure 2074-A2). Any glass envelope deformity equal to or greater than 75 percent of the external lead diameter shall be cause for rejection.

B.1.5 Extraneous matter. A device shall be rejected if there are unattached solder balls, semiconductor material, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

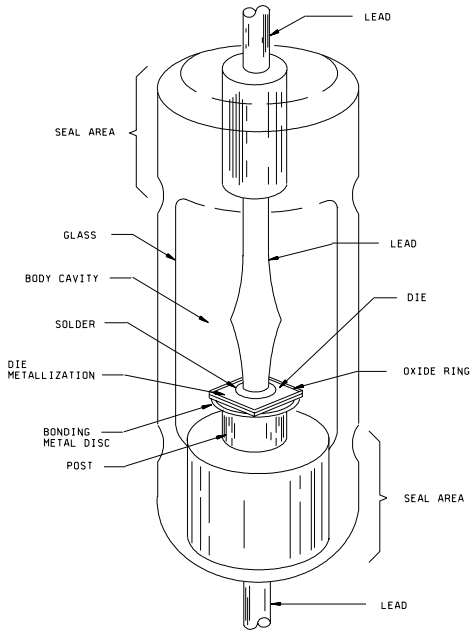

FIGURE 2074-B1. Internal construction.

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B.1.6 Die to post solder connection.

a. Solder voids (see figure 2074-B2). A device shall be rejected if solder flow is less than 50 percent of the perimeter of the minimum available contact area of the post.

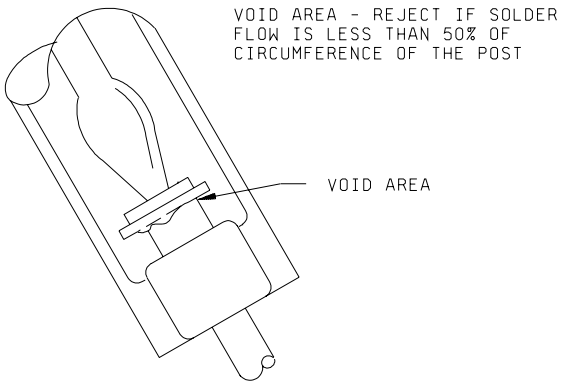

FIGURE 2074-B2. Solder voids.

b. Solder overflow (see figure 2074-B3). A device shall be rejected if any solder flow touches the opposite surface of the die.

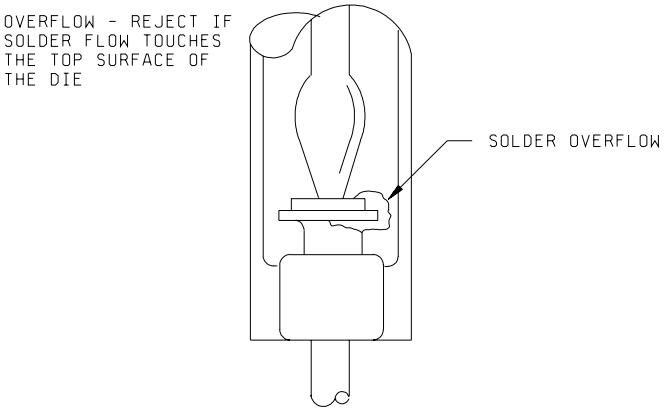

FIGURE 2074-B3. Solder bridge.

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B.1.7 Lead to die solder connection (see figure 2074-B4). A device shall be rejected if more than 50 percent of the perimeter of the available contact area of the lead is void of solder.

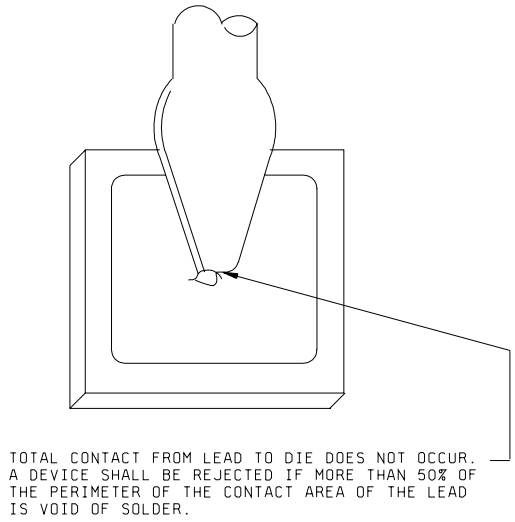

FIGURE 2074-B4. Solder voids.

a. Solder overflow (see figure 2074-B5). A device shall be rejected if solder flow extends beyond 50 percent of the distance from the metal to the outer edge of the oxide.

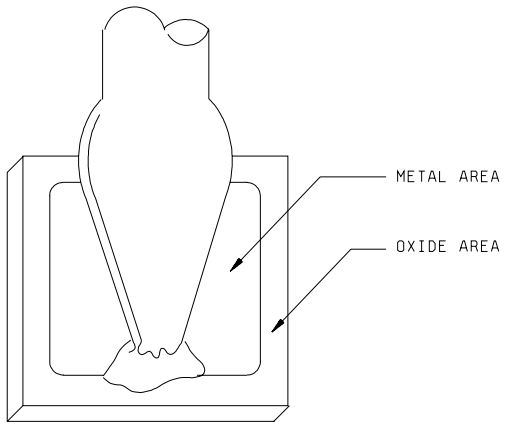

FIGURE 2074-B5. Solder overflow.

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b. Solder protrusion, slivers, and spikes (see figure 2074-B6). A device shall be rejected if solder slivers and spikes are not securely attached to the main body. A securely attached sliver of spike is one having a cross sectional area greater at the area of attachment than anywhere else on the solder protrusion and having no necked down areas. Solder protrusions, slivers, and spikes whose length exceeds twice the smallest width of attachment shall be rejected.

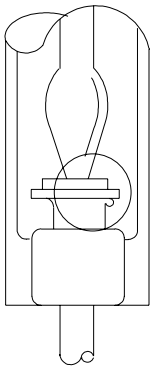

FIGURE 2074-B6. Solder slivers and spikes.

c. Solder balls. A device shall be rejected if there are any insecurely attached solder balls. An insecurely attached solder ball is one whose major cross sectional area is more than twice the cross sectional area of the attachment.

B.1.8 Die-to-die solder connection (see figure 2074-B7). A device shall be rejected if more than 50 percent of the perimeter of the available contact area of the die is void of solder.

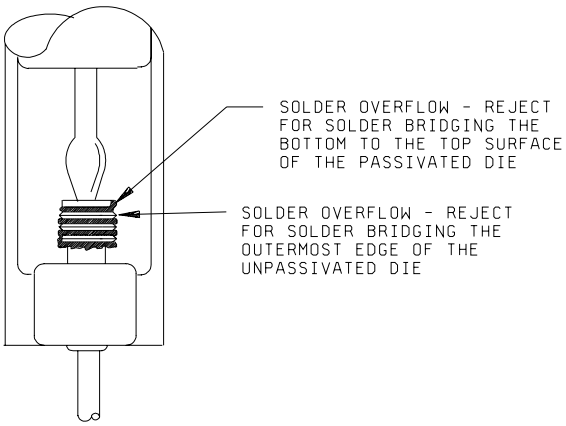

FIGURE 2074-B7. Die-to-die solder connection.

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AXIAL LEAD AND SURFACE MOUNT, DOUBLE PLUG, TRANSPARENT BODY (DUMET PLUG, ROUND END-CAP, SOFT GLASS)

C.1 Axial lead and surface mount, double plug, transparent body (dumet plug, round end-cap, soft glass). This appendix is a mandatory part of the standard. The information contained herein is intended for compliance.

C.1.1 Glass cracking. Cracks (see figure 2074-C1). Spiral or longitudinal cracks of any length originating at either end that propagate in the direction of the die are cause for rejection. Reject for cracks that are not confined to the glass surface or the outer 25 percent of the seal length. Cracks confined to the outer 25 percent of the designed seal length that propagate back toward the starting edge (away from the die area) are acceptable. Small surface impact marks, “c” cracks, and microcracks are acceptable if they are confined to the glass surface with no other cracks radiating from them.

REJECT: CRACKS NOT CONFINED TO SURFACE OR OUTER 25% OF SEAL LENGTH - "A"
REJECT: CRACKS OF ANY LENGTH THAT PROPAGATE TOWARD DIE - "B"
REJECT: SPIRAL CRACKS PROPAGATING TOWARD DIE - "C"
ACCEPT: SMALL C-CRACKS OR MICRO CRACKS IN GLASS SURFACE - "D"
ACCEPT: CRACKS IN OUTER 25% OF SEAL LENGTH THAT PROPAGATE AWAY FROM DIE - "E"

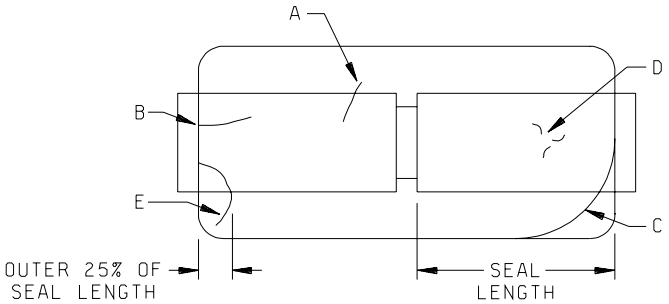

FIGURE 2074-C1. Glass cracks.

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C.1.2 High seal (see figure 2074-C2). Any device which displays a glass case off center condition reducing the seal band of either plug by more than 25 percent of its designed length shall be cause for rejection.

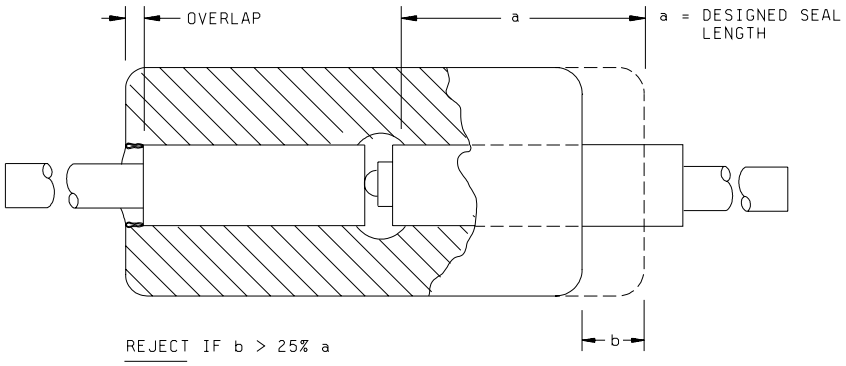

FIGURE 2074-C2. High seal.

C.1.3 Insufficient seal (see figure 2074-C3). Any anomaly such as bubbles, plug blisters, separations, leaching, or undersealing that affects the combined seal length of either plug by reducing the a sealing band to less than 50 percent of the designed seal length on any package type shall be cause for rejection.

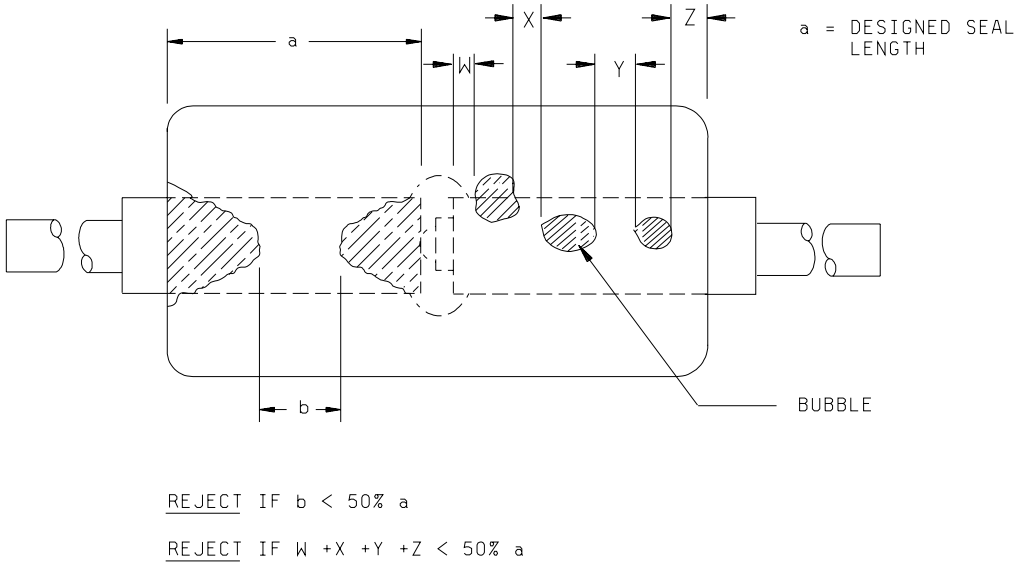

FIGURE 2074-C3. Insufficient seal.

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C.1.4 Plug alignment and displacement (see figures 2074-C4 and 2074-C5). All devices shall be inspected for proper plug alignment. A plug displacement distance more than 25 percent of the diameter of the plug shall be cause for rejection. The plug shall not tilt to the degree that it touches the chip or is misaligned from the other plug axis more than 5 degrees.

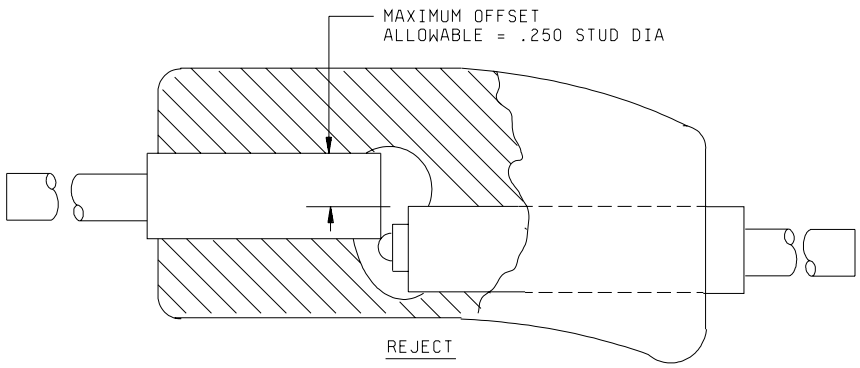

FIGURE 2074-C4. Plug alignment.

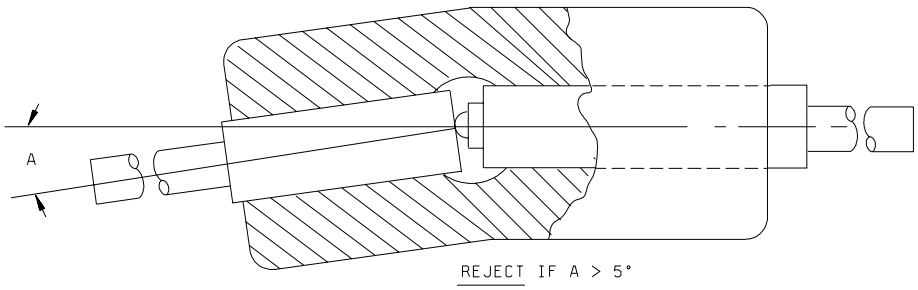

FIGURE 2074-C5. Plug displacement.

C.1.5 Extraneous matter. A device shall be rejected if there are unattached solder balls, semiconductor material, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

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C.1.6 Lead connections (see figure 2074-C6). Lead to plug connections shall be inspected for incomplete welds. Any partial welds less than 75 percent of total weld area shall be cause for rejection.

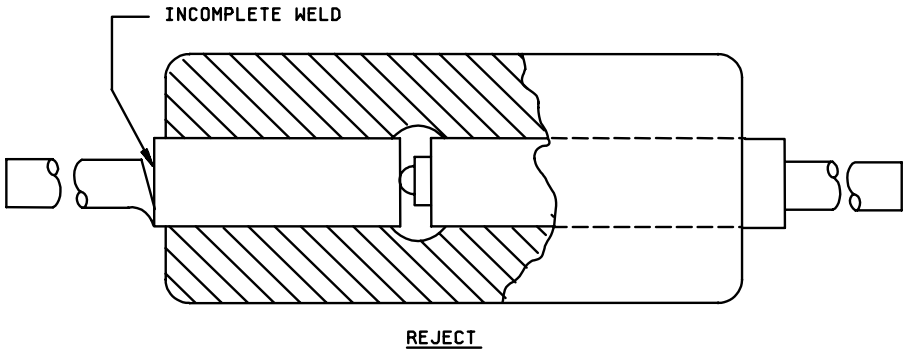

FIGURE 2074-C6. Incomplete weld.

C.1.7 Die defects (reject).

C.1.7.1 Die tilt greater than 5 degrees, or slug, or preform makes contact to chip on bump side.

C.1.7.2 Any die that exhibits chip outs exceeding .25 inch (6.35 mm) of the die width, or extending to within 2.0 mils of the junction, shall be rejected.

C.1.8 Criteria for round end-cap surface mount devices.

C.1.8.1 Glass-to-metal seal shall be .015 inch (0.381 mm) min for DO-213AA and .020 inch (0.508 mm) min for DO-213AB, around the diameter of each slug.

C.1.8.2 Slug exposure shall not exceed 30 percent of the slug length .014 inch (0.3556 mm) min for DO-213AA and .022 inch (0.5588 mm) min for DO-213AB.

C.1.8.3 There shall be no cracks in the device within .010 inch (0.254 mm) of the die.

C.1.8.4 There shall be no cracks in the glass that are pointed towards the die.

C.1.8.5 There shall be no conductive contaminants in the die cavity area.

C.1.8.6 For plug alignment, including end-caps, see C.1.4.

C.1.8.7 For end-cap connections, see C.1.6.

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AXIAL LEAD AND SURFACE MOUNT, DOUBLE PLUG, TRANSPARENT BODY (TUNGSTEN OR MOLYBDENUM PLUG, SQUARE END-CAP, HARD GLASS).

D.1 Axial lead and surface mount, double plug, transparent body (tungsten or molybdenum plug, square end-cap, hard glass). This appendix is a mandatory part of the standard. The information contained herein is intended for compliance.

D.1.1 Glass.

a. No cracks allowed.

b. Chip outs (see figure 2074-D1). Edge chip outs that expose a plug and are not confined to the outer 25 percent of the designed seal length are cause for rejection. Edge chip outs (regardless of size) that expose a plug and create a sharp angle or “V” shape that points toward the die area are rejects

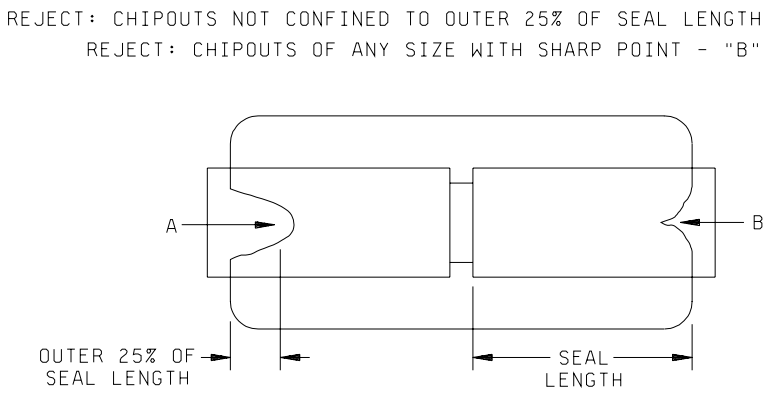

FIGURE 2074-D1. Chip outs.

c. Holes. Any hole over the die or slug area greater that 50 percent of the glass thickness in depth is cause for rejection, except that holes of any depth are acceptable in the outer 25 percent of the designed seal length.

d. Deformities (see figure 2074-D2.). Any glass surface deformity that causes the glass surface to be displaced by more than 10 percent of the designed glass diameter, or that results in the device not meeting a dimensional requirement, is cause for rejection.

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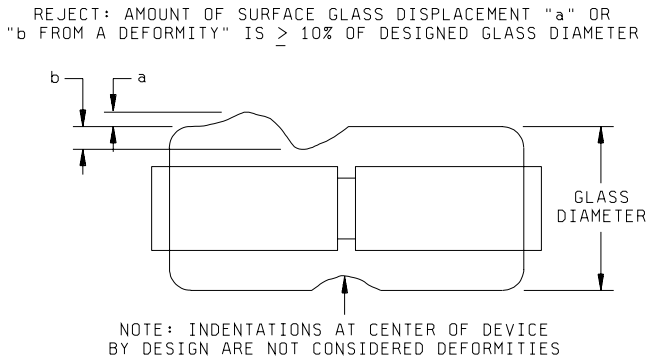

FIGURE 2074-D2. Deformity.

e. Surface damage and discoloration. Any device with surface abrasions, chips, scratches, rough or discolored (darkened) glass over the die area that result in the die not being clearly visible, is a reject. Using liquid immersion to improve die visibility is acceptable.

D.1.2 Seal.

a. Glass positioning and missing glass (see figure 2074-D3.). Off center glass and portions of missing glass that reduce the seal length on either plug by more than 25 percent of the designed seal length is cause for rejection.

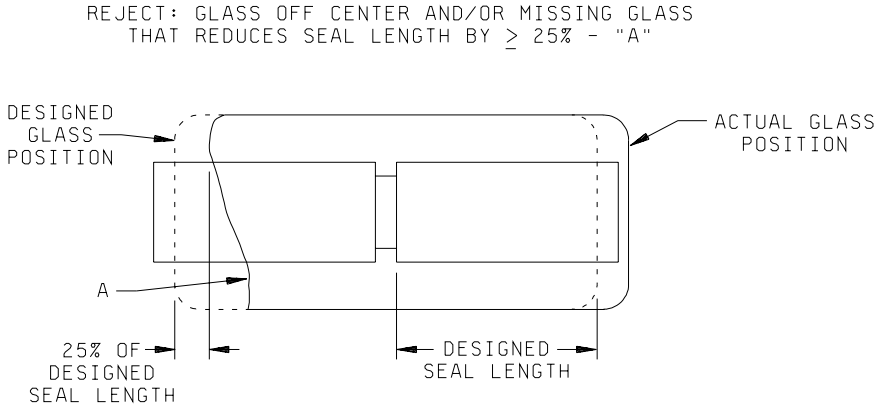

FIGURE 2074-D3. Positioning.

b. Insufficient seal (see figure 2074-D4.). Seal surface anomalies such as undercut, separations, plug blisters, scratches or cracks, bubbles, silicon chips, fibers, or missing plating which, when combined, reduce the sealing length along any linear path to less than 50 percent of the designed seal length are cause for rejection. NOTE: Lines or “strings” of small bubbles are considered to be seal anomalies for the entire length of the line.

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REJECT: SEAL LENGTH "a" REDUCED TO ≤ 50% OF DESIGNED SEAL LENGTH

REJECT: COMBINED SEAL LENGTHS "x"+"y"+"z" ALONG ANY LINE ≤ 50% OF DESIGNED SEAL LENGTH

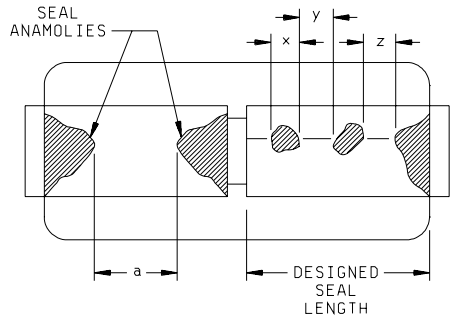

FIGURE 2074-D4. Insufficient seal.

c. Extraneous or loosely attached materials. Any unattached or loosely attached solder, braze, silicon chips, flaked plating, fibers, or other opaque extraneous material in the die cavity (for cavity devices) that is greater than 1.0 mil in any dimension are cause for rejection. No solder, braze, or other bonding materials shall extend from a plug into the area between plugs.

D.1.3 Alignment. NOTE: Any die to plug non-contact that occurs as a result of die or plug misalignment is most accurately evaluated by thermal impedance testing. In cases where pass/fail status of a device is unclear based on the alignment requirements presented herein, thermal impedance testing may be used to determine the acceptability of the device.

a. Die alignment. Any die that tilts more than 5 degrees with respect to the surface of either plug or that tilts sufficiently to make any unintended contact with the plug is cause for rejection. (See figure 2074-D5.) Any die that is out of axial alignment such that it extends beyond the slug more than 20 percent of its length or width is cause for rejection. (See Figure 2074-D6.)

REJECT: DIE TILT "a" IS ≥ 5°

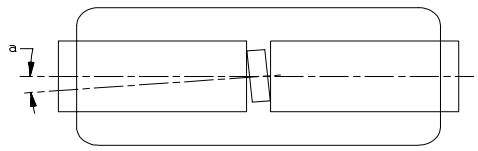

FIGURE 2074-D5. Tilt.

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REJECT: LENGTH OF DIE NON-CONTACT "a" IS ≥ 20% OF DIE LENGTH

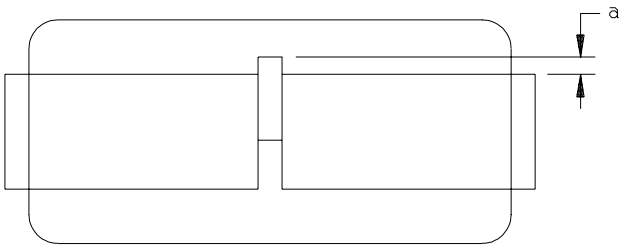

FIGURE 2074-D6. Die non-contract.

b. Plug alignment. Plugs that are not axially aligned other than in the die area to within 12.5 percent of the diameter of the plug are cause for rejection. (See figure 2074-D7.) Any plug that tilts more than 5 degrees with respect to the other or that tilts sufficiently to make any unintended contact with the die is cause for rejection (see figure 2074-D8).

REJECT: PLUG OFFSET "a" IS ≥ 1/8(12.5%) OF PLUG DIAMETER

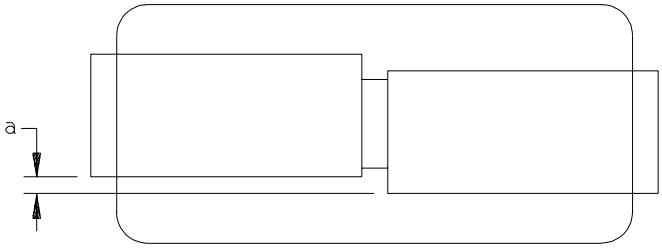

FIGURE 2074-D7. Plug offset.

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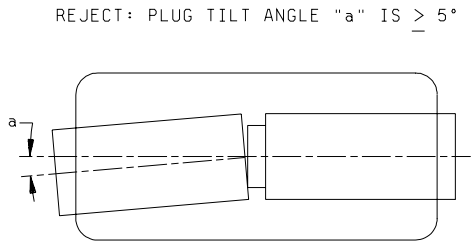

FIGURE 2074-D8. Plug tilt angle.

D.1.4 Lead and end-cap attach.

a. Lead alignment (leaded devices). Leads that are not axially aligned to within one lead diameter, or leads that are not contained completely within the diameter of the plug, are cause for rejection (see figure 2074-D9).

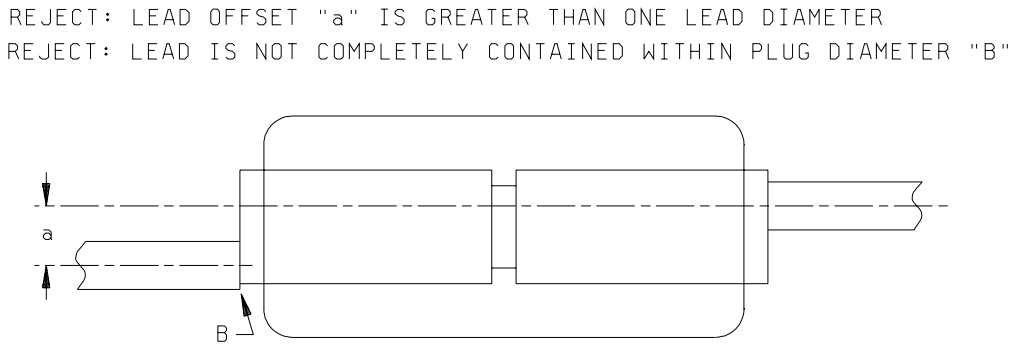

FIGURE 2074-D9. Lead offset.

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b. Braze (leaded devices). Leads that are not brazed to the plug around at least 90 percent of the lead perimeter are cause for rejection. Any cracks or fissures in the braze are cause for rejection. Pin holes in the braze are acceptable.

c. End-caps (surface mount). Reject for end-caps that do not allow at least 3.0 mils clearance from the glass body to the mounting surface on all four sides (see figure 2074-D10). Reject for end-caps that are not perpendicular to the plugs to within 5 degrees (see figure 2074-D11). Reject for end-caps that are bent sufficiently to cause the device to exceed any specified diode or end-cap dimension (see figure 2074-D12). Reject for end-cap rotation where mounting surfaces are not co-planer to each other to within 5 degrees (see figure 2074-D13). Reject for tabs that have indentations, holes, or other damage affecting more than 25 percent of any mounting surface (see figure 2074-D14). Reject for end-caps that exhibit flaking, blistering, or peeling.

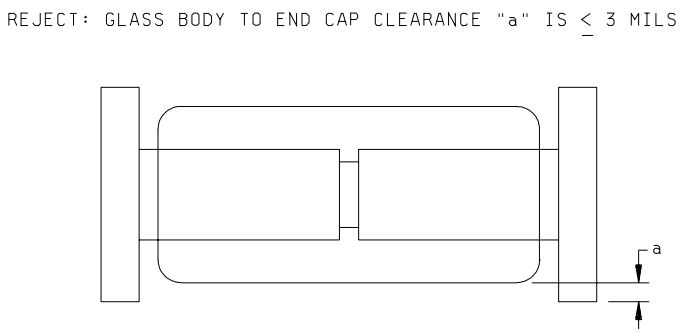

FIGURE 2074-D10. End-cap clearance.

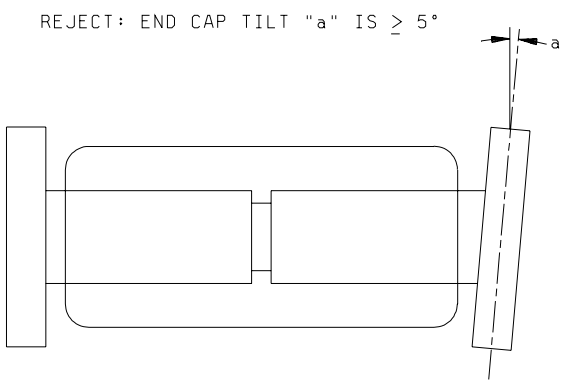

FIGURE 2074-D11. End-cap tilt.

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REJECT: DEVICE WITH END CAP DEFORMATION THAT
EXCEEDS ANY SPEIFIED DEMENSION - "A"

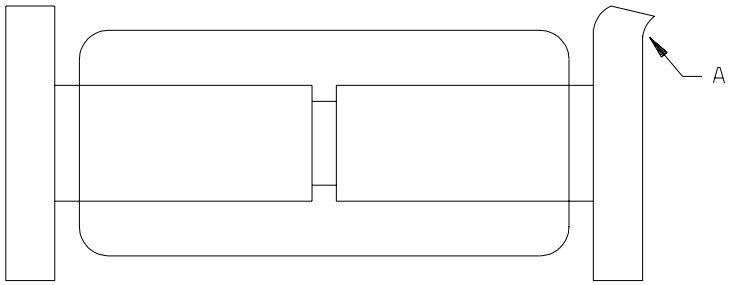

FIGURE 2074-D12. End-cap deformation.

REJECT: END CAP ROTATION "a" $\geq$ 5°

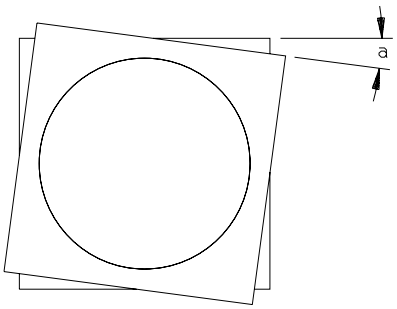

FIGURE 2074-D13. End-cap rotation.

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REJECT: ANY MOUNTING SURFACE REDUCED TO ≤ 75%
OF IT'S DESIGNED AREA DUE TO NICKS("A"), PITS("B"),ECT.

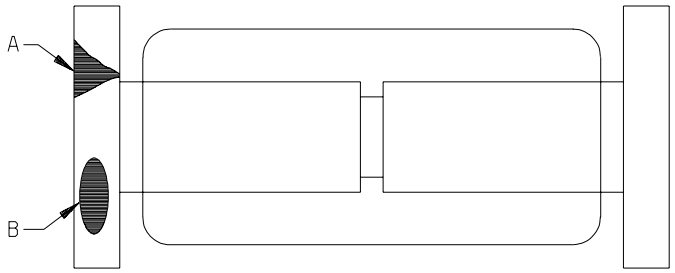

FIGURE 2074-D14. Nicks.

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AXIAL LEAD, TRANSPARENT BODY, POINT CONTACT

E.1 Axial lead, transparent body, point contact. The following additional criteria shall be specified for the point contact construction after encapsulation but before body coating or painting. This appendix is a mandatory part of the standard. The information contained herein is intended for compliance.

E.1.1 Glass cracks and chips (see figure 2074-A1) No cracks shall be allowed in the vicinity of the cavity. Any crack originating at either end of the package or crack that extends into the body of the glass toward the cavity more than 25 percent of the glass-to-glass or glass-to-metal seal length shall be cause for rejection. Any glass chip deep enough to expose the plug or lead surface and extending longitudinally into the glass-to-metal seal toward the cavity to reduce the effective seal length to less than one external lead diameter shall be cause for rejection.

E.1.2 Incomplete seal. All devices shall be inspected for glass-to-metal seal or glass-to-glass seal. Both seals shall be a minimum of one external lead diameter over the entire sealed portion (sealed interface).

E.1.3 Bubbles in seal. All devices shall be inspected for bubbles in the glass-to-metal or glass-to-glass seal. A series of bubbles that reduce the effective seal length to less than one external lead diameter shall be cause for rejection. Bubbles in the glass, but not effecting the glass-to-glass or glass-to-metal seal area, are not cause for rejection.

E.1.4 Glass package deformities (see figure 2074-A2). Any glass envelope deformity equal to or greater than 75 percent of the external lead diameter shall be cause for rejection.

E.1.5 Extraneous matter. A device shall be rejected if there are unattached solder balls, semiconductor material, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

E.1.6 Pressure contact defects. The following misalignments or deformities shall be cause for rejection.

a. Whisker touches glass body wall (see figure 2074-E1).

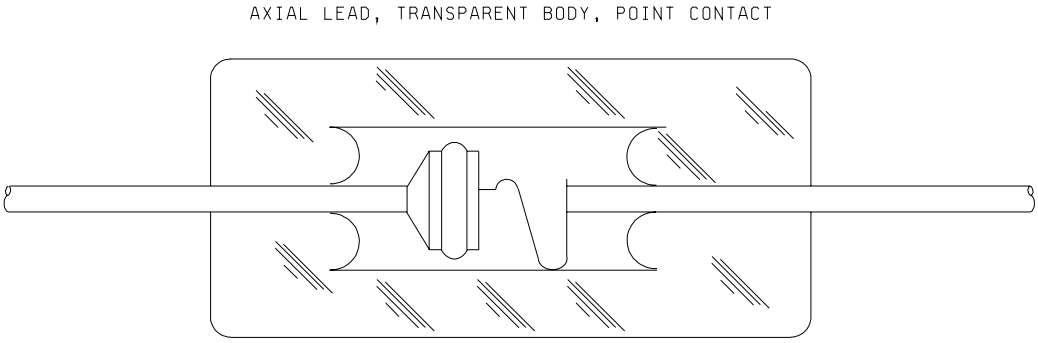

FIGURE 2074-E1. Whisker touches glass body wall (reject).

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b. Whisker loops touch one another (see figure 2074-E2).

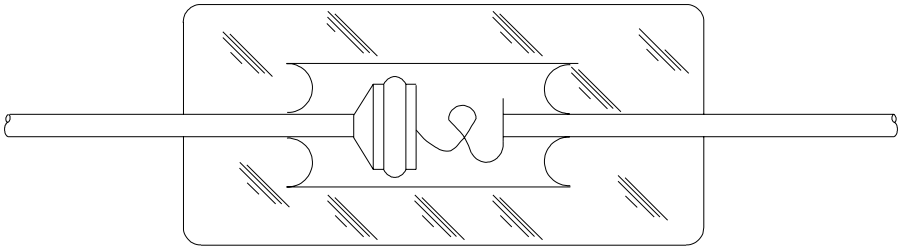

FIGURE 2074-E2 . Whisker loops touch one another (reject).

c. Whisker angle over 10 degrees from normal (see figure 2074-E3).

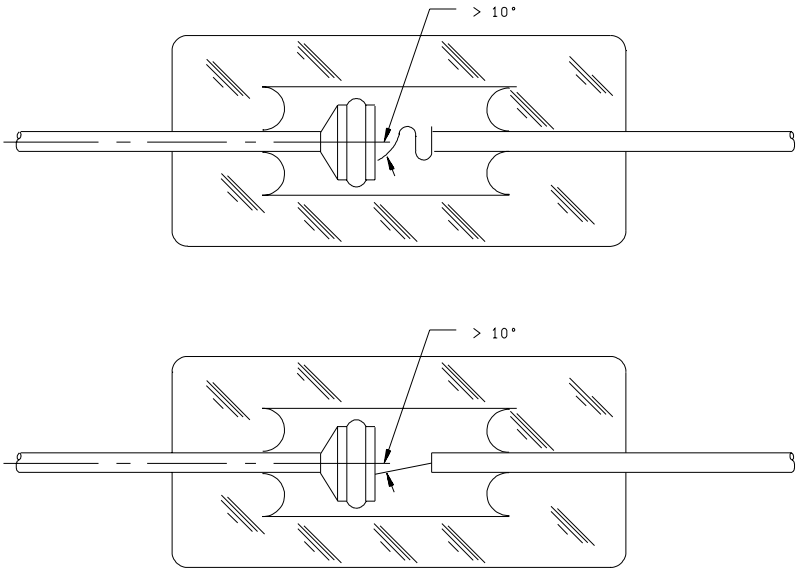

FIGURE 2074-E3 . Whisker angle over 10 degrees from normal (reject).

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E.1.7 Whisker weld to post. Any device that exhibits weld splash or splatter (tear dropped or balled) between whisker and post shall be rejected when it exceeds 25 percent of nominal lead diameter. The profile of whisker weld to the post shall not allow light penetration by more than 50 percent of lead diameter when using back lighting techniques.

E.1.8 Solder voids. A device shall be rejected if solder flow is less than 50 percent of the perimeter of the minimum available contact area of the die.

E.1.9 Die to post contact area. Solder shall be smoothly formed from one element to another and shall be fused to a minimum of one-half the available bonding area. Any solder overflow that touches the opposite surface of the die shall be cause for rejection.

E.1.10 Die alignment. A device shall be rejected if the die surface is not within 15 degrees of being normal to the centerline of the mounting post.

E.1.11 Lead alignment defects (applicable to that portion of each lead within the glass envelope). A device whose lead is either misaligned or bent so that it makes an angle with the principle device axis greater than 10 degrees shall be rejected.

E.12 Die touches glass package (see figure 2074-E4). A device shall be rejected if the die touches the glass envelope.

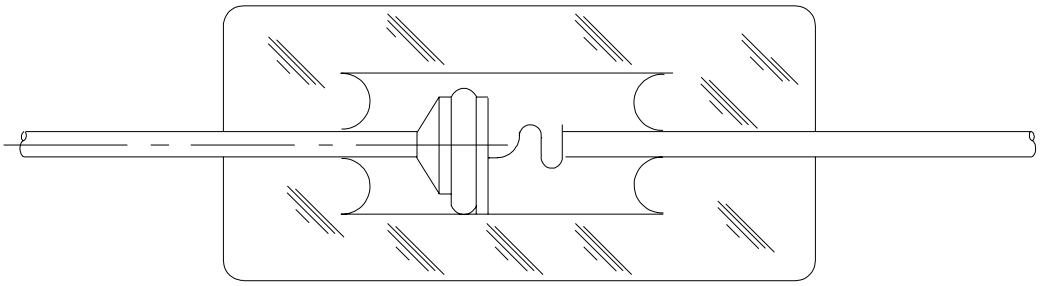

FIGURE 2074-E4. Die touches glass package (reject).

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AXIAL LEAD, DOUBLE PLUG, OPAQUE BODY, POWER RECTIFIER AND REGULATOR

F.1 Axial lead, double plug, opaque body. This appendix is a mandatory part of the standard. The information contained herein is intended for compliance.

F.1.1 Die mounting and alignment. After bonding die to the heat sink, plugs, or leads, the following shall be inspected for defects.

a. Die geometry. A die shall be rejected if it is chipped or broken to the extent that 75 percent or less of the original surface remains.

b. Axial alignment of plugs and die. Plugs shall be aligned axially within 12.5 percent of the diameter of either plug.

c. Tilted die. A device shall be rejected if the die is tilted so that the die surface is greater than 5 degrees from being perpendicular to the mounting post axis.

F.1.2 Die cracks. Any die exhibiting cracks that reduce the total die area (or cracks extending into or across the junction area) to less than 75 percent of its original area shall be cause for rejection.

F.1.3 Inadequate brazing. A device shall be rejected if less than 90 percent of the visible metallized surface (perimeter) is brazed to the heat sink or lead.

F.1.4 Flaking or loose material. No unattached solder, braze, or other bonding material shall extend from the plugs. Any blistering or peeling of plug surface shall be cause for rejection.

F.1.5 Extraneous matter. A device shall be rejected if there is any extraneous, particulate matter between the terminal plugs or on the plug surface. No foreign stains shall be permitted on plug surfaces.

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METAL BODY, AXIAL LEAD, SOLDER CONTACT DESIGN

G.1. Axial lead, metal body, solder contact design. This appendix is a mandatory part of the standard. The information contained herein is intended for compliance.

G.1.1 Examinations before capping.

a. Solder defects (see figures 2074-G1 and 2074-G2). Any device with a solder protrusion that extends more than twice the smallest protrusion width shall be rejected. Solder shall be smoothly formed from one element to another and shall be fused to a minimum of 50 percent of the perimeter between adjacent elements.

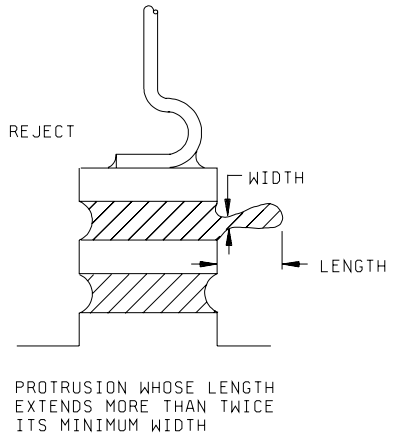

FIGURE 2074-G1. Solder protrusion.

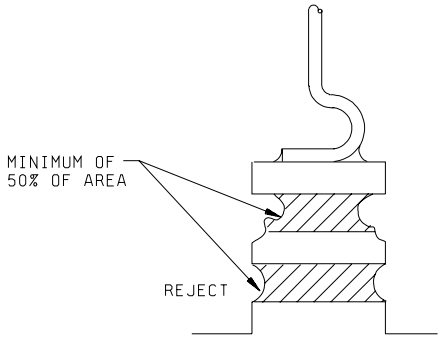

FIGURE 2074-G2. Solder flow.

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b. Alignment (see figure 2074-G3). Any device whose element has its geometric center displaced more than 33 percent of its width from the die, or die stack centerline, shall be rejected.

c. Tilt (see figure 2074-G4). Any element of a device that is tilted more than 10 degrees from the mounting plane shall be cause for rejection.

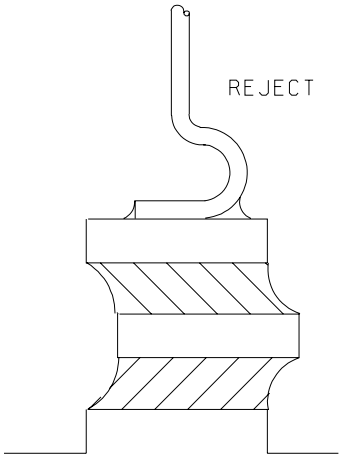

FIGURE 2074-G3. Element alignment.

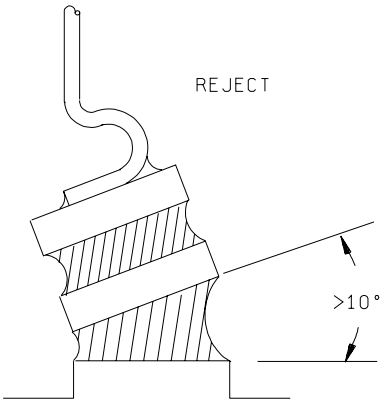

FIGURE 2074-G4. Element tilt.

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d. Die chip outs (see figure 2074-G5). Any device die that exhibits chip outs extending more than 25 percent of the die width or to within 2.0 mils of the junction area shall be cause for rejection.

e. Die cracks (see figure 2074-G6). Any die exhibiting cracks that reduce the total die area (or cracks extending into or across the junction area) to less than 75 percent of its original area shall be cause for rejection.

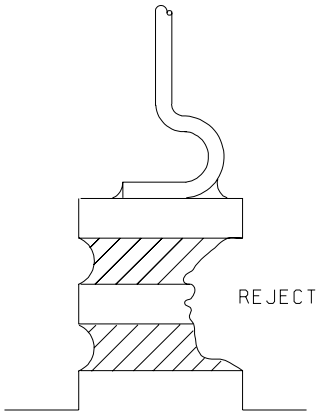

FIGURE 2074-G5. Die chip out.

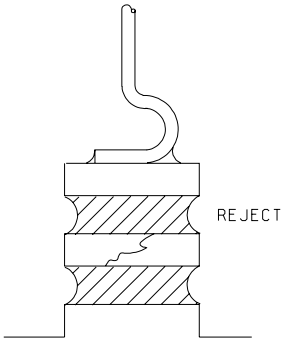

FIGURE 2074-G6. Die cracks.

f. Extraneous matter. A device shall be rejected if there are unattached solder balls, semiconductor material, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

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METAL BODY, STUD MOUNTED, SOLDER CONTACT DESIGN

H.1 Metal body, stud mounted, solder contact design. The following inspections shall be made prior to capping. This appendix is a mandatory part of the standard. The information contained herein is intended for compliance.

H.1.1 Die and lead assembly (see figures 2074-H1 and 2074-H2). The die and lead assembly shall be located on the base pedestal so that there is complete contact over the design contact area. The lead shall be free of nicks and scrapes that reduce the lead diameter by more than 5 percent. The die and lead assembly shall not be tilted more than 5 degress with respect to the base.

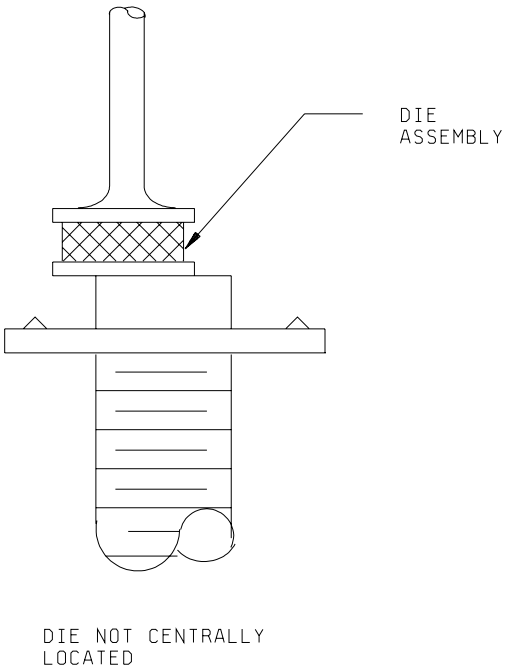

FIGURE 2074-H1. Offset die.

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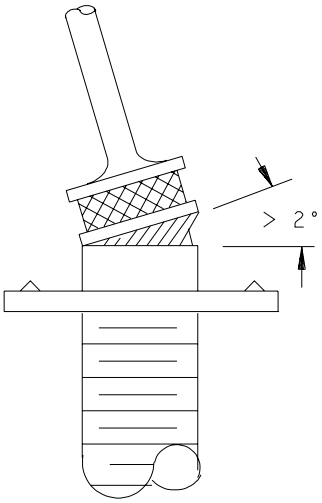

TILTED DIE ASSEMBLY

FIGURE 2074-H2 . Tilted die.

H.1.2 Extraneous matter.

a. Solder slivers and spikes. A device shall be rejected if solder slivers and spikes are not securely attached to the parent body of the solder. A securely attached sliver or spike is one having a cross sectional area greater at the area of attachment than anywhere else on the solder protrusion and having no necked-down areas.

b. Foreign matter. A device shall be rejected if there are unattached solder balls, semiconductor materials, chips, flaked plating, or opaque material that is larger than the smallest distance between exposed active areas.

c. Multiple die attachments. A device shall be rejected if the attached portion of an adjacent die exceeds 25 percent of the die area.

H.1.3 Assembly defects.

a. Tilted elements. A device shall be rejected if any element of the assembly is tilted in excess of 10 degrees from the normal mounting plane.

b. Misaligned elements. A device shall be rejected if any element of the assembly is misaligned or displaced in excess of 33 percent of its width from the die or die stack centerline, bridges two active regions, or extends beyond the isolation region of the oxide.

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METAL BODY, DIAMOND BASE REGULATORS, SOLDER CONTACT DESIGN

I.1 Metal body, diamond base regulators, solder contact design (see figure 2074-I1). This appendix is a mandatory part of the standard. The information contained herein is intended for compliance.

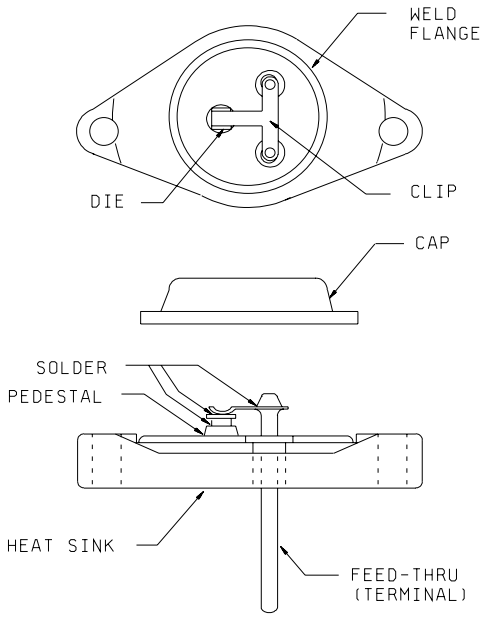

FIGURE 2074-I1 . Diamond base construction.

I.1.1 Die-to-pedestal and die-to-clip solder connections.

a. Solder voids. A device shall be rejected if solder flow is less than 50 percent of the perimeter of the minimum available contact area.

b. Solder overflow. A device shall be rejected if any solder flow bridges from the top to bottom surface of the die or reduces the normal separation of two active regions by 50 percent or more.

I.1.2 Clip-to-post and feed-through to heat sink solder connections.

a. Solder voids. A device shall be rejected if the wetting action of the solder to each member of the connection is not continuous.

b. Solder overflow. A device shall be rejected if any solder flow extends on to any portion of the weld flange of the heat sink.

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METHOD 2075.1

DECAP INTERNAL VISUAL DESIGN VERIFICATION

1. Purpose. The purpose of this test method is to verify that design and construction are the same as those documented in the qualified design report and for which qualification approval has been granted. This test is destructive and would normally be employed on a sampling basis during qualification, or quality conformance inspection, of a specific device type.

2. Apparatus. Equipment used in this examination shall be capable of demonstrating conformance to the requirements of the applicable acquisition document and shall include optical equipment with sufficient magnification to verify all structural features of the devices.

3. Procedure. Devices shall be selected at random from the inspection lot and examined using sufficient magnification to verify that design and construction are in accordance with the requirements of the applicable design documentation or other specific requirements (see 4.). Specimens of constructions which do not contain an internal cavity (e.g., sealed or embedded devices) or those which would experience destruction of internal features of interest as a result of opening, may be obtained from manufacturing prior to sealing. Specimens of constructions with an internal cavity shall be selected from devices which have completed all manufacturing operations and they shall be delidded or opened taking care to minimize damage to the areas to be inspected. When specified by the applicable specification sheet, specimens of constructions with an internal cavity may be obtained from manufacturing prior to sealing.

3.1 Photographs of die topography and intraconnection pattern. When specified, a color photograph or transparency shall be made showing the topography of elements formed on the die or substrate and the metallization pattern. This photograph shall be at a minimum magnification of 80X except that if this results in a photograph larger than 3.5 x 4.5 inches (88.90 x 114.30 mm), the magnification may be reduced to accommodate the 3.5 x 4.5 inches (88.90 x 114.30 mm) view. In addition, a color photograph for all qualifications reports and design changes is required. The photograph shall be submitted with the 36D form.

3.2 Failure criteria. Devices which fail to meet the detailed requirements for design and construction shall constitute a failure.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Any applicable requirements for design and construction.

b. Allowance for obtaining internal cavity devices prior to encapsulation (see 3.).

c. Requirement for photographic record, if applicable (see 3.1), and disposition of photographs.

d. Sample size.

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METHOD 2076.3

RADIOGRAPHY

1. Purpose. The purpose of this test is to nondestructively detect defects within the sealed case, especially those resulting from sealing of the lid to the case, and internal defects such as foreign objects, improper interconnecting wires, and voids in the die attach material. This test establishes methods, criteria, and standards for radiographic examination of discrete devices.

NOTE: For certain case types, the electron shielding effects of device construction materials (packages or internal) may effectively prevent radiographic identification of certain types of defects from some or all possible viewing angles. This factor should be considered in relation to the design of each when application of this test method is specified.

2. Apparatus. The apparatus and materials for this test shall include:

a. Radiographic equipment with a sufficient voltage range to penetrate the device. The focal distance shall be adequate to maintain a sharply defined image of a object with a major dimension of .001 inch (0.025 mm).

b. Radiographic film (Fuji IX50 or equivalent) or medium: Film should be selected to provide the resolution required to view all internal components, including bond wires.

c. Radiographic viewer capable of .001 inch (0.025 mm) resolution in any major dimension.

d. Holding fixtures capable of holding devices in the required positions without interfering with the accuracy or ease of image interpretation.

e. Radiographic quality standards capable of verifying the ability to detect all specified defects for particular package types being x-rayed.

f. A .062 inch (1.57 mm) minimum lead topped table shall be used to prevent back scatter of radiation.

3. Procedure. The x-ray exposure factors, voltage, milliampere setting and time settings shall be selected or adjusted as necessary to obtain satisfactory exposures and achieve maximum image details within the sensitivity requirements for the device or defect features the radiographic test is directed toward. Unless otherwise specified, the x-ray voltage shall be the lowest consistent with these requirements and shall not exceed 150 kV. Although higher voltages may be necessary to penetrate certain packages, these levels may be damaging to some device technologies and should only be used when approved by the manufacturer.

3.1 Mounting and views. The devices shall be mounted in the holding fixture so that the devices are not damaged or contaminated and are in the proper plane as specified. The devices may be mounted in any type of fixture and masking with lead diaphragms, or barium clay may be employed to isolate multiple specimens, provided the fixtures or masking materials do not block the path of the x-rays to the film or any portion of the device. The manufacturer shall provide an image of the device, either drawing or photograph, to show the correct construction of the device and the component placement and orientation.

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3.1.1 Views.

a. Unless otherwise specified, flat packages and single ended cylindrical devices shall have one view taken with the x-rays penetrating in the Y direction as defined in figures 1 and 2 of the general requirements herein. When more than one view is required, the second and third views, as applicable, shall be taken with the x-rays penetrating in the X and Z directions respectively.

b. Unless otherwise specified, stud-mounted and cylindrical axial lead devices shall have one view taken with the x-rays penetrating in the X direction as defined in figures 1 and 2 of the general requirements herein. When more than one view is required, the second and third views, as applicable, shall be taken with the x-rays penetrating in the Z direction and at 45E between the X and Z directions.

c. All JANS devices shall have two views minimum. The views should be specified by the manufacturer to show the all internal components, including bond wires. Extra views shall be specified when necessary to show all bond wires along their length (X1, X2, and Z axis.) and the Y axis. Stud-mounted and axial lead device views shall be taken with x-rays penetrating in the X and Z directions.

3.2 Radiographic quality standard. The radiographic quality standard shall consist of a suitable standard penetrameter such as radiographic quality standard ASTM type B - image quality indicator for semiconductor radiography or equivalent device. Each radiograph shall have two image quality standards exposed with each view located (and properly identified) in opposite corners of the film. The radiographic density of penetrameters chosen shall bracket the density of the devices beings inspected. While this is the minimum resolution required, the presence and clarity of these standards does not relieve the requirement to prepare the x-rays to produce images that allow for detailed inspection of the internal components. For real time radiography images, the image resolution shall be verified to insure that the image quality meets the quality standard of ASTM type B – image quality indicator for semiconductor radiography or equivalent device.

3.3 Film and marking. When used, the radiograph film shall be in a film holder backed with a minimum of .062 inch (1.57 mm) lead or the holder shall be placed on the lead topped table (see 2.f herein). The film shall be identified using techniques that legibly print the following information, photographically on the radiograph:

a. Device manufacturer's name or code identification number.

b. Device type or Part or Identifying Number (PIN).

c. Production lot number, date code, or inspection lot number.

d. Radiographic film view number and date.

e. Device serial or cross reference numbers, when applicable (see 3.3.2 herein).

f. X-ray laboratory identification, if other than device manufacturer.

g. X-ray axis views (X, Y, or Z).

3.3.1 Nonfilm techniques The use of nonfilm techniques is permitted under the following conditions:

a. Permanent records are required. Records not stored on radiographic film shall be archived using a reproducible electronic medium. The preferred medium is a Portable Document File (PDF) with a resolution equal to or better than attainable with radiographic films. The use of other formats such as CD-ROM's and DVD recordings of radiography procedure are allowed with the permission of the qualifying activity, provided the proper clarity, definition, and magnification can be demonstrated

b. The equipment is capable of producing results of equal quality when compared with film techniques. Digital images shall be screened on display monitors capable of producing equal or better magnification than that used to screen films.

c. All requirements of this method are complied with except those pertaining to the actual film.

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3.3.2 Real time radiography.

3.3.2.1. Apparatus. The apparatus and materials for this test shall include:

a. Radiographic equipment with a sufficient voltage range to penetrate the device. The focal distance shall be adequate to maintain a sharply defined image of a object with a major dimension of .001 inch (0.025 mm).

b. Radiographic viewer capable of .001 inch (0.025 mm) resolution in any major dimension.

c. Holding fixtures capable of holding devices in the required positions without interfering with the accuracy or ease of image interpretation.

d. Radiographic quality standards capable of verifying the ability to detect all specified defects for particular package types being x-rayed.

3.3.2.2. Procedure. The x-ray exposure factors, voltage, milliampere setting, and time settings shall be selected or adjusted as necessary to obtain satisfactory exposures and achieve maximum image details within the sensitivity requirements for the device, or defect features, the radiographic test is directed toward. Unless otherwise specified, the x-ray voltage shall be the lowest consistent with these requirements and shall not exceed 150 kV. Although higher voltages may be necessary to penetrate certain packages, these levels may be damaging to some device technologies. Higher voltages should be used only when approved by the manufacturer because they are necessary in some cases. Real time radiographic systems shall be characterized for their dose rate. The dose rate should be identified and a safe time limit established to ensure devices under test are not subjected to excessive levels of radiation.

3.3.2.3 Mounting and views. The devices shall be mounted in the holding fixture so that the devices are not damaged or contaminated and are in the proper plane as specified. The devices may be mounted in any type of fixture and masking with lead diaphragms, or barium clay may be employed to isolate multiple specimens, provided the fixtures or masking materials do not block the path of the x-rays to the film or any portion of the device. The manufacturer shall provide an image of the device, either drawing or photograph, to show the correct construction of the device and the component placement and orientation.

3.3.2.3.1 Views.

a. Unless otherwise specified, flat packages and single ended cylindrical devices shall have three views taken with the x-rays penetrating in the Y direction as defined in figures 1 and 2 of the general requirements herein. When more than one view is required, the second and third views, as applicable, shall be taken with the x-rays penetrating in the X and Z directions respectively. We are not limited by views with real time therefore views X, Y, and Z should be taken for each device. Manufacturers recommended directions should be included as well.

b. Unless otherwise specified, stud-mounted and cylindrical axial lead devices shall have one view taken with the x-rays penetrating in the X direction as defined in figures 1 and 2 of the general requirements herein. When more than one view is required, the second and third views, as applicable, shall be taken with the x-rays penetrating in the Z direction and at 45E between the X and Z directions.

c. All JANS devices shall have two views minimum. The views should be specified by the manufacturer to show all internal components, including bond wires. Extra views shall be specified when necessary to show all bond wires along their length (X1, X2, and Z axis.) and the Y axis. Stud-mounted and axial lead device views shall be taken with x-rays penetrating in the X and Z directions.

3.3.3 Serialized devices. When device serialization is required, each device shall be readily identified by a serial number. The devices shall be radiographed in consecutive, increasing serial order. When a device is missing, the blank space shall contain either the serial number or other x-ray opaque objects to readily identify and correlate the x-ray data. When more than one consecutive device is missing within serialized devices, the serial number of the last device before the skip and the first device after the skip may, at the manufacturer's option, be used in place of the multiple opaque objects.

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3.3.4 Special device marking. When specified (see 4.c herein), the devices that have been x-rayed and found acceptable shall be identified with a blue dot on the external case. The blue dot shall be approximately .062 inch (1.57 mm) in diameter. The color selected from FED-STD-595 shall be any shade between 15102-15123 or 25102-25109. The dot shall be placed so that it is readily visible but shall not obliterate other device markings. (Other colors, for example green, can also be used) Use blue dot for film radiography and green dot for real time radiography.

3.4 Tests. The x-ray exposure factor shall be selected to achieve resolution of .001 inch (0.025 mm) major dimension, less than 10 percent distortion and an "H" and "D" film density between 1 and 2.5 in the area of interest of the device image. Radiographs shall be made for each view required (see 4 herein.). This requirement does not apply to real time radiography.

3.5 Processing. The radiographic film manufacturer's recommended procedure shall be used to develop the exposed film, and the film shall be processed so that it is free of processing defects such as fingerprints, scratches, fogging, chemical spots, and blemishes. This requirement does not apply to real time radiography.

3.6 Operating personnel. Personnel who will perform radiographic inspection shall have training in radiographic procedures and techniques so that defects revealed by this method can be validly interpreted and compared with applicable standards. Operators shall be trained and certified in the operation of the specific real time radiographic system they operate. The following minimum vision requirements shall apply for visual acuity of personnel inspecting film as well as personnel authorized to conduct radiographic tests:

a. Distant vision shall equal at least 20/30 in both eyes, corrected or uncorrected.

b. Near vision shall be such that the operator can read Jaegger type No. 2 at a distance of 16 inches (406.4 mm), corrected or uncorrected.

c. Vision tests shall be performed by an oculist, optometrist, or other professionally recognized personnel at least once a year.

3.7 Interpretation of radiographs. Utilizing the equipment specified herein, radiographs shall be inspected to determine if each device conforms to this standard or if it is defective and shall be rejected. Interpretation of the radiograph shall be made under low light level conditions without glare on the radiographic viewing surface. The radiographs shall be examined on a suitable illuminator with variable intensity or on a viewer suitable for radiographic inspection on projection type viewing equipment. The radiograph shall be viewed at a magnification between 6X and 20X. Viewing masks may be used when necessary. Any radiograph not clearly illustrating the features in the radiographic quality standards is not acceptable and another radiograph of the devices shall be taken. In the event that parts of the device cannot be clearly seen and evaluated in accordance with 3.9 herein, the radiographer shall so note on the radiography report that the criteria has not been evaluated and cannot be confirmed.

3.7.1 Interpretation of real time images. Utilizing the equipment specified herein, real time images shall be inspected to determine if each device conforms to this standard or if it is defective and shall be rejected. The radiograph shall be viewed at a magnification between 6X and 20X. Viewing masks may be used when necessary. Any radiograph not clearly illustrating the features in the radiographic quality standards is not acceptable and another radiograph of the devices shall be taken. In the event that parts of the device cannot be clearly seen and evaluated in accordance with 3.8 herein, the radiographer shall so note on the radiography report that the criteria has not been evaluated and cannot be confirmed.

3.8 Reports and records.

3.8.1 Reports of inspection. For JANS devices, or when specified for other device classes, the manufacturer shall furnish inspection reports with each shipment of devices. The report shall describe the results of the radiographic inspection, and list the order number or equivalent identification, the PIN, the date code, the quantity inspected, the quantity rejected, and the date of test. For each rejected device, the PIN, the serial number, when applicable, and the cause for rejection shall be listed. Any criteria that cannot be evaluated due to resolution of the film shall be noted on the report.

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3.8.2 Radiograph submission. When specified, one set of the applicable radiographs shall accompany each shipment of devices. Real time radiography image results submitted on suitable media will be provided.

3.8.3 Radiograph and report retention. When specified, the manufacturer shall retain a set of the radiographs or a set of the real time radiography images and a copy of the inspection report. These shall be retained for the period specified.

3.9 Examination and acceptance criteria.

3.9.1 Device construction. Acceptable devices shall be of the specified design and construction with regard to the characteristics discernible through radiographic examination. Devices that deviate significantly from the specified construction shall be rejected.

3.9.2 Individual device defects. The individual device examination shall include, but not be limited to, inspection for foreign particles, solder or weld "splash" build up of bonding material, proper shape and placement of lead wires or whiskers, and bond of lead or whisker to semiconductor element. Devices for which the radiograph reveals any of the following defects shall not be accepted.

3.9.2.1 Presence of extraneous material. Extraneous matter or foreign particles shall include:

a. Any foreign material greater than .003 inch (0.076 mm) or of any lesser size which is sufficient to bridge non-connected conducting elements of the device.

b. Any wire tail extending beyond its bond end by more than two diameters at the semiconductor bond pad or by more than four wire diameters at the package post.

c. Any burr on a post greater than .003 inch (0.076 mm) in its major dimension.

d. Metal flaking on the header or posts inside the package.

e. Excessive bonding material build-up.

(1) Bonding material that is higher than one times the height of the semiconductor die.

(2) There shall be no visible loose extraneous material greater than .001 inch (0.025 mm) allowed. Excessive bonding material which is not loose and passes the requirements of 3.9.2.1.e (1) shall be allowed unless the height of the accumulation is greater than the width of its base or the material necks down at any point from the top of the accumulation to the base.

3.9.2.2 Unacceptable construction. In the examination of devices, the following aspects shall be considered unacceptable construction and devices that exhibit any of the following defects shall be rejected:

a. Total contact area voids less than one-half of the total contact area is required for mechanical strength. For thermal integrity, total contact area voids in excess of 15 percent of the total contact area, for all power and case mounted devices and 30 percent for all other devices is rejectable unless otherwise specified on the applicable specification sheet. Voids less than twice the thickness of the die are not applicable. If one or more devices fail this die attach criteria the entire lot shall be re-tested to the applicable thermal impedance requirements. In addition, if the die attach image shows any unusual anomalies or any significant voiding directly under the active area or multiple relatively large voids, the entire lot shall be re test to the applicable thermal impedance requirements.

b. A single void which traverses either the length or width of the semiconductor die and exceeds 10 percent of the total intended contact area.

(1) Voids: When radiographing devices, certain types of mounting do not give true representations of voids. When such devices are inspected, the mounting shall be noted on the inspection report (see figure 2076-1).

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(2) Wires present, other than those connecting specific areas of the semiconductor die to the external leads.

(3) Angle between semiconductor die surface and edge less than 45 degrees.

(4) Defective seal: Any device wherein the integral lid seal is not continuous or is reduced from its designed sealing width by more than 75 percent.

NOTE: Expulsion resulting from the final sealing operation is not considered extraneous material as long as it can be established that it is continuous, uniform, and attached to the parent material and does not exhibit a ball, splash, or tear-drop configuration.

(5) Inadequate clearance: Acceptable devices shall have adequate internal clearance to assure that the elements cannot contact one another or the case. No crossover of wires connected to different electrical elements shall be allowed. Depending upon the case type, devices shall be rejected for the following conditions:

(a) Flat pack and dual-in-line (see figure 2076-2).

1. Any lead wire that appears to touch or cross another lead wire or bond (Y plane only).

2. Any lead wire that deviates from a straight line from bond to external lead and appears to be within .002 inch (0.0504 mm) of another bond (Y plane only).

3. Lead wires that do not deviate from a straight line from bond to external lead and appear to touch another wire or bond (Y plane only).

4. Any lead wire that touches or is less than .002 inch (0.0504 mm) from the case or external lead to which it is not attached (X and Y plane).

5. Any bond that is less than .001 inch (0.0254 mm) (excluding bonds connected by a common conductor) from another bond (Y plane only).

6. Any wire making a straight line run (with no arc) from die bonding pad to package post.

7. Any cracks, nicks, neckdown, or cuts on lead wires that reduces the wire diameter by more than 25 percent

(b) Round or "box" transistor type (see figure 2076-3).

1. Any lead wire that touches or is less than .002 inch (0.0504 mm) from the case or external lead to which it is not attached (X and Y plane).

2. Lead wires that sag below an imaginary plane across the top of the bond (X plane only).

3. Any lead wire that appears to touch or cross another lead wire or bond (Y plane only) if bonded to different electrical elements.

4. Any lead wire that deviates from a straight line from bond to external lead appears to touch or to be within .002 inch (0.0504 mm) of another wire or bond (Y plane only).

5. Any bond that is less than .001 inch (0.0254 mm) (excluding bonds connected by a common conductor) from another bond (Y plane only).

6. Any wire making a straight line run (with no arc) from die bonding pad to package post, unless specifically designed in this manner (e.g., clips, rigid connecting leads, or heavy power leads).

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7. Any internal post that is bent more than 10 degrees from the vertical (or intended design position), or is not uniform in length and construction, or comes closer than one post diameter to another post.

8. Any post in a low profile case (such as a TO-46) which comes closer to the top of the case than 20 percent of the total inside dimension between the header and the top of the case. Any device in which the semiconductor element is vertical to the header, and comes closer than .002 inch (0.0504 mm) to the header, or to any part of the case.

9. Any cracks, nicks, neckdown, or cuts on lead wires that reduces the wire diameter by more than 25 percent

(c) Axial lead type (see figure 2076-4).

1. Whisker embedded within glass body wall.

2. Whisker tilted more than 5 degrees in any direction from the device lead axis or deformed to the extent that it touches itself.

3. Either half of an S or C bend whisker that is compressed so that any dimension is reduced to less than 50 percent of its design value. On diodes with whiskers metallurgically bonded to the post and to the die, the whisker may be deformed to the extent that it touches itself if the minimum whisker clearance zone specified in figure 2076-4a is maintained for metal packages.

4. Whiskerless construction device with plug displacement distance more than one-fourth of the diameter of the plug with respect to the central axis of the device.

5. Semiconductor element mounting tilted more than 15E from normal to the main axis of the device.

6. Die hanging over edge of header or pedestal more than 20 percent of the die contact area by design.

7. Less than 75 percent of the semiconductor element base area is bonded to the mounting surface.

8. Voids in the welds which reduce the lead to plug connection by more than 25 percent of the total weld area.

9. Devices with package deformities such as body glass cracks, incomplete seals (e.g., voids, position of glass), die chip outs, and severe misalignment of S- and C-shaped whisker connections to die or post that exceed the limits of the applicable visual inspection requirements.

3.9.3 Encapsulated non-cavity assemblies of discrete devices. External to the individual devices, the encapsulating material shall be examined and rejected for the following defects.

3.9.3.1 Extraneous material. Extraneous matter of any shape with any dimension exceeding .020 inch (0.51 mm). Also, any two adjacent particles of such matter with total dimensions exceeding .030 inch (0.76 mm).

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4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Number of views, if other than indicated in 3.1 and 3.1.1.

   b. Radiograph submission, if applicable (see 3.8.2).

   c. Marking, if other than indicated in 3.3 and marking of samples to indicate they have been radiographed, if required (see 3.3.3).

   d. Sample defects and criteria for acceptance or rejection, if other than indicated in 3.9.

   e. Radiograph and report retention, if applicable (see 3.8.3).

   f. Test reports when required.

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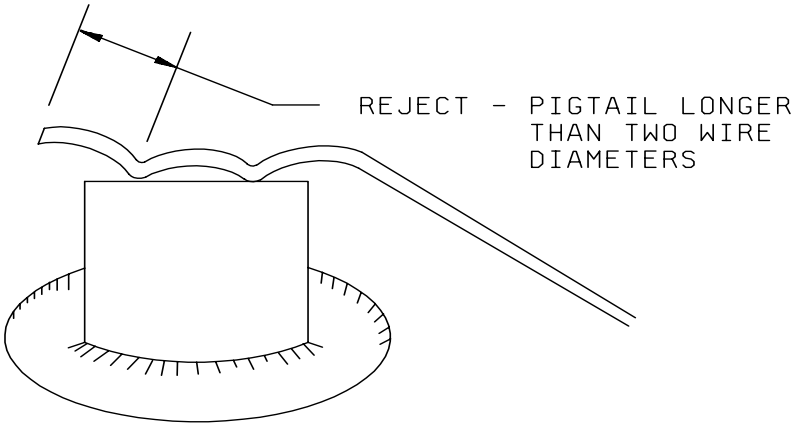

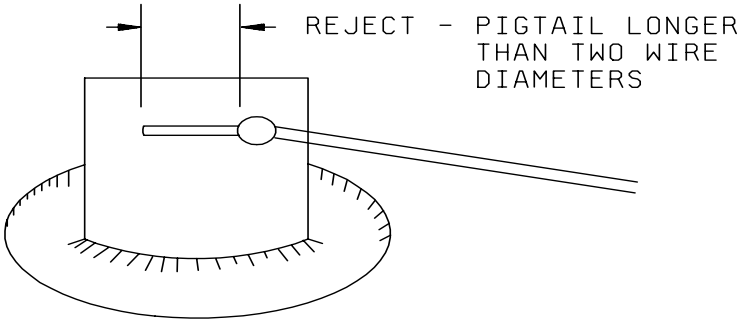

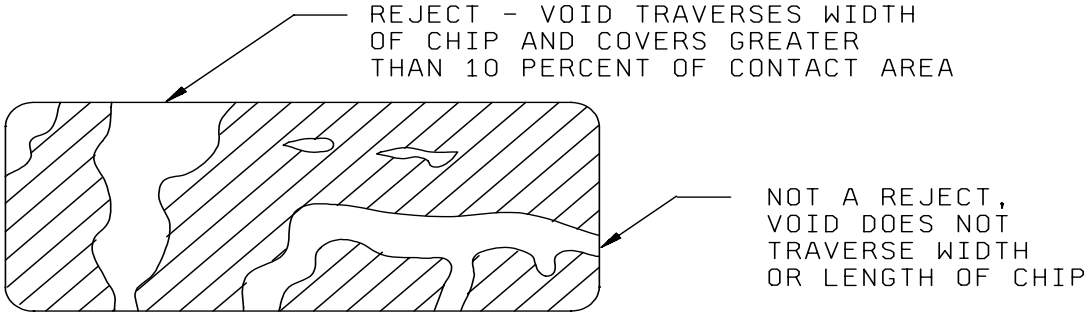

FIGURE 2076-1. Acceptable and unacceptable voids and excessive pigtails.

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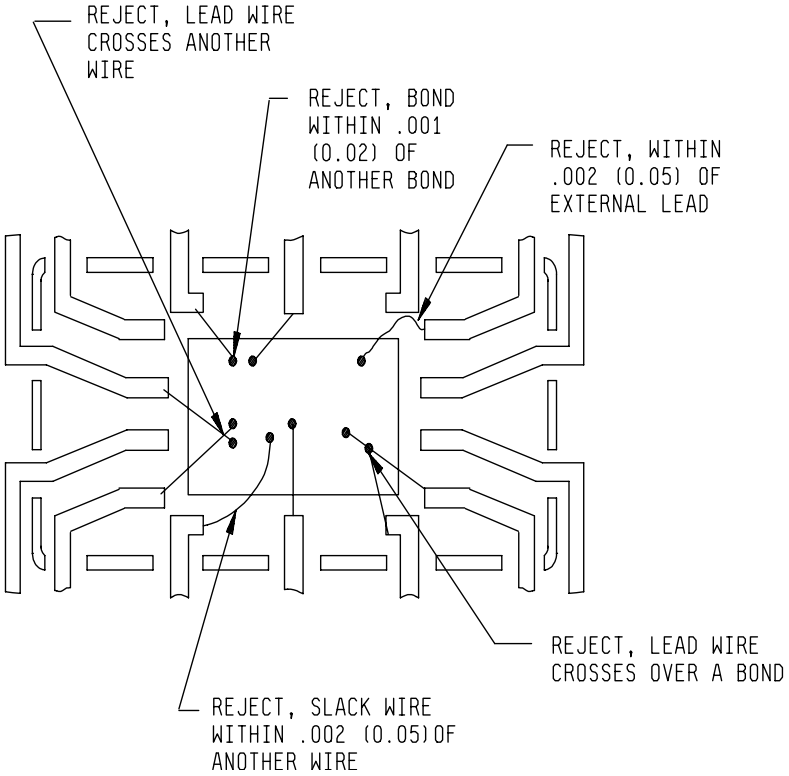

FIGURE 2076-2. Clearance in dual-in-line or flat pack type device.

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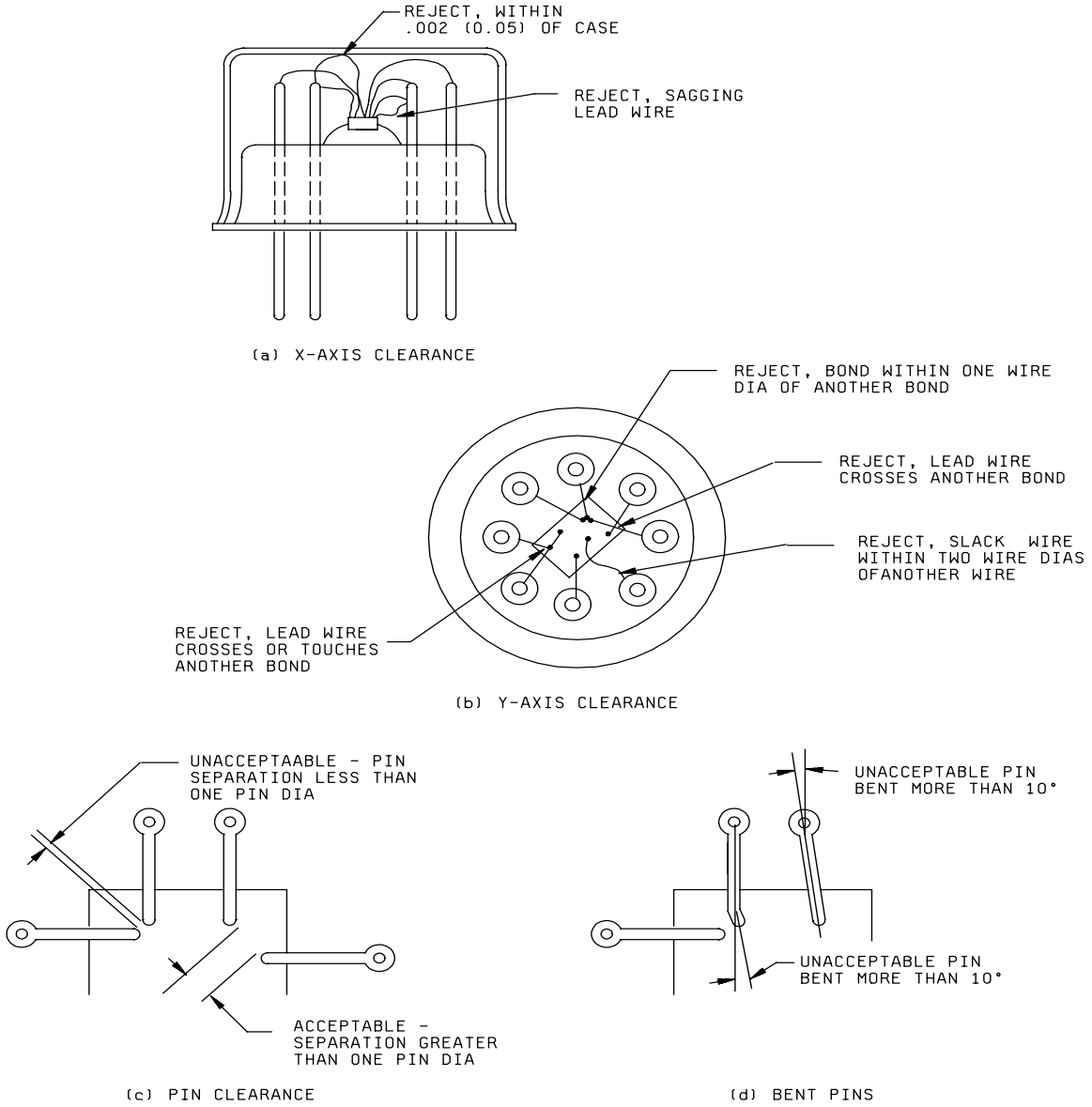

FIGURE 2076-3. Clearance in round or box transistor type device.

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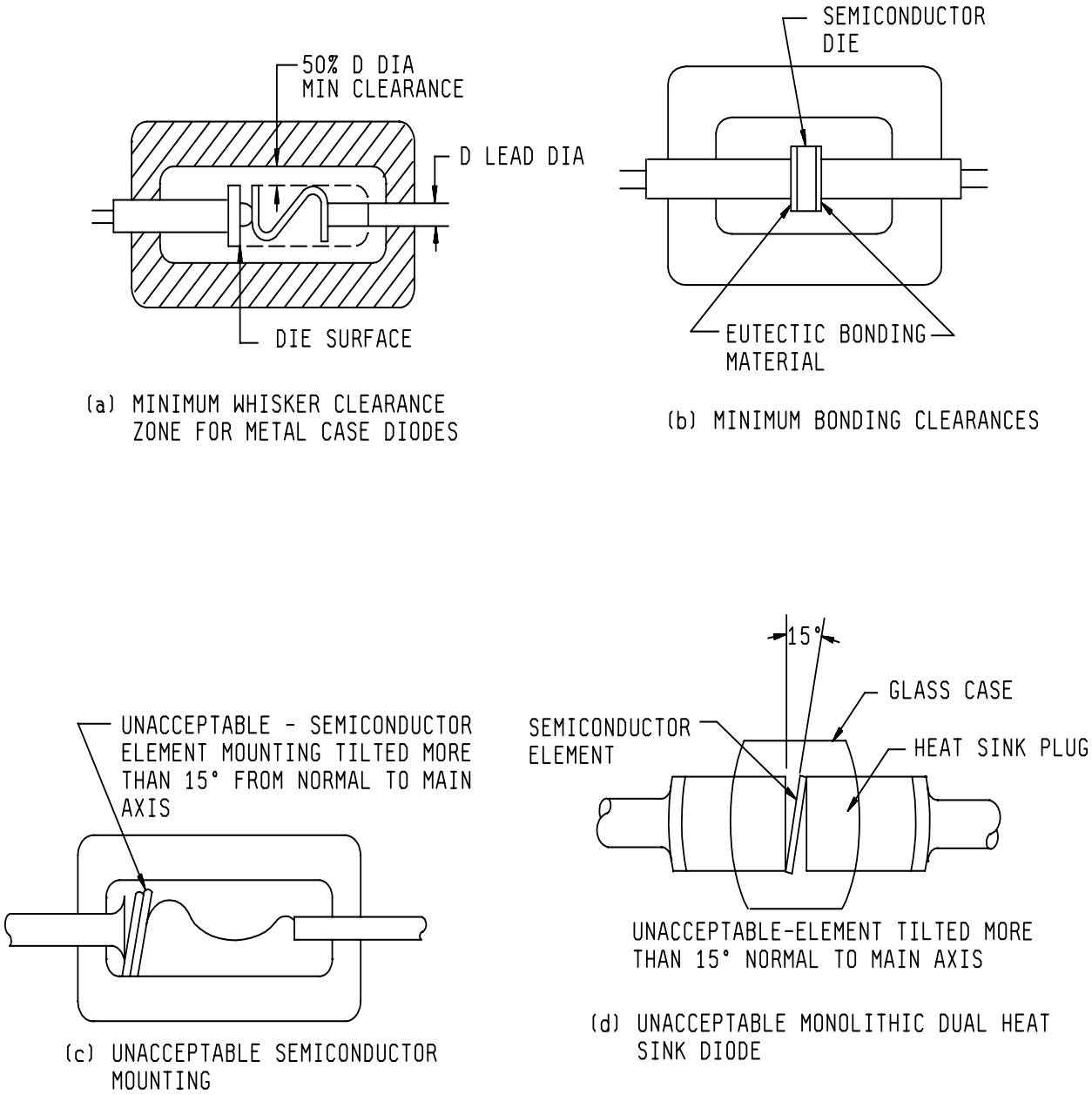

FIGURE 2076-4. Clearance in cylindrical axial lead type device.

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METHOD 2077.3

SCANNING ELECTRON MICROSCOPE INSPECTION OF METALLIZATION

1. Purpose. This test method provides a means of judging the quality and acceptability of metallization on semiconductor dice. It addresses the specific metallization defects that are batch process oriented and which can best be identified utilizing this method. It should not be used as a test method for workmanship and other type defects best identified using the visual inspection criteria of test method 2072. The term, "dice", for the purpose of this test method, includes diodes and transistors which have expanded metallization contacts or metallization interconnects.

2. Apparatus. The apparatus for this inspection shall be a scanning electron microscope (SEM) having an ultimate resolution of 100 Å or less and a variable magnification to at least 20,000X. The apparatus shall be such that the specimen can be tilted to a viewing angle (see figure 2077-1) of 60 degrees or greater, and can be rotated through 360 degrees. Evidence of using competent SEM operating personnel, as well as acceptable techniques and equipment that meet the requirements of this test method, shall be demonstrated for the approval of the qualifying activity or, when applicable, a designated representative of the acquiring activity.

3. Procedure.

3.1 Sample selection. Proper sampling is an integral part of this test method. Statistical techniques, using random selection, are not practical here because of the large sample size that would be required. This test method specifies means of minimizing test samples while maintaining confidence in test integrity by designating for examination wafers in specific locations on the wafer holder(s) in the metallization chamber, and specific dice on the wafers. These dice are in typical or worst case positions for the metallization configuration. Dice selected for SEM examination shall not be immediately adjacent to the wafer edge, and they shall be free of smearing or inking, since this could obscure processing faults for which they are to be inspected. Metallization acceptance shall be based on examination of sample dice, using either a single wafer acceptance basis or a process lot acceptance basis. A process lot is a batch of wafers which has been received together, those common processes which determine the slope and thickness of the oxide step and which have been metallized as a group.

3.1.1 Sampling condition A, unglassivated devices. This sampling condition applies to devices which have no glassivation over the metallization. Steps 1 and 2 (See 3.1.1.1 and 3.1.1.2 herein), both apply when acceptance is on a lot acceptance basis. Only step 2 applies when acceptance is on a single wafer acceptance basis.

3.1.1.1 Step 1: Slice selection. From each lot to be examined on a lot acceptance basis, wafers shall be selected from the designated positions on the wafer holder(s) in the metallizing chamber. In accordance with the definition of lot in 3.1, if there is more than one process lot in a metallization chamber, each process lot shall be grouped approximately in a separate sector within the wafer holder, and a separate set of wafers shall be selected for each process lot being examined on a lot acceptance basis. Table 2077-I and figure 2077-2 specify the number and sites of wafers to be selected. Dice selection from the selected wafers shall be in accordance with the sampling plan established for a single wafer in step 2 (see 3.1.1.2).

3.1.1.2 Step 2: Dice selection. When a wafer is to be evaluated (for acceptance on a single wafer basis, or with one or more wafers on a lot acceptance basis), either of the following sampling conditions may be used at the manufacturer's option.

3.1.1.2.1 Sampling condition A_1: Quadrants. Immediately following the dicing operation (i.e., scribe and break, saw, etch) and before relative die location on the wafer is lost, four dice shall be selected. The positions of these dice shall be near the periphery of the wafer and approximately 90 degrees apart (see figure 2077-2).

3.1.1.2.2 Sampling condition A_2: Segment. After completion of all processing steps and, prior to dicing, two segments shall be separated from opposite sides of each wafer to be examined. These segments shall be detached along a chord approximately one-third of the wafer radius in from the edge of the wafer. One die from near each end of each segment (i.e., four dice) shall then be subjected to SEM examination.

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TABLE 2077-I. Wafer sampling procedures.

Metallization chamber configuration	Number of process lots in chamber 1/	Required number of samples in accordance with process lot		Sampling plan in accordance with process lot
		Evaporation	Sputtering	
Projected plane view of the wafer holder is a circle. Wafer holder is stationary or "wobbulates".	1	5	2	Four from near the periphery of the wafer holder and 90 degrees apart. One from the center of the holder. See figure 2077-2a.
	2	3, 4, or 5	2	See figures 2077-2b or 2077-2c.
	3	3 or 4	2	See figure 2077-2d.
	4	3	2	See figure 2077-2e.
Wafer holder is symmetrical (i.e, circular, square). Deposition source(s) is above or below the wafer holder. Wafer holder rotates about its center during deposition.	1, 2, 3, or 4	2	2	For each process lot, one from the periphery of the wafer holder, and from close proximity to the center of rotation. See figure 2077-2f.
Planetary system. One or more symmetrical wafer holders (planets) rotate about their own axes while simultaneously revolving about the center of the chamber. Deposition source(s) is above or below the wafer holders.	1, 2, 3, or 4 for each planet	2	2	For each process lot, one from near the periphery of a planet, and one from near the center of the same planet. 2/ See figure 2077-2f.

1/ If there is more than one process lot in a metallization chamber, each process lot shall be grouped approximately in a separate sector within the wafer holder. A sector is an area of the circular wafer holder bounded by two radii and the subtended arc; quadrants and semicircles are used as examples on figure 2077-2.

2/ Sample wafers need to be selected from only one planet if all process lots contained in the chamber are included in that planet. Otherwise, sample wafers of the process lot(s) not included in that planet shall be selected from another planet(s).

NOTE: If a wafer holder has only one circular row, or if only one row is used on a multi-rowed wafer holder, the total number of a specified sample wafers shall be taken from that row.

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3.1.2 Sampling condition C: Glassivated devices. This sampling condition applies to devices which have glassivation over the metallization. Steps 1 and 2 (see 3.1.2.1 and 3.1.2.2 herein), both apply when acceptance is on a lot acceptance basis. Only step 2 applies when acceptance is on a single wafer acceptance basis.

3.1.2.1 Step 1: Wafer selection. From each lot to be examined on a lot acceptance basis, wafers shall be selected from the designated positions on the wafer holder in the metallizing chamber. In accordance with the definition of lot in 3.1, if there is more than one process lot in a metallization chamber, each process lot shall be grouped approximately in a separate sector within the wafer holder, and a separate set of wafers shall be selected for each process lot being examined on a lot acceptance basis. Table 2077-I and figure 2077-2 specify the number and sites of wafers to be selected. Dice selection from the selected wafers shall be in accordance with the sampling plan established for a single wafer in step 2 (see 3.1.2.2).

3.1.2.2. Step 2: Dice selection. When a wafer is to be evaluated (for acceptance on a single wafer acceptance basis, or with one or more other wafers on a lot acceptance basis), any of the following sampling conditions may be used at the manufacturer's option.

3.1.2.2.1 Sampling condition B_1: Quadrants. This is the recommended condition for glassivated devices. Immediately following the dicing operation (i.e., scribe and break, saw, etch) and before relative die location on the wafer is lost, four dice shall be selected. The positions of these dice shall be near the periphery of the wafer and approximately 90 degrees apart. The glassivation shall then be removed from the dice using a suitable etch. It is recommended that the etchant used have an etch rate for the glassivation which is approximately 200 times that for the metallization. The dice shall be periodically examined during glass removal using a bright field metallurgical microscope to determine when all the glassivation has been removed and to minimize the possibility of etching the metallization.

3.1.2.2.2 Sampling condition B_2: Segment, prior to glassivation. This sampling condition may be used only if the glassivation processing temperature is lower than +400°C. Two segments shall be separated from opposite sides of each wafer to be examined immediately before the glassivation coating operation; (i.e., subsequent to metallization, etching, and sintering, but before glassivation). These segments shall be detached along a chord approximately one-third of the wafer radius in from the edge of the wafer. One die from near each end of each segment (i.e., four dice) shall be subjected to SEM examination.

3.1.2.2.3 Sampling condition B_3: Segment, after glassivation. Two segments shall be separated from opposite sides of each wafer subsequent to sintering and glassivation. These segments shall be detached along a chord approximately one-third of the wafer radius in from the edge of the wafer. The glassivation shall then be removed from the segment using a suitable etch (see 3.1.2.2.1 for the etch rate). The segment shall be periodically examined using a bright field metallurgical microscope to determine when all the glassivation has been removed and to minimize the possibility of etching the metallization. One die from near each end of each segment (i.e., four dice) shall be subjected to SEM examination.

3.2 Lot control during SEM examination. After dice sample selection for SEM examination, the manufacturer may elect either of two options as follows.

3.2.1 Option 1. The manufacturer may continue normal processing of the lot with the risk of later recall and rejection of product if SEM inspection, when performed, shows defective metallization. If this option is elected, positive control and recall of processed material shall be demonstrated by the manufacturer by having adequate traceability documentation.

3.2.2 Option 2. Prior to any further processing, the manufacturer may store the dice or wafers in a suitable environment until SEM examination has been completed and approval for further processing has been granted.

3.3 Specimen preparation. Specimens shall be mounted in an appropriate manner for examination. Suitable caution shall be exercised in the use of materials such as conducting paints and adhesives for specimen mounting so that important features are not obscured. Specimens may be examined without any special coating to facilitate SEM examination if the required resolution can be obtained, or they may be coated with a vapor-deposited or sputtered film of a suitable conductive material. If the specimens are coated, thickness or quality of the coatings shall be such that no artifacts are introduced.

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3.4 Specimen examination, general requirements. The metallization on all four edge directions shall be examined on each die for each type of contact window step and for each other types of oxide steps (see table 2077-II) (oxide refers to any insulating material used on the semiconductor die, whether S_iO_X or S_iN_X). A single window (or other type of oxide step) may be viewed if metallization covers the entire window (or other type of oxide step) extending up to and over each edge, and onto the top of the oxide at each edge. Other windows (or other types of oxide steps) on the die shall be examined to meet the requirement that all four directional edges of each type of window (or other type of oxide step) shall be examined on each die. General metallization defects, such as peeling and voids, shall be viewed to provide for the best examination for those defects.

TABLE 2077-II. Examination procedure for sample dice.

Device type	Area of examination	Examination	Minimum - maximum magnification	Photographic documentation 1/
Expanded contact bipolar and power FET's (see 3.5.1)	Oxide step (contact windows and other types of oxide steps) 2/	All	4,000X to 20,000X	Two of the worst case oxide steps.
	General metallization 3/	All	1,000X to 6,000X	Worst case general metallization.

1/ See 3.8 (an additional photograph may be required).
2/ Scanning examination shall include all four directional edges of oxide steps (documentation need only show the worst case). Oxide steps include contact windows (emitters, bases, collectors, drains, sources, diffused resistors) and other types (i.e., diffusion cuts for emitters, bases, collectors, and field oxide steps). See 3.7.1 for accept/reject criteria.
3/ See 3.7 for accept/reject criteria.

NOTE: For multi-layered-metal interconnection systems, see 3.5.3 and 3.7.3. Window coverage also shall be examined.

3.4.1. Viewing angle. Specimens shall be viewed at an appropriate angle to accurately assess the quality of the metallization. Contact windows are normally viewed at an angle of 45 degrees to 60 degrees or greater (see figure 2077-1).

3.4.2. Viewing direction. Specimens shall be viewed in an appropriate direction to accurately assess the quality of the metallization. This inspection shall include examination of metallization at the edges of contact windows and other types of oxide steps (see 3.4) in any direction that provides clear views of each edge and that best displays any defects at the oxide step. The viewing direction may be perpendicular to an edge, parallel with an edge, or at some oblique angle.

3.4.3 Magnification. The magnification ranges shall be between 4,000X and 20,000X for examination of oxide steps and between 1,000X and 6,000X for general metallization defects, such as peeling and voids (refer to table 2077-II). When dice are subjected to reinspection, such reinspection shall be accomplished at any magnification within the specified magnification.

3.5 Specimen examination detail requirements.

3.5.1. Expanded contact bipolar. Examination shall be as specified herein and summarized in table 2077-II.

3.5.1.1 Oxide steps. Inspect the metallization at all types of oxide steps (see table 2077-II) and document in accordance with 3.8.

3.5.1.2 General metallization. Inspect all general metallization on each die for defects such as peeling and voids. Document in accordance with 3.8.

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3.5.2 Power FETs. Examination shall be specified herein and summarized in table 2077-II.

3.5.2.1 Oxide steps. Inspect the metallization at all types of oxide steps (see table 2077-II) and document in accordance with 3.8. For RF or power transistors with interdigitated or mesh structures, each base-emitter stripe pair within each pattern shall be inspected as a minimum. Particular attention shall be directed to lateral etching defects and undercut at base and emitter oxide steps. Documentation shall be as specified in 3.8.

3.5.2.2 General metallization. Inspect all general metallization on each die for defects such as peeling and voids. Document in accordance with 3.8.

3.5.3 Multi-layered metal interconnection systems. Multi-layered metal is defined as two or more layers of metal or any other material used for interconnections. Each layer of metal shall be examined. The principal current-carrying layer shall be examined with the SEM; the other layers (i.e., barrier or adhesion) may be examined using either the SEM or an optical microscope, at the manufacturer's option. Accept/reject criteria for multi-layered metal systems are given in 3.7.3. The glassivation (if any) and each successive layer of metal shall be stripped by selective etching with suitable reagents, layer-by-layer, to permit the examination of each layer. If it is impractical to remove the metal on a single die layer-by-layer, one or more dice immediately adjacent to the original die shall be etched so that all layers shall be exposed and examined. Specimen examination shall be in accordance with 3.5.

3.6 Acceptance requirements.

3.6.1. Single slice acceptance basis. The metallization of a wafer shall be judged acceptable only if all sample dice from that wafer are acceptable.

3.6.2 Lot acceptable basis. An entire lot shall be judged acceptable only when all sample dice from all sample wafers are acceptable. At the manufacturer's option, if a lot is rejected in accordance with this paragraph, each wafer from that lot may be individually examined. Acceptance shall then be in accordance with 3.6.1.

3.7 Accept/reject criteria. Rejection of dice shall be based upon batch process oriented defects. Rejection shall not be based upon workmanship and other type defects such as scratches, smeared metallization, or tooling marks. In the event that the presence of such defects obscures the detailed features being examined, an additional die shall be examined which is immediately adjacent to the die with the obscured metallization. Illustrations of typical defects are shown on figure 2077-3 through figure 2077-20.

3.7.1 Oxide steps. The metallization on all four directional edges of every type of oxide step(s) (contact window or other type of oxide step) shall be examined (see 3.4.2). The metallization shall be unacceptable if thinning and one or more defects such as voids, separations, notches, cracks, depressions, or tunnels reduce the cross-sectional area of the metal at the directional edge to less than 50 percent of metal cross-sectional area on either side of the directional edge. When less than 50 percent, for the metallization to be acceptable, all four directional edges shall be covered with metallization (see 3.4.2) and shall be acceptable except in the cases described in 3.7.1.1 and 3.7.1.2.

3.7.1.1 Oxide steps without metallization. In the event that a directional edge profile of a particular type of oxide step cannot be found which is covered with metallization (see 3.4.2) and therefore, a judgment of the quality of the metallization at that directional edge profile cannot be made, this shall not be cause for rejection if:

a. It is established that the edge profile from which metal is absent does not occur in a current-carrying direction, such determination being made either by scanning all oxide steps of this type on the balance of the die, or by examination of a topographical map supplied by the manufacturer which shows the metal interconnect pattern, and;

b. Duplicate sample wafers are examined, these duplicates being located adjacent to the original sample wafers, in the wafer holder, and being rotated so as to be oriented approximately 180 degrees with respect to the original sample wafers during metallization. If the conditions of both 3.7.1.1.a. and 3.7.1.1.b. are met, a lot acceptance basis may be used. If only condition a is met, a single wafer acceptance basis must be used.

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3.7.1.2 Oxide steps with less than 50 percent metallization. If less than the specified percent of the metallization is present at a particular directional edge profile (see figure 2077-3), wafer lot rejection shall not be invoked if:

a. It is established that the edge profile from which metal is absent does not occur in a current-carrying direction, such determination being made either by scanning all oxide steps of this type on the balance of the die, or by examination of a topographical map supplied by the manufacturer which shows the metal interconnect pattern;

b. Acceptance is on a wafer basis only, and;

c. The device is a power FET, no less than 20 percent of the metallization is present, and the maximum calculated current density does not exceed the value which corresponds to the applicable conductor material in accordance with table 2077-III.

TABLE 2077-III. Conductor material.

Conductor material	Maximum allowable continuous current density (RMS for pulse applications)
Aluminum (99.99 percent pure or doped) without glassivation	2×10^5 amps/cm^2
Aluminum (99.99 percent pure or doped) with glassivation	5×10^6 amps/cm^2
Gold	6×10^5 amps/cm^2
All other (unless otherwise specified)	2×10^5 amps/cm^2

3.7.2 General metallization. General metallization is defined for the purpose of this test method as the metallization at all locations except at oxide steps, and shall include metallization (stripes) in the actual contact window regions. Any metallization pulling or lifting (lack of adhesion) shall be unacceptable. Any defects, such as voids which reduce the cross-sectional area of the metallization stripe by more than 50 percent, shall be unacceptable.

3.7.3 Multi-layered metal interconnection systems. These systems may be more susceptible to undercutting than single-layered metal systems and shall, therefore, be examined carefully for this type of defect, in addition to the other types of defects. Refer to 3.5.3 for specimen examination requirements and definition of multi-layered metal systems.

3.7.3.1 Oxide steps. The criteria of 3.7.1 shall apply to both the principal conducting metal and the barrier layer. If by design, a barrier layer is not intended to cover the oxide steps, 3.7.1 shall not apply to the barrier layer.

3.7.3.1.1 Barrier or adhesion layer as a nonconductor. When a barrier or adhesion layer is designed to conduct less than 10 percent of the total current, this layer shall be considered as only a barrier or adhesion layer. Consequently, this barrier or adhesion barrier layer shall not be used in current density calculations and shall not be required to satisfy the step coverage requirements. The barrier or adhesion layer shall be required to cover only these regions where the barrier function is designed with the manufacturer providing suitable verification of this function. The thickness of the barrier or adhesion layer shall not be permitted to be added to the thickness of the principal conducting layer when estimating the percentage metallization step coverage. Therefore, the principal conducting layer shall satisfy the percentage step coverage by itself.

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3.7.3.2 General metallization. The criteria of 3.7.2 shall apply here only for the principal conducting metal layer. Other metal layers (nonprincipal conducting layers such as barrier or adhesion layers) may be examined with the SEM, or with an optical microscope, the choice of equipment being at the manufacturer's option. Two specific cases of general metallization are considered. In the examination of other metal layers for the specific case of interconnection stripes (i.e., exclusive of contact window area), a defect consuming 100 percent of the cross-sectional area of the strip shall be acceptable provided the length of that defect is not greater than the width of the metallization strip (see figure 2077-20). For the specific case of contact window area metallization, at least 70 percent of the contact window area must be covered by the principal metal layer and any underlying metal layer(s). For the metal layer(s) above the principal conducting layer in the contact window area, a defect consuming 100 percent of the cross-sectional area of the metallization strip shall be acceptable provided the length of that defect is not greater than the width of the stripe. In the examination of the specific case of contact window area metallization for multi-metal systems, at least one of each type of contact window present shall be examined.

3.8 Specimen documentation requirements. After examination of dice from each wafer, a minimum of three photographs for each lot shall be taken and retained. Two photographs shall be of worst case oxide steps and the third photograph of worst case general metallization. If any photograph shows another apparent defect within the field of view, another photograph shall be taken to certify the extent of that apparent defect (see table 2077-II).

3.8.1 Required information. The following information shall be traceable to each photograph:

a. Manufacturer's lot identification number.

b. SEM operator/inspector's identification.

c. Date of SEM photograph.

d. Manufacturer.

e. Device/circuit identification (type or PIN).

f. Area of photographic documentation.

g. Magnification.

h. Electron beam accelerating voltage.

i. Viewing angle.

3.9 Control of samples. SEM samples shall not be shipped in any manner as functional devices.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. Single slice acceptance basis when required by the acquiring activity.

b. Requirements for photographic documentation (number and kind) if other than as specified in 3.8.

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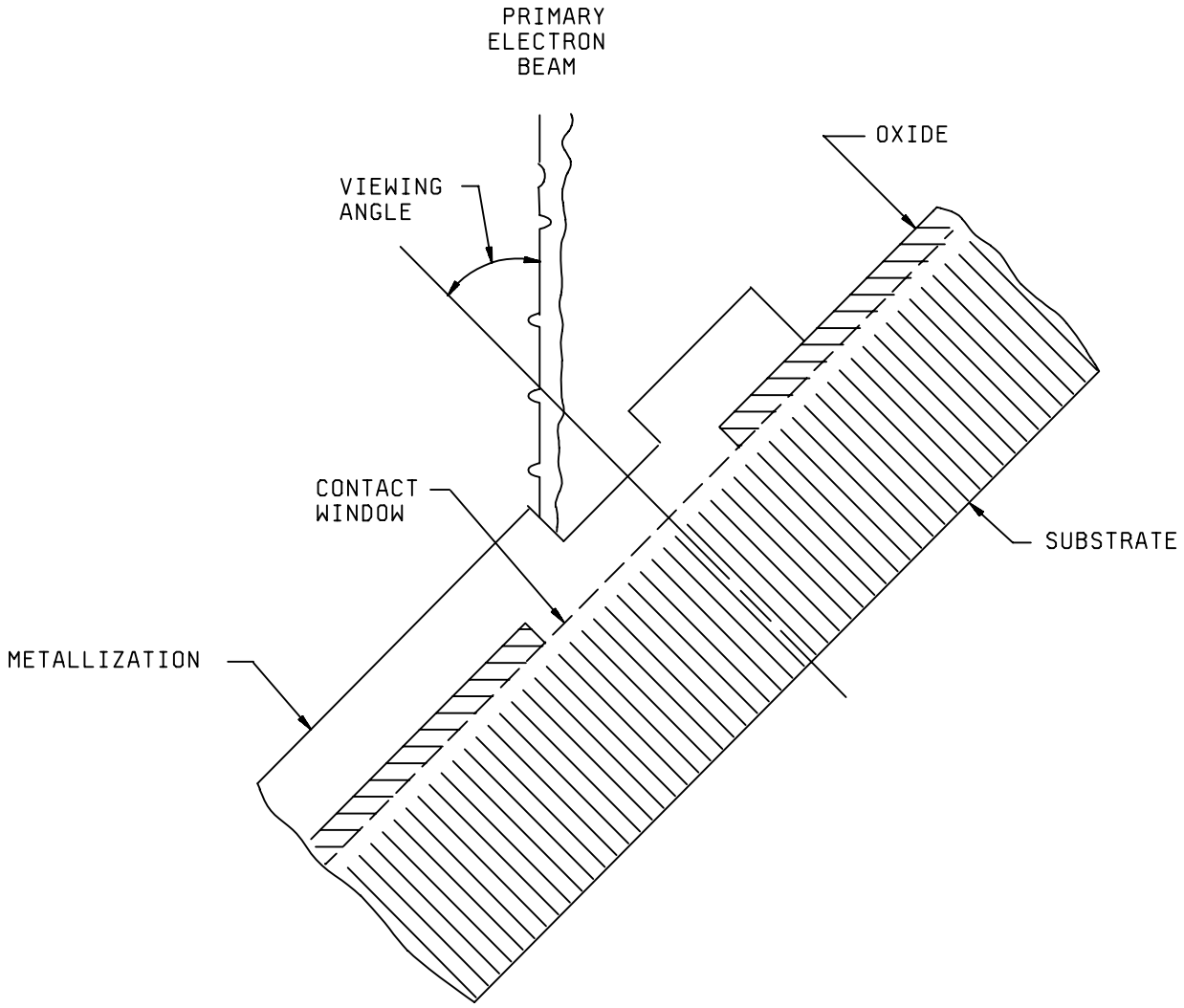

FIGURE 2077-1. Viewing angle.

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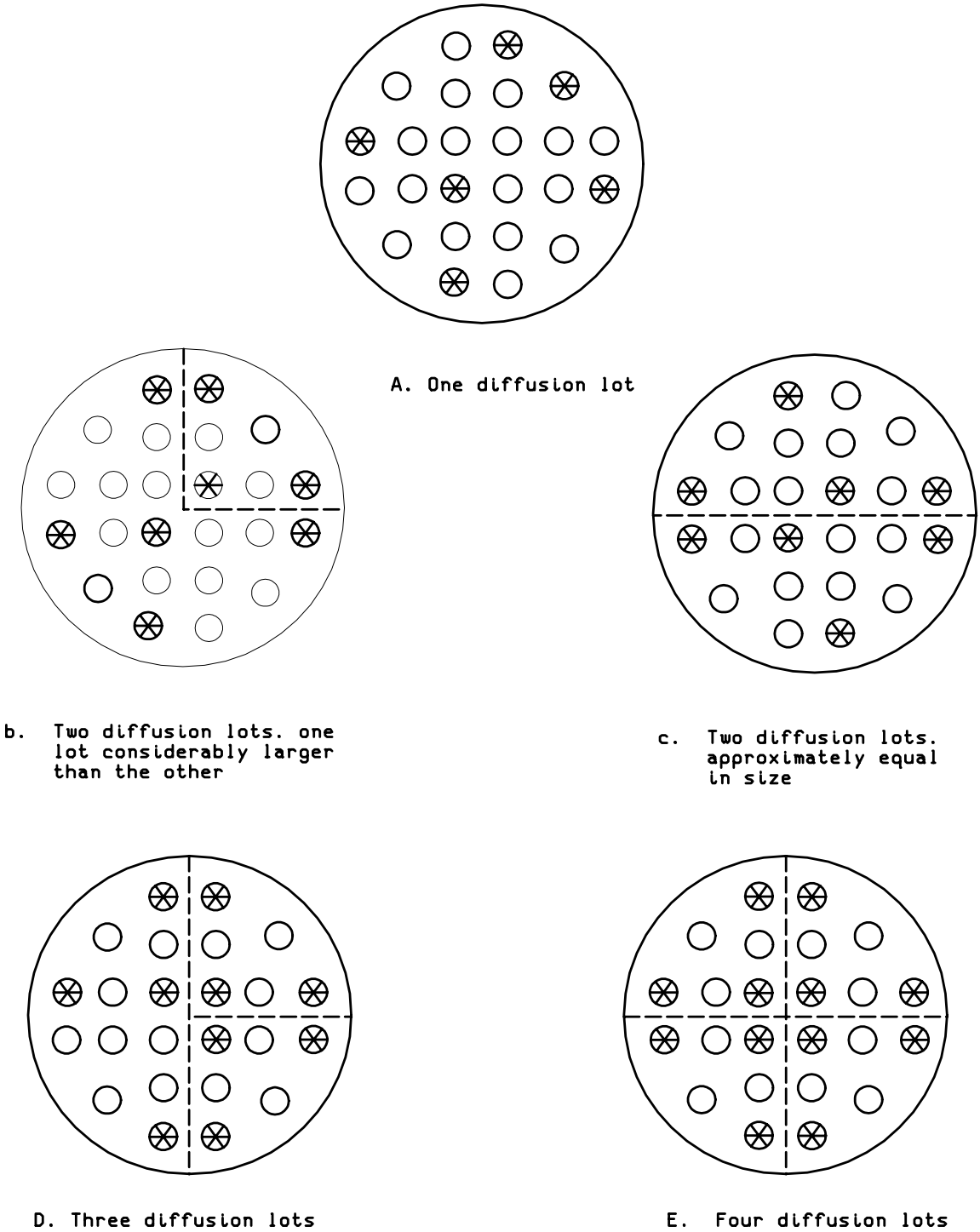

FIGURE 2077-2. Wafer sampling procedures (refer to table 2077-II).

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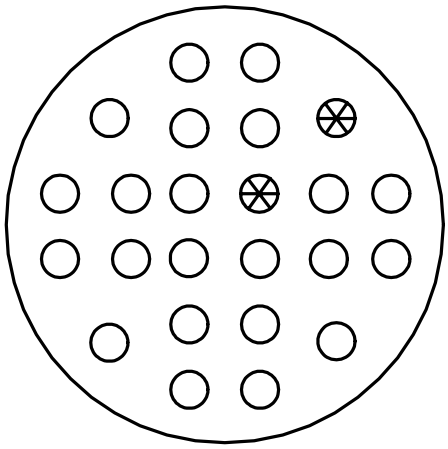
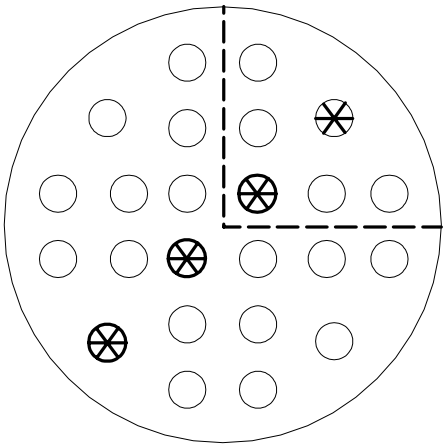
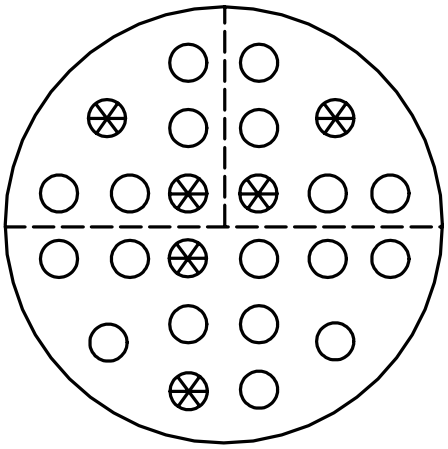


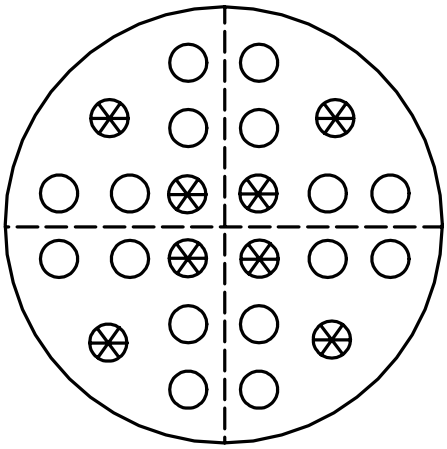
One diffusion lot



Two diffusion lots



Three diffusion lots



Four diffusion lots

f. Rotating and planetary systems.

FIGURE 2077-2. Wafer sampling procedures (refer to table 2077-II) - Continued.

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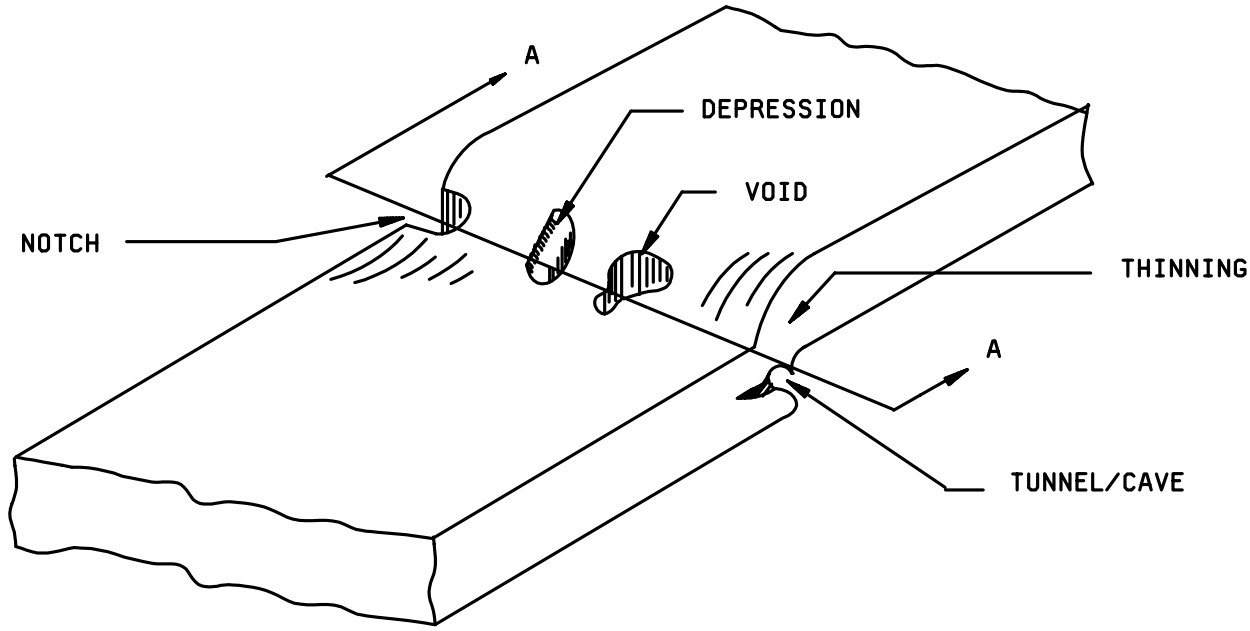
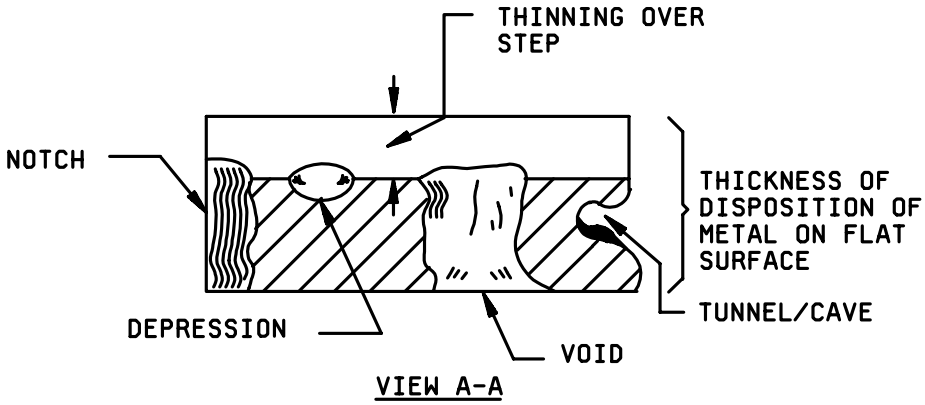


METALLIZATION AT OXIDE
STEP SHOWING TYPICAL DEFECTS



CROSS-SECTION AREA (ENLARGED) OF METALLIZATION
AT OXIDE STEP SHOWN ABOVE

FIGURE 2077-3. Concept of reduction of cross-sectional area of metallization as accept/reject criteria (any combination of defects and thinning over a step which reduces the cross-sectional area of the metal to less than 50 percent of metal cross-sectional area as deposited on the flat surface, is cause for rejection).

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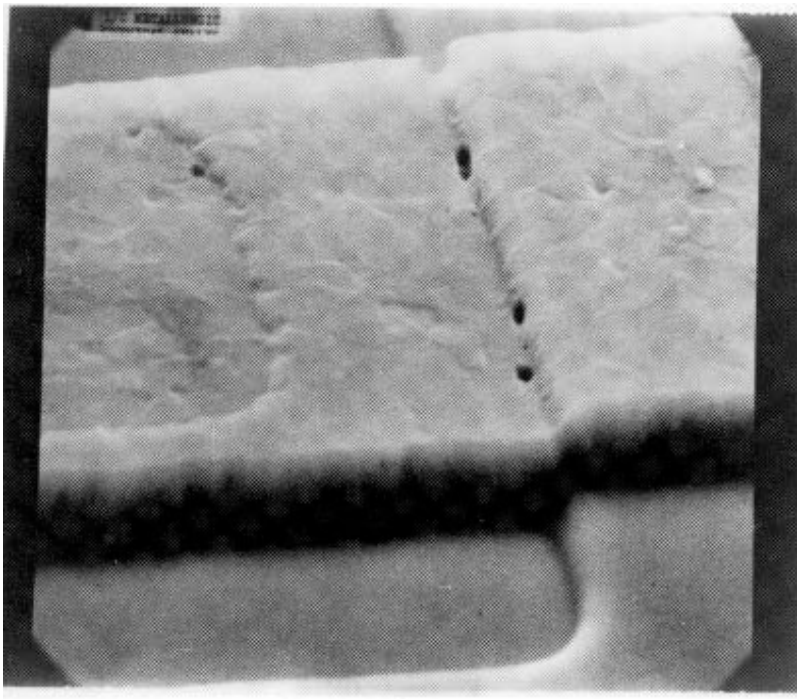

FIGURE 2077-4. (3,400X)Void near oxide step (accept).

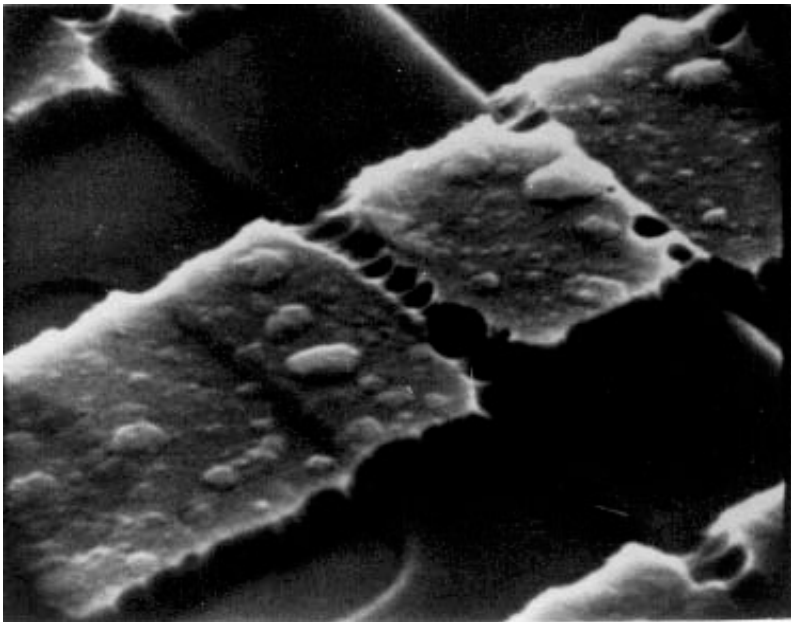

FIGURE 2077-5. (3,300X) Voids at oxide step (reject).

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NOTE: Tunnel does not reduce cross-sectional area more than 50 percent.

FIGURE 2077-6. (10,000X) Tunnel/cave at oxide step (accept).

FIGURE 2077-7. (5,000X)Tunnel/cave at oxide step (reject).

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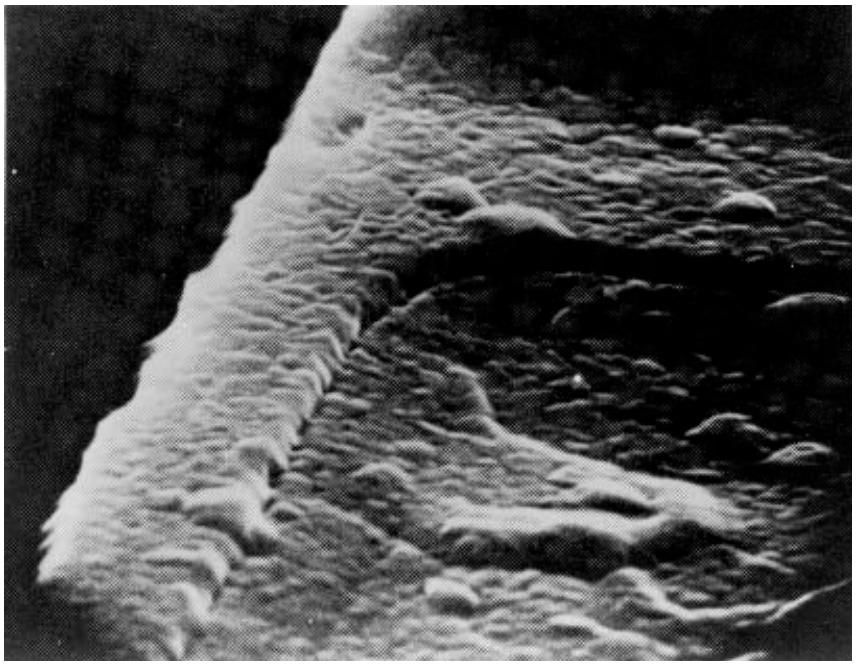

FIGURE 2077-8. (10,000X) Separation of metallization at oxide step (base contact) (accept).

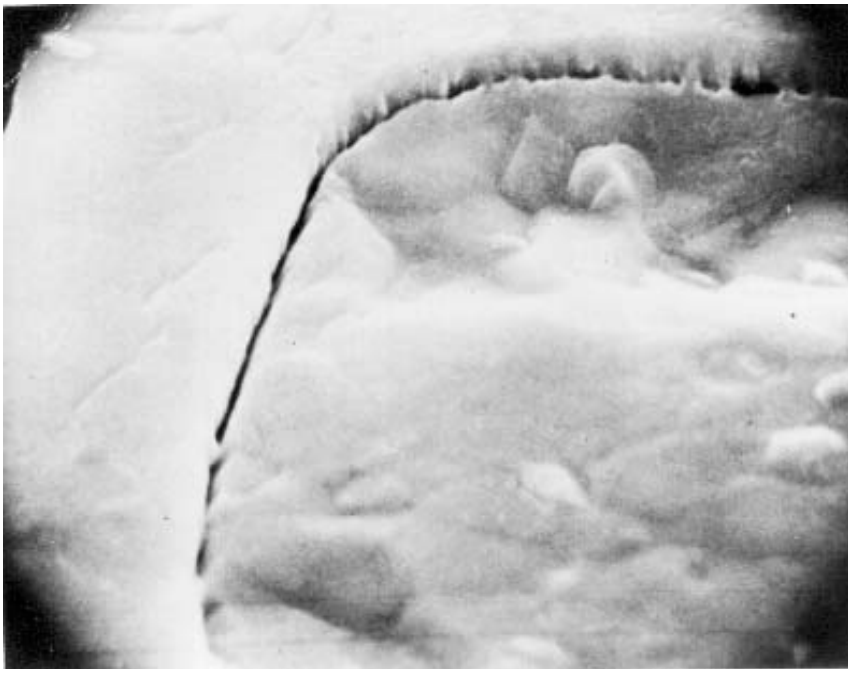

FIGURE 2077-9. (7,000X) Separation of metallization at contact step (reject).

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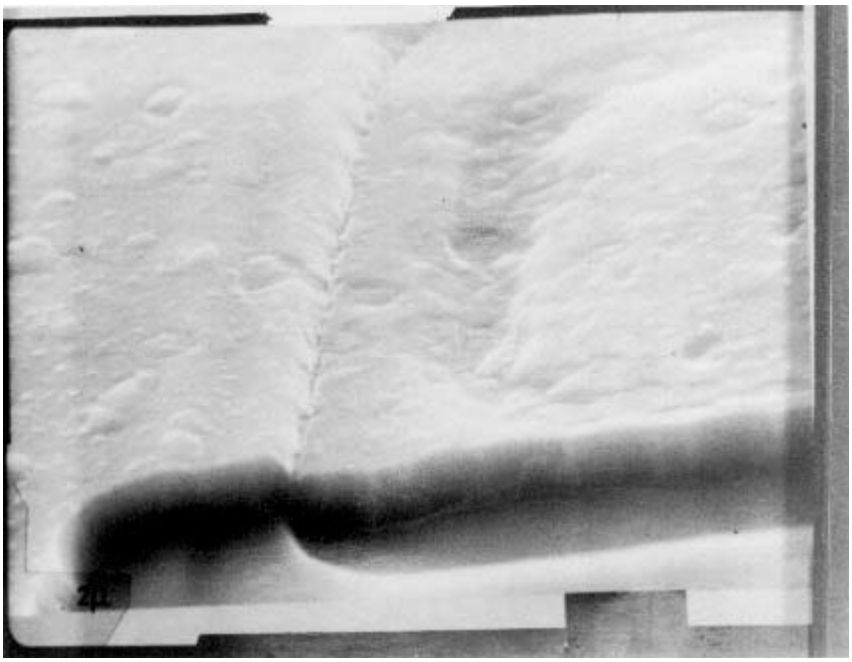

FIGURE 2077-10. (20,000X) Crack-like defect at oxide step (accept).

FIGURE 2077-11. (7,000X) Crack-like defect at oxide step (reject).

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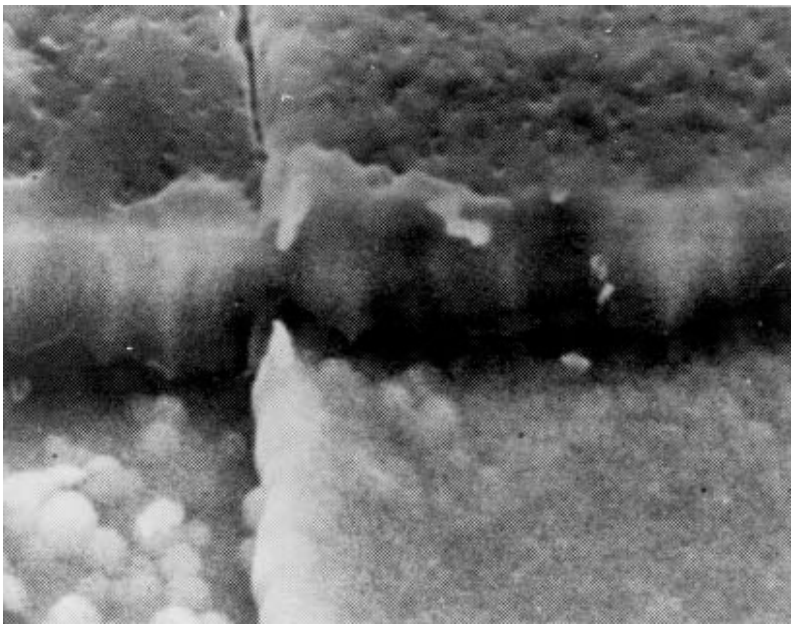

FIGURE 2077-12. (7,200X) Thinning at oxide step with more than 50 percent of cross-sectional area remaining at step (multi-level-metal) (accept).

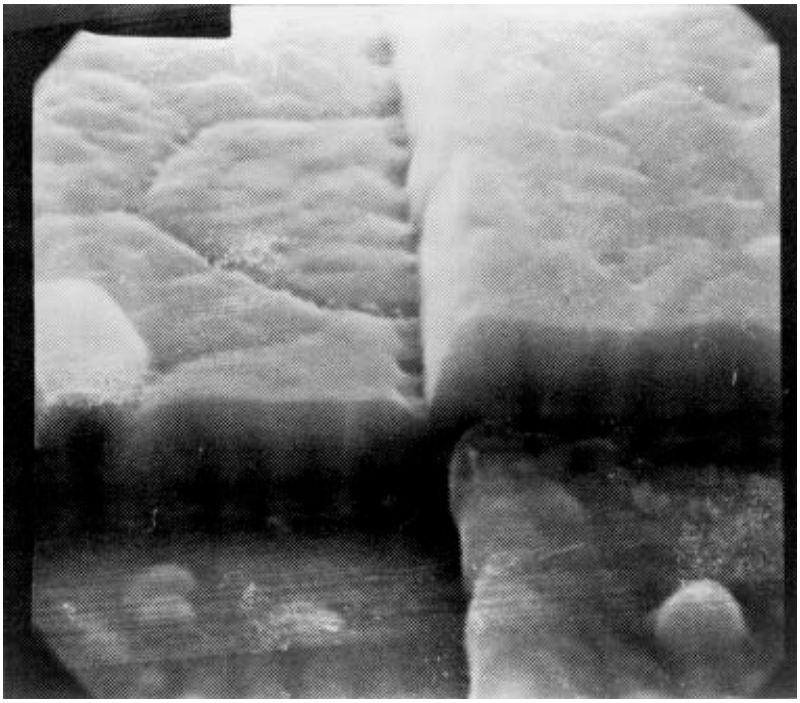

FIGURE 2077-13 (7,200X) Thinning at oxide step with less than 50 percent of cross-sectional area remaining at step (multi-level-metal) (reject).

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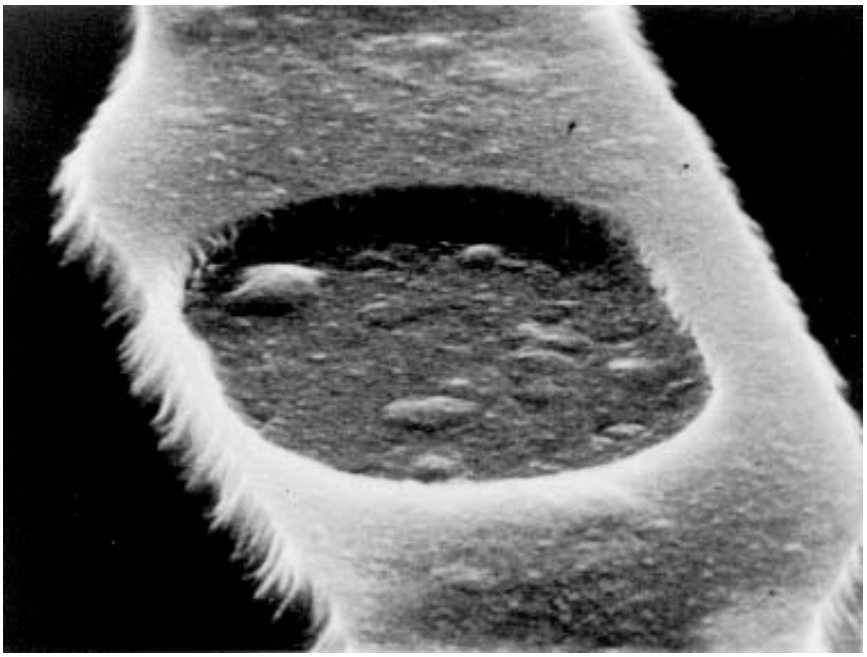

FIGURE 2077-14. (6,000X) Steep oxide step (MOS) (accept).

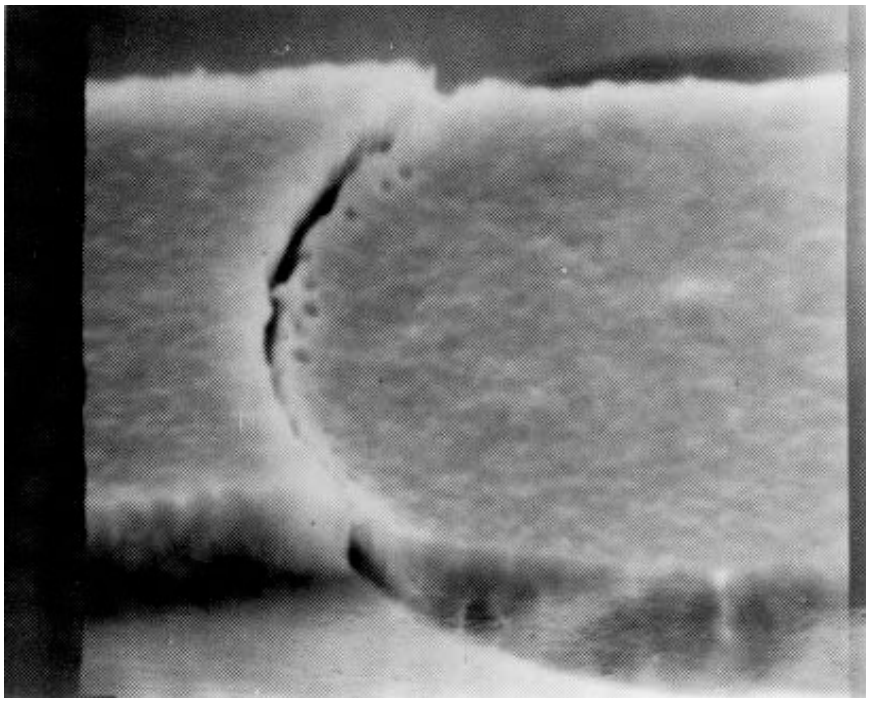

FIGURE 2077-15. (9,500X) Steep oxide step (MOS) (reject).

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FIGURE 2077-16. (5,000X) Peeling or lifting of general metallization in contact window area (reject).

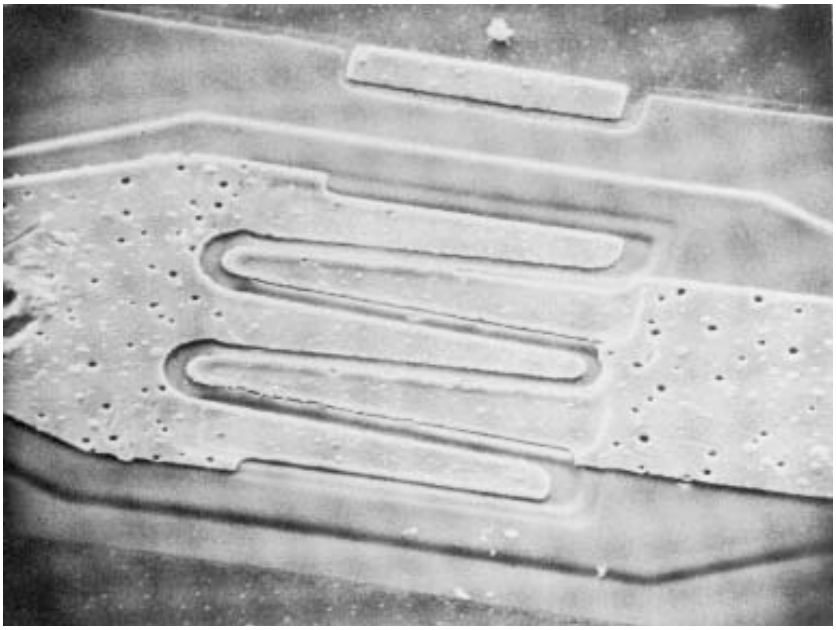

FIGURE 2077-17. (10,000X) General metallization voids (accept).

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FIGURE 2077-18. (5,000X) General metallization voids (reject).

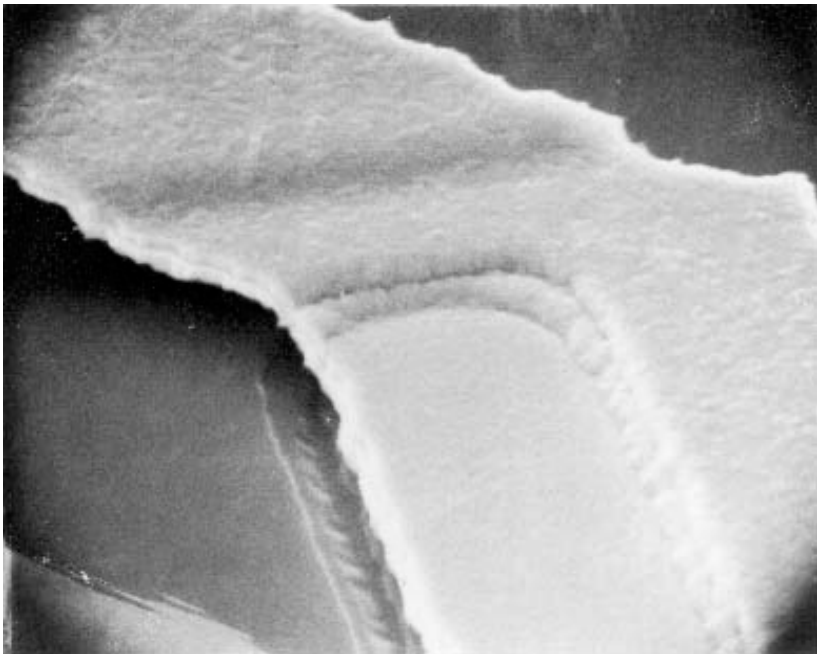

FIGURE 2077-19. (5,000X) Etch-back/undercut type of notch at oxide step (multi-layered-metal) (accept).

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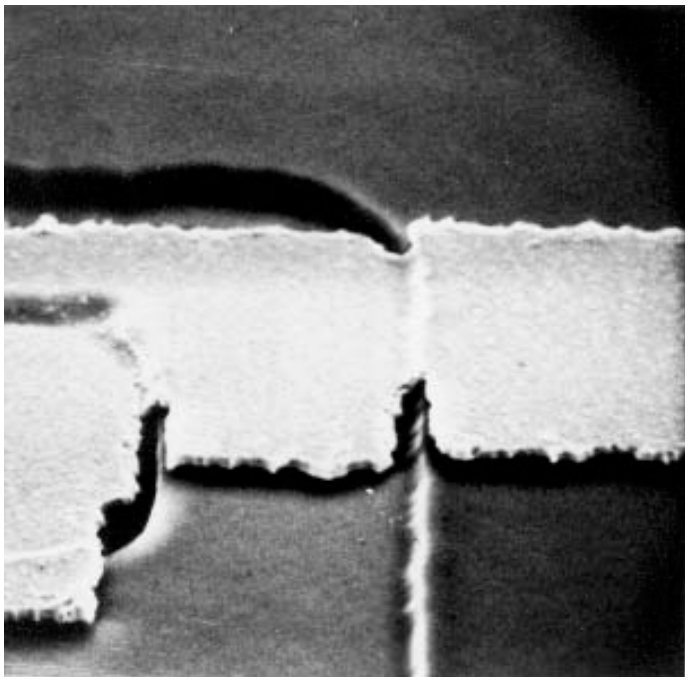

FIGURE 2077-20. (5,000X) Barrier or adhesion layer etch-back/undercut type of notch at oxide step (multi-layered-metal) (accept).

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METHOD 2078

INTERNAL VISUAL FOR WIRE BONDED DIODES/RECTIFIERS

1. Purpose. The purpose of this inspection is to verify the construction and workmanship of devices utilizing junction passivated diode and rectifiers chips that use wire to chip technology. This test will be performed prior to capping or encapsulation.

2. Apparatus. The apparatus for this inspection shall consist of the following:

a. Optical equipment capable of the specified magnifications.

b. Light sources of sufficient intensity to adequately illuminate the devices being inspected.

c. Adequate fixturing for handling the devices being inspected without causing damage.

d. Adequate covered storage and transportation containers to protect devices from mechanical damage and environmental contamination.

e. Any visual standards (drawings and photographs) necessary to enable the inspector to make objective decisions as to the acceptability of the devices being examined.

3. Definitions.

3.1 Glassivation. The top layer of transparent insulating material that covers the active circuit area metallization, but excludes the bond pads.

3.2 Passivation. Silicon oxide, nitride, or other insulating material that is grown or deposited directly on the die prior to the deposition of any metal.

4. Procedure.

4.1 General. The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the requirements of this test method. It is optional that the chips used have passed Mil-STD-750 Method 2073 prior to assembly.

a. Inspection control. Within the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment (one which controls airborne particle count and relative humidity). The use of an inert gas environment, such as dry nitrogen shall satisfy the requirements for storing in a controlled environment. Devices examined in accordance with this test method shall be inspected and stored in a class 100,000 environment, in accordance with FED-STD-209, except that the maximum allowable relative humidity shall not exceed 65 percent.

b. If devices are subjected to a high temperature bake (> 100°C) immediately prior to sealing, the humidity control is not required. Unless a cleaning operation is performed prior to sealing, devices shall be in covered containers when transferred from one controlled environment to another.

c. Magnification. High magnification inspection shall be performed perpendicular to the die surface with normal incident illumination. Low magnification inspection shall be performed with either a monocular, binocular, or stereo microscope, and the inspection performed within any appropriate angle, with the device under suitable illumination. The inspection criteria of 4.1.4 and 4.1.6.1 may be examined at "high magnification" at the manufacturer's option. High power magnification may be used to verify a discrepancy noted at a low power.

Chip size 1/	High magnification	Low magnification
30 mils or less	100X to 200X	30X to 50X
31 to 60 mils	75X to 150X	30X to 50X
61 to 150 mils	35X to 120X	10X to 30X
Greater than 150 mils	25X to 75X	10X to 30X

1/ Length of shortest dimension.

TABLE 2078. Die magnification requirements.

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4.1.1 Die metallization defects (high magnification). A die which exhibits any of the following defects shall be rejected.

4.1.1.1 Metallization scratches, islands and voids exposing underlying material (see figure 2078-1 and 207-2).

a. A scratch or smear that extrudes metal such that it extends over the next geometric boundary such as guard rings.

b. Any die containing a void in the metallization at the bonding pad covering more than 25 percent of the pad area.

c. Any scratch or void which isolates more than 25 percent of the total metallization of an active region from the bonding pad.

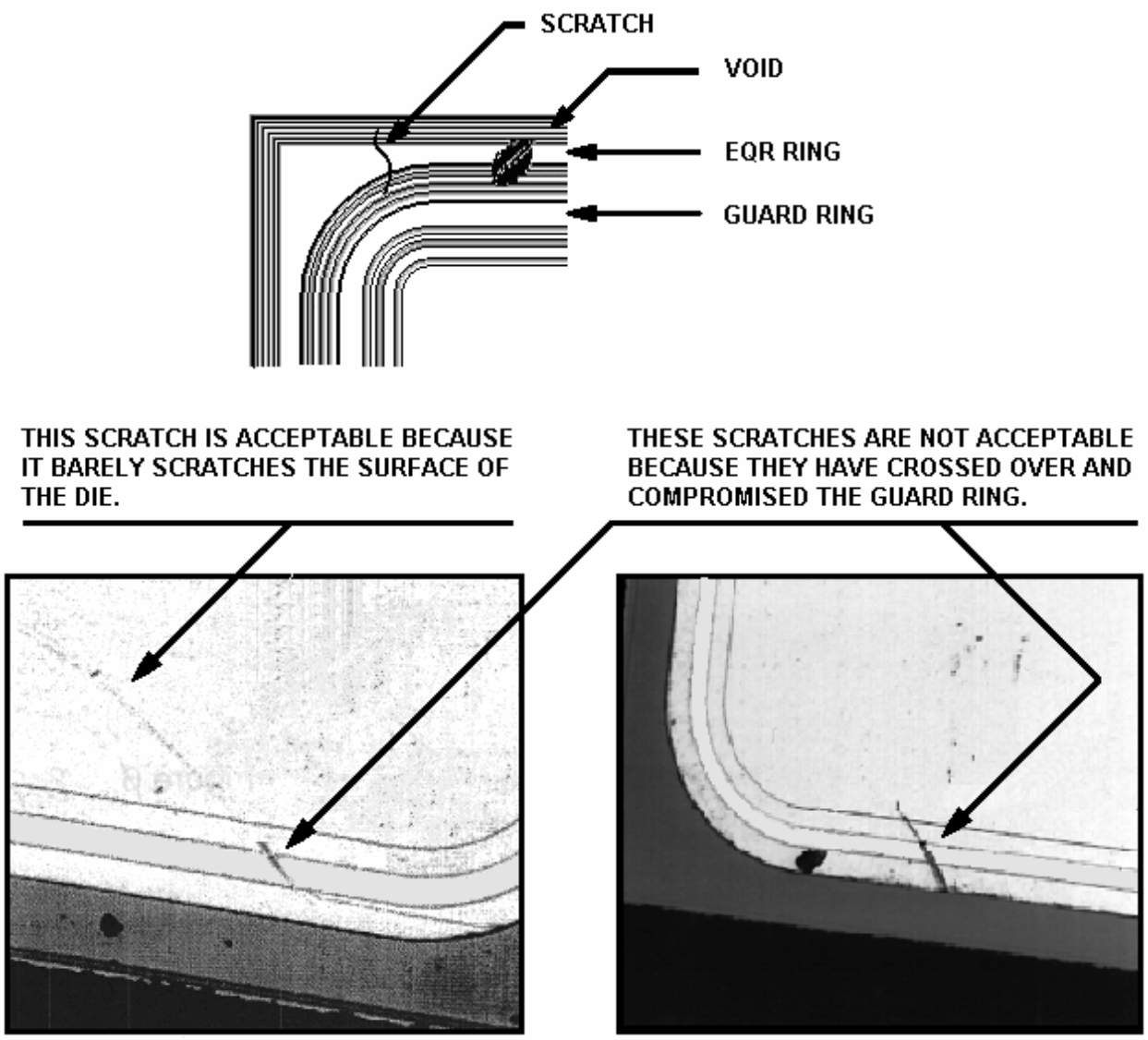

FIGURE 2078-1. Metallization scratches and voids.

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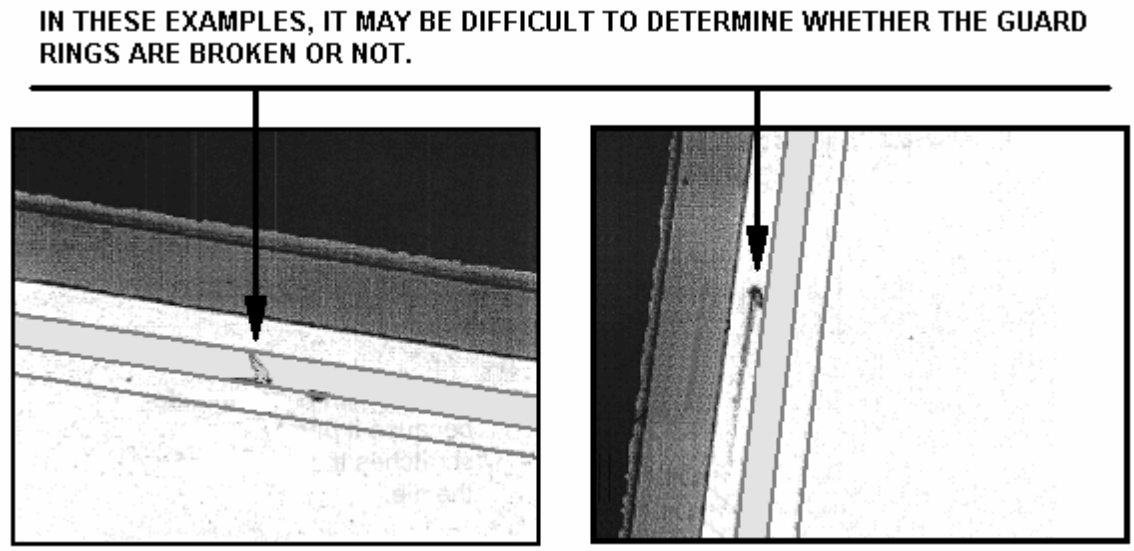

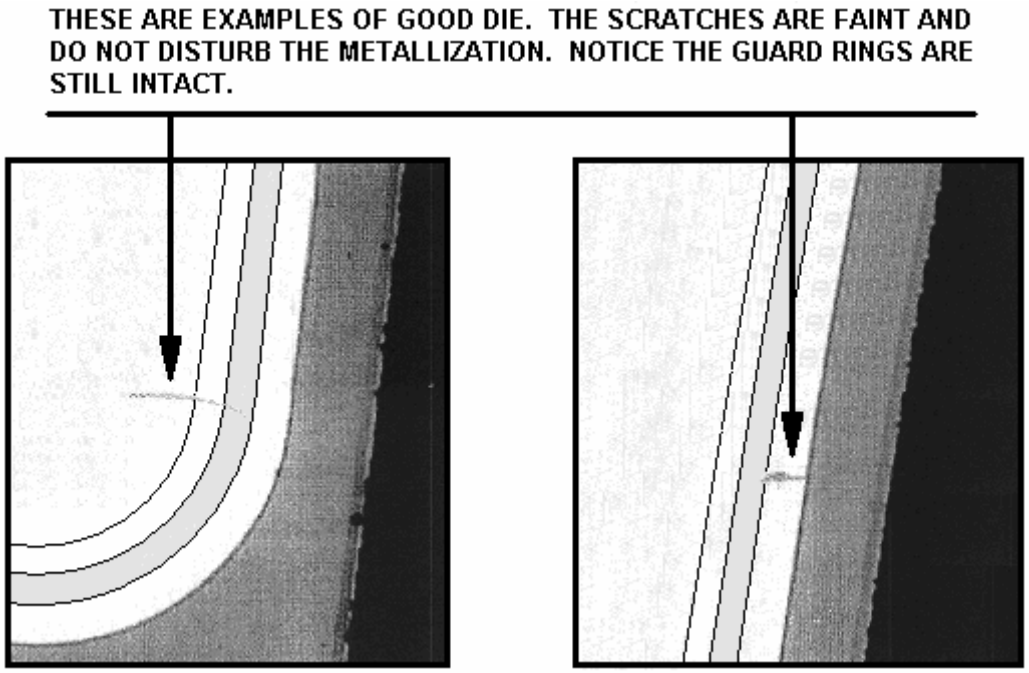

FIGURE 2078-2. Metallization scratches and voids (continued)

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4.1.1.2 Metallization corrosion. Any metallization which shows evidence of corrosion.

4.1.1.3 Metallization adherence. Any metallization which has lifted, peeled, or blistered.

4.1.1.4 Metallization probing. Criteria contained in 4.1.1.1 shall apply as limitations on probing damage.

4.1.1.5 .Metallization alignment.

a. Except by design, contact window that has less than 75 percent of its area covered by continuous metallization.

b. On metal overlay devices, any misalignment causing the metal to be extended to more than 50% of the way to the next geometric boundary.

4.1.2 Passivation and diffusion faults (high magnification). A device which exhibits any of the following defects (see figure 2078-3) shall be rejected:

a. Any diffusion fault that allows bridging between any two diffused areas including field rings and guard rings or any two metallization strips.

b. Any passivation fault including pinholes not covered by glassivation that exposes semiconductor material and allows bridging between any two diffused areas, any two metallization strips, or any such combination not intended by design.

c. Unless intended by design, a diffusion area which is discontinuous.

d. On metal overlay devices, an absence of passivation visible at the edge and continuing under the metallization causing an apparent short between the metal and the underlying material (closely spaced double or triple lines on the edges of the defect indicate that it may have sufficient depth to penetrate down to the silicon).

e. Except by design, any active junction not covered by passivation or glassivation.

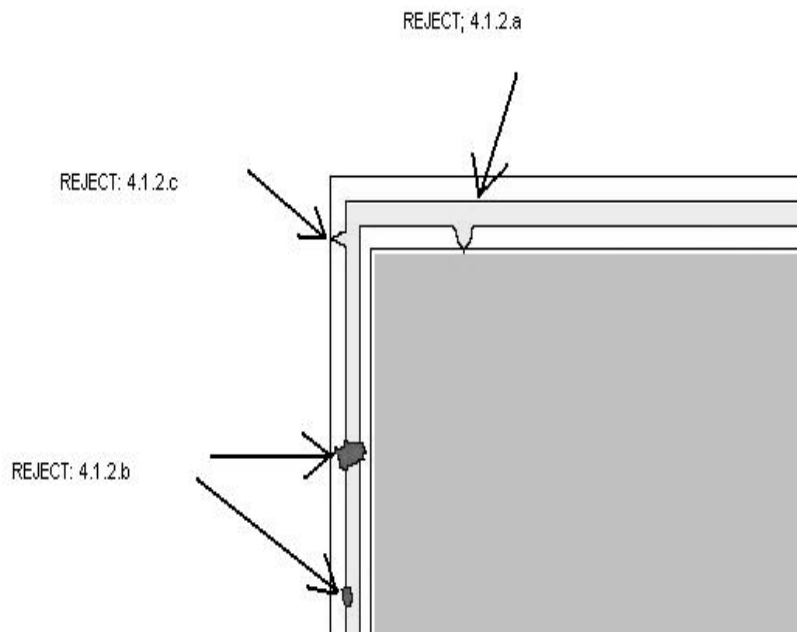

FIGURE 2078-3. Passivation and diffusion faults.

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4.1.3 Sawing and die defects (high magnification). A device which exhibits any of the following defects (see figure 2078-4 and 2078-5) shall be rejected:

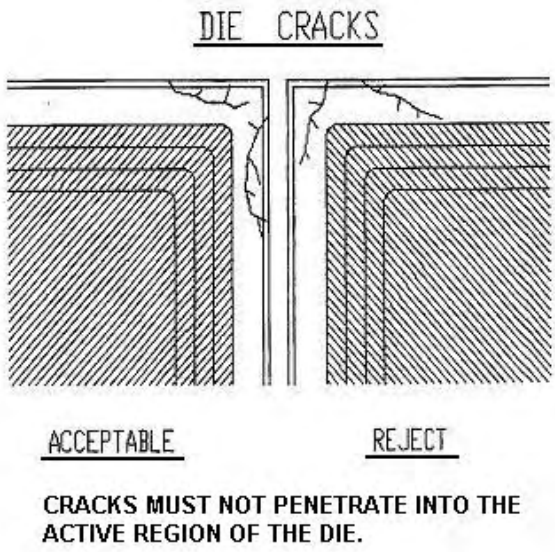
a. Unless by design, less than 0.1 mil passivation visible between active metallization or bond pad periphery and the edge of the die.

b. Any chip-out or crack extending to within 1 mil of a diffusion boundary.

c. Die having attached portions of the active area of another die.

d. Any crack which exceeds 2.0 mils in length inside the scribe grid or scribe line that points toward active metallization or active area and extends into the oxide area.

e. Any crack or chip-out that extends to any active metallization area.



g. Any chip-out which extends to a guard ring.

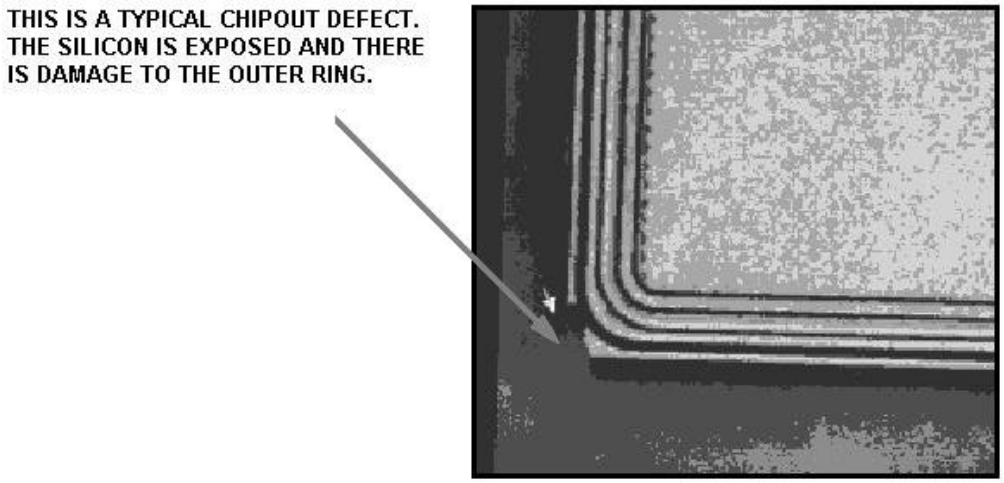


FIGURE 2078-4. Cracks and chips.

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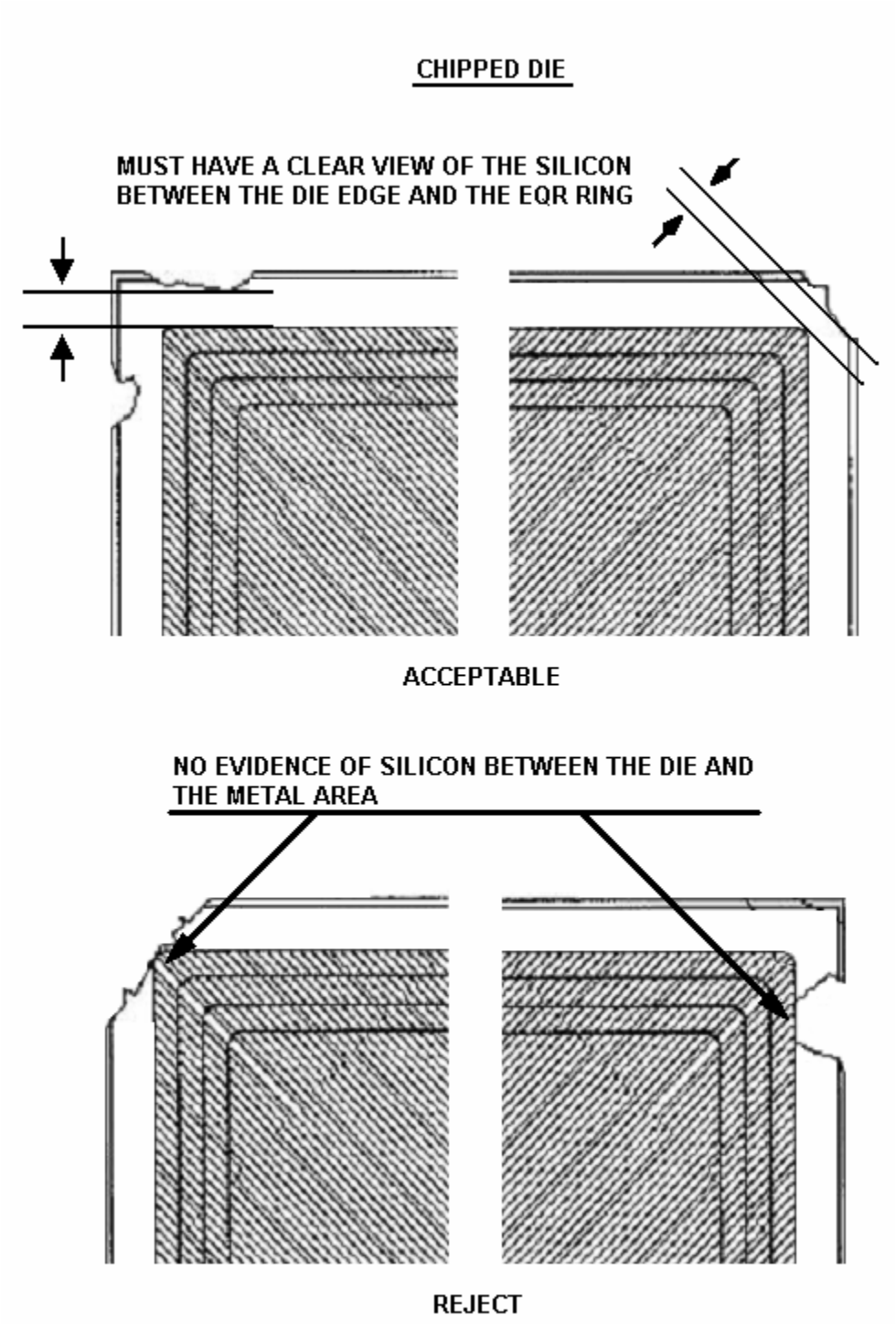

FIGURE 2078-5. Cracks and chips (continued).

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4.1.4 Bond inspection (low magnification). This inspection and criteria shall be the required inspection for the bond type(s) and location(s) to which they are applicable when viewed from above (see figures 2078-6 and 2078-7). Wire tail is not considered part of the bond when determining physical bond dimensions. A device, which exhibits any of the following defects, shall be rejected.

4.1.4.1 Gold ball bonds.

a. Gold ball bonds on the die or package post where the ball bond diameter is less than 2.0 times or greater than 5.0 times the wire diameter.

b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.

c. Gold ball bonds where the exiting wire is not within the boundaries of the bonding pad.

d. Any visible intermetallic formation at the periphery of any gold ball bond.

4.1.4.2 Wedge bonds.

a. Ultrasonic wedge bonds on the die or package post that are less than 1.2times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 5.0 times the wire diameter in length.

b. Thermo compression wedge bonds on the die or package post that are less than 1.2 times or greater than 3.0 times the wire diameter in width or are less than 1.5 or greater than 5.0 times the wire diameter in length.

4.1.4.2.1 Stitch Wire Bonds, usually done with a wedge bonder, is where a single bond wire has 2 or more bonds along its length to the chip. These can be evaluated using the criteria for single wedge bonds with the following guidelines:

1) Multiple stitch bonds on a common bonding pad:
   a. The bond closest to the wire end should meet all the criteria of a single bond except there is no cutoff tail requirement.

   b. The bond farthest from the wire end must meet the cutoff tail requirement.

   c. Wire rise clearance criteria between bonds is waived.

   d. Shape and deformation criteria of each bond is the same as for a single bond.

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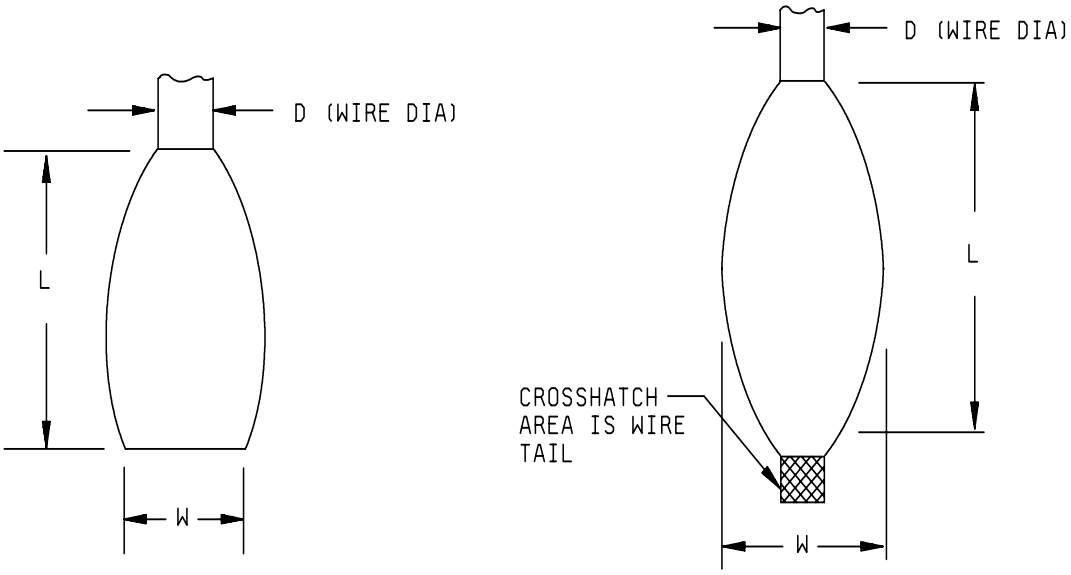


B. Wedge.

Ultrasonic

NOTES:

1. 1.2 D ≤ W ≤ 3.0 D (width).
2. 1.5 D ≤ L ≤ 5.0 D (length)

Thermo compression

NOTES:

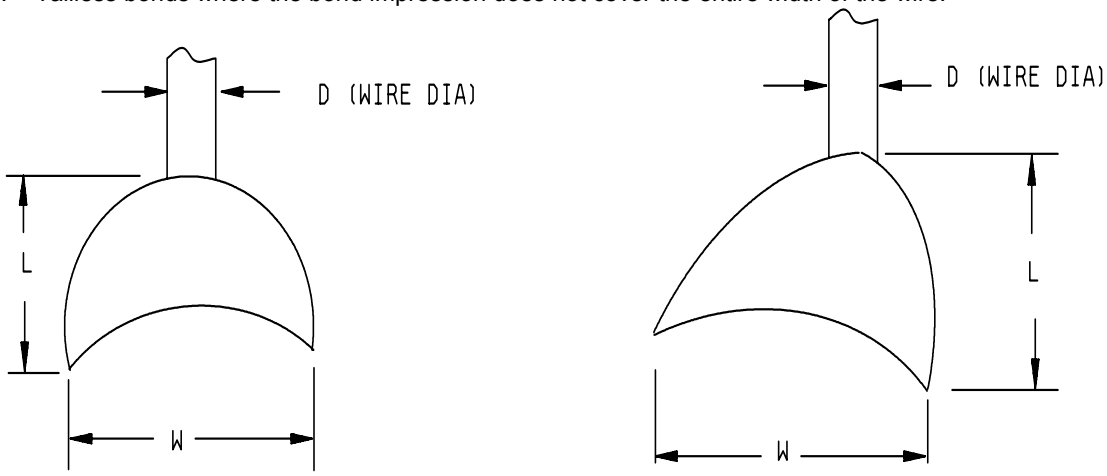
1. 1.2 D ≤ W ≤ 3.0 D (width).
2. 1.5 D ≤ L ≤ 5.0 D (length).

FIGURE 2078-6. Bond dimensions.

4.1.4.3 Tailless bonds (crescent).

a. Tailless bonds on the die or package post that are less than 1.2 times or greater than 5.0 times the wire diameter in width, or are less than 0.5 times or greater than 3.0 times the wire diameter in length.

b. Tailless bonds where the bond impression does not cover the entire width of the wire.



A. Tailless or crescent.

NOTES:

1. 1.2.D ≤ W ≤ 5.0 D (width).
2. 0.5 D ≤ L ≤ 3.0 D (length).

FIGURE 2078-7. Bond dimensions (continued).

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4.1.4.4 General (gold ball, wedge, and tailless). As viewed from above, a device which exhibits any of the following defects shall be rejected:

a. Bonds on the die where less than 75 percent of the bond is within the unglassivated bonding pad area (except where due to geometry, the bonding pad is smaller than the bond, the criteria shall be 50 percent).

b. Wire bond tails that extend over and make contact with any metallization not covered by glassivation and not connected to the wire.

c. Wire bond tails (pigtails) that exceed two wire diameters in length at the bonding pad or four wire diameters in length at the package post (see figure 2078-8).

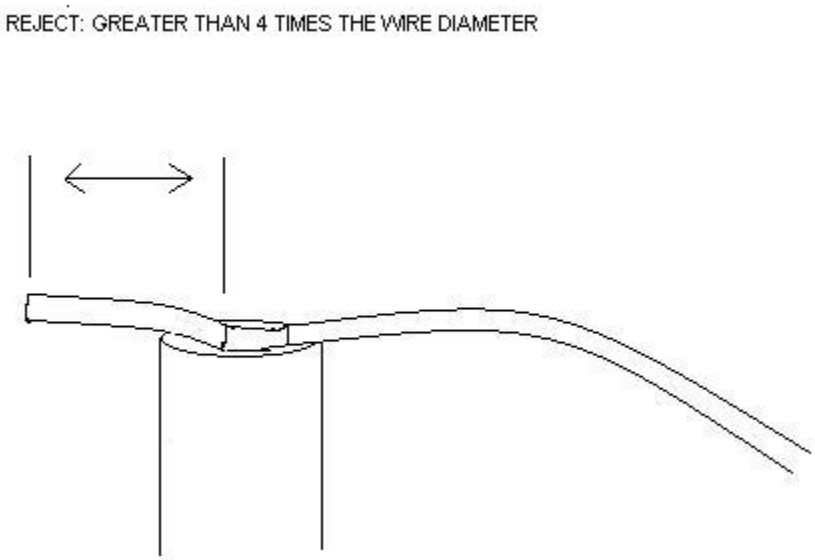

FIGURE 2078-8 PIGTAIL LENGTH

d. Bonds on the package posts that are not bonded entirely on the flat surface of the post top.

e. A bond on top of another bond.

f. Bonds placed so that the separation between bonds and adjacent glassivated die metallization is less than 0.25 mil or the separation between adjacent bonds is less than 0.25 mil. This criteria does not apply to designs which employ multiple bond wires in place of a single wire.

i. Bonds located where any of the bond is placed on an area containing die preform mounting material.

j. For aluminum wires over 2.0 mils diameter, the bond width shall not be less than 1.0 times the wire diameter.

4.1.5 Internal lead wires (low magnification). This inspection and criteria shall be required inspection for the location(s) to which they are applicable when viewed from above. A device which exhibits any of the following defects shall be rejected:

a. Any wire that comes closer than two wire diameters or 5 mils, whichever is less, to unglassivated operating metallization, another wire (common wires and pigtails excluded) package post, unpassivated die area, or any portion of the package, including the plane of the lid to be attached. (Within a 5.0 mil spherical radial distance from the perimeter of the bond on the die surface, the separation can be 1.0 mil.)

b. Nicks, tears, bonds, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent. See figure 2078-9.

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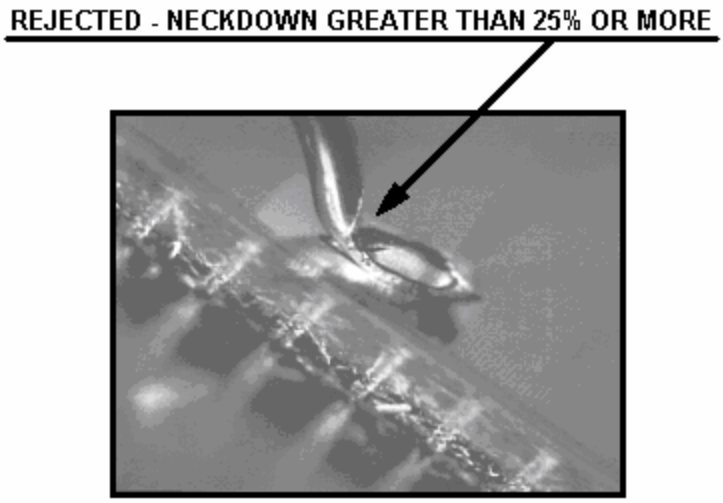

FIGURE 2078-9.

c. Missing or extra lead wires.

d. Bond lifting or tearing at interface of pad and wire.

e. Any wire which runs from die bonding pad to package post and has no arc or stress relief (See figure 2078-10).

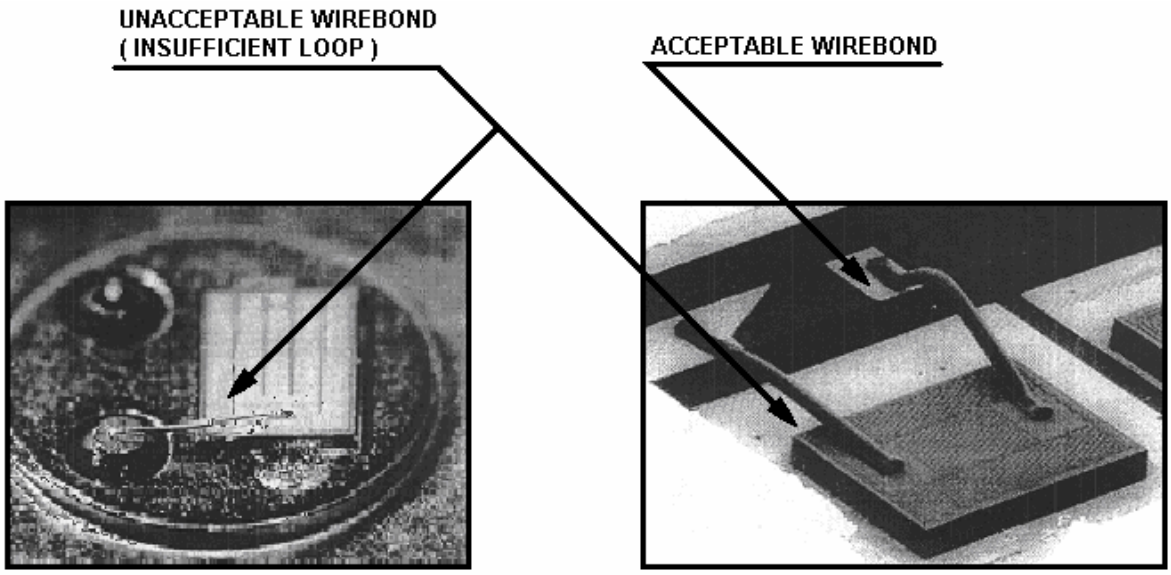

FIGURE 2078-10

f. Except in common connectors, wires which cross other wires.

g Wire(s) not in accordance with bonding diagram. (See figure 11)

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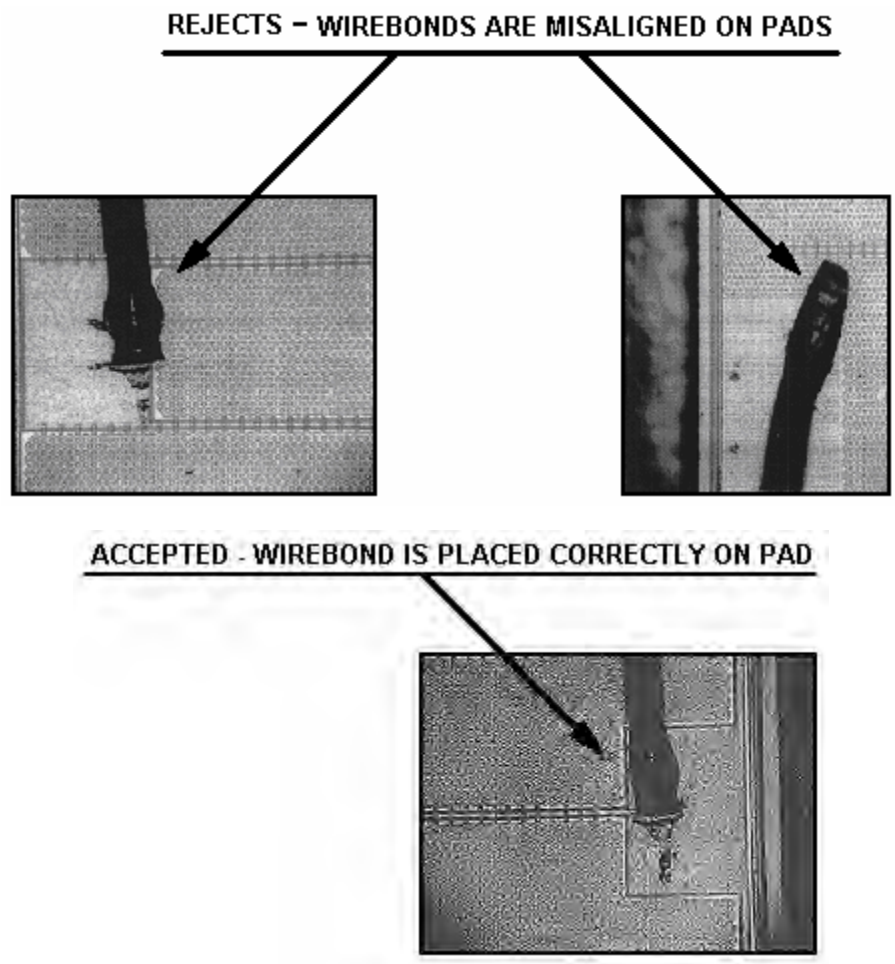

FIGURE 2078-11

h. Wire is kinked (unintended sharp bend) with an interior angle of less than 90° or twisted to an extent that stress marks appear.

i. Wire (ball bonded devices) not within 10° of the perpendicular to the surface of the chip for a distance of greater than 0.5 mil before bending toward the package post or other termination point.

f. Excessive lead burn at lead post weld.

k. Pigtail longer than 4 times the wire diameter. (See figure 8)

l. A bow or loop between double bonds at post greater than four times wire diameter.

m. Excessive loops, bows, or sags in any wire such that it could short to another wire, to another pad, to another package post, to the die or touch any portion of the package.

n. When clips are used, solder fillets shall encompass at least 50 percent of the clip-to-die and post-to-clip periphery. There shall be no deformation or plating defects on the clip.

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4.1.6 Package conditions (magnification as indicated). A device which exhibits any of the following defects shall be rejected.

4.1.6.1 Conductive foreign material on die surface. All foreign material or particles may be blown off with a nominal gas blow (approximately 20 psi (138 kPa)) or removed with a soft camel hairbrush. The device shall then be inspected for the following reject criteria (low magnification):

a. Loosely attached foreign particles (conductive particles which are attached by less than one-half of their largest dimension), which are present on the surface of the die that are large enough to bridge the narrowest unglassivated metal spacing (silicon chips shall be included as conductive particles).

b. Embedded foreign particles on the die that bridge two or more metallization paths or semiconductor junctions, or any combination of metallization or junction.

c. Liquid droplets, chemical stains, or photoresist on the die surface that bridge any combinations of unglassivated metal or bare silicon areas.

d. Ink on the surface of the die that covers more than 25 percent of a bonding pad area or that bridges any combination of unglassivated metallization or bare silicon areas.

4.1.6.2 Die mounting (low magnification).

a. Die mounting material buildup that extends onto the top surface of the die or extends vertically above the top surface of the die and interferes with bonding.

b. Die to header mounting material which is not visible around at least three complete sides or 75 percent of the die perimeter. Wetting criteria is not required if the devices pass an approved electrical die attach evaluation test.

c. Any flaking of the die mounting material.

d. Any balling of the die mounting material which does not exhibit a fillet when viewed from above.

4.1.6.3 Die orientation.

a. Die is not located or orientated in accordance with the applicable assembly drawing of the device.

b. Die is visibly tipped or tilted (more than 10°) with respect to the die attach surface.

4.1.6.4 Internal package defects (low magnification inspection) (applicable to headers, bases, caps, and lids).

a. Any header or post plating which is blistered, flaked, cracked, or any combination thereof.

b. Any conductive particle which is attached by less than one-half of the longest dimension.

c. A bubble or a series of interconnecting bubbles in the glass surrounding the pins which are more than one-half the distance between the pin and body or pin-to-pin.

d. Header posts which are severely bent.

e. Any glass, die, or other material greater than 1.0 mil in its major dimension which adheres to the flange or side of the header and would impair sealing.

f. Any stain, varnish, or header discoloration which appears to extend under a die bond or wire bond.

g. For isolated stud packages:

(1) Any defect or abnormality causing the designed isolating paths between the metal island to be reduced to less than 50 percent of the design separation.

(2) A crack or chip-out in the substrate.

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4.1.6.5 Presence of extraneous matter. Extraneous matter (foreign particles) shall include, but not be limited to:

a. Any foreign particle, loose or attached, greater than .003 inch (0.08 mm) or of any lesser size which is sufficient to bridge non-connected conducting elements of the device.

b. Any wire tail extending beyond its normal end by more than two diameters at the semiconductor die pad or by more than four wire diameters at the package post (see figure 2078-11).

c. Any burr on a post (header lead) greater than .003 inch (0.08 mm) in its major dimension or of such configuration that it may break away.

d. Excessive semiconductor die bonding material buildup (see figure 2078-12 and 2078-13). A semiconductor die shall be mounted and bonded so that it is not tilted more than 10° from mounting surface. The bonding agent that accumulates around the perimeter of the semiconductor die and touches the side of the semiconductor die shall not accumulate to a thickness greater than that of the semiconductor die. Where the bonding agent is built up but is not touching the semiconductor die, the build up shall not be greater than twice the thickness of the semiconductor die. There shall be no excess semiconductor die bonding material in contact with the active surface of the semiconductor die or any lead or post, or separated from the main bonding material area.

e. Flaking on the header or posts or anywhere inside the case.

f. Extraneous ball bonds anywhere inside case, except for attached bond residue when re-bonding is allowed.

4.1.7 Glassivation and silicon nitride defects (high magnification). No device shall be acceptable that exhibits any of the following defects:

a. Glass crazing that prohibits the detection of visual criteria contained herein.

b. Any glassivation which has delaminated. (Lifting or peeling of the glassivation may be excluded from the criteria above, when it does not extend more than 1.0 mil distance from the designed periphery of the glassivation, provided that the only exposure of metal is adjacent to bond pads or of metallization leading from those pads.)

c. Except by design, two or more adjacent active metallization paths which are not covered by glassivation.

d. Glassivation which covers more than 25 percent of the design bonding pad area.

4.2 Post organic protective coating visual inspection. If devices are to be coated with an organic or silicone protective coating, the devices shall be visually examined in accordance with the criteria specified in 4.1 prior to application of the coating. After the application and cure of the organic protective coating the devices shall be visually examined under a minimum of 10X
magnification. Devices, which exhibit any of the following defects, shall be rejected:

a. Except by design, any unglassivated or unpassivated areas or insulating substrate which has incomplete coverage.

b. Open bubbles, cracks or voids in the organic protective coating.

c. A bubble or a chain of bubbles which covers two adjacent metallized surfaces.

d. Organic protective coating, which has flaked or peeled.

e. Organic protective coating, which is tacky.

f. Conductive particles, which are embedded in the coating and are large enough to bridge the narrowest unglassivated active metal spacing (silicon chips shall be included as conductive particles).

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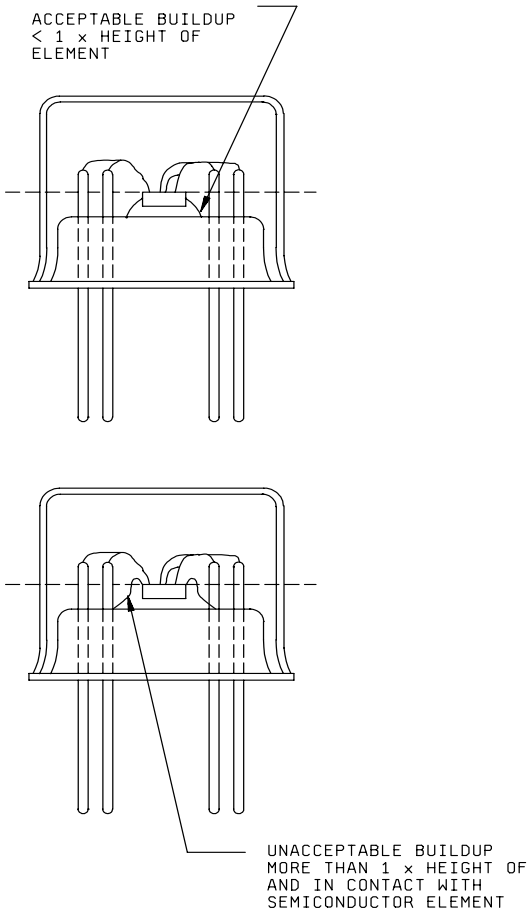

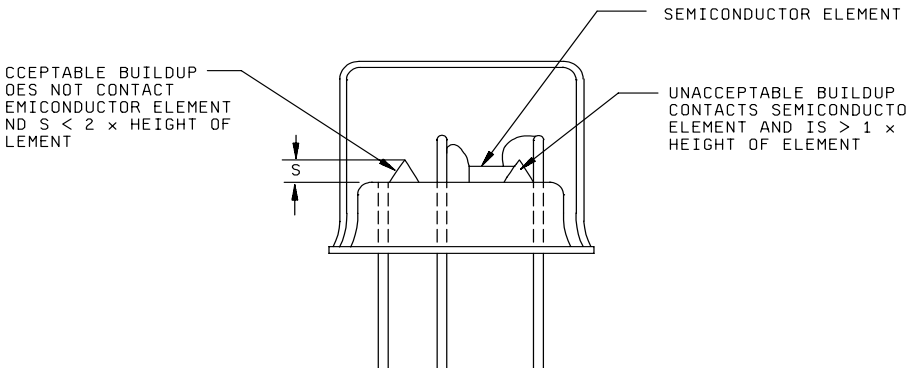

DETAIL A

NOTE: Die and wire are not necessarily visible.

FIGURE 2078-12. Extraneous bonding material build-up.

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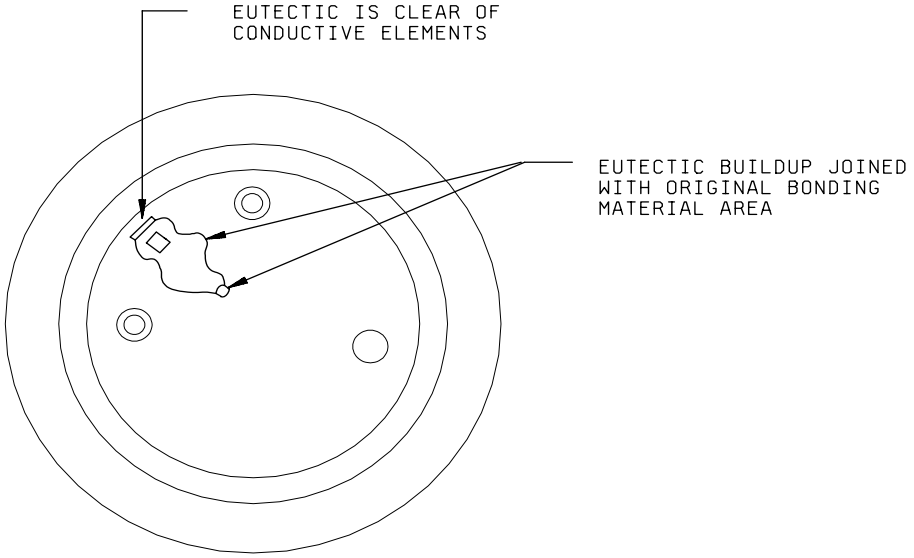
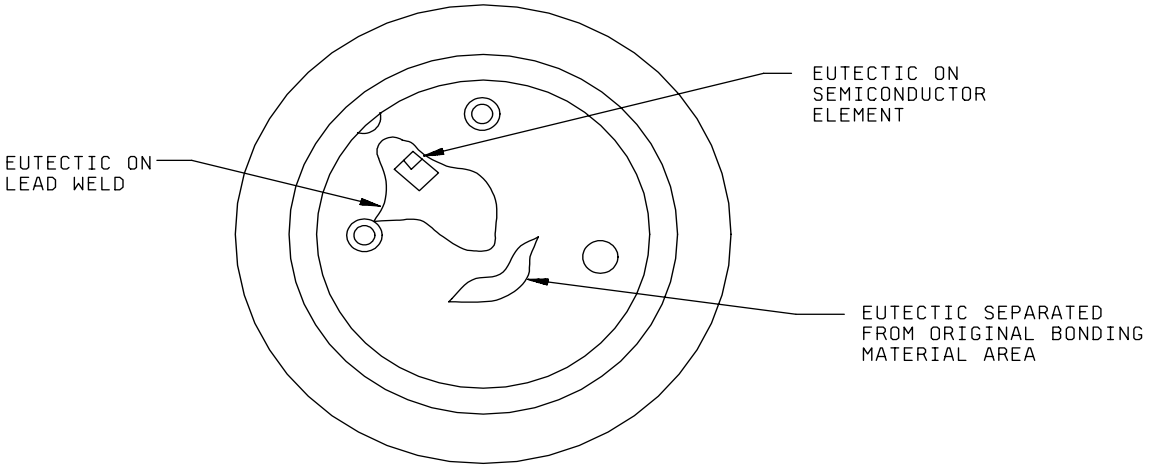


ACCEPTABLE



UNACCEPTABLE

FIGURE 2078-13. Acceptable and unacceptable excess material.

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METHOD 2081

FORWARD INSTABILITY, SHOCK (FIST)

1. Purpose. This test method is intended to detect any device discontinuity "ringing" or shifting of the forward dc voltage characteristic monitored during shock.

2. Apparatus. The shock testing apparatus shall be capable of providing shock pulses of the specified peak acceleration and pulse duration to the body of the device. The acceleration pulse, as determined from the unfiltered output of a transducer with a natural frequency greater than or equal to five times the frequency of the shock pulse being established, shall be a half-sine waveform with an allowable distortion not greater than ±20 percent of the specified peak acceleration. The pulse duration shall be measured between the points at 10 percent of the peak acceleration during rise time and at 10 percent of the peak acceleration during decay time. Absolute tolerances of the pulse duration shall be the greater of ±0.6 ms or ±15 percent of the specified duration for specified durations of 2 ms and greater. For specified durations less than 2 ms, absolute tolerances shall be the greater of ±0.1 ms or ±30 percent of the specified duration. The monitoring equipment shall be an oscilloscope or any "latch and hold" interrupt detector of appropriate sensitivity.

3. Procedure. The shock testing apparatus shall be mounted on a sturdy laboratory table or equivalent base and leveled before use. The device shall be rigidly mounted or restrained by its case with suitable protection for the leads. Special care is required to ensure positive electrical connection to the device leads to prevent intermittent contacts during shock. The device shall be subjected to five shock pulses of 1,000 g peak minimum for the pulse duration of 1 ms in each of two perpendicular planes. For each blow, the carriage shall be raised to the height necessary for obtaining the specified acceleration and then allowed to fall. Means may be provided to prevent the carriage from striking the anvil a second time. With the specified dc voltage and current applied, the forward dc characteristic shall be displayed on a oscilloscope swept at 60 Hz and shall be monitored continuously during the shock test.

4. Failure criteria. During the shock test, any discontinuity, flutter, drift, or shift in oscilloscope trace or any dynamic instabilities shall be cause for rejection of the semiconductor DUT(s).

5. Summary. The following conditions shall be specified in the specification sheet:

   a. Acceleration and duration of pulse, if other than that specified (see 3.).

   b. Number and direction of blows, if other than that specified (see 3.).

   c. Electrical-load conditions (see 3.).

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METHOD 2082

BACKWARD INSTABILITY, VIBRATION (BIST)

1. Purpose. This test method is intended to detect any device discontinuity "ringing" or shifting of the reverse dc voltage characteristic monitored during vibration.

2. Apparatus. The vibration testing apparatus shall be capable of providing the required frequency vibration at the specified levels. The monitoring equipment shall be an oscilloscope or any "latch and hold" interrupt detector of appropriate sensitivity.

3. Procedure. The device shall be rigidly fastened on the vibration platform. Special care is required to ensure positive electrical connection to the device leads to prevent intermittent contacts during vibration. Care must also be exercised to avoid magnetic fields in the area of the device being vibrated. The device shall be vibrated with a simple harmonic motion at 60 ±3 Hz, with .1 inch (2.54 mm) minimum double amplitude displacement for a period of 30 seconds minimum in the X orientation planes (see note below). The acceleration shall be monitored at a point where the "g" level is equivalent to that of the support point for the device(s). With the specified dc voltage and current applied (for zeners only) and with the specified reverse dc voltage applied (for diodes and rectifiers only), the reverse dc characteristic shall be displayed on an oscilloscope swept at 60 Hz and shall be monitored continuously during the vibration test.

NOTE: g level calculation:

$g = .0512f^2DA.$

f = frequency in Hz.

DA = double amplitude in inches.

4. Failure criteria. During the vibration test, any discontinuity, flutter, drift, or shift in oscilloscope trace or any dynamic instabilities shall be cause for rejection of the semiconductor DUT.

5. Summary. The following conditions shall be specified in the specification sheet.

a. Frequency range and time period, if other than that specified.

b. Peak acceleration, if other than that specified.

c. Orientation plan, if other than that specified.

d. Voltage and lead conditions.

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METHOD 2101.1

DPA PROCEDURES FOR DIODES

1. Purpose. This method describes detail procedures and evaluation guidelines for the destructive physical analysis (DPA) of commonly specified diodes. It is intended to provide techniques for determining compliance with specified construction requirements, as well as for evaluating processes, workmanship, and material consistency of the product in relation to MIL-PRF-19500 requirements.

2. Scope. This method pertains to all diode constructions including metal can, except where the die is encapsulated in a package normally specified for transistors. Diodes in transistor packages shall be evaluated using method 2102.

3. Sampling. Sampling for DPA shall be as specified in the applicable diode specification sheet or acquisition procedure requirements, by contract. Destructive analysis shall be totally compliant with the specification sheet for electrical and mechanical requirements or as otherwise specified in the acquisition requirements.

4. Procedure. The DPA samples shall be subjected to all procedures specified by contract which are applicable to the device construction. If a device does not conform to the specific requirements herein, or contains systemic anomalies known to directly affect reliability, the disposition of the lot shall be according to contract. Random anomalies detected when devices are subjected to tests or examinations which are additional, or more rigorous than those in the detail specification, for the product assurance level being inspected, shall be noted in the report but shall not cause the lot to be considered nonconforming.

TABLE 2101-I Mandatory procedures. 1/

Techniques	See
Electrical testing in accordance with group A, subgroup II of detail specification	4.3
Electrical testing in accordance with group A, subgroups III and IV and design ratings	4.4
External visual	4.5
Radiographic inspection	4.6
Hermetic seal	4.7
Hermetic seal for polymeric encapsulated devices such as bridge assemblies which contain hermetically sealed diodes shall be performed after the removal of the encapsulant	4.8 and 5.4
PIND testing	4.9
Residual gas analysis	4.10
For transparent diodes, internal visual inspection	4.11
Axial lead tensile test	4.12
Resistance to solvents	4.13
Solderability	4.14
Terminal strength	4.15
Decap analysis	5

1/ A list of techniques to be tailored for DPA performance according to the end item mission requirements and appropriate to the device construction. The tests required from this list shall be specified in the contract.

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4.1 General. DPA status shall be completely documented in a report containing the following required information:

a. PIN and MIL-PRF-19500 reliability level.

b. Device manufacturer.

c. Lot date code.

d. When applicable and where acquired, an order.

e. Sample size for each test.

f. Results of each test.

g. Stamp or signature of analyst for each test.

h. Shipment quantity represented by the DPA.

i. Radiographs, one of each required view.

j. PIND, sample size, and results.

k. Photographs including one of entire device excluding leads.

l. One copy of electrical data.

m. One copy of all mechanical dimensions data.

n. When applicable, MIL-STD-750 test method number.

o. Destruct sample evidence will remain with lot.

4.2 Tests. For MIL-PRF-19500 products, the test methods specified herein shall be performed by specific MIL-PRF-19500 qualified manufacturers, their customers, or approved sources appearing on the DSCC lab suitability list.

4.3 Electrical and mechanical verification.

a. Group A, subgroup 2 inspections for room temperature dc tests shall be performed prior to DPA to verify electrical compliance of the sample. Variables data shall be taken and remain as part of the record for the lot.

b. Package dimensions as described in the outline drawing shall be measured and recorded when required. Variables data from incoming or source inspection may be used to satisfy certain requirements of this procedure if the requirements of 4.2 herein are met and the contracting parties are in agreement.

4.4 Optional electricals. Optional electrical tests such as group A, subgroup 3 of MIL-PRF-19500 for high and low temperature and subgroup 4 for dynamic characteristics may be performed. Additional design capability tests from the specification sheet; such as surge current, transient thermal resistance, and temperature coefficient may be performed. These will be specified by the contract.

4.5 External visual. External visual shall be performed according to method 2071. All text on the device body shall be recorded. If the identifier BeO is found, the manufacturer shall be contacted for information regarding alternative decap techniques.

4.6 Radiography inspection. Radiographic inspection shall be performed in accordance with method 2076.

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4.7 Hermetic seal. Hermetic shall be performed. Devices shall be subject to gross and fine leak in accordance with method 1071. Omit the fine leak requirement for double plug construction type diodes. Substitute gross leak, condition E, as applicable, for double plug types and method 2068 for double plug opaque glass body types. Paint shall be removed prior to subjecting glass devices to hermetic seal evaluations.

4.8 Hermetic seal for polymeric encapsulated devices. Hermetic seal for polymeric encapsulated devices such as bridge assemblies, which contain hermetically sealed diodes, shall have the diodes evaluated after removal of the encapsulant (see 5.4 herein).

4.9 PIND testing. PIND testing shall be performed on devices with internal die cavities to method 2052, condition A.

4.10 Water vapor testing. Water vapor testing to method 1018 shall be performed on additional unopened devices to one of the three allowed procedures if it has been determined after delidding (see 5.3 herein) that corrosion or potentially corrosive elements such as chlorine or potassium salts are present in the cavity.

4.11 Internal visual. Internal visual shall be performed prior to any destructive procedures for diodes of clear glass construction. Criteria shall be in accordance with method 2074. Opaque or metal can construction shall be evaluated for internal features after the decap procedure (see 5. herein).

4.12 Axial lead tensile test. Axial lead tensile strength shall be tested in accordance with method 2005.

4.13 Resistance to solvents. Resistance to solvents shall be performed in accordance with method 1022.

4.14 Solderability. Solderability shall be performed on "as received" devices within 30 days of receipt according to method 2026. Care in handling shall be exercised to prevent lead surface contamination prior to and during this test.

4.15 Terminal strength. Terminal strength shall be performed in accordance with method 2036.

5. Decap analysis. Decapping techniques for die inspection and die bond analysis shall be performed. (All inspections requiring an intact diode shall be completed at this point.)

5.1 Axial lead or surface mount construction.

a. The diode shall be encapsulated longitudinally in a mounting compound suitable for use as a carrier for further sample processing. The mounting compound will be selected to have expansion and contraction properties as close as possible to the device body encapsulant to prevent the generation of stress cracks in sample preparation.

b. For clear glass construction the sample shall be positioned in such a way that one side of the die is parallel to the sectioning apparatus (see figure 2101-1). This will assure that polishing of the cross section will reveal areas from which approximate dimensions may be determined.

c. The sample shall be sectioned using a laboratory grade grinding and lapping table. Precautions shall be taken to prevent damage to the sample by overly aggressive grit paper selection. In the case of cavity type constructions, the process of grinding shall stop immediately upon opening the cavity to allow for the insertion and curing of clear backfilling compound material. This is done to assure that the internal constituents of the assembly are encased and protected from damage to the die as the grinding process continues.

d. The DPA sample may be polished and stained to enhance construction details at one or several planes. The specimen will be recorded by photomicroscopy when it is determined that the center of the die has been reached (see figure 2101-1). Two photographs will be taken; one containing means for dimensioning the image, or the optical magnification shall be indicated.

e. Due to the brittle characteristics of the various materials in the construction method, damage may be induced by the sectioning technique. For glass diodes with metallurgical bond, die, or glass cracks, damage may be induced as the compression built into the seal is relaxed as the structure is weakened in the cross sectioning process. This method may not be used for disposition of metallurgical bond voids.

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5.2 Scribe, break and dig method for glass axial lead and surface mount types.

a. In this method the device is deliberately destroyed to allow visibility to the die attachment area.

b. The diode body is scored circumferentially at the location of the die plane (see figure 2101-2). This is usually accomplished with a diamond scribe. The device is then snapped into two pieces. (Observe eye protection against glass particles). Alternatively the glass body may be chemically dissolved and the die snapped (provided the die and die metallization are not attacked by the chemical that can be a common problem with this alternative). At this time the two plug surfaces may be inspected for both silicon and die metallization residue.

c. The silicon remaining on each plug may be chemically removed to provide visibility to the attachment interface materials or by further scraping or digging through all of the bond interfaces; however, this step is not mandatory. Photographs will be taken of both separated attachment surfaces. A means may be provided in the photo to dimension the image.

5.2.1 Die bond evaluation. Metallurgically bonded construction types shall be evaluated to the requirements of 30.14 of MIL-PRF-19500. Both separated contact interfaces shall be optically evaluated for the bond area in accordance with table 2101-II (die attach criteria). If a device does not satisfy the die attach criteria, as specified, a thermal transient response test (method 3101, MIL-STD-750) shall be performed, on a sample basis to establish acceptability for use.

TABLE 2101-II. Die attach criteria.

Construction	Percent design contact area to be bonded (typical)
Category I: Eutectic, thermally matched	80
Category II: Solder	50
Silver button with braze 1/	25
Category III: Silver button side	Unspecified
Back side 2/	10
Zeners, Schottky, and rectifier devices as applicable 3/	0

1/ Dumet silver button design contact area is the entire button top view area in intimate contact with the plug or braze preform interface. When both sides of the die are adequately bonded, the button to silicon interface (the area from which silver has grown, but not including any area which may be expanded over protective oxides) may become the area where separation occurs using the scribe and break technique to open the glass. The button to silicon interface will then become the measured design contact area. The percent bond area will be determined by the silicon pulled and remaining on the backside of the button.

2/ Dumet silver button construction: The percent area requirement applies only to the back contact or silicon side. The button to plug interface shall be bonded at point of contact or the tangent formed at their interface.

3/ The requirements of 5.2.1 do not apply for thermally matched noncavity category III construction.

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5.3 Stud mount or axial lead metal can.

a. Determine internal construction techniques from construction documentation or radiographic inspection.

b. For crimp construction, encapsulate one device in a specimen mounting compound suitable for grinding, lapping, and polishing procedures. Section the crimp perpendicular to the longitudinal axis to the point where the crimp is made (as determined from the construction details in the drawings or radiographic image) and determine the quality of the mechanical attachment process (see figure 2101-3).

c. This same sample may be used to observe the construction and dimensions of the internal elements. This will be accomplished by cross section of the device along the longitudinal axis and backfilling the internal cavity with epoxy as soon as the case is penetrated to prevent damage in the grinding operations to follow. Section the device to the approximate center of the die by carefully examining the device at various planes and reducing the grit abrasiveness to limit sectioning damage. Polish and stain the sample to enhance die construction. Then photograph the internal elements.

d. To view all internal surfaces, unmounted samples shall be delidded by cutting the crimp terminal just below the mechanical attachment then removing the lid by cutting circumferentially with a delidding device above the seating flange (see figure 2101-3). Care must be taken to prevent damage to the post connection at the top of the die when delidding.

e. The device shall be evaluated for die attachment position, die to preform and header interface, die topography, and post or "C" bend attachment. Photographs of internal construction will be made.

f. Bond strength testing using method 2037 is optional for construction with metal clips or wires.

g. When practical, die shear or punch testing for metal cans shall be in accordance with method 2017.

5.4 Plastic encapsulated assemblies.

a. Complex devices such as bridges containing several discrete devices shall be evaluated externally for all major features as applicable and described above for individual devices.

b. Internal construction shall be evaluated by removing the device encapsulating material with appropriate reagents using standard laboratory practice. Where uncertainty about the destructiveness of chemicals exists on internal construction elements, experiments on electrical rejects should occur or the manufacturer should be contacted for guidance.

c. Individual diode placement and method of attachment to assembly terminals shall be evaluated. Attention shall be focused on internal conductor diameters and minimum bridging distance of electrically isolated points.

d. Individual discrete diodes shall be removed from the assembly in a manner which does not impart mechanical shock or overtemperature conditions. They shall be evaluated according to the method appropriate to their construction as specified in the appropriate method herein.

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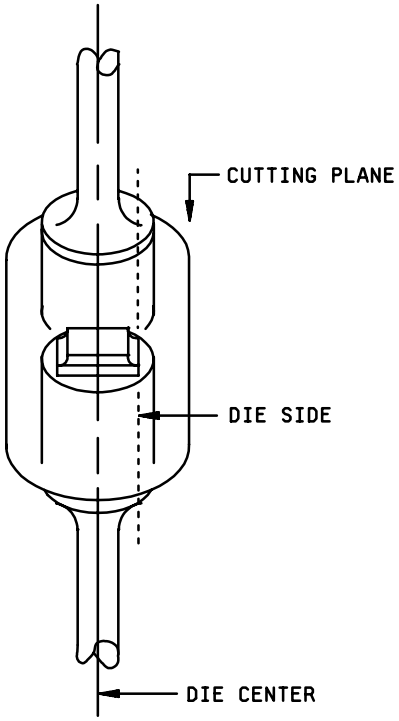

FIGURE 2101-1. Axial lead or surface mount construction.

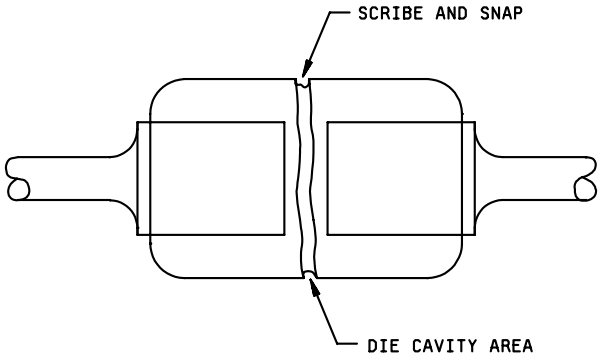

FIGURE 2101-2. Axial lead or surface mount construction.

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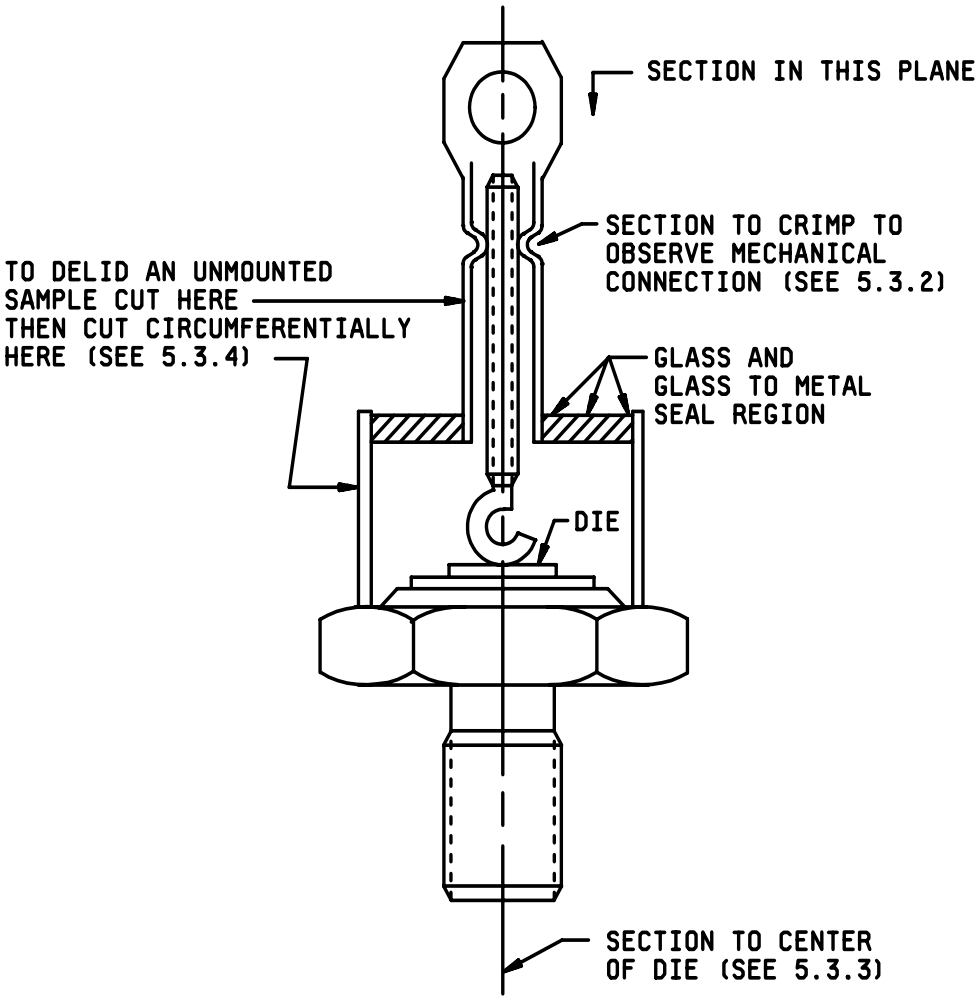

FIGURE 2101-3. Stud package.

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METHOD 2102

DESTRUCTIVE PHYSICAL ANALYSIS FOR WIRE BONDED DEVICES

1. Purpose. This test method describes procedures and evaluation guidelines for the destructive physical analysis (DPA) of wire bonded semiconductor devices. It is intended to provide techniques for determining compliance with construction requirements, as well as evaluating processes, consistency, and workmanship with respect to MIL-PRF-19500 requirements.

2. Scope. This method covers all hermetically sealed, wire bonded device types.

3. Requirements

3.1 Apparatus. Equipment requirements shall be as specified in the various test methods for each procedure listed. Equipment for delidding will vary from package to package and may be custom built or provided commercially.

3.2 Sampling. Sampling for DPA shall be specified in the applicable detail specification or acquisition procedure requirements, by contract. If no quantity is given, three parts shall be used. If internal water vapor (RGA) is to be performed in 4.9, this sample shall be separate. Parts used for DPA testing must pass group A, subgroup 2 testing as a minimum.

3.3 Applicable inspections. MIL-PRF-19500, the applicable specification sheet, the reliability level, and any order or contract requirements determine if a listed inspection is applicable. In the event of a conflict, the following order of precedence shall be applied; a) purchase order or contract, b) specification sheet, c) MIL-PRF-19500, and d) individual test methods. The actual revisions of the specifications referenced within shall be determine from the date code unless superseded by the order or contract or the specification sheet. For the purpose of investigation, higher magnifications than specified or alternate equipment may be used; however, the report shall clearly indicate whether the observed phenomena was a violation when inspected at the prescribed inspection magnification, at the time of manufacture. The term "when specified" is used herein to identify tests specified in MIL-PRF-19500 which do not apply to all quality levels. These tests are to be performed only on device types which require them as part of the manufacturing process.

4. Procedure. Unless otherwise stated, inspections shall be performed in the order specified.

4.1 Device identification. If unique serial numbers do not already exist identifying each device, they shall be assigned to the sample devices. Serial number identity of all samples and parts of samples shall be maintained throughout the complete analytical process.

4.2 External visual. Perform visual in accordance with method 2071.

4.3 Record markings. The report shall include all markings on the device such as part number, manufacturer, date code, and serial number.

4.4 Electrical test. Group A, subgroup 2 reverse leakage and "on" parameters shall be read and recorded. If read and record data traceable to each individual sample has been previously taken and submitted with the samples, this testing need not be repeated. Sustaining voltage and thermal tests are not to be attempted by the DPA lab since special test circuits or equipment may be required to prevent device damage.

4.5 Hermeticity. Perform gross leak testing in accordance with method 1071, and the associated specification sheet. Fine leak shall be performed if RGA is required in 4.10.

4.6 Radiographic Inspection. When specified, perform radiographic inspection in accordance with method 2076.

4.7 PARTICLE IMPACT NOISE DETECTION. When specified, perform PIND test in accordance with method 2052, condition A or B. Devices failing PIND shall have particle capture, particle dimensional analysis, and particle element (chemical) analysis performed.

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4.8 Decapsulation. Delidding may be performed by any method, however, since delidding techniques require a level of skill and special equipment in good condition to prevent damage to internal components, any internal damage or anomalies observed shall be cause to review the delidding technique used and the potential for the damage or anomaly to have been caused by the delidding process. The decapsulation process used shall be detailed in the DPA report.

4.8.1 Photographs. Two magnified photographs shall be taken with a magnification such that in the first one, little more than both ends of all wires are visible (or would be visible if an opaque coating used were not present) and in the second, the chip fills the field of view to the maximum possible.

4.8.2 Design verification. Perform design verification in accordance with method 2075.

a. If a design base line exists, the DPA samples shall be compared to that baseline. Differences shall be documented but may not be rejectable if the difference only involves one or more of the following.

(1) The linear or rotational position of the chip.

(2) The position of the wire bonds within the same wire bonding terminal or pad.

(3) The length of the wires.

Violations of the specified internal visual requirements (when specified) take precedence over the above allowances.

b. If no prior baseline exists, the construction details may be requested from the manufacturers design group. Manufacturers shall not be required to provide details unless such agreements were made in advance of purchase.

4.9 Conformal coating removal. If applicable chemicals used to remove compliant coatings must be compatible with remaining materials of interest. Procedures and materials shall be documented and shall be indicated in the DPA report. It is encouraged that a chemical recommendation be obtained from the manufacturer of the device when the manufacturer is not performing the DPA. Additional photos shall be taken in accordance with 4.8.1 following coating removal, and 4.10 shall be repeated.

4.10 Internal visual (when specified). When specified, perform internal visual in accordance with method 2072 for transistors, method 2069 for method 2073 for diode elements. In the event that foreign material (loose or attached) is found:

a. Identify the elements contained in that material using Energy Dispersive Spectroscopy (EDS) or other suitable techniques.

b. If the material contains corrosive ions such as chlorine:

(1) Select 3 additional devices from the lot.

(2) Establish the presence of moisture within the package using internal water vapor (RGA), method 2018 of MIL-STD-883, dew point method 1018 or other suitable means.

(3) If the moisture level passes, the presence of free ions is acceptable.

(4) Data from any DPA performed by or directed by the original equipment manufacturer that shows defects to this test method shall be shared with the manufacturer.

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4.11 Bond strength. Perform bond pull in accordance with method 2037.

4.12 SEM. When specified- perform SEM examination as required in accordance with the specification sheet and method 2077.

4.13 Die shear. Perform die shear in accordance with method 2017 unless specified otherwise in the specification sheet.

5. Data recording and reporting

5.1 Data recording. The data taken at each step of the analysis shall be permanently recorded. The data sheet shall be referenced as an outline for the testing flow. This data shall identify the test method used for each step, the results obtained for each sample device at each step, the identity of the person performing each step, and the date on which each step was accomplished. Photographs, additional comment sheets, and any data taken by agencies other than the DPA lab shall be clearly identified to maintain traceability to each sample device.

5.2 Report. The analysis report shall identify the part number, lot number, manufacturer, and source of the sample devices. The report shall include the one of all data generated during the analysis. A separate summary of any noncomformances or anomalous conditions found shall be included. The reporting laboratory may include comments or recommendations to the requesting agency if they deem this appropriate.

5.2.1 Sample retention. All samples, along with one copy of the final DPA report, shall be stored and available for review for a minimum of 5 years from the date of the report.

5.3 Acceptance. This test method only specifies the procedures to be used in DPA. Fitness for use of the devices represented by the analyzed sample must be determined by the agency requesting the DPA. Acceptance or rejection of the lot shall be as contractually agreed between the manufacturer and the procuring activity.

6. Summary. The following conditions shall be specified by the agency requesting the DPA:

a. The acquisition document to which the lot was acquired.

b. Sample size, if different than specified.

c. Any tests to be added to, or deleted from, those specified in this test method.

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METHOD 2103

DESIGN VERIFICATION FOR SURFACE MOUNT DEVICES

1. Purpose. The purpose of this test is to qualify the ability of a surface mounted package to withstand the stresses developed by a thermal mismatch (due to differences in thermal expansion properties) between a standard printed circuit card and the device under evaluation.

2. Scope. This test procedure is applicable to all surface mount device packages.

3. Background. The initial issue of this test method is intended for the evaluation of leadless packages. Alternate engineering or characterization data may also be used to demonstrate performance under the stresses imposed by this test. No attempt has been made to include conformal coatings in this test since the wide range of compounds and use conditions precludes standardization.

4. Requirements. Testing shall be performed in accordance with IPC-9701, test condition TC1, and test duration NTC-E.

5. Acceptance Criteria. Acceptance criteria shall be in accordance with IPC-9701.

6. Documentation. Documentation shall be in accordance with IPC-9701.

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3000 Series

Electrical characteristics tests for bipolar transistors

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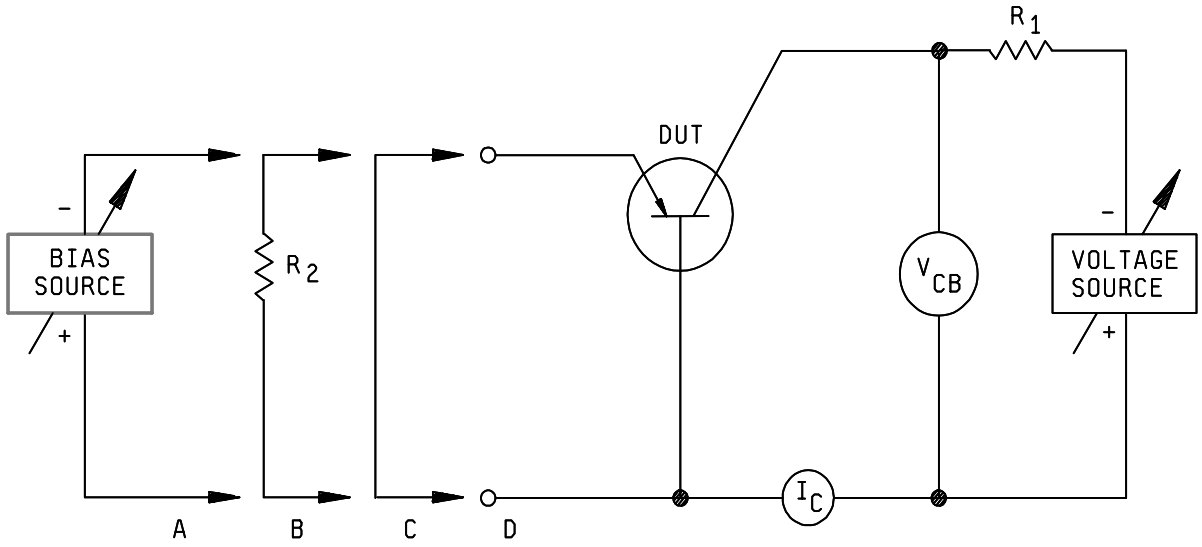
METHOD 3001.1

BREAKDOWN VOLTAGE, COLLECTOR TO BASE

1. Purpose. The purpose of this test is to determine if the breakdown voltage of the device under the specified conditions is greater than the specified minimum limit.

2. Test circuit. See figure 3001-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the ammeter drop.

FIGURE 3001-1. Test circuit for breakdown voltage, collector to base.

3. Procedure. The resistor R_1 is a current-limiting resistor and should be of sufficiently high resistance to avoid excessive current flowing through the device and current meter. The voltage shall be gradually increased, with the specified bias conditions (condition A, B, C, or D) applied, from zero until either the minimum limit for $V_{(BR)CBX}$ or the specified test current is reached. The device is acceptable if the minimum limit for $V_{(BR)CBX}$ is reached before the test current reaches the specified value. If the specified test current is reached first, the device is rejected.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test current (see 3.).

b. Bias condition:

A: Emitter to base: Reverse bias (specify bias voltage).

B: Emitter to base: Reverse return (specify resistance of R_2).

C: Emitter to base: Short-circuit.

D: Emitter to base: Open-circuit.

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METHOD 3005.1

BURNOUT BY PULSING

1. Purpose. The purpose of this test is to determine the capabilities of the device to withstand pulses.

2. Procedure. The device shall be subjected to a pulse or pulses of the length, voltages, currents, and repetition rate specified with the specified prepulse conditions.

3. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Prepulse conditions (see 2.).

   b. Pulse width (see 2.).

   c. Pulse voltages and currents (see 2.).

   d. Repetition rate (see 2.).

   e. Measurements after test.

   f. Length of test or number of cycles.

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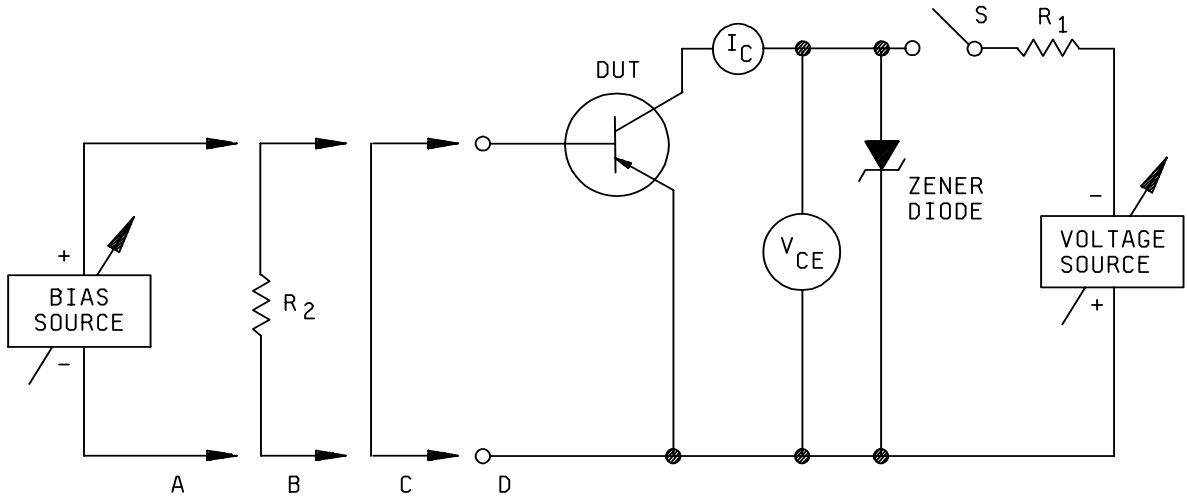
METHOD 3011.2

BREAKDOWN VOLTAGE, COLLECTOR TO EMITTER

1. Purpose. The purpose of this test is to determine if the breakdown voltage of the device under the specified conditions is greater than the specified minimum limit.

2. Test circuit. See figure 3011-1.



NOTES:
1. A PNP device is shown. For NPN types, reverse the polarities of the voltage and bias sources and zener diode.
2. An electronic switch, S may be necessary to provide pulses of short duty cycle to minimize the rise of junction temperature.
3. The current sensor, or ammeter, shall present essentially a short circuit to the terminals between which the current is being measured, or the voltage readings shall be corrected accordingly.
4. It is important to prevent, or dampen, potentially damaging oscillations in devices exhibiting negative resistance breakdown characteristics. Protection can be in the form of a circuit which circumvents the negative resistance region, such as one which provides suitable base current as the collector voltage is increased; however, the specified bias condition and test current must be applied when the voltage is measured. Additional protection can be provided with a zener diode, or transient voltage protection circuit to limit to collector voltage at, or slightly above, the specified minimum limit.
5. Regardless of the protection used, extreme care must be exercised to ensure the collector current and junction temperature remain at a safe value, as given in the applicable specification sheet.

FIGURE 3011-1. Test circuit for breakdown voltage, collector to emitter.

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3. Procedure. The resistor R_1 is a current-limiting resistor and should be of sufficiently high resistance to avoid excessive current flowing through the device and current sensor. The voltage shall be increased, with the specified bias conditions (condition A, B, C, or D) applied, until the specified test current is reached. The device is acceptable if the voltage applied at the specified test current is greater than the minimum limit for $V_{(BR)CEX}$.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test current (see 3.).

   b. Duty cycle and pulse width, when required (see figure 3011-1, above).

   c. Bias condition:

      A: Emitter to base: Reverse bias (specify bias voltage).

      B: Emitter to base: Resistance return (specify resistance value of R_2).

      C: Emitter to base: Short-circuit.

      D: Emitter to base: Open-circuit.

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METHOD 3015

DRIFT

1. Purpose. The purpose of this test is to determine the drift of a parameter specified in the applicable specification sheet of the device.

2. Apparatus. The apparatus used for the performance of the drift test shall be the same as that utilized for testing the associated parameter.

3. Procedure. The voltages and currents specified in the applicable specification sheet shall be applied. In the period from 10 seconds to 1 minute, the measurement specified in the applicable specification sheet shall drift no more than the amount specified in the applicable specification sheet.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test currents and voltages (see 3.).

   b. Test parameter (see 3.).

   c. Test apparatus or test circuit (see 2.).

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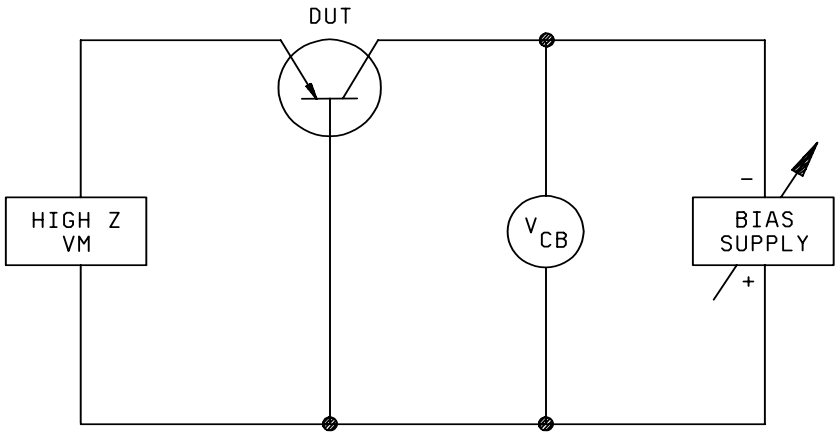
METHOD 3020

FLOATING POTENTIAL

1. Purpose. The purpose of this test is to measure the dc potential between the specified, open-circuited terminal and reference terminal when a dc potential is applied to the other specified terminals.

2. Test circuit. See figure 3020-1.



NOTE: The circuit shown is for measuring the emitter floating potential. For other device configurations, the above circuitry should be modified in such a manner that is capable of demonstrating device conformance to the minimum requirements of the individual specification sheet.

FIGURE 3020-1. Test circuit for floating potential.

3. Procedure. The specified dc voltage shall be applied to the specified terminals and the dc voltage of the open-circuited terminal and reference terminal shall be monitored.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test voltage (see 3.).

   b. Input resistance of high impedance voltmeter (see figure 3020-1).

   c. Test voltage application and reference terminals (see 3.).

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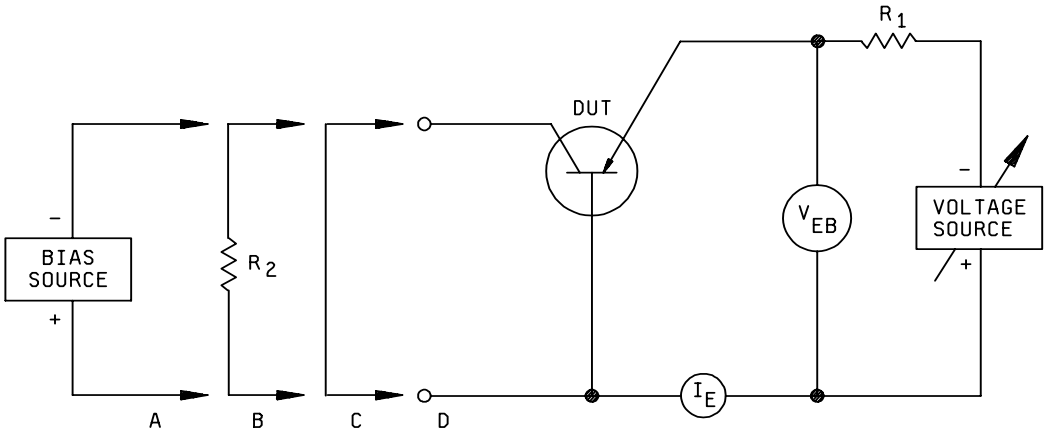
METHOD 3026.1

BREAKDOWN VOLTAGE, EMITTER TO BASE

1. Purpose. The purpose of this test is to determine if the breakdown voltage of the device under the specified conditions is greater than the specified minimum limit.

2. Test circuit. See figure 3026-1.



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the ammeter drop.

FIGURE 3026-1. Test circuit for breakdown voltage, emitter to base.

3. Procedure. The resistor R_1 is a current-limiting resistor and should be of sufficiently high resistance to avoid excessive current flowing through the device and current meter. The voltage shall be gradually increased, with the specified condition (A, B, C, or D) applied, from zero until either the minimum limit for $V_{(BR)EBX}$ or the specified test current is reached. The device is acceptable if the minimum limit for $V_{(BR)EBX}$ is reached before the test current reaches the specified value. If the specified test current is reached first, the device is rejected.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test current (see 3.).

b. Bias condition:

A: Collector to base: Reverse bias (specify bias voltage).

B: Collector to base: Resistance return (specify resistance of R_2).

C: Collector to base: Short-circuit.

D: Collector to base: Open-circuit.

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METHOD 3030

COLLECTOR TO EMITTER VOLTAGE

1. Purpose. The purpose of this test is to measure the voltage between the collector and emitter of the device under specified conditions.

2. Test circuit. See figure 3030-1.

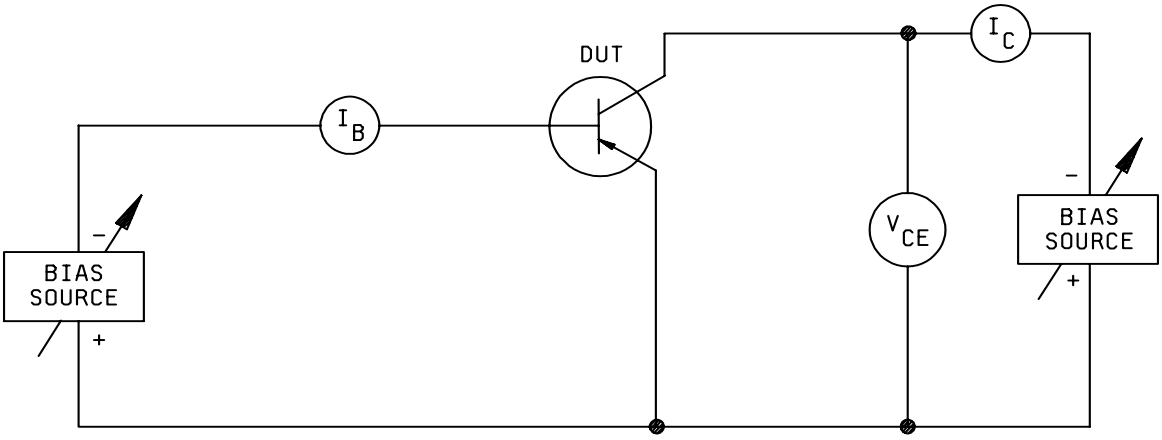

FIGURE 3030-1. Test circuit for collector to emitter voltage.

3. Procedure. The bias supplies shall be adjusted until the specified voltages and currents are achieved. The voltage between the collector and emitter shall then be measured. If high current values are to be used in this measurement, suitable pulse techniques may be used to provide pulses of short duty cycle to minimize the rise in junction temperature.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test voltages and currents (see 3.).

   b. Duty cycle and pulse width if applicable (see 3.).

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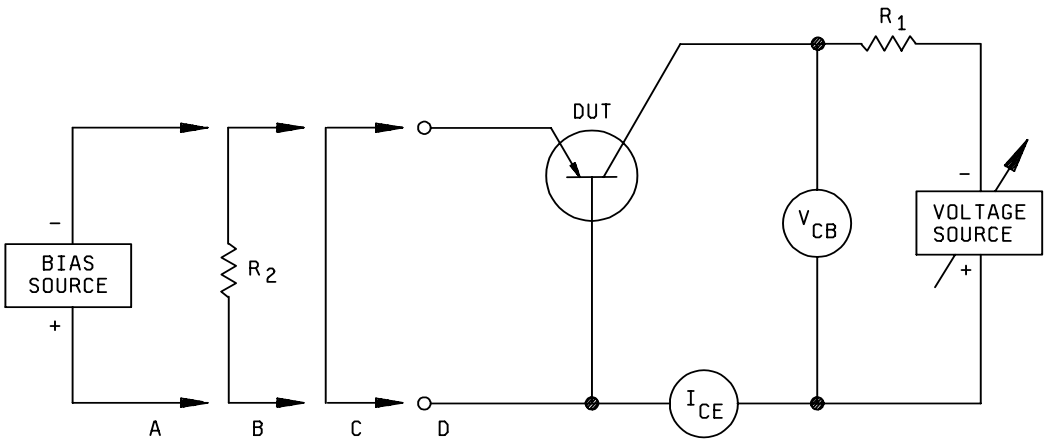
METHOD 3036.1

COLLECTOR TO BASE CUTOFF CURRENT

1. Purpose. The purpose of this test is to measure the cutoff current of the device under the specified conditions.

2. Test circuit. See figure 3036-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter shall be corrected for the drop across the ammeter.

FIGURE 3036-1. Test circuit for collector to base cutoff current.

3. Procedure. The specified dc voltage shall be applied between the collector and the base with the specified bias condition (A, B, C, or D) applied to the emitter. The measurement of current shall be made at the specified ambient or case temperature.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test voltage (see 3.).

b. Test temperature if other than +25°C ±3°C and whether case or ambient (see 3.).

c. Bias condition:

A: Emitter to base: Reverse bias (specify bias voltage).

B: Emitter to base: Resistance return (specify resistance of R_2).

C: Emitter to base: Short-circuit.

D: Emitter to base: Open-circuit.

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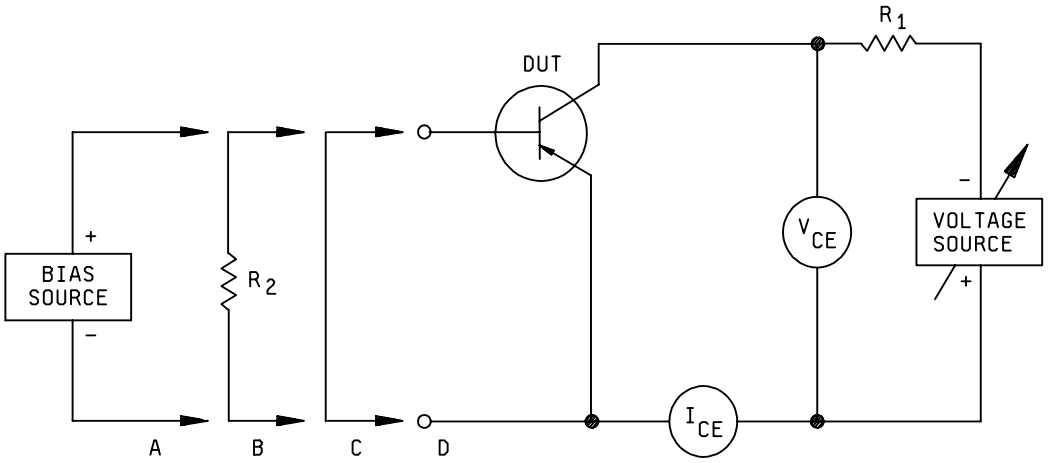
METHOD 3041.1

COLLECTOR TO EMITTER CUTOFF CURRENT

1. Purpose. The purpose of this test is to measure the cutoff current of the device under the specified conditions.

2. Test circuit. See figure 3041-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter shall be corrected for the drop across the ammeter.

FIGURE 3041-1. Test circuit for collector to emitter cutoff current.

3. Procedure. The specified voltage shall be applied between the collector and emitter with the specified bias condition (A, B, C, or D) applied to the base. The measurement of current shall be made at the specified ambient or case temperature.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test voltage (see 3.).

b. Test temperature if other than +25°C ±3°C and whether case or ambient (see 3.).

c. Bias condition:

A: Emitter to base: Reverse bias (specify bias voltage).

B: Emitter to base: Resistance return (specify resistance value of R_2).

C: Emitter to base: Short-circuit.

D: Emitter to base: Open-circuit.

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METHOD 3051

SAFE OPERATING AREA (CONTINUOUS DC)

1. Purpose. The purpose of this test is to verify the boundary of the Safe Operating Area (SOA) of a transistor as constituted by the interdependency of the specified voltage, current, power, and temperature in a temperature stable circuit.

2. Test circuit. See figure 3051-1.

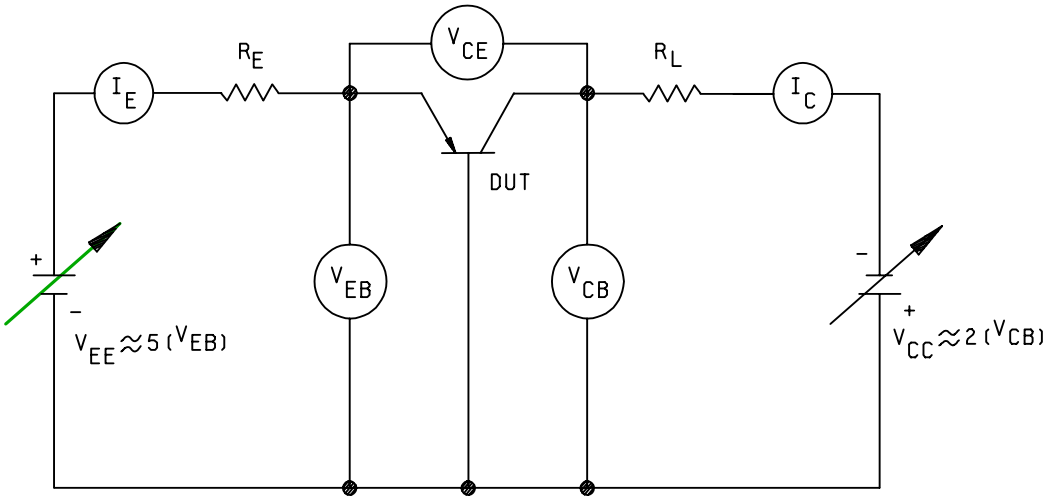

FIGURE 3051-1. Test circuit for SOA (continuous dc).

3. Procedure.

   a. Starting with V_{CC} and V_{EE} at a low value, increase V_{CC} to approximately obtain specified V_{CE}. Increase V_{EE} to approximately obtain specified I_C. Increase V_{CC} and subsequently adjust V_{EE} to obtain specified V_{CE} and I_C. Operate the transistor at the specified temperature and for the specified time duration.

   b. Decrease V_{CC} to obtain V_{CE} near zero. Turn off V_{EE}. Turn off V_{CC}.

   c. The transistor shall be considered a failure if I_C varies ±10 percent during operation, or exceeds the end-points.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

   a. Maximum SOA graph: I_C versus V_{CE} (see 3.).

   b. Temperature, case or ambient (see 3.).

   c. Values of V_{CE} and I_C.

   d. Operating time (see 3.).

   e. Measurements after test.

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METHOD 3052

SAFE OPERATING AREA (PULSED)

1. Purpose. The purpose of this test is to verify the capability of a transistor to withstand pulses of specific voltage, current, and time, establishing a SOA.

2. Test circuit. See figure 3052-1.

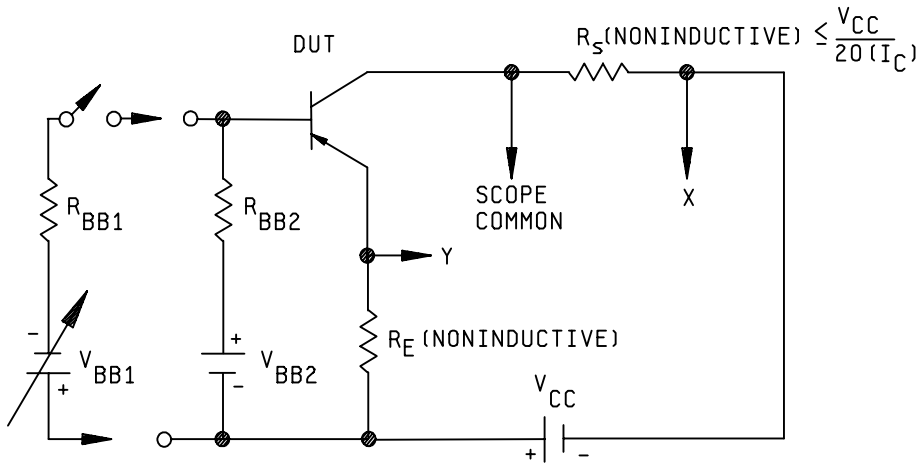

FIGURE 3052-1. Test circuit for SOA (pulsed).

3. Procedure. Starting at a low value, adjust V_{BB2} and V_{CC} to the specified levels. With the duty cycle and pulse width preset to specified conditions, increase V_{BB1} voltage to achieve the specified I_C.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. Maximum SOA graph: I_C versus V_{CE}.

b. Temperature, case or ambient.

c. Input pulse and bias conditions:

(1) Pulse duty cycle.

(2) Pulse width.

(3) t_r and t_f.

(4) Values for R_{BB2}, R_{BB1}, and V_{BB2} (see figure 3052-1).

(5) Number of pulses or test duration.

d. Values of R_E, V_{CC}, and I_C (see 3.).

e. Measurements after test.

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METHOD 3053

SAFE OPERATING AREA (SWITCHING)

1. Purpose. The purpose of this test is to verify the capability of a transistor to withstand switching between saturation and cutoff for various specified loads, establishing a SOA.

2. Test circuit. See figure 3053-1.

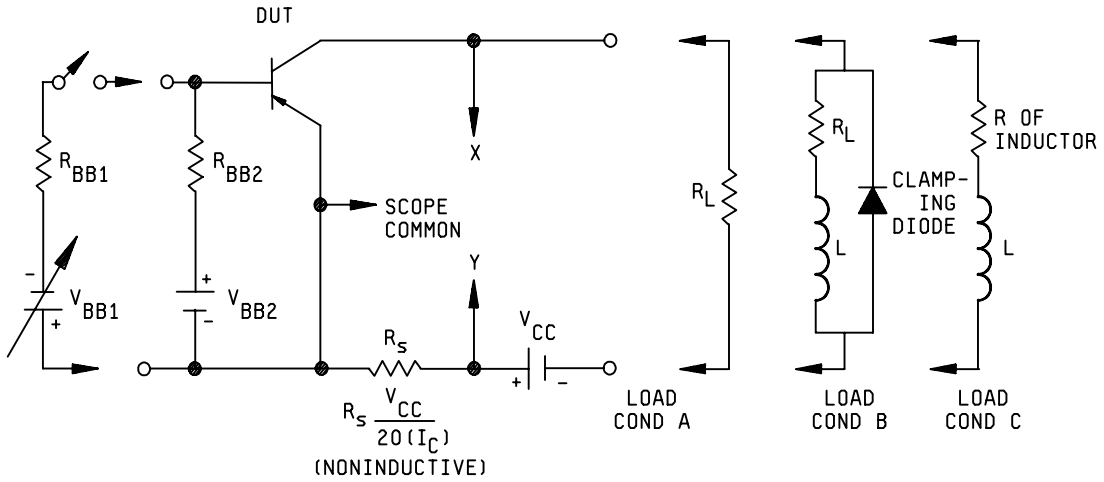

FIGURE 3053-1. Test circuit for SOA (switching).

3. Procedure. The output load circuit configuration shall be as specified (condition A, B, or C). Starting at a low value, adjust V_{BB2} and V_{CC} to the specified levels. With the duty cycle and repetition rate preset to specified conditions, increase V_{BB1} voltage to achieve the specified I_C; and the output waveform (I_C versus V_{CE}) shall be observed on the scope. When the transistor is turned off (switched), the observed trace shall be a smooth curve between saturation and cutoff. Any oscillations or inconsistencies on the trace shall be cause for rejection.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. Maximum SOA graph, with parameter coordinates as follows:

(1) I_C versus V_{CE} for load condition A.

(2) I_C versus V_{CE} for load condition B.

(3) I_C versus L as functions of R_{BB2} and V_{BB2}, for load condition C.

b. Load condition:

A: Resistive load.

B: Clamped inductive load.

C: Unclamped inductive load.

c. Temperature, case or ambient.

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d. Input pulse and bias conditions:

(1) Number of pulses or test duration.

(2) Pulse width.

(3) Pulse duty cycle.

(4) t_r and t_f.

(5) R_{BB1} and V_{BB1}.

(6) R_{BB2} and V_{BB2}.

e. Specific conditions for load and output bias:

Condition A: Values of R_L, I_C, and V_{CC}.

Condition B: Values of R_L, I_C, V_{CC}, diode type or characteristics, inductance and dc resistance of L.

Condition C: Values of I_C, V_{CC}, and characteristics of inductor L including its inductance, Q, dc resistance, and resonant frequency.

f. Measurements after test.

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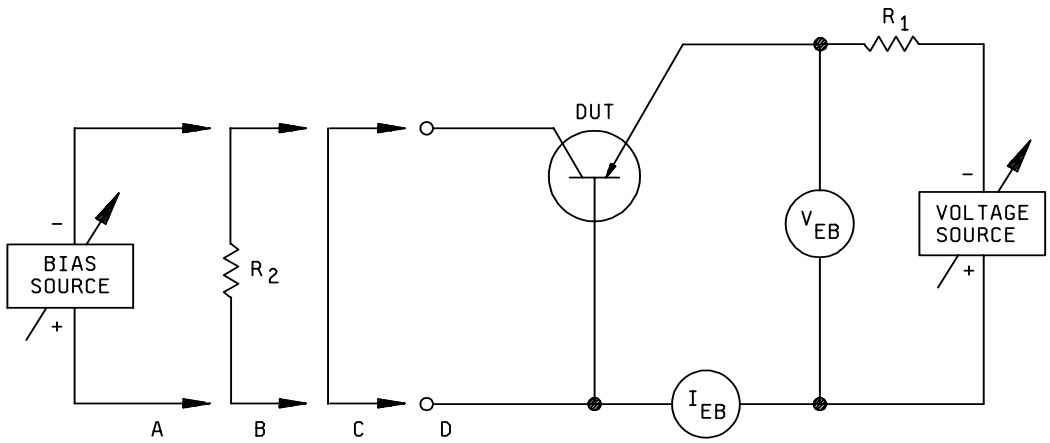
METHOD 3061.1

EMITTER TO BASE CUTOFF CURRENT

1. Purpose. The purpose of this test is to measure the cutoff current of the device under the specified conditions.

2. Test circuit. See figure 3061-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter shall be corrected for the drop across the ammeter.

FIGURE 3061-1. Test circuit for emitter to base cutoff current.

3. Procedure. The specified direct current voltages shall be applied between the emitter and the base with the specified bias condition (condition A, B, C, or D) applied to the collector. The measurement of current shall be made at the specified ambient or case temperature.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. Test voltage (see 3.).

b. Test temperature if other than +25°C ±3°C and whether ambient or case (see 3.).

c. Bias condition

A: Collector to base: Reverse bias (specify bias voltage).

B: Collector to base: Resistance return (specify resistance of R_2).

C: Collector to base: Short-circuit.

D: Collector to base: Open-circuit.

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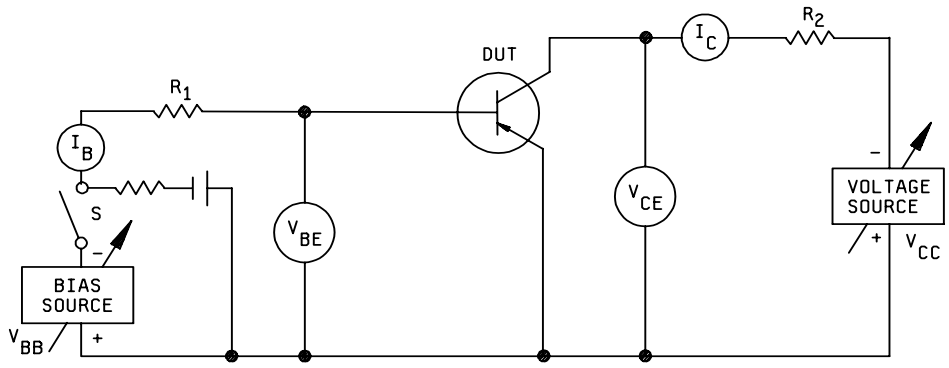
METHOD 3066.1

BASE EMITTER VOLTAGE (SATURATED OR NONSATURATED)

1. Purpose. The purpose of this test is to measure the base to emitter voltage of the device in either a saturated or nonsaturated condition.

2. Test circuit. Circuit and procedure shown are for base to emitter. For other parameters the circuit and procedure should be changed accordingly. (See figure 3066-1)



NOTE: If necessary, switch S shall be used to provide pulses of short duty cycle to minimize the rise in junction temperature. When pulsing techniques are used, oscillograph methods shall be used to measure V_{BE} and the other necessary parameters and the duty cycle and pulse width shall be specified.

FIGURE 3066-1. Test circuit for base emitter voltage (saturated or nonsaturated).

3. Procedure.

3.1 Test condition A (saturated). The resistor R_1 shall be made large. If the pulse method is used, the resistor R_2 shall be chosen in combination with V_{CC} so that the specified collector current is achieved at a value of V_{CC} low enough to ensure that the device will not be operated in breakdown between pulses. If the pulse method is not used, resistor R_2 can be any convenient value. The current I_B and voltage V_{CC} shall be adjusted until I_B and I_C achieve their specified values. Then, $V_{BE} = V_{BE(sat)}$.

3.2 Test condition B (nonsaturated). For this test, resistor R_2 shall be zero. The specified values of I_B and V_{CE} shall be applied. V_{BE} is then measured. Alternately, the specified V_{CE} shall be applied and I_B adjusted to obtain the specified I_C.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. Duty cycle and pulse width, when required.

b. Test condition letter (see 3.).

c. Test voltages or currents (see 3.).

d. Parameter to be measured.

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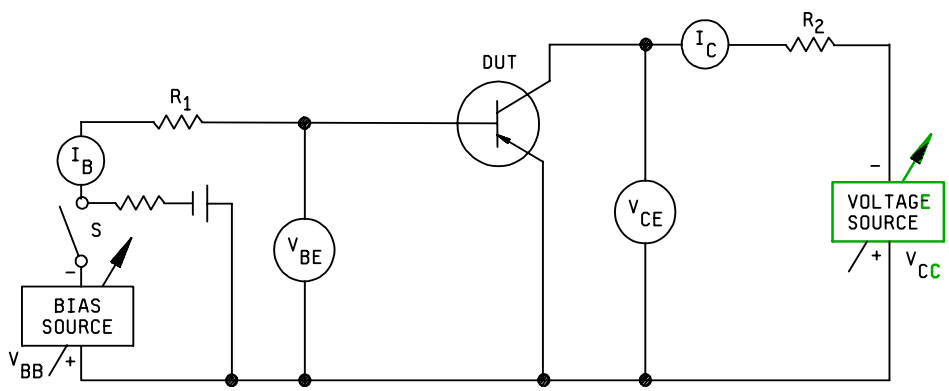
METHOD 3071

SATURATION VOLTAGE AND RESISTANCE

1. Purpose. The purpose of this test is to measure the saturation voltage and resistance of the device under the specified conditions.

2. Test circuit. Circuit and procedure shown are for collector to emitter. For other parameters the circuit and procedure should be changed accordingly. (See figure3071-1.)



NOTE: If necessary, switch S shall be used to provide pulses of short duty cycle to minimize the rise in junction temperature. When pulsing techniques are used, oscillograph methods shall be used to measure V_{BE} and the other necessary parameters and the duty cycle and pulse width shall be specified.

FIGURE 3071-1. Test circuit for saturation voltage and resistance.

3. Procedure. The resistor R_1 shall be made large. If the pulse method is used, resistor R_2 shall be chosen in combination with V_{CC} so that the specified collector current may be achieved at a value of V_{CC} low enough to ensure that the device is not operated in breakdown between pulses. If pulse methods are not used, R_2 may be any convenient value. The current I_B and V_{CC} shall be adjusted until I_B and I_C achieve their specified values. $V_{CE(sat)}$ is then equal to the voltage measured by voltmeter V_{CE} under the specified conditions. Saturation resistance may be determined from the same circuit conditions, as follows:

$$r_{CE(sat)} = \frac{V_{CE}(sat)}{I_C}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. Duty cycle and pulse width, when required (see 3.).

b. Test voltages or currents (see 3.).

c. Parameter to be measured.

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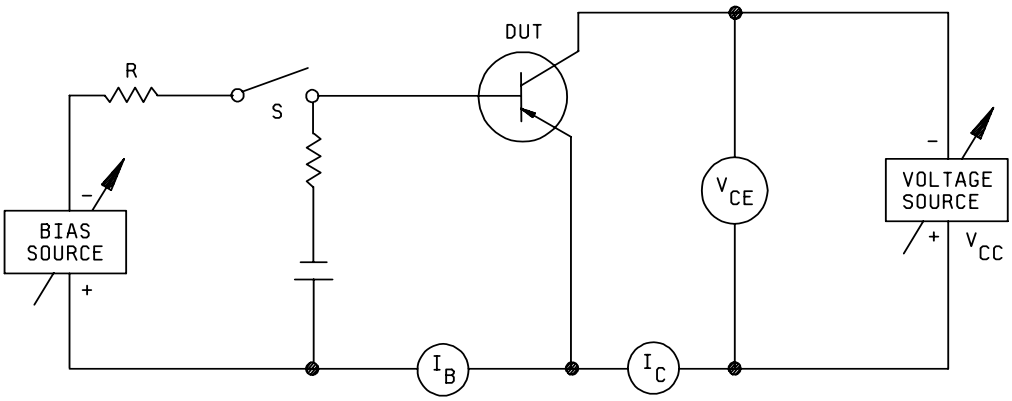
METHOD 3076.1

FORWARD-CURRENT TRANSFER RATIO

1. Purpose. The purpose of this test is to measure the forward-current transfer ratio of the device under the specified conditions.

2. Test circuit. Circuit and procedure shown are for common emitter. For other parameters the circuit and procedure should be changed accordingly. (See figure 3076-1)



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter shall be corrected for the drop across the ammeter.

FIGURE 3076-1. Test circuit for forward-current transfer ratio.

3. Procedure. The voltage V_{CE} shall be set to the specified value and the current I_B shall be adjusted until the specified current I_C is achieved.

Then, $h_{FE} = \frac{I_C}{I_B}$

If high-current values are to be used in this measurement, switch S shall be used to provide pulses of short duty cycle to minimize the rise in junction temperature. When pulsing techniques are used, oscillograph methods may be used to measure I_C and I_B.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. Test voltage or current (see 3.).

b. Duty cycle and pulse width, when required (see 3.).

c. Parameter to be measured.

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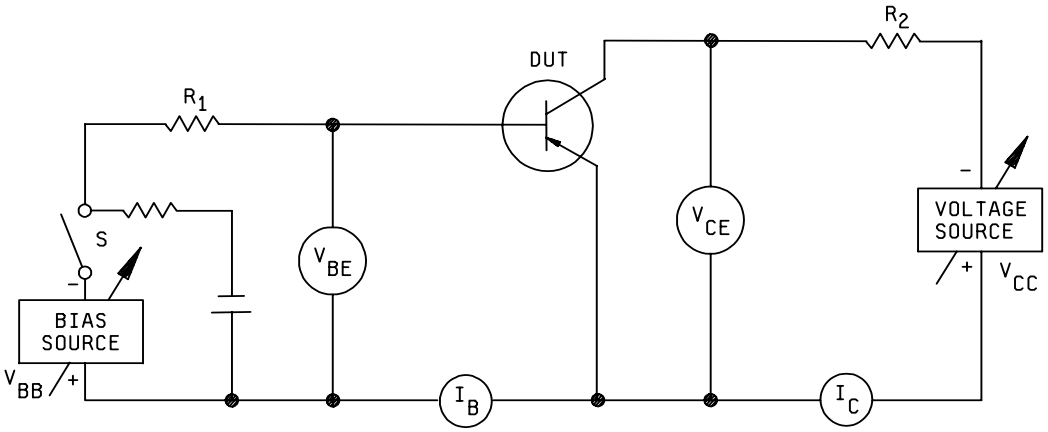
METHOD 3086.1

STATIC INPUT RESISTANCE

1. Purpose. The purpose of this test is to measure the input resistance of the device under the specified conditions.

2. Test circuit. Circuit and procedure shown are for common emitter. For other parameters the circuit and procedure should be changed accordingly. (See figure 3086-1)



NOTE: If necessary, switch S shall be used to provide pulses of short duty cycle to minimize the rise in junction temperature. When pulsing techniques are used, oscillograph methods shall be used to measure V_{BE} and other necessary parameters and the duty cycle and pulse width shall be specified.

FIGURE 3086-1. Test circuit for static input resistance.

3. Procedure. The resistor R_1 shall be made large. If the pulse method is used, resistor R_2 shall be chosen in combination with V_{CC} so that the specified collector current is achieved at a value of V_{CC} low enough to ensure that the device will not be operated in breakdown between pulses. If the pulse method is not used, resistor R_2 can be any convenient value. The current I_B and V_{CC} shall be adjusted until I_B and I_C achieve their specified values.

$$\textit{Then:} \quad h_{IE} = \frac{V_{BE}}{I_B}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. Pulse duty cycle and width, when required (see 3.).

b. Test voltages or currents (see 3.).

c. Parameter to be measured.

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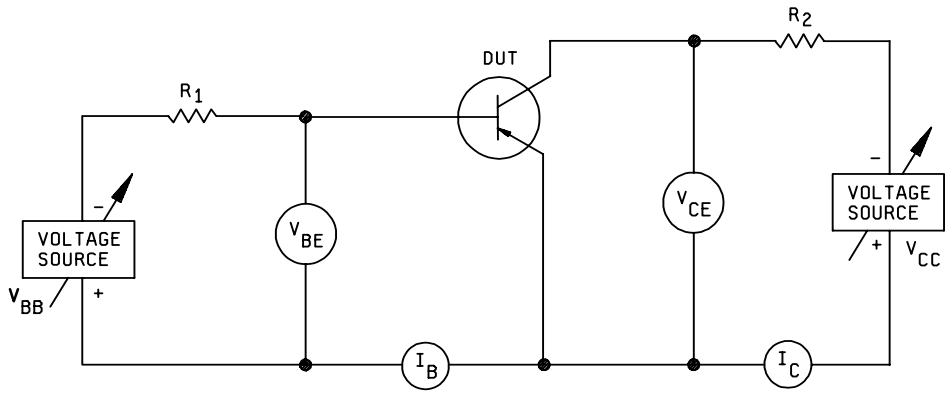
METHOD 3092.1

STATIC TRANSCONDUCTANCE

1. Purpose. The purpose of this test is to measure the static transconductance of the device under the specified conditions.

2. Test circuit. See figure 3092-1.



NOTE: For other configurations, the circuit may be modified in such a manner that it is capable of demonstrating device conformance to the minimum requirements of the applicable specification sheet.

FIGURE 3092-1. Test circuit for static transconductance.

3. Procedure. The resistor R_1 shall be made large or the voltage source V_{BB} shall be replaced by a constant current source. The resistor R_2 shall be chosen in combination with V_{CC} so that the specified collector current is achieved at a value of V_{CC} which is lower than $V_{(BR)CEO}$. The current I_B shall be adjusted until V_{CE} and I_C achieve their specified values. The current I_C or I_E and the voltages V_{BE}, V_{BC}, or V_{EB} shall then be measured. Using the values obtained through these measurements, the static transconductance shall be calculated as follows:

For common emitter:

$$g_{ME} = \frac{I_C}{V_{BE}}$$

For common collector:

$$g_{MC} = \frac{I_E}{V_{BC}}$$

For common base:

$$g_{MB} = \frac{I_C}{V_{EB}}$$

If high current values are to be used in the measurement, suitable pulse techniques may be used to provide pulses of short duty cycle to minimize the rise in junction temperature.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. Test voltage or current (see 3).

b. Duty cycle and pulse width, if applicable.

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3100 Series

Circuit-performance and thermal-resistance measurements

For thermal-resistance measurements, at least three temperature sensitive parameters (TSP) of the transistor can be used; the collector to base cutoff current, I_{CBO}; the forward voltage drop of the emitter to base diode, V_{EB}; and the forward voltage drop of the collector to base diode, V_{CB}. The methods described in this standard refer to the thermal resistance between specified reference points of the device. For this type of measurement, power is applied to the device at two values of case, ambient, or other reference point temperature, such that identical values of I_{CBO}, V_{EB}, or V_{CB} are read during the cooling portion of the measurement.

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METHOD 3100

JUNCTION TEMPERATURE MEASUREMENT AT BURN-IN AND LIFE TEST

1. Purpose. This purpose of this test is to verify a desired junction temperature (T_J) is achieved during burn-in and life-test environments, and is conducted on a representative sample of devices. There are two methods that may be used. Both use a temperature sensitive parameter (TSP) that is initially measured at the desired T_J and selected test-current levels. In the first test, method A, a selected low measuring current that does not cause significant self-heating is used (similar to thermal resistance test methods). In the second test, method B, a series of sequential current pulses are taken to characterize the TSP at the desired T_J in the same operating current region expected for the burn-in and life-test environments. These TSP values are again later compared during burn-in or life-test to verify the same T_J. In either case, a direct sampling method of T_J in the burn-in or life-test environment minimizes or eliminates possible errors introduced by ambient conditions, K factor, and non-linearity of component thermal resistance when applied at high temperatures. The method also allows the burn-in and life-test environment to be accurately characterized for thermal resistance junction to ambient ($R_{\theta JA}$) that can be used again to further advantage for similar products in the same test environment.

2. Scope. This applies to diode and transistor bipolar products requiring T_J verification during power burn-in that generates self-heating of T_J well above ambient or case temperature with applied power. It may also use an oven chamber or hot plate for achieving elevated ambient or case temperatures. The applied power testing may include ac operating life (ACOL) conditions for rectifiers, dc power in the operating breakdown region for zeners, and forward dc power conditions for signal diodes and others. Transistors also involve applied dc power conditions. This generally does not apply to high temperature reverse bais (HTRB) unless sufficient power is applied to cause significant self-heating. Equivalent heating power options are also described in method A to accommodate existing TSP equipment measurement methods for thermal resistance.

3. Rationale. Increased requirements for semiconductor performance, reliability, and quality have forced the need for knowledge and greater accuracy of semiconductor devices T_J at burn-in and life-testing. This is necessary for making long-term calculations for reliability levels if using accelerating effects of burn-in or life-testing.
Accurate T_J measurements can be difficult because of the many variables. Electrical considerations (power, voltage-current levels, waveforms, etc.), environmental consideration (mounting configuration, surroundings, mounting methodology, etc.), and selection of the T_J sensing method will affect results. It should also be noted that the thermal resistance characteristics of any semiconductor device are not necessarily constant with temperature or power dissipation, thus requiring thermal measurements under conditions that best duplicate actual operation in the burn-in or life-test environment for determining T_J.

4. Symbols and definitions. Many features are identical to those used for measuring thermal resistance for method A. For both methods, the burn-in and life-test environment shall simply be known as the test environment. Further details may be found in other references including EIA-531, JESD51-1, and test methods 3101, 3131, and 4081 of this general specification.

a. TSP Temperature sensitive parameter at the measuring current.

b. T_J Junction temperature.

c. T_A Ambient temperature in the test environment.

d. $R_{\theta JA}$ Thermal resistance from junction to ambient.

e. $R_{\theta JL}$ Thermal resistance from junction to lead.

f. $R_{\theta JC}$ Thermal resistance from junction to case.

g. $R_{\theta JEC}$ Thermal resistance from junction to end-cap.

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h. I_M Measuring current for the TSP (V_F or V_{BE}).

i. I_H Heating current.

j. t_H Heating time.

k. t_{MD} Measurement delay time

l. P_H Heating power.

m. V_F Forward voltage.

n. V_{BE} Base-emitter voltage.

o. V_{CE} Collector-emitter voltage.

p. I_C Collector current.

q. I_B Base current.

r. $V_{(BR)}$ Breakdown voltage.

s. V_Z Zener voltage.

t. I_F Forward current.

u. I_O Average I_F for 50 or 60 Hz sine wave and 180 degree conduction angle.

v. I_R Reverse standby current.

w. EC End-cap.

x. DUT Device under test.

5. Equipment. Applicable to both methods A and B unless otherwise noted.

5.1 TSP measurement. Test equipment to initially measure the TSP in a controlled temperature chamber, bath, or hot plate is required at a desired T_J for the sample DUT.

5.2 Power supplies and arrays. The equipment used shall also include the burn-in or life-test power supplies and panel/socket arrays for electrical contacts or heat sinking where the T_J is to be sample measured for the DUTs. This test environment is the same as used for all other remaining devices intended for burn-in screening or life-test.

5.3 Oven chamber. An oven chamber, bath, or hot plate to place the panel socket arrays with all the devices shall be used if elevated ambient temperatures are required.

5.4 Measuring TSP. For method A, equipment for measuring the TSP shall be similar to that described for thermal resistance in EIA-531, JESD51-1, test methods 3101, 3131, or 4081. The TSP is sampled in a short measurement delay time (t_{MD}) after switching to a low measuring current (I_M) from the applied heating power source. The duty factor for sampling the TSP shall be 1percent or less of the heating time (t_H). It is considered optimum to use the same mode of power or heating current (I_H) as the power used in the test environment conditions. However, this method also allows for a dc forward heating current (I_H) power source often used in thermal resistance test methods to provide equivalent rms power.

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5.5 Sample-and-hold tester. For method B, a sample-and-hold tester for recording a sequential set of TSP measurements at operating currents in the same vicinity as the test environment operating current is required such as a Frothingham VF40, or equivalent, with the approval of the quality activity. The test pulses shall be kept narrow and widely spaced where additional heating of the junction will be insignificant.

5.6 Voltage and current measurements. In method B, a voltmeter and current meter shall be used to accurately measure the expected voltage and current levels in the test.

5.7 Thermocouple. A small bare-wire thermocouple of 36 AWG is required for ACOL evaluation.

6. Procedure for method A. This method uses a selected low measuring current for the TSP that does not cause significant self-heating (similar to thermal resistance test methods). The DUTs are a sample of serialized devices where the TSP is initially recorded at the desired temperature. They shall also be of the same construction as other devices in the test environment and be of sufficient quantity to provide a good sample for averaging. Unless otherwise specified, this shall be a minimum of five devices.

6.1 TSP measurement. First determine the nominal T_J desired for the burn-in or life-test. For military burn-in screening, the minimum T_J shall be specified by the applicable spec sheet. The maximum T_J is the rating for the DUT unless otherwise specified.

6.1.1 Desired T_J. In a separate temperature controlled chamber, bath, or hot-plate environment, the nominal T_J desired for the burn-in or life-test will initially be established within plus or minus 2°C (or as required) for recording the TSP. Additional T_J tolerance considerations are also noted in 6.3.3.

6.1.2 Recording TSP. After the DUTs have been introduced and brought to thermal equilibrium, the TSP shall be recorded in a serialized manner at a low steady-state measuring current (I_M) for method A. This would be the forward voltage of a diode (V_F) or base emitter voltage (V_{BE}) of a transistor. The magnitude of I_M shall be large enough to ensure the V_F or V_{BE} is turned on, but not large enough to cause significant self heating. For transistors, it is optimum to remove any bias voltage to the collector that generates current gain affecting I_M. However some thermal resistance equipment requires use of a collector voltage for a V_{BE} measurement. If so, that same test condition shall be used for measuring the TSP in burn-in as described in 6.3.2 and 6.4.1.e.

6.2 Test environment mounting.

6.2.1 Verifing T_J. The sample DUTs shall then be mounted in the test environment using sockets strategically located representing the coolest and hottest regions to verify T_J. This shall also include all other devices intended for the power test environment to duplicate the same cumulative heating effects. Those sockets used for the DUTs shall also be the same design as all others in the test environment. The DUTs shall also be electrically connected to the TSP measuring equipment that requires a set of Kelvin-sense leads to monitor junction voltage. The leads shall be attached so as to minimize heat sinking. Also see 6.5 on further ACOL considerations.

6.3 Test environment measurement.

6.3.1 Ambient temperature. The ambient temperature (T_A) shall be as specified at thermal equilibrium conditions including any convection or circulating air effects in an oven chamber where applicable. For hot-plate applications, the surface temperature and uniformity shall also be as specified to achieve desired case temperature (T_C) control as stated in 6.1.1 and 6.4.1.c.

6.3.2 Appling current or power. The same heating current (or equivalent rms power) shall be applied in increasing increments for all devices while sampling for TSP on each DUT with a low duty factor at I_M in accordance with equipment description in 5.4. Working with each serialized DUT one at a time, monitor the junction voltage TSP at I_M while slowly increasing the heating current. The TSP will decline with increasing T_J for V_F or V_{BE}.

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6.3.3 TSP for the desired T_J. 6.3.1 and 6.3.2 shall be repeated until the same TSP is achieved for the desired T_J in step 6.1.2 on the sample DUTs after the same equivalent current or rms power is applied for all devices in the test environment. The power applied for this desired T_J level for each DUT shall be recorded. The average power for the DUTs shall also be determined and used as the value thereafter for applied power per unit during burn-in or life-test in 6.3.4. If thermal resistance from junction to ambient ($R_{\theta JA}$) is desired for future reference as described in 10.2, the T_A should also be recorded at this time.

NOTE: The T_J is also selected based on overall tolerances of the test environment. Also see 10.3 and equation 9 for slight T_J variations with the averaging effects of applied power above. For worst-case tolerances, the T_J should be placed nominally at the midpoint between the minimum and maximum allowed T_J required for the test environment. For example, this may be 155°C if the minimum is 135°C and maximum is 175°C. If either the applied heating power (P_H) or the desired T_J exceeds the DUT ratings, see steps 6.3.3.1 and 6.3.3.2. If not, proceed to 6.3.4.

6.3.3.1 Current and power ratings. If applied heating current or power P_H exceeds the rating of the device for burn-in screening to achieve the desired T_J, the following options apply:

a. The heat sinking may be reduced in the test environment.

b. The T_A may be increased until the desired T_J is achieved when allowed in the applicable specification sheet.

c. The current or power may be increased not to exceed the current density capability of the device.

6.3.3.2 T_J for JANS. The T_J may be higher than typical device ratings of 150°C to 200°C when applied to JANS life-test of MIL-PRF-19500 for a faster accelerated test environment. These may be specified at T_J values of 225°C to 275°C. However, these options shall not exceed temperatures where the DUTs (and remaining devices) cannot operate effectively as a semiconductor in the test environment. This may also be identified as the intrinsic or secondary breakdown region (thermal generation of electron-hole pairs starts approaching or exceeding the background doping levels of the PN junctions). This may also be observed by significant increases in reverse leakage current, or in more severe cases, the decline (or collapse) of reverse breakdown voltage (V_{BR}) on rectifiers, V_Z for higher voltage zeners, or V_{CE} for transistors. Also see note in 6.4.1.b for rectifiers.

6.3.4 Criteria once T_J is achieved. After the desired T_J is achieved for all devices, the burn-in or life-test may proceed with the average power per unit in 6.3.3 until completed for the required number of hours.

6.4 Power requirements. It is desirable to apply the same type of rms heating power required for the test environment in 6.3 for each DUT as applied to all other devices before switching to the I_M level for measuring the TSP. However power supply equipment for thermal resistance test methods using dc forward heating current (I_H) and a low duty factor sample-and-hold method at I_M for the TSP may not offer that added flexibility. In such cases, the same equivalent rms P_H may be used with a forward-heating current (I_H) as described in thermal resistance test methods where $P_H = I_H \times V_H$. When equivalent rms heating power is in question, the duplication of lead, case, or end-cap temperatures (T_L, T_C or T_{EC}) is required to verify identical rms power as described in 6.5 for ACOL considerations.

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6.4.1 Test environment and DUT power options

a. Signal and Schottky diodes (dc burn-in with I_F): The required heating power is forward dc current (I_F) multiplied times the forward voltage (V_F) observed during the dc burn-in or life-test (or $P_H = I_F \times V_F$). No equipment handicaps should exist with this test environment since I_F equates to the forward heating current (I_H) for thermal resistance test methods.

b. Rectifiers (ACOL burn-in with I_O): The required ac operating life at rated I_O may be approximated in equivalent rms heating power by $P_H = I_O\ (0.107 + 0.785\ V_{FM})$ where V_{FM} is the peak forward voltage observed during the half-sine wave and I_O is the rated average rectified output current for 50 Hz or 60 Hz sine-wave input and a 180 degree conduction angle (see JESD282). With this definition, the peak forward current in each half-sine wave is $3.14 \times I_O$. This P_H also assumes the power in the reverse direction is negligible due to leakage current (I_R) and applied reverse voltage (V_{RRM}) as defined in JESD282 or test method 1038 of MIL-STD-750.

   For equipment limitations to measure TSP, the DUT samples may also use the same effective forward power where P_H is the forward heating current (I_H) multiplied times the forward heating voltage (V_H) as described in 6.4. The same effective power with ACOL may be verified with identical T_L, T_C, or T_{EC}. See 6.5 to measure T_L, T_C, or T_{EC}. Also see background information in 9.3 for the correlation of RMS power with T_L, T_C, or T_{EC}.

   NOTE: A reverse power loss may not be observed if limiting resistors have externally absorbed the intended reverse voltage (V_{RRM}) in an ACOL test environment due to high leakage currents (I_R x R voltage drop), or due to collapsing voltage as described in 6.3.3.2. The required V_{RRM} shall be sample monitored to verify it has been successfully applied where applicable to all the other remaining rectifier devices under ACOL power. Limiting or ballast resistors are often used in series with each device that are then placed in parallel array connections with typical power supplies for burn-in or life-test methods. This regulates I_O or limits excessive current flow if a device electrically degrades or shorts to allow continued burn-in or life-testing of remaining devices for the period of time required.

c. Schottky (HTRB burn-in with I_R): To minimize high power and burn-in current levels, the required P_H is applied as an HTRB with reverse voltage (V_R) and selected range of reverse current (I_R) for all devices at elevated temperature. At low power where there is no significant self heating, the T_C may be assumed the same value as T_J. In this example, the $P_H = I_R \times V_R$ where I_R is increased at elevated temperature. For test equipment options, the DUT sample may also use the equivalent forward rms power (P_H) as described in 6.4. Where applicable, the T_C may simply be measured directly for the T_J equivalent as described in 8.

d. Zeners (dc burn-in with I_Z): The required P_H is the zener burn-in current (I_Z) multiplied times the nominal zener voltage (V_Z) where $P_H = I_Z \times V_Z$. The V_Z is also adjusted for the expected T_J using the rated temperature coefficient of the zener (α_{VZ}). For equipment limitations, the DUT sample may use the equivalent forward rms power (P_H) as described in 6.4.

e. Transistors (dc burn-in with I_C): The required heating power is the collector current (I_C) multiplied times the collector emitter voltage (V_{CE}) during the dc burn-in or life-test plus any significant base current (I_B) multiplied times base emitter voltage (V_{BE}) where $P_H = I_C \times V_{CE} + I_B \times V_{BE}$. Typically the $I_B \times V_{BE}$ power may be negligible. The low duty factor sample measurement for the TSP shall be with the same conditions as in 6.1.2.

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6.5 ACOL considerations (rectifiers). If the parts for burn-in or life-test are to receive ACOL conditions, an additional step shall be added after 6.2.1 to ensure equivalent heating and T_J to the DUT samples.

6.5.1 Thermocouple mounting. When the voltage monitoring leads are being attached to the DUTs for testing in the burn-in configuration in 6.2.1, also solder on a fine 36 AWG bare wire thermocouple to each of them. The thermocouple should be mounted at zero distance from the body of the part. The thermocouple shall be mounted to not interfere when the DUT is placed in the burn-in or life-test fixtures.

6.5.2 Thermocouple usage. Also solder a thermocouple as described in 6.5.1 to the nearest device of each DUT location that receives ACOL power in the test environment.

6.5.3 Thermocouple temperature. As each of the serialized DUT parts are set to the desired T_J using the dc current method in the burn-in or life-test environment, also record the thermocouple temperature reading. These thermocouple readings are then used to set the ac power levels in 6.5.4.

6.5.4 Average T_J. Apply power to heat the remaining diodes using the required ACOL while monitoring the thermocouple temperature. Increase the ac power input until the thermocouple in 6.5.2 reaches the temperature level of the DUTs in 6.5.3 at the desired T_J. Record the ACOL power conditions applied for each device described in 6.5.2. These values are then averaged for determining ACOL power applied for all devices. This process guarantees that all the devices will be tested at the required average T_J for burn-in or life-test. Also see 9.3 for further background information.

NOTE: The rectifier diode with the lowest V_F or the lowest ambient temperature (T_A) position in the test environment would require the greatest power for a given thermocouple reading to ensure the same T_J is achieved.

7. Procedure for method B. This method uses a sequential set of current pulses to characterize the TSP at the T_J in the same operating current region expected for the burn-in or life-test environment. The DUTs are a sample of devices where the TSP is recorded at the desired temperature. They shall also be of the same construction as other devices in the test environment and shall be of sufficient quantity to provide a good sample for averaging. Unless otherwise specified, this shall be a minimum of five devices.

7.1 TSP measurement. First determine the nominal T_J desired for the burn-in or life-test. For military burn-in screening, the minimum T_J shall be specified by the applicable specification sheet. The maximum T_J is the rating for the DUT unless otherwise specified.

7.1.1 Desired T_J. In a separate temperature controlled chamber, bath, or hot-plate environment, the nominal T_J desired for the burn-in or life-test will initially be established within ± 2°C (or as required) for recording the TSP. Additional T_J tolerance considerations are also noted in 7.3.3.

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7.1.2 Recording TSP measurements. A sample-and-hold tester shall be programmed for recording a sequential set of TSP measurements at operating currents in the same vicinity as anticipated for the test environment. This will perform incremental pulse V_F-I_F, V_Z-I_Z, or V_{BE}-I_{CE} tests.

a. Choose the incremental current range so that the recorded values will be centered near the current level that is expected for the burn-in or life-test environment.

b. Program the sample-and-hold test equipment to record junction TSP voltage readings with a sufficiently low duty factor that will not warm the DUT when taking sequential readings. Typical test parameters for a leaded switching diode may be as follows:

(1) 0.5 ms pulse width.

(2) 1 second wait interval.

(3) 500 mA starting level for I_F.

(4) 20 steps at 5 mA increasing increments.

NOTE: The smaller the incremental steps, the more accurate the chart will be when correlating to values taken in burn-in or life-test. Since this test is performed with a low duty factor power and thermally stable parts, any holding fixture may be used, but Kelvin leads are required.

7.1.3 Data. After the DUTs have been introduced and brought to thermal equilibrium, the TSP shall be recorded in a serialized manner by cycling each part through the expected current range and printing out the data for each identified device. Each set of data is applicable only for that particular serialized part and T_J.

7.2 Test environment mounting.

7.2.1 Verify T_J. The sample DUTs shall then be mounted in the test environment using sockets strategically located representing the coolest and hottest regions to verify T_J. All other devices intended for burn-in or life-test shall also be mounted in the test environment to duplicate the same cumulative heating effects. Those sockets used for the DUTs shall also be the same design as all others in the test environment. The DUTS shall also be electrically connected to the TSP measuring equipment that requires a set of Kelvin sense leads to monitor junction voltage. These leads shall be attached so as to minimize heat sinking. Also see 7.4 for ACOL considerations.

7.3 Test environment measurement.

7.3.1 Thermal equilibrium. The ambient temperature (T_A) shall be as specified at thermal equilibrium conditions including any convection or circulating air effects in an oven chamber where applicable.

7.3.2 Desired level. A common heating current shall be applied in increasing increments for all devices while sampling for TSP on each DUT. Working with each serialized DUT one at a time, monitor the junction voltage TSP while slowly varying the common junction current. When the DUT being monitored is at thermal equilibrium where both its current and voltage readings match a set of readings on the chart taken in 7.1.3, the T_J of that DUT is known to be at the desired level. This is graphically displayed on figure 3100-1. For accuracy, the voltage readings should optimally use the same test equipment that can record in both a sample-and-hold mode in 7.1.3 and continuously in 7.3.2.

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7.3.3 Desired T_J. Paragraph 7.3.2 shall be repeated until both the current and voltage readings match a set of corresponding readings for the desired T_J level on each serialized DUT after the same equivalent rms power is applied for all devices in the test environment. The power applied for this desired T_J level for each DUT shall be recorded. The average power for the DUTs shall also be determined and used as the value thereafter for applied power per unit during burn-in or life-test in 7.3.4. If the thermal resistance from junction to ambient $R_{\theta JA}$ is desired for later reference as indicated in 10.2, the T_A should also be recorded.

NOTE: The T_J is also selected based on overall tolerances of the test environment. Also see 10.3 and equation 9 for slight T_J variations with the averaging effects of applied power above. For worst case tolerances, the T_J should be placed nominally at the midpoint between the minimum and maximum allowed T_J required for the test environment. For example, this may be 155°C if the minimum is 135°C and maximum is 175°C. If either the applied heating power (P_H) or the desired T_J exceeds the DUT ratings, see 7.3.3.1 and 7.3.3.2. If not, proceed to 7.3.4.

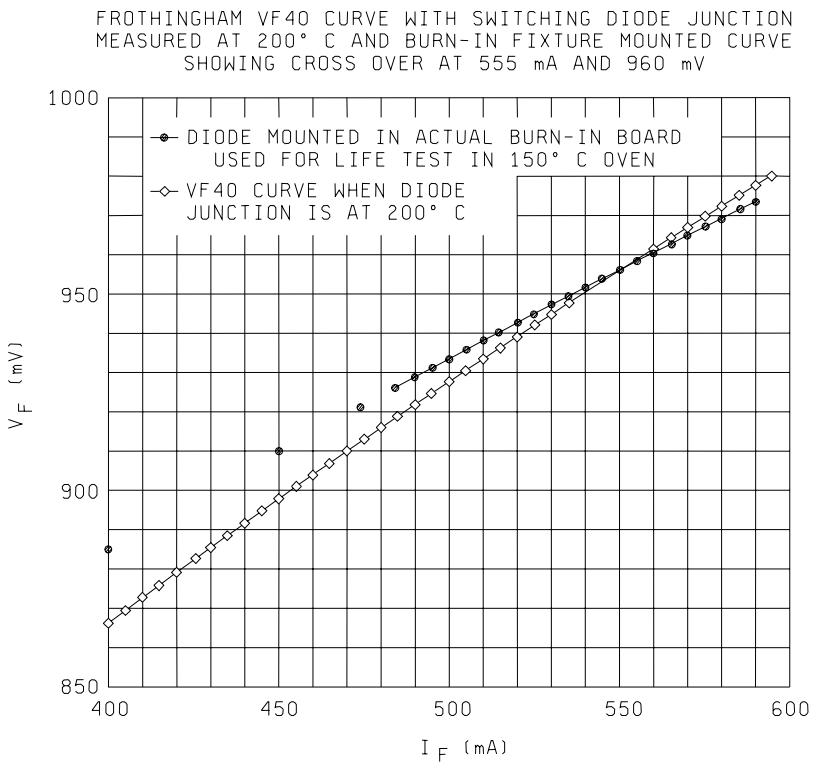

FIGURE 3100-1. Frothingham VF40 curve.

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7.3.3.1 Power rating. If the applied heating power (P_H) exceeds the rating of the device for burn-in screening to achieve the desired T_J, the following options apply:

a. The heat sinking may be reduced in the test environment.

b. The T_A may be increased until the desired T_J is achieved when allowed by the applicable specification sheet.

c. The current or power may be increased not to exceed the current density capability of the device.

7.3.3.2 T_J for JANS. The T_J may be higher than typical device ratings of 150°C to 200°C when applied to JANS life-test in groups B, C, and E of MIL-PRF-19500 for a faster accelerated test environment. These may be specified at T_J values of 225°C to 275°C. However, these options shall not exceed temperatures where the DUTs (and remaining devices) cannot operate effectively as a semiconductor in the test environment. This may also be identified as the intrinsic or secondary breakdown region (thermal generation of electron-hole pairs starts approaching or exceeding the background doping levels of the PN junctions). This may also be observed by significant increases in reverse leakage current, or in more severe cases, the decline (or collapse) of reverse breakdown voltage (V_{BR}) on rectifiers, V_Z for higher voltage zeners, or V_{CE} for transistors. Also see note in 6.4.1.b for rectifiers.

7.3.4 Desired T_J After the desired T_J is achieved for all devices, the burn-in or life-test may proceed with the average power per unit in 7.3.3 until completed for the required number of hours.

7.4 ACOL considerations (rectifiers). If the sample-and-hold test equipment is equipped with synchronized test capabilities for measuring the TSP voltage in the desired forward conducting half-cycle region for ACOL operation, this can again be tested in a similar manner described in 7.3. As described in 7.3.2, this should optimally be provided with the same voltage test equipment. For synchronized capabilities, a Frothingham model VF40DB or equivalent may be used. If a synchronized test capability is not available, alternative steps shall be added after 7.2.1 to ensure equivalent heating and T_J to the DUT samples. These are described in 7.4.1 through 7.4.4.

7.4.1 Thermocouple mounting. When the voltage monitoring leads are being attached to the DUTs for testing in the burn-in configuration in 7.2, also solder on a fine 36 AWG bare wire thermocouple to each of them. The thermocouple should be mounted at zero inch distance from the body of the part. The thermocouple will have to be mounted to not interfere when the DUT is placed in the burn-in or life-test fixtures.

7.4.2 Thermocouple usage. Also solder a thermocouple as described in 7.4.1 to the nearest device of each DUT location that receives ACOL power in the test environment.

7.4.3 Thermocouple temperature. As each of the serialized DUT parts is set to the desired T_J using the dc current method in the ACOL test environment, also record the thermocouple temperature reading. These thermocouple readings are then used to set the ac power levels in 7.4.4.

7.4.4 Average T_J. Apply power to heat the remaining diodes using the required ACOL while monitoring the thermocouple temperature. Increase the ac power input until the thermocouple in 7.4.2 reaches the temperature level of the DUT in 7.4.3 at the desired T_J. Record the ACOL power conditions applied for each device described in 7.4.2. These values are then averaged for determining ACOL power applied for all devices. This process guarantees that all the devices will be tested at the required average T_J for burn-in or life-test. Also see 9.3 for further background information.

NOTE: The rectifier diode with the lowest V_F or the lowest ambient temperature (T_A) position in the test environment would require the greatest power for a given thermocouple reading to ensure the same T_J is achieved.

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8. Procedure for method C. This method only applies to case mounted power devices where the operating power or current region expected for the burn-in or life-test environment is still well below that of the rating of the device. In these examples, the T_J of the device is not significantly higher than the case temperature T_C. This operating feature and direct measurement of case temperature may be used to confirm the minimum required T_J is met for the burn-in or life-test environment.

9. Background information.

9.1 Equations for T_J, T_A, P_H, and $R_{\theta JA}$. The observed values of the T_J rise above T_A in the test environment would be the product of effective rms heating power (P_H) multiplied times the total effects of component thermal resistance from junction to ambient ($R_{\theta JA}$)…
This may also be stated as follows:

$$T_J = T_A + P_H \times R_{\theta JA} \qquad \text{Equation 1}$$

The T_A is the ambient temperature in the immediate vicinity of an open burn-in rack or the ambient inside a convection oven chamber for life-test. If T_A is recorded at 6.3.3 or 7.3.3, then the $R_{\theta JA}$ can also be determined as follows:

$$R_{\theta JA} = (T_J - T_A)/P_H \qquad \text{Equation 2}$$

9.2 Thermal resistance definitions for $R_{\theta JL}$, $R_{\theta JC}$, $R_{\theta JEC}$, $R_{\theta LA}$, $R_{\theta CA}$, and $R_{\theta ECA}$. The thermal resistance ($R_{\theta JA}$) is the total of the DUT thermal resistance junction to lead or case ($R_{\theta JL}$ or $R_{\theta JC}$), and the thermal resistance of the test environment from lead or case (test socket) to ambient ($R_{\theta LA}$ or $R_{\theta CA}$). For example:

$$R_{\theta JA} = R_{\theta JL} + R_{\theta LA}$$
$$\text{or} \quad R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

This also applies to surface mount devices that may use an end-cap- reference rather than case. In this example:

$$R_{\theta JA} = R_{\theta JEC} + R_{\theta ECA}$$

The T_J in each of these examples can be determined as follows:

$$T_J = T_A + P_H \times (R_{\theta JL} + R_{\theta LA}) = T_L + P_H \times R_{\theta JL} \qquad \text{Equation 3}$$
$$T_J = T_A + P_H \times (R_{\theta JC} + R_{\theta CA}) = T_C + P_H \times R_{\theta JC} \qquad \text{Equation 4}$$
$$T_J = T_A + P_H \times (R_{\theta JEC} + R_{\theta ECA}) = T_{EC} + P_H \times R_{\theta JEC} \qquad \text{Equation 5}$$

Earlier methods have also determined T_J based on these relations that use thermal resistance of the component and also the reference point temperature (T_L, T_C, T_{EC}) measured in the test environment with applied power (P_H). Possible sources of error included the use of maximum rated thermal resistance rather than actual value (see note), nonlinear features affecting thermal resistance or K factor at notably higher temperatures during life-test and difficulty in measuring reference temperature (T_L, T_C, T_{EC}) particularly for enclosed convection air ovens.

NOTE: For accurate determination of T_J, this requires the actual component thermal resistance value rather than the maximum rating. This distinction is important to ensure adequate T_J values are achieved in 6.3.3 or 7.3.3.

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9.3 Correlation of RMS power with T_L, T_C, or T_{EC}. The lead, case, or end-cap temperature reference points within the test environment are as follows:

$$T_L = T_A + P_H \times R_{\theta LA} \qquad \text{Equation 6}$$
$$T_C = T_A + P_H \times R_{\theta CA} \qquad \text{Equation 7}$$
$$T_{EC} = T_A + P_H \times R_{\theta ECA} \qquad \text{Equation 8}$$

If the T_L, T_C, or T_{EC} is the same between any two devices in identical test environment conditions for ambient temperature and thermal resistance of the test socket from component to ambient, then the effective rms power shall be the same between them as may be observed in Equation 6, 7, and 8. This feature may be used to advantage in determining equivalent P_H levels in different power modes as described in 6.5 and 7.4. Also when the same equivalent heating power levels are applied to devices of identical design with the same thermal resistance at the same T_L, T_C, or T_{EC}, then the same T_J is achieved as shown in Equation 3, 4, and 5.

10. Summary.

10.1 Repeatable T_J values. This procedure may not require repeating for every lot processed for burn-in and life-test if this method verifies the same T_J values (within acceptable tolerances) for thermally identical test environments and devices to be tested as demonstrated in 9.1 and Equation 1. This would occur in a test environment with the same T_A and heat-sinking effects ($R_{\theta LA}$, $R_{\theta CA}$, or $R_{\theta ECA}$), as well as components of the same thermal resistance ($R_{\theta JL}$, $R_{\theta JC}$, or $R_{\theta JEC}$). These conditions provide the same effective $R_{\theta JA}$ and the same T_J values as demonstrated in 9.2. The value of $R_{\theta JA}$ is determined in 10.2.

10.2 The effective thermal resistance. $R_{\theta JA}$ for the test environment can be determined for the devices or DUTs with the P_H recorded at 6.3.3 or 7.3.3 with ambient temperature (T_A) and junction temperature (T_J) with Equation 2 in 9.1. The $R_{\theta JA}$ for identical test environments and products can then be used to advantage for determining other desired T_J values when needed at applied power levels P_H or ambient temperature (T_A) conditions.

10.3 Average power. When an individual (average) power level P_H is selected for the test environment in 6.3.3 or 7.3.3, small variations in power ΔP_H to this average will exist over the sample number of DUTs to achieve the same TSP or T_J. As a result, slight variations in ΔT_J will also occur for continuing the burn-in or life-test in 6.3.4 or 7.3.4 with typical power supplies and wiring harnesses. This ΔT_J may also be determined from Equation 1 as shown below in Equation 9.

$$\Delta T_J = T_A + \Delta P_H \times R_{\theta JA} \qquad \text{Equation 9}$$

This added consideration for T_J tolerances in 6.3.3 or 7.3.3 is of interest since the same operating current or power condition is applied to all devices for continuing burn-in or life-test in 6.3.4 or 7.3.4 with typical power supplies and wiring harnesses. These slight T_J variations may be from small variations in socket and component thermal resistance. It may also be from notable variations in ambient temperature in the immediate vicinity of each DUT placed at different locations in the test environment.

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METHOD 3101.4

THERMAL IMPEDANCE (RESPONSE) TESTING OF DIODES

1. Purpose. The purpose of this test is to determine the thermal performance of diode devices. This can be done in two ways, steady-state thermal impedance or transient thermal impedance testing. Steady-state thermal impedance (referred to as thermal resistance) determines the overall thermal performance of devices. A production oriented screening process, referred to as thermal transient testing, is a subset of thermal impedance testing and determines the ability of the diode chip-to-header interface to transfer heat from the chip to the header, and is a measure of the thermal quality of the die attachment. It is relevant to designs which use headers, or heat conducting plugs, with mass and thermal conductivity allowing effective discrimination of poor die attachments. This is particularly true with power devices. The method can be applied to rectifier diodes, transient voltage suppressors, power zener diodes, and some zener, signal, and switching diodes. This method is intended for production monitoring, incoming inspection, and pre-burn in screening applications. Some zener constructions, particularly when used with small junction area designs, cool too rapidly (from a heating current) to provide accurate measurement when forward (diode) current is used for this test. For such devices, a method is provided to apply currents in the zener direction and make a measurement much closer to the termination of the heating current. In this way, no minority carriers are involved and inductive effects are minimized due to lower test current. This may be considered a lab measurement because cable lengths in an ATE may prevent accurate measurements so close to cessation of the heating current. This laboratory method is intended on initial zener device design verification for correlation to forward direction thermal impedance testing (such as with an ATE) prior to establishing a production test limit. Correlation assurance shall be provided in the forward production monitoring that thermal impedance in the reverse direction (zener) shall not exceed the specified limit. If this zener test method exceeds the forward method by 10 percent or more, production monitoring (with an ATE in the forward direction) will require a lower limit, for some devices, than that required by the more accurate lab method (see 5.1).

1.1 Background and scope for thermal transient testing. Steady-state thermal impedance and transient thermal impedance of semiconductor devices are sensitive to the presence of these voids in the die attachment material between the semiconductor chip and package since voids impede the flow of heat from the chip to the substrate (package). Due to the difference in the thermal time constants of the chip and package, the measurement of transient thermal response can be made more sensitive to the presence of voids than can the measurement of steady-state thermal response. This is because the chip thermal time constant is generally several orders of magnitude shorter than that of the package. Thus, the heating power pulse width can be selected so that only the chip and the chip-to-substrate interface are heated during the pulse by using a pulse width somewhat greater than the chip thermal time constant but less than that of the substrate. Heating power pulse widths ranging from 1 to 400 ms for various package designs have been found to satisfy this criterion. This enables the detection of voids to be greatly enhanced, with the added advantage of not having to heat sink the DUT. Thus, the transient thermal impedance or thermal response techniques are less time consuming than the measurement of thermal resistance for use as a manufacturing screen, process control, or incoming inspection measure for die attachment integrity evaluation.

2. Symbols and definitions. The following symbols and terminology shall apply for the purpose of this test method in the forward direction: (When using the zener method, see below):

a. ΔT_J: The change in T_J caused by the application of P_H for a time equal to t_H.

b. ΔV_F The change in the TSP, V_F, due to the application of (P_H) to the DUT.

c. CU: The comparison unit, consisting of ΔV_F divided by V_H, that is used to normalize the transient thermal response for variations in power dissipation; in units of mV/V.

d. I_H: The current applied to the DUT during the heating time in order to cause power dissipation.

e. I_M: The measurement current used to forward bias the temperature sensing diode junction for measurement of V_F. NOTE: When using the zener, delete forward and use zener bias.

f. K: Thermal calibration factor equal to the reciprocal of VTC; in °C/mV.

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g. P_H: The (P_H) pulse magnitude; product of V_H and I_H.

h. $R_{\theta JX}$: Thermal resistance from device junction to a defined reference point; in units of °C/W.

$R_{\theta JC}$: Thermal resistance from device junction to a point on the outside surface of the case immediately adjacent to the device chip; in units of °C/W.

$R_{\theta JA}$: Thermal resistance from device junction to an ambient (world); in units of °C/W.

i. t_H: The duration of P_H applied to the DUT.

j. T_J: The DUT junction temperature.

k. t_{MD}: Measurement delay time is defined as the time from the start of (P_H) removal to the start of the final V_F measurement time, referred to as t_{SW}.

l. TSP: The temperature sensitive parameter of V_F or V_Z.

m. t_{SW}: Sample window time during which final V_F measurement is made. The value of t_{SW} should be small; it can approach zero if an oscilloscope is used for manual measurements.

n. V_F: The forward biased junction voltage of the DUT used for junction temperature sensing. NOTE: When using the zener method, delete forward and use zener bias.
V_{Fi}: The initial V_F value before application of heating power(P_H).
V_{Ff}: The final V_F value after application of (P_H).

o. V_H: The heating voltage resulting from the application of I_H to the DUT.

p. VTC: Voltage-temperature coefficient of V_F with respect to T_J at a fixed value of I_M; in mV/°C.

q. V_Z: The zener voltage. (See note (1) below.)

r. $Z_{\theta JC}$: Thermal impedance from device junction to a point on the outside surface of the case immediately adjacent to the device chip measured using time equal time constant of device; in units of °C/W.

s. $Z_{\theta JX}$: Thermal impedance from device junction to a time defined reference point; in units of °C/W.

NOTES: (1) When using the zener method, the following changes shall further apply to the definitions whenever they appear in the text.

Letter symbols: I_F becomes I_Z
V_F becomes V_{ZL}
V_H becomes V_{ZH}
V_{Fi} becomes V_{ZLi}
V_{Ff} becomes V_{ZLf}
ΔV_F becomes ΔV_{ZL}
Wording: forward bias becomes reverse bias.

(2) ΔV_F, K, and CU parameter values will be substantially different when using the zener method (as compared to the forward biased method). Some difference will be observed between zeners with different nominal voltages.

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3. Apparatus. The apparatus required for this test shall include the following, configured as shown on figure 3101-1, as applicable to the specified test procedure:

a. A constant current source capable of adjustment to the desired value of I_H and able to supply the V_H value required by the DUT. The current source should be able to maintain the desired current to within ±2 percent during the entire length of heating time.

b. A constant current source to supply I_M with sufficient voltage compliance to turn the TSP junction fully on.

c. An electronic switch capable of switching between the heating period conditions and measurement conditions in a time frame short enough to avoid DUT cooling during the transition; this typically requires switching in the microsecond or tens of microseconds range.

d. A voltage measurement circuit capable of accurately making the V_{Ff} measurement within the time frame with millivolt resolution.

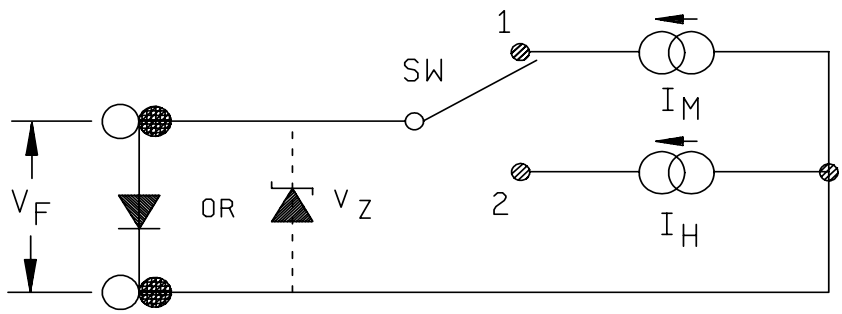

FIGURE 3101-1. Thermal impedance testing setup for diodes.

4. Test operation.

4.1 General description. The test begins with the adjustment of I_M and I_H to the desired values. The value of I_H is usually at least 50 times greater than the value of I_M. Then with the electronic switch in position 1, the value of V_{Fi} is measured. The switch is then moved to position 2 for a length of time equal to t_H and the value of V_H is measured. Finally, at the conclusion of t_H, the switch is again moved to position 1 and the V_{Ff} value is measured within a time period defined by t_{MD} (or $t_{MD} + t_{SW}$, depending on the definitions stated previously). The two current sources are then turned off at the completion of the test. (See figures 3101-2a and 3101-2b.)

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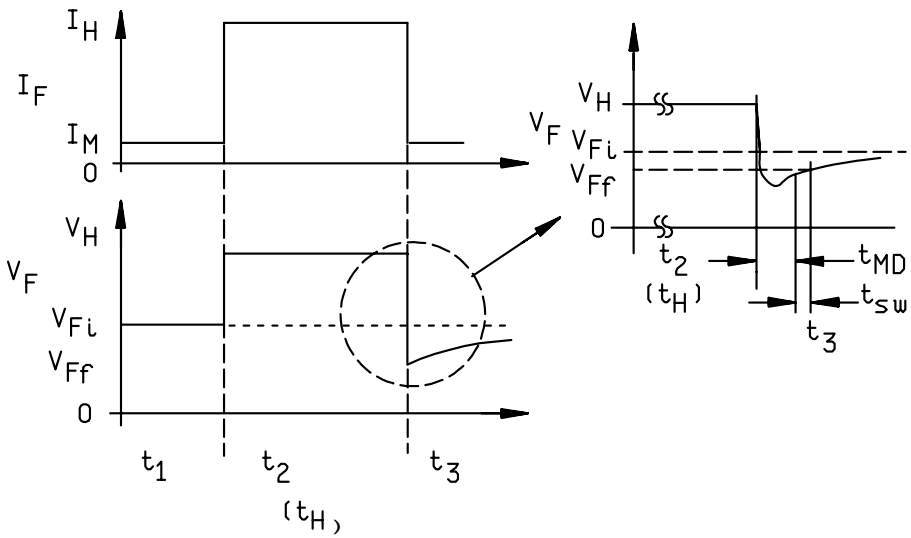
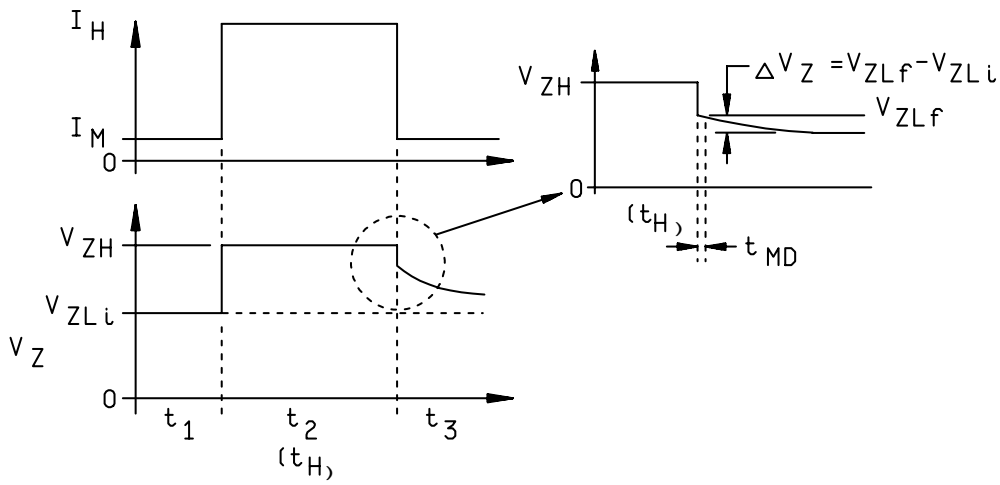


Forward biased method

FIGURE 3101-2a. Thermal impedance testing waveforms.



Zener biased method

FIGURE 3101-2b. Thermal impedance testing waveforms.

4.2 Notes.

a. Some test equipment may provide a ΔV_F directly instead of V_{Fi} and V_{Ff}; this is an acceptable alternative. Record the value of ΔV_F.

b. Some test equipment may provide $Z_{\theta JX}$ directly instead of V_{Fi} and V_{Ff} for thermal resistance calculations; this is an acceptable alternative. Record the value of $Z_{\theta JX}$.

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c. Alternative waveforms, as may be generated by ATE using the general principles of this method, may be used upon approval of the qualifying activity.

d. The zener biased method in figure 3101-2b illustrates a positive TSP when the zener is in avalanche breakdown. It is also possible to portray a negative TSP for low voltage zeners when they are in the field emission or tunneling mode. A near zero TSP can also result from these two off-setting factors of a specific operating current that shall be avoided by changing to a higher or lower current. Also see 6 herein for TSP.

5. Acceptance limit.

5.1 General discussion. Variations in diode characteristics from one manufacturer to another cause difficulty in establishing a single acceptance limit for all diodes tested to a given specification sheet. Ideally, a single acceptance limit value for ΔV_F would be the simplest approach. However, different design, materials, and processes can alter the resultant ΔV_F value for a given set of test conditions. Listed below are several different approaches to defining acceptance limits. The ΔV_F limit is the simplest approach and is usually selected for screening purposes. Paragraphs 5.3 through 5.6 require increasingly greater detail or effort. In some examples, absolute thermal impedance limits are required for correlation to surge performance such as for zeners. In such examples, setting a limit for zener diode construction with the forward biased (the usual ATE) method requires prior evaluation of $Z_{\theta JX}$ (and $R_{\theta JX}$, when desired) by the zener biased method. If the zener method result is more than 10 percent higher, the limit shall be based on the more accurate zener biased measurement. In such a case, if it is desired to use the forward biased method, the limit (of ΔV_F, $Z_{\theta JX}$, or $R_{\theta JX}$) shall be reduced by the extent (percentage) difference between the two methods.

5.2 ΔV_F limit. A single ΔV_F limit is practical if the K factor and V_H values for all diodes tested to a given specification sheet are nearly identical. Since these values may be different for different manufacturers, the use of different limits is likely to more accurately achieve the desired intent. (A lower limit does not indicate a better die bond when comparing different product sources.) The diode specification sheet would list the following test conditions and measurement parameters:

a. I_H (in A).

b. t_H (in ms).

c. I_M (in mA).

d. t_{MD} (in μs).

e. t_{SW} (in μs).

f. ΔV_F (maximum limit value, in mV).

5.3 ΔT_J limit. (Much more involved than ΔV , but useful for examining questionable devices.) Since ΔT_J is the product of K (in accordance with 6 herein) and ΔV_F, this approach is the same as defining a maximum acceptable T_J rise for a given set of test conditions.

5.4 CU limit. (Slightly more involved than ΔT_J.) The ΔT_J limit approach described above does not take into account potential power dissipation variations between devices. The V_H value can vary, depending on chip design and size, thus causing the power dissipation during the heating time to be different from device to device. This variation will be small within a lot of devices produced by a single manufacturer but may be large between manufacturers. A CU limit value takes into account variations in power dissipation due to differences in V_H by dividing the ΔV_F value by V_H.

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5.5 (K•CU) limit. (Slightly more involved but provides greater detail.) This is a combinational approach that takes into account both K factor and power dissipation variations between devices.

5.6 $Z_{\theta JX}$ limit. (For full characterization; not required for screening purposes, but preferred if the proper ATE is available.) The thermal impedance approach uses an absolute magnitude value specification that overcomes the problems associated with the other approaches. Thermal impedance is time dependent and is calculated as follows:

$$Z_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_F)}{(I_H)(V_H)} \right| \text{°C/W}$$

5.7 $R_{\theta JX}$ limit. (For thermal resistance specification testing.) The thermal resistance to some defined point, such as the case ($R_{\theta JC}$), lead ($R_{\theta JL}$), or end cap ($R_{\theta JEC}$), is an absolute magnitude value specification used for equilibrium conditions. The t_H heating time shall therefore be extended to longer times (typically 20 to 50 seconds). In the example of $R_{\theta JC}$, $R_{\theta JL}$, or $R_{\theta JEC}$ measurements, the case, lead or end cap reference points shall be carefully stabilized and monitored in temperature which requires an infinite heat sink or careful monitoring for optimum results. The ΔT_J in the equation below is the difference in T_J to the case, lead, or end cap reference temperature as applicable by package type.

$$R_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_F)}{(I_H)(V_H)} \right| \text{°C/W}$$

NOTE: Some automated test equipment designed primarily for thermal impedance testing with short heating times (t_H) may not include capabilities of controlling or monitoring these reference temperatures for an accurate thermal resistance test measurement at long heating times. Also see method 4081, MIL-STD-750 for further details on testing thermal resistance of diodes.

5.8 General comment for thermal transient testing. One potential problem in using the thermal transient testing approach lies in trying to make accurate enough measurements with sufficient resolution to distinguish between acceptable and nonacceptable diodes. As the diode-under-test current handling capability increases, the thermal impedance under transient conditions will become a very small value. This raises the potential for rejecting good devices and accepting bad ones. Higher I_H values shall be used in this case.

6. Measurement of the TSP V_F (or V_Z). The calibration of V_F versus T_J is accomplished by monitoring V_F for the required value of I_M as the environmental temperature (and thus the DUT temperature), and is varied by external heating. It is not required if the acceptance limit is ΔV_F (see 5.2), but is relevant to the other acceptance criteria (see 5.3 through 5.6). The magnitude of I_M shall be chosen so that V_F is a linearly decreasing function over the normal T_J range of the device. I_M shall be large enough to ensure that the diode junction is turned on but not large enough to cause significant self heating. An example of the measurement method and resulting calibration curve is shown on figure 3101-3.

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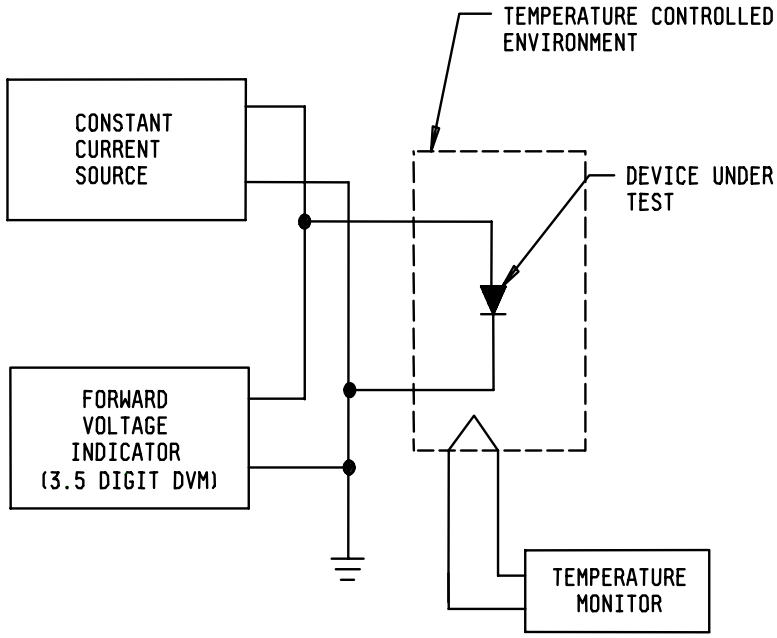
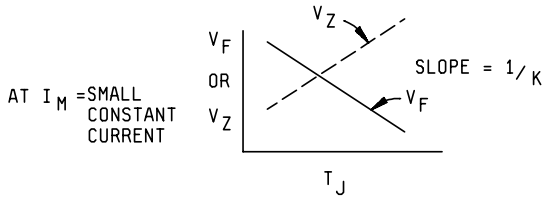


Step 1: Measure V_{F1} at T_{J1} using I_M
Step 2: Measure V_{F2} at T_{J2} using I_M

Step 3: $K = \left| \frac{T_{J2} - T_{J1}}{V_{F2} - V_{F1}} \right| {}^{\circ}C / mV$



I_M shall be large enough to overcome surface leakage effects but small enough not to cause significant self heating. When using the zener direction, the I_M may also require adjustment to avoid a near zero TSP where the avalanche breakdown effects are offset by tunneling or field emission. (See 4.2.d.)

T_J is externally applied: (e.g., via oven, liquid) environment.

FIGURE 3101-3. Example curve of V_F versus T_J.

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A calibration factor K (which is the reciprocal of the slope of the curve on figure 3101-3) can be defined as:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{F2} - V_{F1}} \right| \ °C/mV$$

It has been found experimentally that the K-factor variation for all devices within a given device type class is small. The usual procedure is to perform a K factor calibration on a 10 to 12 piece sample from a device lot and determine the average K and standard deviation (σ). If σ is less than or equal to 3 percent of the average value of K, then the average value of K can be used for all devices within the lot. If σ is greater than 3 percent of the average value of K, then all the devices in the lot shall be calibrated and the individual values of K shall be used in determining device acceptance. As an alternative to using individual values of K, the manufacture may establish internal limits unique to their product that ensures atypical product removal from the population (lot-to-lot and within-the-lot). The manufacture shall use statistic techniques to establish the limits to the satisfaction of the Government.

7. Establishment of test conditions and acceptance limits. Thermal resistance measurements require that I_H be equal to the required value stated in the device specification sheet, typically at rated current or higher. Values for t_H, t_{MD}, and heat sink conditions are also taken from the device specification sheet. The steps shown below are primarily for thermal transient testing and thermal characterization purposes.

The following steps describe how to set up the test conditions and determine the acceptance limits for implementing the transient thermal test for die attachment evaluation using the apparatus and definitions stated above in 6.

7.1 Initial device testing procedure. The following steps describe in detail how to set up the apparatus described previously for proper testing of various diodes. Since this procedure thermally characterizes the diode out to a point in heating time required to ensure heat propagation into the case (i.e., the $R_{\theta JX}$ condition), an appropriate heat sink should be used or the case temperature should be monitored.

Step 1: From a 20 to 25 piece sample, pick any one diode to start the setup process. Set up the test apparatus as follows:

I_H = 1.0 A	(Or some other desired value near the DUTs normal operating current: Typically higher for power diodes, and lower for zener diodes, when measured in the zener direction.)
t_H = 10 - 50 ms	Unless otherwise specified, for most devices rated up to 15 W power dissipation.
50 - 100 ms	Unless otherwise specified, for most devices rated up to 200 W power dissipation.
≥ 250 ms	For steady-state thermal resistance measurement. The pulse shall be shown to correlate to steady-state conditions before it can be substituted for steady-state condition. See method 4081, MIL-STD-750 for further details on testing thermal resistance of diodes.

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t_{MD} = 100 μs max — For non-magnetic or non-inductive lead/package where inductive delay or stored charge do not influence the reading, t_{MD} = 70 μs is a good choice. A larger value may be required on power devices with magnetic/inductive package elements which generate non-thermal electrical transients; unless otherwise specified, this would be observed in the t_3 region of figure 3101-2. If, however, a value of t_{MD} greater than 300 μs is required in order to be able to test outside of the inductive switching region, then correlation shall be made back to 70 μs from whatever value of t_{MD} you require. Example: At 70 μs your thermal impedance readings (in ºC/W) show instability or extreme sensitivity to different I_H values. Repeat taking data from 70 μs to well beyond 1,000 us and plot the thermal impedance vs t_{MD} on log-log paper. You will have a curved line at low values of t_{MD} until the correct value of t_{MD} is reached or exceeded, at which point the plot should be almost straight. Extend the straight-line portion past where the plot curves signify inductance to lower t_{MD} values. Where the straight extension crosses 70 μs, that is the actual value of thermal impedance. If you read thermal impedance using the longer value of t_{MD} where the curve makes the transition to straight line, you need to multiply that reading by the ratio of the 70 μs thermal impedance divided by what you have actually measured. This is straightforward extraplolation. Again, only on log-log plot paper can you use this approach.

I_M = 10 mA — (Or some nominal value approximately two percent, or less, of I_H.) IMPORTANT: Diodes like Schottky and Gold Doped switching rectifiers can have enough saturation current so that the K-factor varies with temperature at lower values of I_M. It is safest to have previously measured at least once for each family type, the K-factor at 25ºC increments from 25ºC up to at least 150ºC (or T_J max) plus vary the current over a decade. Pick an I_M value where K-factor remains fairly consistent. If you can't make it consistent, then use the K-factor that corresponds with the actual T_J achieved in the thermal impedance test (may require some calculations to iterate this value).

Step 2: Insert device into the apparatus test fixture and initiate a test. (For best results, a test fixture that offers some form of heat sinking would be desirable. Heat sinking is not needed if either the power dissipation during the test is well within the diode's free-air rating or the maximum heating time is limited to less than that required for the heat to propagate through the case.)

Step 3: If ΔV_F is in the 100 to 300 mV range, or ΔV_{ZL} is equivalent to the same ΔT_J, then proceed to the next step. This range approximately corresponds to a junction temperature change of roughly +50°C to +150°C and is sufficient for initial comparison purposes.

If ΔV_F is less than 50 mV, return to step 1 and increase heating power into device by increasing I_H. Exception: You have reached maximum rated I_H. In that case you shall accept the accuracy associated with using a smaller ΔV_F. Be sure you have equipment with at least 100 μV resolution for ΔV_F.

If ΔV_F is greater than 150 mV, approximately corresponding to a junction temperature change greater than +150°C, it would probably be desirable to reduce the heating power by returning to step 1 and reducing I_H. Note that some automatic test equipment automatically guards against this problem.

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NOTE: The test equipment shall be capable of resolving ΔV_F to within 5 percent. If not, the higher value of ΔV_F shall be selected until the 5 percent tolerance is met. Two different devices can have the same T_J rise even when P_H is different, due to widely differing V_H. Within a given lot, however, a higher V_H is more likely to result in a higher T_J rise. For such examples, this screen can be more accurately accomplished using the CU value. As defined in 2 herein, CU provides a comparison unit that takes into account different device V_H values for a given I_H test condition.

Step 4: Test each of the sample devices and record the data detailed in 8.

Step 5: Select out the devices with the highest and lowest values of CU or $Z_{\theta JX}$ and put the remaining devices aside.

The ΔV_F values can be used instead of CU or $Z_{\theta JX}$ if the measured values of V_H are very tightly grouped around the average value.

Step 6: Using the devices from step 5, collect and plot the heating curve data for the two devices in a manner similar to the examples shown on figure 3101-4.

Step 7: Interpretation of the heating curves is the next step. Realizing that the thermal characteristics of identical chips should be the same if the t_H is less than or equal to the thermal time constant of the chip, the two curves should start out the same for the low values of t_H. Non-identical chips (thinner or smaller in cross section) will have completely different curves, even at the smaller values of t_H. As the value of t_H is increased, thereby exceeding the chip thermal constant, heat will have propagated through the chip into the die attachment region. Since the heating curve devices of step 5 were specifically chosen for their difference, the curves of figure 3101-4a or 3101-4b diverge after t_H reaches a value where the die attachment variance has an affect on the device T_J and $Z_{\theta JX}$ as best observed on figure 3101-4b for a log-log plot. Increasing t_H further will eventually result in a flattening of the curve as the heating propagates in the device package and thermal impedance approaches the thermal resistance value of the device. If the device package has little thermal mass and is not well mounted to a good heat sink, the curve will not flatten very much, but will show a definite change in slope.

Step 8: Using the heating curve, select the appropriate value of t_H to correspond to the inflection point in the transition region between heat in the chip and heat in the package.

If there are several different elements in the heat flow path: Chip, die attachment, substrate, substrate attach, and package for example in a hybrid, there will be several plateaus and transitions in the heating curve. Appropriate selection of t_H will optimize evaluation sensitivity to other attachment areas.

Step 9: Return to the apparatus and set t_H equal to the value determined from step 8.

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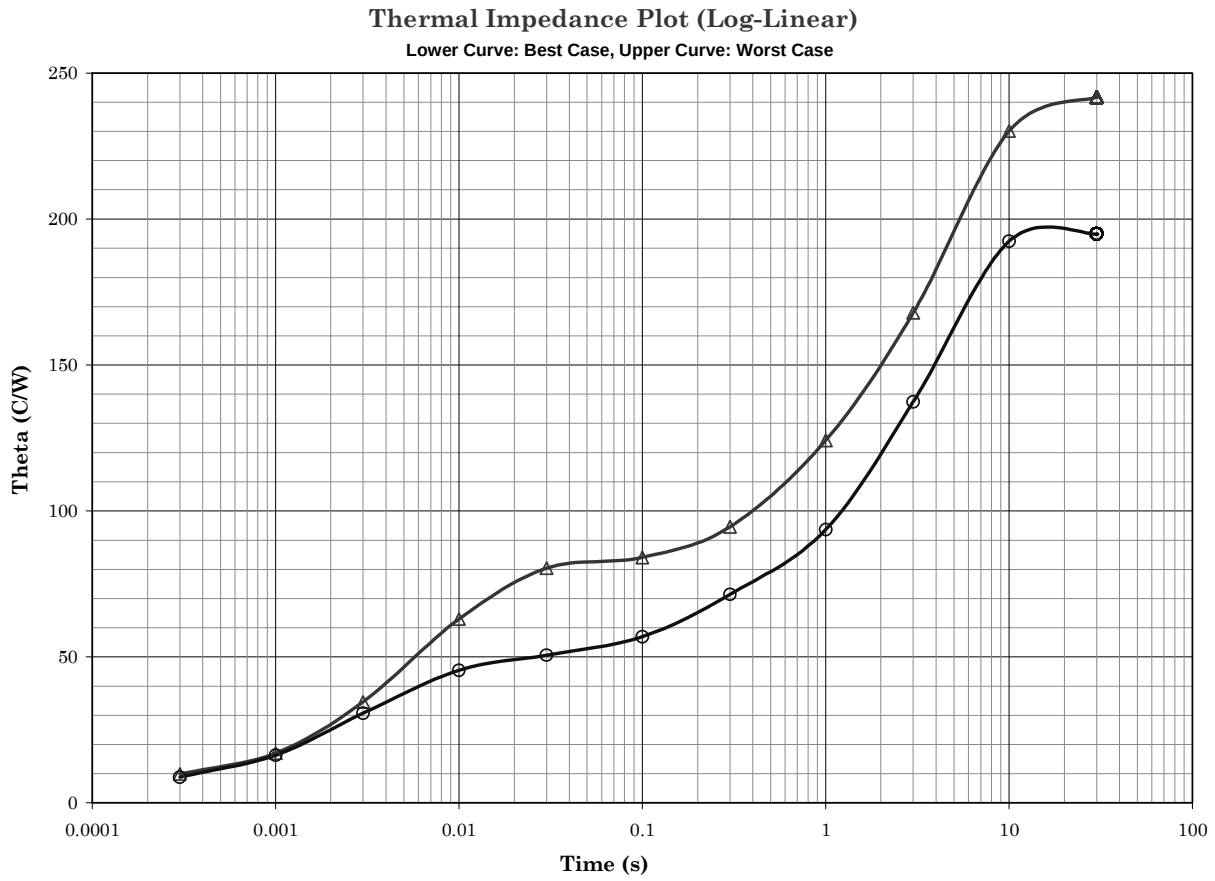

Figure 3101-4a: Log-linear plot (sometimes not as desirable as the log-log plot due to loss of short pulse time resolution) illustrates the ability of short test pulses during thermal impedance to detect poor die bonds. While log-log plots are requested, log-linear plots may be substituted with approval of the qualifying activity. See figure 3101-4b for a log-log example.

Notes:

1). Both figure 3101-4a and figure 3101-4b are of the same data.

2). The log-linear incorrectly leads you to believe that maximum void test sensitivity is available anywhere above 10ms.

FIGURE 3101-4a. Heating curves for two extreme devices (log-linear).

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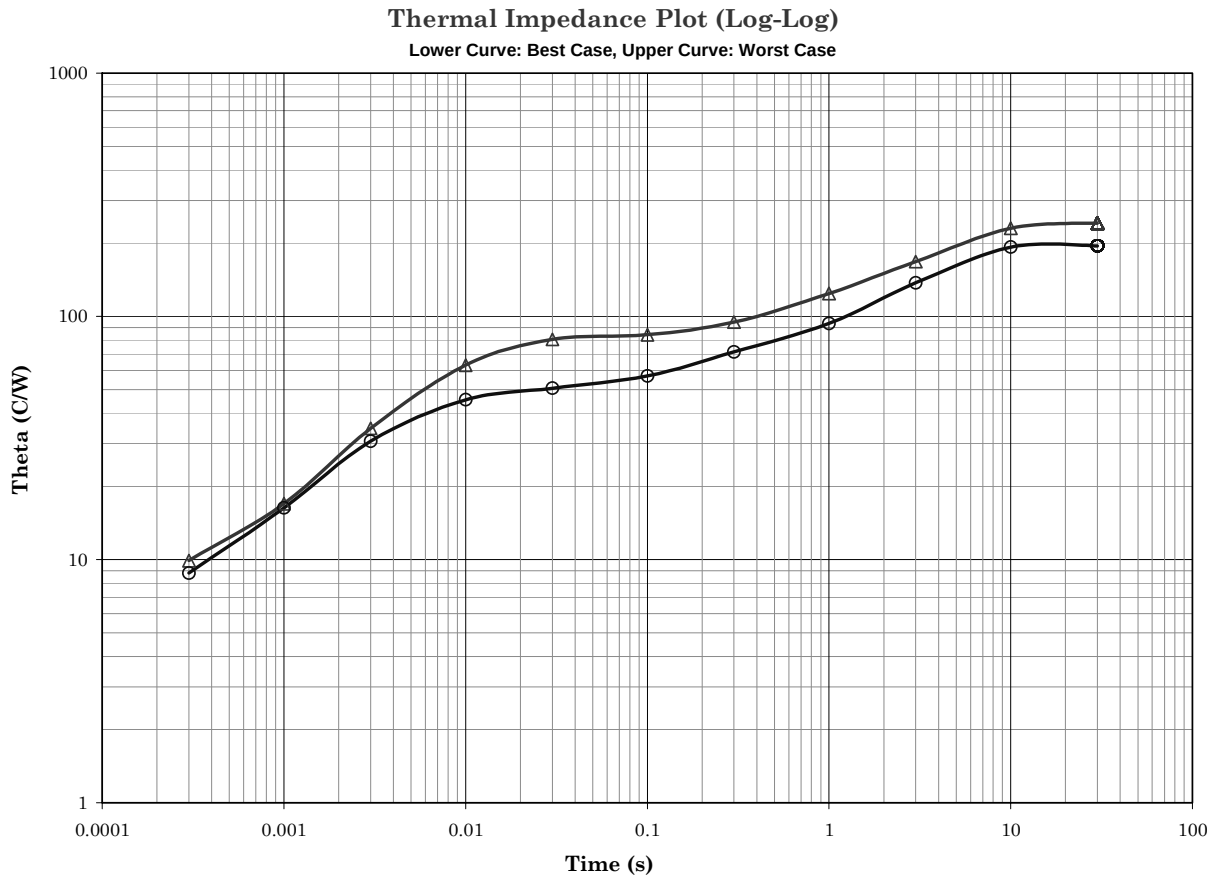

Figure 3101-4b: Log-log plot (preferred) illustrates the ability of short test pulses during thermal impedance to detect poor die bonds. The time period wherein the two curves (best vs worst) are farthest apart is the best time to use for thermal impedance die bond testing. Note that since the range from 10 ms to 100 ms in this example are nearly parallel, any place in that region is acceptable, however, 10 m to 30ms results in faster testing so that would be the logical choice. Each construction design may have a different “sweet zone”.

Notes:

1). Both Figure 3101-4a and Figure 3101-4b are of the same data.

2). The log-log curve deals with resolution accuracy just like any automatic tester. Here the log-log curve makes it clear that you will lose resolution accuracy above 100ms.

FIGURE 3101-4b. Heating curves for two extreme devices (log-log).

Step 10: Because the selected value of t_H is much less than that for thermal equilibrium, it is possible to significantly increase the (P_H) without degrading or destroying the device. The increased power dissipation within the DUT will result in higher ΔV_F or CU values that will make determination of acceptable and unacceptable devices much easier.

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Step 11: The pass/fail limit, the cut-off point between acceptable and nonacceptable devices, can be established in a variety of ways:

a. Correlation to other die attachment evaluation methods, such as die shear and x-ray. While these two methods have little actual value from a thermal point of view, they do represent standardization methods as described in various standards.

b. Maximum allowable junction temperature variations between devices. Since the relationship between ΔT_J and ΔV_F is about 0.5°C/mV for forward bias testing, or a measurable equivalent for zener direction testing, the T_J spread between devices can be easily determined. The T_J predicts reliability. Conversely, the T_J spread necessary to meet the reliability projections can be translated to a ΔV_F or CU value for pass/fail criteria.

To fully utilize this approach, it will be necessary to calibrate the devices for the exact value of the T_J to V_F characteristic. The characteristic's slope, commonly referred to as K factor, is easily measured on a sample basis using a voltmeter, environmental chamber, temperature indicator, and a power supply setup as described in 6 herein. A simple set of equations yield the (T_J) once K and ΔV_F are known:

$$\Delta T_J = (K)\ (\Delta V_F)$$

$$T_J = T_A + \Delta T_J$$

Where T_A is the ambient or reference temperature. For thermal transient test conditions, this temperature is usually equivalent to lead temperature (T_L) for axial lead devices or case temperature (T_C) for case mounted devices.

c. Statistically, from a 20 to 25 device sample, the distribution of ΔV_F or CU values should be a normal one with defective devices out of the normal range. Figure 3101-5 shows a ΔV_F distribution for a sample lot of diodes. NOTE: The left-hand side of the histogram envelope is fairly well defined but the other side is greatly skewed to the right. This is because the left-hand side is constrained by the absolute best heat flow that can be obtained with a given chip assembly material and process unless a test method error is introduced. The other side has no such constraints because there is no limit as to how poorly a chip is mounted.

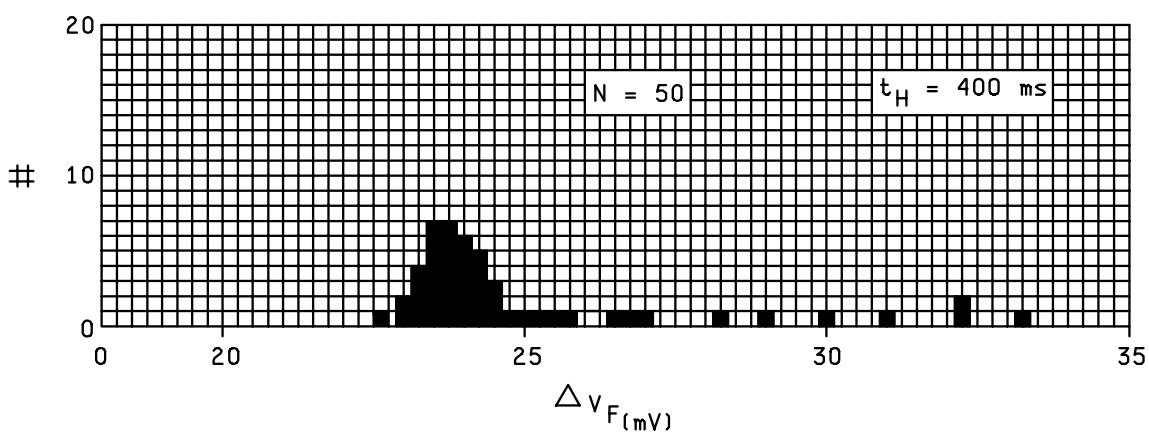

FIGURE 3101-5. Typical ΔV_F (or $Z_{\theta JX}$) distribution with asymmetrical histogram distribution.

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The usual rule of thumb in setting the maximum limit for ΔV_F , CU, or $Z_{\theta JX}$ is to use the distribution average value and three standard deviations (σ). For example:

$$\left|\left(\Delta V_F\right)\right| = \overline{\Delta V}_F + X\sigma$$

high
limit

$$\left|\left(CU\right)\right| = \overline{CU} + X\sigma$$

high
limit

$$\left|\left(Z_{\theta JX}\right)\right| = \overline{Z_{\theta JX}} + X\sigma$$

high
limit

Where X = 3 in most cases and $\overline{\Delta V_F}$, $\overline{\Delta CU}$, and $\overline{\Delta Z_{\theta JX}}$ are the average distribution values.

The statistical data required is obtained by testing 25 or more devices under the conditions of step 11.

The maximum limit determined from this approach should be correlated to the diode's specified thermal resistance. This will ensure that the ΔV_F or CU limits do not pass diodes that would fail the thermal resistance or transient thermal impedance requirements.

Step 12: Once the test conditions and pass/fail limit have been determined, it is necessary only to record this information for future testing requirements of the same device in the same package. It is also recommended that a minimum limit is established to ensure a test method error or other anomaly is investigated.

Step 13: After the pass/fail limits are established, there shall be verification they correlate to good and bad bonded devices or the electrical properties such as surge.

The steps listed above are summarized in table 3101-I.

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TABLE 3101-I. Summary of test procedure steps.

General description		Steps	Comments
A	Initial setup	1 through 4	Approximate instrument settings to find variations among devices in 10 to 15 piece sample.
B	Heating curve generation	5 through 6	Using highest and lowest reading devices, generate heating curves.
C	Heating curve interpretation	7 through 9	Heating curve is used to find more appropriate value for t_H corresponding to heat in the die attachment area (for some other desired interface in the heat flow path).
D	Final setup	10	Heating power applied during t_H is increased in order to improve measurement sensitivity to variations among devices.
E	Pass-fail determination	11 through 12	A variety of methods is available such as JESD 34 for setting the fail limit; the statistical approach is the fastest and easiest to implement.
F	Verification	13	Mechanical / electrical correlation

7.2 Routine device thermal transient testing procedure. Once the proper control settings have been determined for a particular device type from a given manufacturing process or vendor, repeated testing of that device type simply requires that the same test conditions be used as previously determined.

New device types, or the same devices manufactured with a different process, will require a repeat of 7.1 for proper thermal transient test conditions.

8. Test conditions and measurements to be specified and recorded.

8.1 Thermal transient and equilibrium measurements.

8.1.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___mA

b. I_H heating current ___A

c. t_H heating time ___ms

d. t_{MD} measurement time delay ___μs

e. t_{SW} sample window time __ μs

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8.1.2 Data. Record the following data:

a. V_{Fi} initial forward voltage ___V

b. V_H heating voltage ___V

c. V_{Ff} final forward voltage ___V

NOTE: Some test equipment may provide a ΔV_F instead of V_{Fi} and V_{Ff}; this is an acceptable alternative. Record the value of ΔV_F.

Some test equipment may provide direct display of calculated CU or $Z_{\theta JX}$; this is an acceptable alternative. Record the value of CU or $Z_{\theta JX}$.

8.2 K factor calibration. (Optional for criteria 8.3.a or 8.3.b, mandatory for 8.3.c, 8.3.d, or 8.3.e.)

8.3 Test conditions. Specify the following test conditions:

a. I_M current magnitude ___mA

b. Initial junction temperature ___°C

c. Initial V_F voltage ___mV

d. Final junction temperature ___°C

e. Final V_F voltage ___mV

8.4 K factor. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{F2} - V_{F1}} \right| \ °C/mV$$

K factor ___°C/mV

8.5 Specification limit calculations. One or more of the following should be measured or calculated, as stated on the device specification sheet (see 5.1):

ΔV_F	___mV	(For no significant variation in K and V_H among devices).
CU	___mV/V	(For big variation in V_H among devices).
ΔT_J	___°C	(For big variation in K among devices).
K•CU	___°C/V	(For big variation in K and V_H among devices).
$Z_{\theta JX}$	___°C/W	(For big variation in K, V_H, and I_H among devices, same as K▪CU for diodes/rectifiers).
$R_{\theta JX}$	___°C/W	

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9.0 Thermal impedance production guidelines, logistics of the thermal impedance test. The goal of Thermal Impedance production screening is to detect and remove any components that have defects that can affect reliability or performance. The key components for this test upon the DUT are:

a. Determine a temperature sensitive parameter (K-factor) in the DUT and calibrate it (usually in mV/C but not necessarily always). This parameter is normally measured at a current chosen so that it does not affect the accuracy of the thermal impedance test.

b. Determine a measurement P_T power (voltage x current) and t_m measurement pulse time. The pulse time should be sufficient to delineate the semiconductor package layer being monitored for quality. For example, 10 ms to 30 ms measures the die attach integrity and 100 ms to 300 ms measures both the die attach plus an additional die tab attach to the package header. See 9.2 herein. The pulse power should be sufficient to heat the junction up at least 50°C unless limited by a maximum power density rating of the junction.

c. Determine a t_{md} measurement delay time (time between when power pulse is turned off and the K-factor is applied to provide the junction temperature.

d. Deploy equipment capable of applying the above pulse and providing an output that either directly calculates the peak junction temperature with the supplied K-factor and provides a thermal impedance reading in C/W or, at the least, provides a delta voltage change that can manually be converted to thermal impedance by dividing by the K-factor and the P_T applied power. This t_{md} delay time is usually provided by the appropriate specification but extenuating circumstances such as chip storage time or package magnetic resonance may dictate using a longer value of t_{md}. This is permitted provided a correlation is established between the required value of t_{md} and the specified value of t_{md} and DSCC is notified.

It is incumbent upon the supplier to notify DSCC of any specified measurement conditions that might fail to achieve the thermal impedance test method's primary goal of detecting and removing and defective components.

9.1 Applying the thermal impedance test to production product. Every semiconductor product type is likely to respond differently in readings to thermal impedance tests. The intent here is not to compare dissimilar product but, rather, to compare product within a single lot to each other (statistical comparison), to a specification maximum limit (when applicable) and, if at all possible, to a design ideal value. With this in mind, the following rules can be applied:

a. Any part failing the specification maximum limit (if one exists) is an automatic reject.

b. Any part falling outside of a normal distribution of thermal impedance readings in a histogram is subject to reject. This distribution should be documented over the course of five production lots and, if each lot has a similar distribution, then the average distribution and pass-fail limits of the combination of all five production lots may be used to establish permanent screening limits. If the K-factor does not vary more than 10 percent from lot-to-lot, then it is permissible to establish a constant K-factor for this particular part number or chip family. Otherwise, the K-factor may need to be re-established for every lot. If every lot, even after correcting for K-factor variations, varies more than 20 percent from each other, once the reason has been determined and no correction is possible, it may be necessary to treat each production lot on a stand-alone basis.

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c. Upper and lower pass-fail limits cannot be determined by using ±3-Sigma. This is because in most cases (except where you have achieved near perfection), the distribution is an a-symmetrical histogram bell curve where the right (high-side) of the curve extends farther away from center normal than the left (low-side). This is because making parts less than perfect (extends right) is easy but making parts better than perfect (extends left) is far less likely. The upper and lower limits can be set one of two ways:

a) Split histogram curve in half at the center peak value and calculate separate 3-sigma limits, one for the upper side and one for the lower side.

b) Visually have Engineering review the histogram curve and select appropriate limits based upon what looks normal and what doesn't.

The value of a lower pass-fail limit is to catch changes in the product that might otherwise go undetected. For example: Braze preform is suddenly too thin, chip size was just changed, or package design was changed by package vendor.

d. Since the original Engineering design-value for thermal impedance remains the one constant through all testing, this is an excellent tool to confirm that thermal impedance is giving meaningful readings and that the design is being executed correctly by production. The design-value should fall somewhere in the lower region of the histogram curve or slightly below the curve. Major deviations indicate that one or the other is in error or that the measurement conditions cannot give an absolute accurate value (though relative values for statistical screening may continue to be usable for screening).

9.2 Heat Flow Distance vs. Elapsed Time Plot. This section is provided to assist in determining the t_m measurement time required to adequately delineate a particular interface. Figure 3101-6 shows effectively how far heat travels in the time shown in the X-axis.

The example listed on the graph shows that heat in 10 mils of silicon takes 1.2 ms to reach the back side. During the 1.2 ms, the heat has remained inside the chip, has not passed through the chip bond interface, and is too short a time to measure the chip bond interface. As a first try, multiply by at least seven to get a minimum test time.

The example continues to show that it would take 8.7 ms for heat to reach through the silicon chip, across the braze layer that is being evaluated, and through, but not outside of, the tab the chip is mounted on. Based on this, 8.7 ms would work as a t_m that would maximize sensitivity to bad bonds but not be influenced by anything beyond the first tab. This is where the popular default value of 10ms came from.

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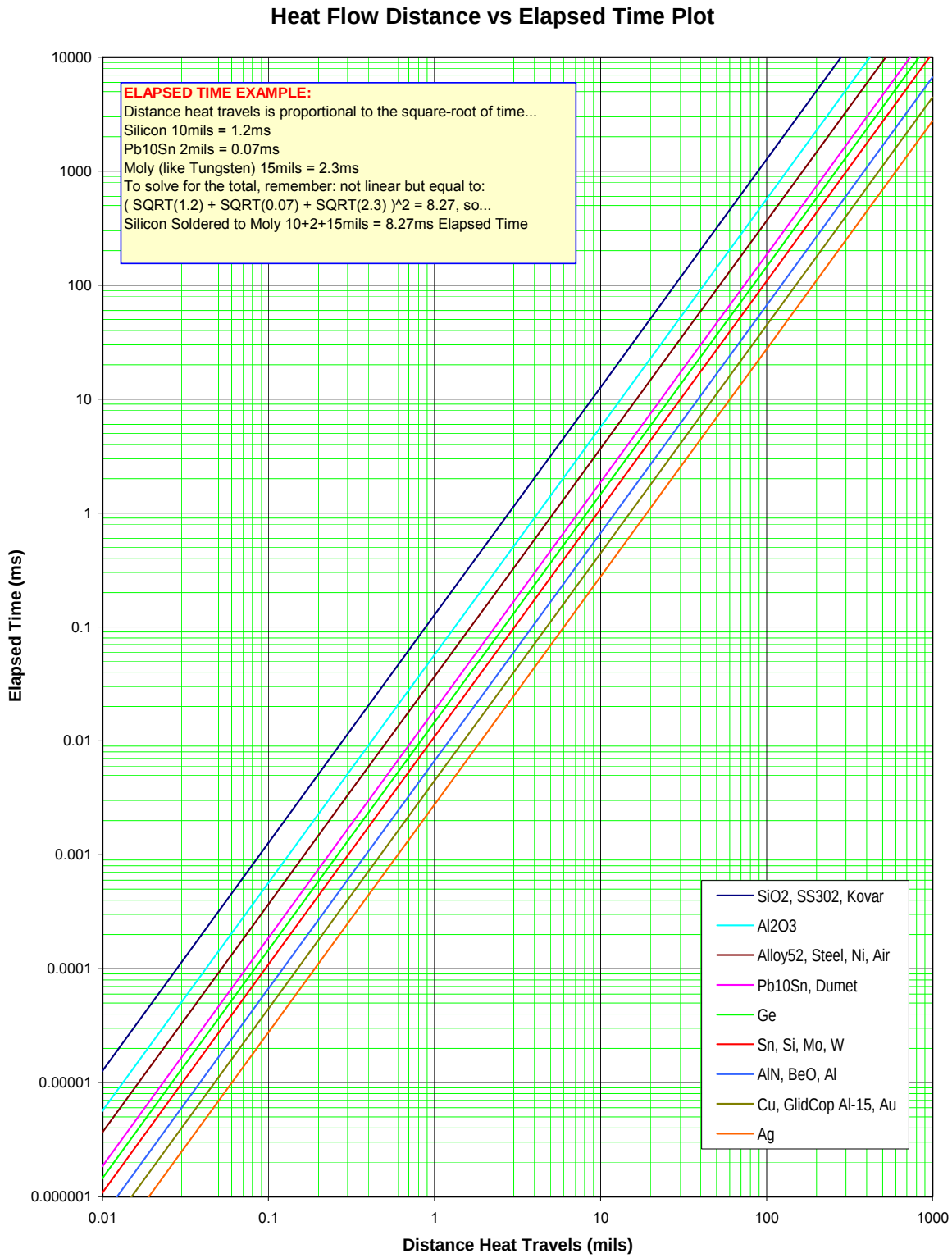

Figure 3101-6. Heat flow distance vs. elapsed time plot.

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METHOD 3103

THERMAL IMPEDANCE MEASUREMENTS FOR INSULATED GATE BIPOLAR TRANSISTORS

(DELTA GATE-EMITTER ON VOLTAGE METHOD)

1. Purpose. The purpose of this test is to measure the thermal impedance of the insulated gate bipolar transistors (IGBT) under the specified conditions of applied voltage, current, and pulse duration. The temperature sensitivity of the gate emitter ON voltage, under conditions of applied collector emitter voltage and low emitter current, is used as the junction temperature (T_J) indicator. This method is particularly suitable to enhancement mode, power IGBTs having relatively long thermal response times. This test method is used to measure the thermal response of the junction to a heating pulse. Specifically, the test may be used to measure dc thermal resistance and to ensure proper die mountdown to its case. This is accomplished through the appropriate choice of pulse duration and heat power magnitude. The appropriate test conditions and limits are detailed in 6.

2. Symbols and definitions. The following symbols and terminology shall apply for the purpose of this test method:

a. I_M: Emitter current applied during measurement of the gate emitter ON voltage.

b. I_H: Heating current through the collector or emitter lead.

c. V_H: Heating voltage between the collector and emitter.

d. P_H Magnitude of the heating power pulse applied to DUT in watts; the product of I_H and V_H.

e. t_H: Heating time during which P_H is applied.

f. VTC: Voltage-temperature coefficient of $V_{GE(ON)}$ with respect to T_J; in mV/°C.

g. K: Thermal calibration factor equal to reciprocal of VTC; in °C/mV.

h. T_J: Junction temperature in degrees Celsius.

T_{Ji}: Junction temperature in degrees Celsius before start of the power pulse.

T_{Jf}: Junction temperature in degrees Celsius at the end of the power pulse.

i. T_X: Reference temperature in degrees Celsius.

T_{Xi}: Initial reference temperature in degrees Celsius.

T_{Xf}: Final reference temperature in degrees Celsius.

j. $V_{GE(ON)}$: Gate emitter ON voltage in millivolts.

$V_{GE(ON)i}$: Initial gate emitter ON voltage in millivolts.

$V_{GE(ON)f}$: Final gate emitter ON in millivolts.

k. $V_{GE(M)}$: Gate emitter voltage during measurement periods.

$V_{GE(H)}$: Gate emitter voltage during heating periods.

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l. $V_{CE(M)}$: Collector emitter voltage during measurement periods.

$V_{CE(H)}$: Collector emitter voltage during heating periods.

m. V_{CG}: Collector gate voltage, adjusted to provide appropriate V_{CE}.

n. t_{MD}: Measurement delay time is defined as the time from the removal of heating power P_H to the start of the $V_{GE(ON)}$ measurement.

o. t_{SW}: Sample window time during which final $V_{GE(ON)}$ measurement is made.

p. $Z_{\theta JX}$: Transient junction-to-reference point thermal impedance in °C/W. $Z_{\theta JX}$ or specified power pulse duration is:

$$Z_{\theta JX} = \left(T_{jf} - T_{ji} - \frac{\Delta T_x}{P_H} \right)$$

Where: ΔT_X = change in reference point temperature during the heating pulse (see 5.2-for short heating pulses, (e.g., die attach evaluation) this term is normally negligible.)

3. Apparatus. The apparatus required for this test shall include the following as applicable to the specified test procedure.

3.1 Case temperature measurement. A thermocouple for measuring the case temperature at a specified reference point. The recommended reference point shall be located on the case under the heat source. Thermocouple material shall be copper-constantan (type T) or equivalent. The wire size shall be no larger than AWG size 30. The junction of the thermocouple shall be welded, rather than soldered or twisted, to form a bead. The accuracy of the thermocouple and its associated measuring system shall be ±0.5°C. Proper mounting of the thermocouple to ensure intimate contact to the reference point is critical for system accuracy.

3.2 Controlled temperature environment. A controlled temperature environment capable of maintaining the case temperature during the device calibration procedure to within ±1°C over the temperature range of +23°C to +100°C, the recommended temperatures for measuring K-factor.

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3.3 K factor calibration. A K factor calibration setup, as shown on figure 3103-1, that measures $V_{GE(ON)}$ for the specified values of V_{CE} and I_M in an environment where temperature is both controlled and measured. A temperature controlled circulating fluid bath is recommended. The current source shall be capable of supplying I_M with an accuracy of ±2 percent. The voltage source V_{CG} is adjusted to supply V_{CE} with an accuracy of ±2 percent. The voltage measurement of $V_{GE(ON)}$ shall be made with a voltmeter capable of 1 mV resolution. The device to current source wire size shall be sufficient to handle the measurement current (AWG size 22 stranded is typically used for up to 100 mA).

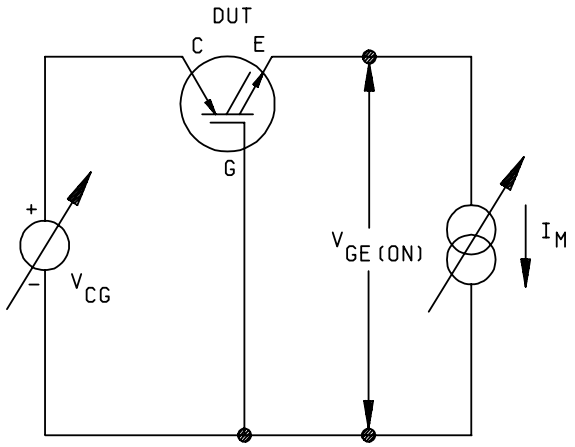

FIGURE 3103-1. K factor calibration setup.

3.4 Thermal testing. There are two approaches to the actual thermal testing, either the common gate or the common source method. Both methods work equally well, although the common source method may be more reliable and less potentially damaging to the DUT. The figures and description below describe the thermal measurement for n-channel enhancement mode devices. Opposite polarity devices can be tested by appropriately reversing the various supplies. Depletion mode devices can be tested by applying the gate emitter voltage (V_{GE}) in the appropriate manner.

3.4.1 Common gate thermal test circuit. A common gate configuration test circuit used to control the device and to measure the temperature using the gate emitter ON voltage as the temperature sensing parameter as shown on figure 3103-2. Polarities shown are for n-channel devices but the circuit may be used for p-channel types by reversing the polarities of the voltage and current sources (For common source test circuit see figure 3103-3).

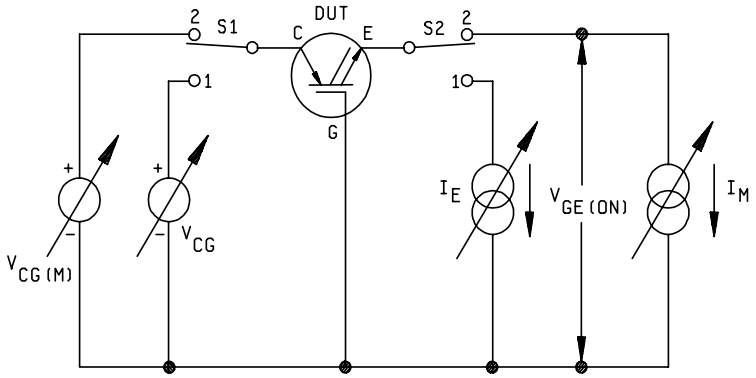

FIGURE 3103-2. Common gate thermal impedance measurement circuit (gate emitter on voltage method).

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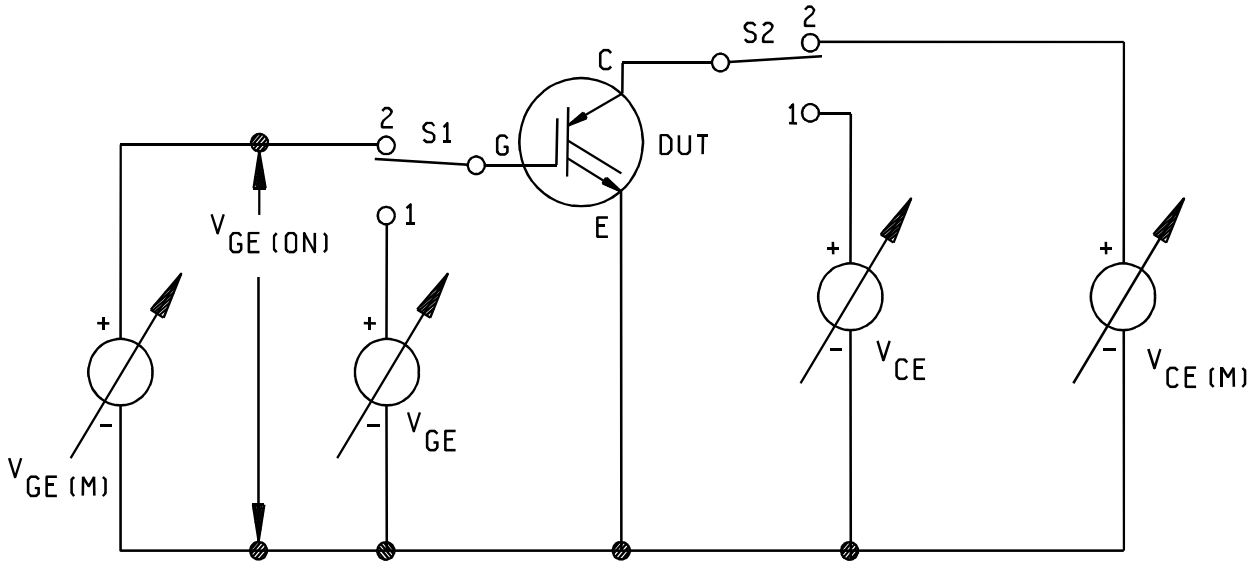
The circuit consists of the DUT, two voltage sources, two current sources, and two electronic switches. During the heating phase of the measurement, switches S1 and S2 are in position 1. The values of V_{CG} and I_E are adjusted to achieve the desired values of I_C and V_{CE} for the P_H heating condition.

To measure the initial and post heating pulse (T_J) of the DUT, switches S1 and S2 are each switched to position 2. This puts the gate at the measurement voltage level $V_{CG(M)}$ and connects the current source I_M to supply measurement current to the emitter. The values of $V_{CG(M)}$ and I_M shall be the same as used in the K factor calibration if actual (T_J)rise data is required. Figures 3103-4 and 3103-5 show the waveforms associated with the three segments of the test.

3.4.2 Common source thermal test circuit. A common source configuration test circuit used to control the device and to measure the temperature using the gate emitter ON voltage as the temperature sensing parameter as shown on figure 3103-3. Polarities shown are for n-channel devices but the circuit may be used for p-channel types by reversing the polarities of the voltage and current sources.



NOTE: The circuit consists of the DUT, four voltage sources, and two electronic switches. During the heating phase of the measurement, switches S1 and S2 are in position 1. The values of V_{CE} and V_{GE} are adjusted to achieve the desired values of I_C and V_{CE} for the P_H heating condition.

FIGURE 3103-3. Common source thermal impedance measurement circuit (gate emitter on voltage method).

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To measure the initial and post heating pulse (T_J) of the DUT, switches S1 and S2 are each switched to position 2. This puts the collector at the measurement voltage level $V_{CE(M)}$ and the gate at $V_{GE(M)}$, which shall be adjusted to obtain I_M. The values of $V_{CE(M)}$ and I_M shall be the same as used in the K factor calibration if actual (T_J)rise data is required. Figures 3103-4 and 3103-5 show the waveforms associated with the three segments of the test.

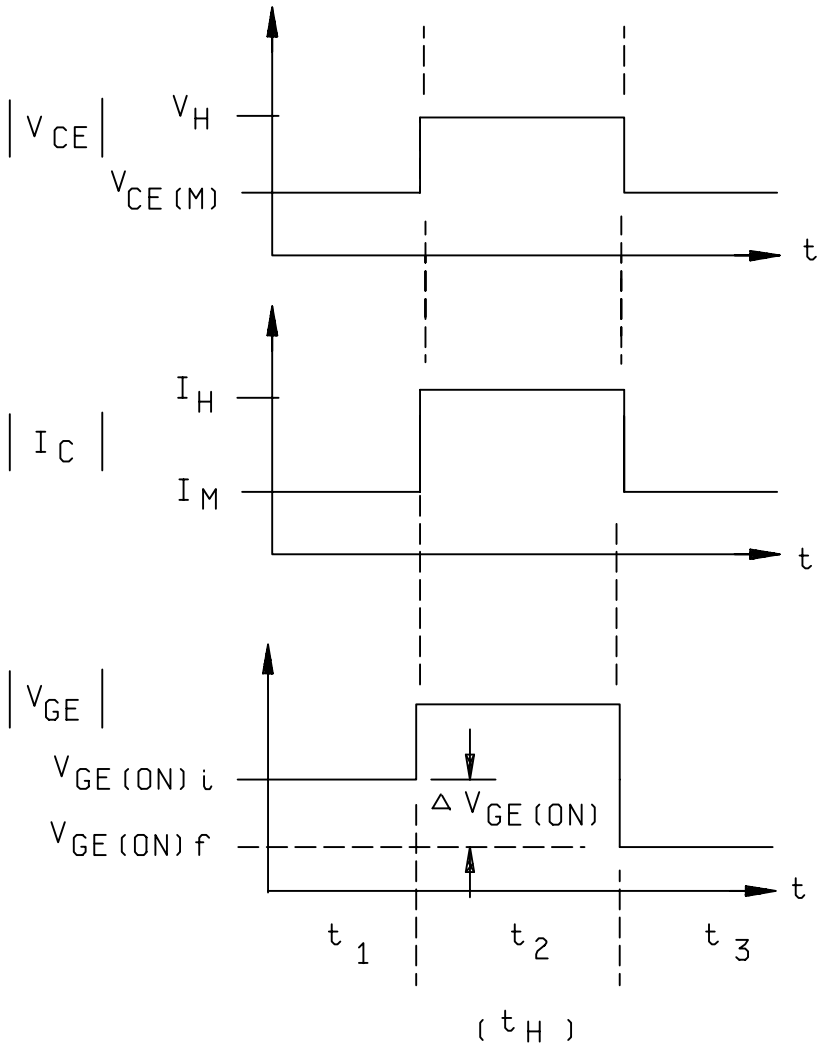

FIGURE 3103-4. Device waveforms during the three segments of the thermal transient test.

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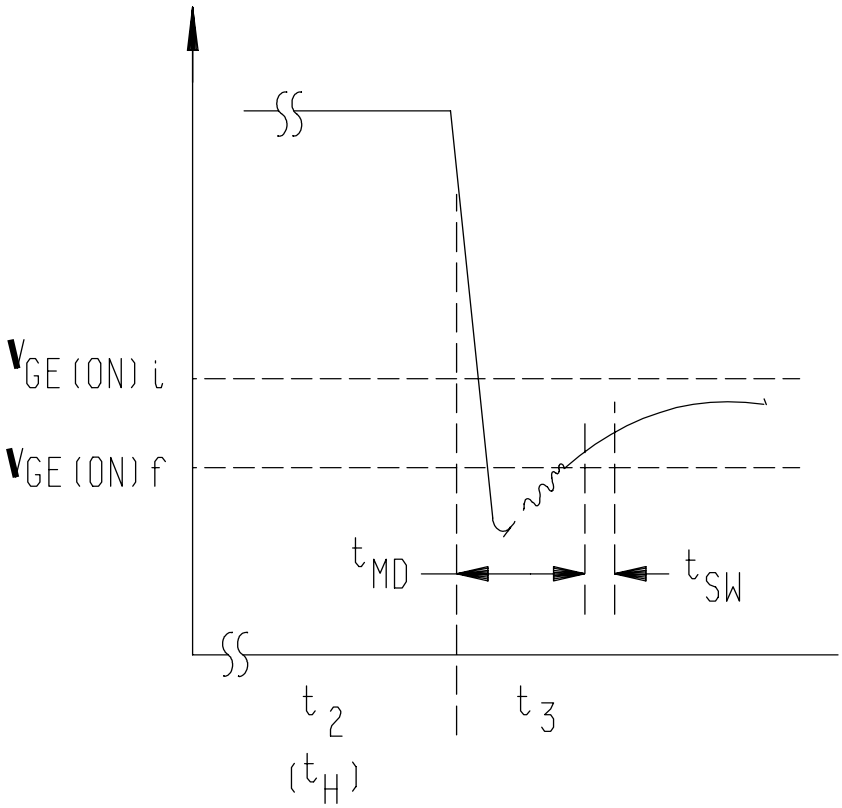

The value of t_{MD} is critical to the accuracy of the measurement and shall be properly specified in order to ensure measurement repeatability. Note that some test equipment manufacturers include the sample and hold window time t_{SW} within their t_{MD} specification.

FIGURE 3103-5. Second V_{GE} measurement waveform.

NOTE: The circuits for both common gate and common source thermal measurements can be modified so that V_{CE} is applied during both measurement and heating periods if the value of V_{CE} is at least ten times the value of $V_{GE(ON)}$. Further, the common gate circuit can be modified so that I_M is continually applied as long as the I_E current source can be adjusted for the desired value of heating current.

3.5 Source-drain forward voltage. Suitable sample-and-hold voltmeter or oscilloscope to measure source drain forward voltage at specified times. $V_{GE(ON)}$ shall be measured to within 5 mV, or within 5 percent of ($V_{GE(ON)i}$ - $V_{GE(ON)f}$), whichever is less.

4. Measurement of the TSP. The required calibration of $V_{GE(ON)}$ versus T_J is accomplished by monitoring $V_{GE(ON)}$ for the required values of V_{CE} and I_M as the heat sink temperature (and thus the DUT temperature) is varied by external heating. The magnitudes of V_{CE} and I_M shall be chosen so that $V_{GE(ON)}$ is a linearly decreasing function over the expected range of T_J during the power pulse. For this condition, V_{CE} shall be at least three times $V_{GE(ON)}$. I_M shall be large enough to ensure that the device is turned on but not so large as to cause any significant self heating. (This will normally be 1 mA for low power devices and up to 100 mA for high power ones.) An example calibration curve is shown on figure 3103-6.

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4.1 K factor calibration. A calibration factor K (which is the reciprocal of VTC or the slope of the curve on figure 3103-4) can be defined as:

$$K = \frac{1}{VTC} = \left| \frac{T_J 1 - T_J 2}{V_{GE(ON)1} - V_{GE(ON)2}} \right| \ °C/mV$$

It has been found experimentally that the K-factor variation for all devices within a given device type class is small. The usual procedure is to perform a K factor calibration on a 10 to 12 piece sample from a device lot and determine the average K and standard deviation (σK). If σK is less than or equal to three percent of the average value of K, then the average value of K can be used for all devices within the lot. If σK is greater than three percent of the average value of K, then all the devices in the lot shall be calibrated and the individual values of K shall be used in thermal impedance calculations or in correcting $\Delta V_{GE(ON)}$ values for comparison purposes.

When screening to ensure proper die attachment within a given lot, this calibration step is not required, (e.g., devices of a single manufacturer with identical PIN and case style). In such cases, the measure of thermal response may be $\Delta V_{GE(ON)}$ for a short heating pulse, and the computation of ΔT_J or $Z_{\Theta JX}$ is not necessary. (For this purpose, t_H shall be 10 ms for TO-39 size packages and 100 ms for TO-3 packages.)

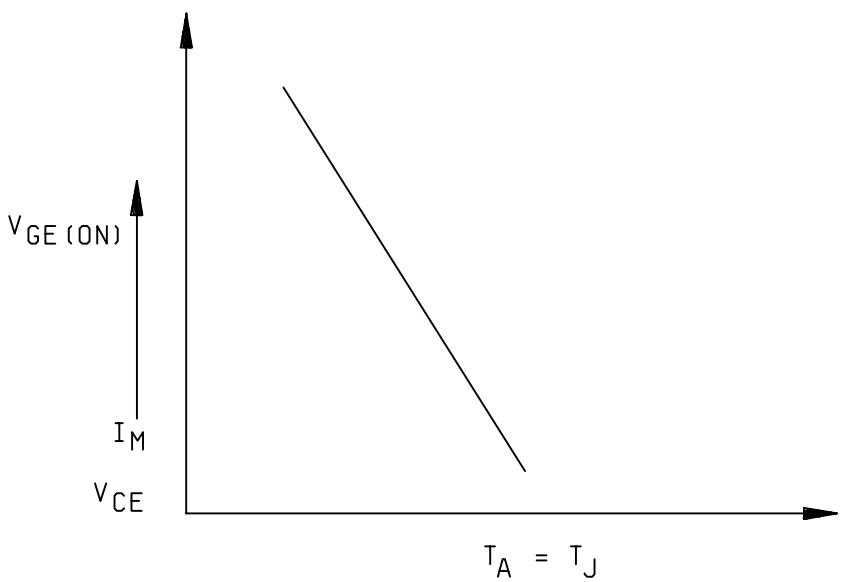

FIGURE 3103-6. Example curve of $V_{GE(ON)}$ versus T_J.

5. Calibration. K factor shall be determined according to the procedure outlined in 4, except as noted in 4.1.

5.1 Reference point temperature. The reference point is usually chosen to be on the bottom of the transistor case directly below the semiconductor chip in a TO-204 metal can or in close proximity to the chip-in other styles of packages. Reference temperature point location shall be specified and its temperature shall be monitored using the thermocouple mentioned in 3.1 during the preliminary testing. If it is ascertained that T_X increases by more than five percent of measured (T_J) rise during the power pulse, then either the heating power pulse magnitude shall be decreased, the DUT shall be mounted in a temperature controlled heat sink, or the calculated value of thermal impedance shall be corrected to take into account the thermal impedance of the reference point to the cooling medium or heat sink.

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Temperature measurements for monitoring, controlling or correcting reference point temperature changes are not required if the t_H value is low enough to ensure that the heat generated within the DUT has not had time to propagate through the package. Typical values of t_H for this case are in the 10 ms to 500 ms range, depending on DUT package type and material.

5.2 Thermal measurements. The following sequence of tests and measurements shall be made.

a. Prior to the power pulse:

(1) Establish reference point temperature T_{Xi}.

(2) Apply measurement voltage V_{CE}.

(3) Apply measurement current I_M.

(4) Measure gate emitter ON voltage $V_{GE(ON)i}$ (a measurement of the initial (T_J)).

b. Heating pulse parameters:

(1) Apply collector emitter heating voltage V_H.

(2) Apply collector heating current I_H as required by adjustment of gate emitter voltage.

(3) Allow heating condition to exist for the required heating pulse duration t_H.

(4) Measure reference point temperature T_{Xf} at the end of heating pulse duration.

NOTE: T_X measurements are not required if the t_H value meets the requirements stated in 5.2.

c. Post-power pulse measurements:

(1) Apply measurement current I_M.

(2) Apply measurement voltage V_{GE}.

(3) Measure gate emitter ON voltage $V_{GE(ON)f}$ (a measurement of the final (T_J)).

(4) Time delay between the end of the power pulse and the completion of the $V_{GE(ON)f}$ measurement as defined by the waveform of figure 3103-4 in terms of t_{MD} plus t_{SW}.

d. The value of thermal impedance, $Z_{\theta JX}$, is calculated from the following formula:

$$Z_{\theta JX} = \frac{\Delta T_J}{P_H} = \left| \frac{K\,(V_{GE(ON)f} - V_{GE(ON)i})}{(I_H)(V_H)} \right| \ ^\circ C/W$$

This value of thermal impedance will have to be corrected if T_{Xf} is greater than T_{Xi} by +5°C. The correction consists of subtracting the component of thermal impedance due to the thermal impedance from the reference point (typically the device case) to the cooling medium or heat sink. T_X measurements are not required if the t_H value meets the requirements stated in 5.2.

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This thermal impedance component has a value calculated as follows:

$$Z_{\theta X\text{-}HS} = \frac{\Delta T_X}{P_H} = \frac{(T_{Xf} - T_{Xi})}{(I_H)(V_H)}$$

Where: HS = cooling medium or heat sink (if used).
Then:

$$Z_{\theta JX|} = Z_{\theta JX|} - Z_{\theta X\text{-}HS}$$

Corrected Calculated

NOTE: This last step is not necessary for die attach evaluation (see 4.1).

6. Test conditions and measurements to be specified and recorded.

6.1 K factor calibration.

6.1.1 Test conditions. Specify the following test conditions:

a. I_M current magnitude ___mA
(See applicable specification sheet for current value)

b. V_{CE} voltage magnitude ___V
(See applicable specification sheet for voltage value)

c. Initial junction temperature ___°C
(Normally +25°C ±5°C)

d. Final junction temperature ___°C
(Normally +100°C ±10°C)

6.1.2 Data. Record the following data:

a. Initial $V_{GE(ON)}$ voltage ___mV

b. Final $V_{GE(ON)}$ voltage ___mV

6.1.3 K factor. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_J 1 - T_J 2}{V_{GE(ON)1} - V_{GE(ON)2}} \right| \ °C/mV$$

6.1.4 For die attachment evaluation, this step may not be necessary (see 4.1).

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6.2 Thermal impedance measurements.

6.2.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___mA
(Shall be same as used for K factor calibration)

b. V_{CE} measuring voltage ___V
(Shall be same as used for K factor calibration)

c. I_H heating current ___A

d. V_H collector emitter heating voltage ___V

e. t_H heating time ___s

f. t_{MD} measurement time delay ___µs

g. t_{SW} sample window time ___µs

NOTE: I_H and V_H are usually chosen so that P_H is approximately two-thirds of device rated power dissipation.

6.2.2 Data. Record the following data:

a. T_{Xi} initial reference temperature ___°C

b. T_{Xf} final reference temperature ___°C

6.2.2.1 $\Delta V_{GE(ON)}$ data:

$\Delta V_{GE(ON)}$ ___mV

6.2.2.2 $V_{GE(ON)}$ data:

a. $V_{GE(ON)i}$ initial source drain voltage ___V

b. $V_{GE(ON)f}$ final source drain voltage ___V

NOTE: T_X measurements are not required if the t_H value meets the requirements stated in 5.2.

6.2.3 Thermal impedance. Calculate thermal impedance using the procedure and equations shown in 5.2.

6.3 $\Delta V_{GE(ON)}$ measurements for screening. These measurements are made for t_H values that meet the intent of 4.1 and the requirements stated in 5.2.

6.3.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___mA

b. V_{GE} measuring voltage ___V

c. I_H heating current ___A

d. V_H collector emitter heating voltage ___V

e. t_H heating time ___s

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f. t_{MD} measurement time delay ___μs

g. t_{SW} sample window time ___μs

The values of I_H and V_H are usually chosen equal to or greater than the values used for thermal impedance measurements.

6.3.2 Specified limits. The following data is compared to the specified limits:

6.3.2.1 $\Delta V_{GE(ON)}$ data:

$\Delta V_{GE(ON)}$ ___mV

6.3.2.2 $V_{GE(ON)}$ data:

a. $VG_{E(ON)i}$ initial source drain voltage ___V

b. $VG_{E(ON)f}$ final source drain voltage ___V

Compute $\Delta V_{GE(ON)}$ ___mV

6.3.2.3 ΔT_J calculation. Optionally calculate ΔT_J if the K factor results produce a σ greater than three percent of the average value of K.

$$\Delta T_J = K(\Delta V_{GE(ON)})°C$$

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METHOD 3104

THERMAL RESISTANCE MEASUREMENTS OF GaAs MOSFETs (CONSTANT CURRENT FORWARD-BIASED GATE VOLTAGE METHOD)

1. Purpose. The purpose of this test is to measure the thermal resistance of the MOSFET under the specified conditions of applied voltage, current, and pulse width. The temperature sensitivity of the forward voltage drop of the gate source diode is used as the (T_J) indicator. This method is particularly suitable for completely packaged devices.

2. Symbols and definitions. The following symbols and terminology shall apply for the purpose of this test method:

a. I_M: Measuring current in the gate-source diode.

b. I_H: Heating current through the drain.

c. V_H: Heating voltage between the drain and source.

d. P_H Magnitude of the heating power pulse applied to DUT in watts; the product of I_H and V_H.

e. t_H: Heating time during which P_H is applied.

f. K: Thermal calibration factor (°C/mV).

g. T_J: Junction temperature in degrees Celsius.

T_{Ji}: Junction temperature in degrees Celsius before start of the power pulse.

T_{Jf}: Junction temperature in degrees Celsius at the end of the power pulse.

h. T_X: Reference temperature in degrees Celsius.

T_{Xi}: Initial reference temperature in degrees Celsius.

T_{Xf}: Final reference temperature in degrees Celsius.

i. V_{GSf}: Forward-biased gate-source junction diode voltage drop in volts.

$V_{GSf(i)}$: Initial gate-source voltage.

$V_{GSf(f)}$: Final gate-source voltage.

j. t_{MD}: The time from the start of heating power (P_H) removal to the completion of the final V_{GSf} measurement.

k. Θ_{JX} Junction-to-reference point thermal resistance in degrees Celsius/watt. Θ_{JX} for specified heating power conditions is:

$$\theta_{JX} = \frac{(T_{Jf} - T_{Ji})}{P_H}$$

l. CU: Comparison unit for screening devices against specification limits. Defined as the change in forward biased gate-source voltage divided by heating current in mV/A.

3. Apparatus. The apparatus required for this test shall include the following as applicable to the specified test procedure.

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3.1 Case reference point temperature. The case reference point temperature shall be measured using a thermocouple. The recommended reference point should be located immediately outside the case under the heat source. Thermocouple material shall be copper-constantan (type T) or equivalent. The wire size shall be no larger than AWG size 30. The junction of the thermocouple shall be welded to form a bead rather than soldered or twisted. The accuracy of the thermocouple and associated measuring system shall be ±0.5°C.

3.2 Controlled temperature environment. A controlled temperature environment capable of maintaining the case temperature during the device calibration procedure to within ±1°C over the temperature range of room temperature (approximately +23°C) to +100°C.

3.3 K factor calibration setup. A K factor calibration setup, as shown on figure 3104-1, that measures V_{GSf} for a specified value of I_M in an environment that is both temperature controlled and measured. The current source must be capable of supplying I_M with an accuracy of ±1 percent and have a compliance of at least 1 volt and not more than 2 volts. The voltage measurement of V_{GSf} should be made to 1 mV resolution. The device-to-current source wire size shall be sufficient to handle the measurement current (AWG size 26 stranded is typically used for up to 10 mA).

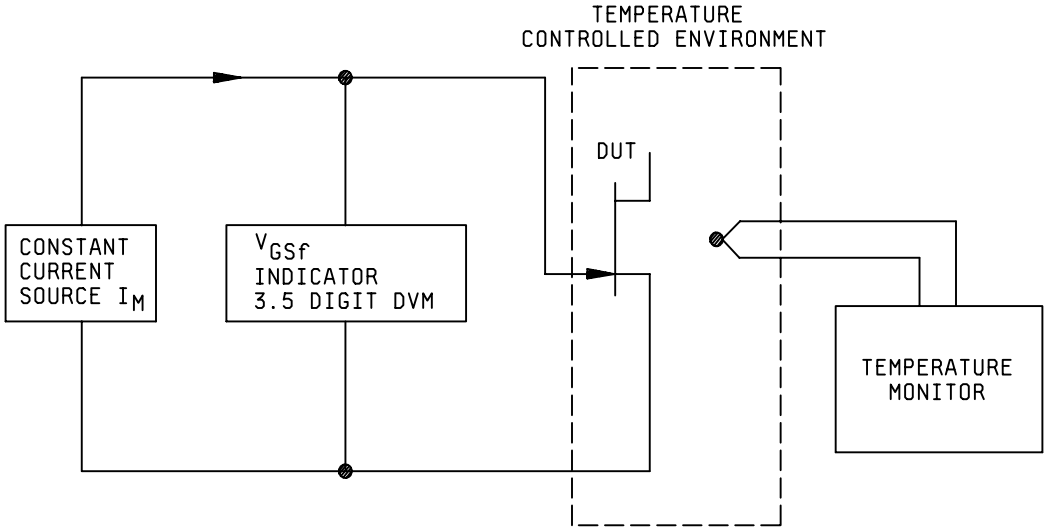

FIGURE 3104-1. K factor calibration setup.

3.4 Controlled temperature heat sink. Controlled temperature heat sink capable of maintaining the specified reference point temperature to within ±5 of the preset (measured) value.

3.5 Test circuit. The circuit used to control the device and to measure the temperature using the forward voltage of the gate-source diode as the temperature sensing parameter is shown on figure 3104-2. Polarities shown are for n-channel devices but the circuit may be used for p-channel types by reversing the polarities of the voltage and current sources.

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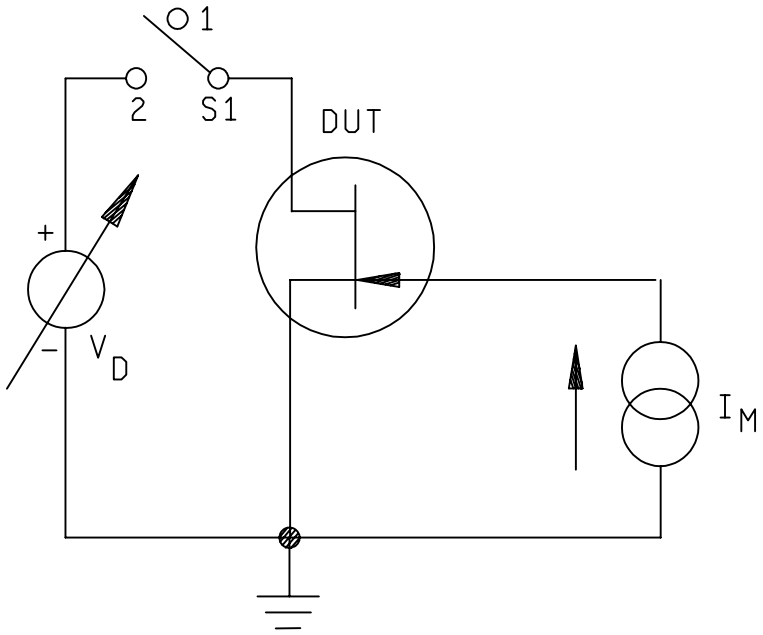

NOTE: The circuit consists of the DUT, one voltage source, one current source, and one electronic switch. During the heating phase of the measurement, switch S1 is in position 2. The value of V_D is adjusted to achieve the desired values of I_D and V_{DS} for the P_H heating condition.

FIGURE 3104-2. Thermal resistance measurement circuit (constant current forward-biased gate voltage method).

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To measure the initial and post heating pulse (T_J) of the DUT, switch S1 is switched to position 1. This disconnects the V_D source during the measurement time and allows for the measurement of $V_{GSf(i)}$ and $V_{GSf(f)}$ before and after the heating time, respectively. Figure 3104-3 shows the waveforms associated with the three segments of the test.

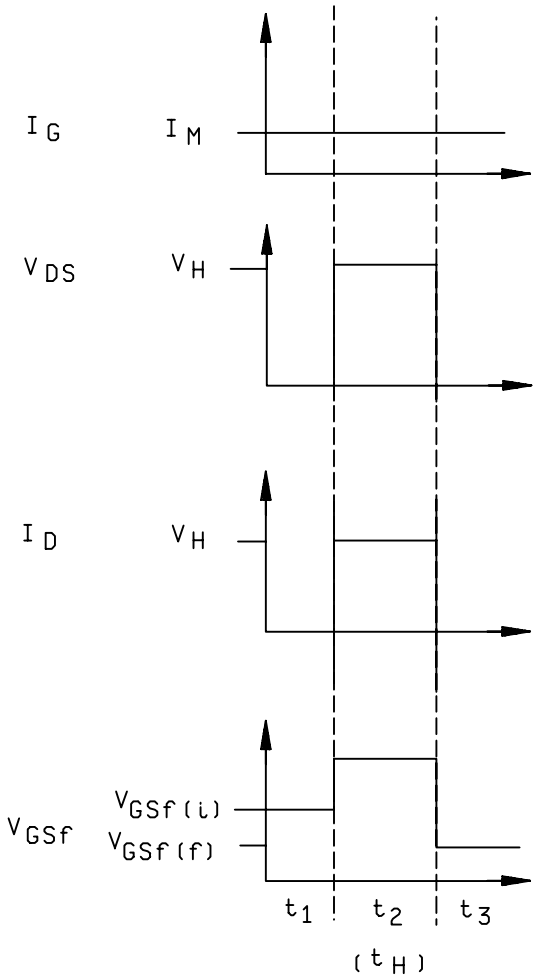

FIGURE 3104-3. Device waveforms during the three segments of the thermal resistance test.

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The time required to make the second V_{GSf} reading is critical to the accuracy of the measurement and must be properly specified in order to ensure measurement repeatability. The definition of measurement delay time (t_{MD}) is described by the waveform on figure 3104-4.

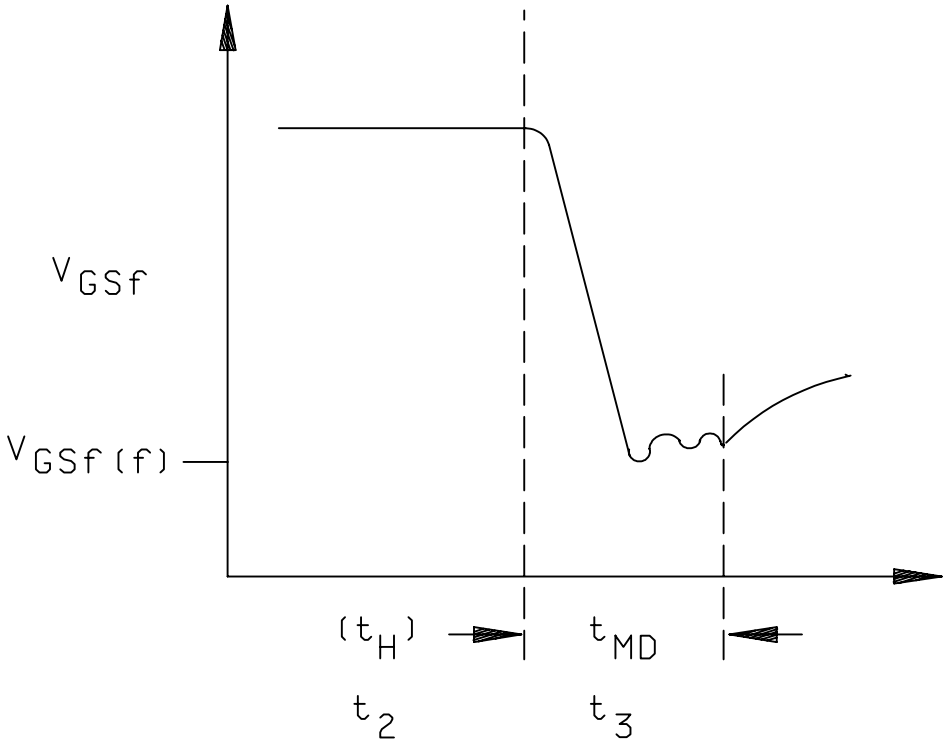

FIGURE 3104-4. Second V_{GSf} measurement waveform.

3.6 Source drain forward voltage. Suitable sample-and-hold voltmeter or oscilloscope to measure source drain forward voltage at specified times. V_{GSf} should be measured with 1 mV resolutions.

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4. Measurement of the TSP V_{GSf}. The required calibration of V_{GSf} versus T_J is accomplished by monitoring V_{GSf} for the required value of I_M without any connection to the drain as the heat sink temperature (and thus the DUT temperature) is varied by external heating. The magnitude of I_M should be chosen so that V_{GSf} is a linearly decreasing function over the expected T_J range during the power pulse. I_M must be large enough to ensure that the gate-source junction is turned on but not large enough to cause significant self heating or device destruction. An example calibration curve is shown on figure 3104-5.

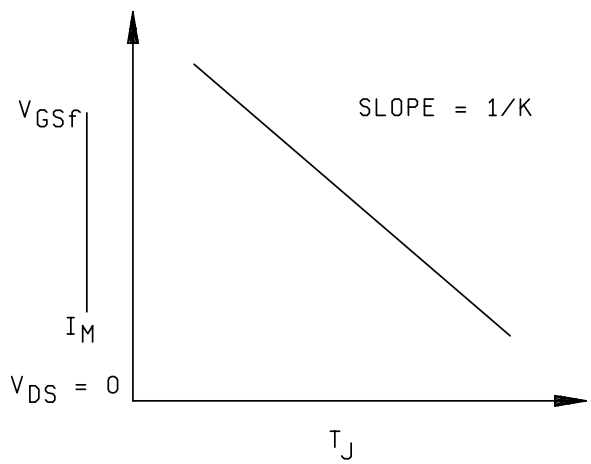

FIGURE 3104-5. Calibration curve.

A calibration factor K (which is the reciprocal of the slope of the curve on figure 3104-5) can be defined as:

$$K = \left| \frac{T_J 1 - T_J 2}{V_{GSf} 1 - V_{GSf} 2} \right| \ °C/mV$$

It has been found experimentally that the K factor should vary less than several percent for all devices within a given device type class. The usual procedure is to perform a K factor calibration on a 10 to 12 piece sample from a device lot and determine the average K and standard deviation (σ). If σ is less than or equal to three percent of the average value of K, then the average value of K can be used for all devices within the lot. If σ is greater than the average value of K, then all the devices in the lot shall be calibrated and the individual values of K shall be used in thermal resistance calculations.

5. Test procedure.

5.1 Calibration. K factor shall be determined according to the procedure outlined in 4.

5.2 Reference point temperature. The reference point is usually chosen to be on the bottom of the transistor case directly below the semiconductor chip. Reference temperature point location shall be specified and its temperature should be monitored using the thermocouple mentioned in 3.1 during the preliminary testing. If it is ascertained that T_{Xf} increases by more than +5°C during the power pulse, then either the heating power pulse magnitude shall be decreased, the DUT shall be mounted in a temperature controlled heat sink, or the calculated value of thermal resistance shall be corrected to take into account the thermal resistance associated with the temperature rise of the reference point.

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5.3 Thermal measurements. The following sequence of tests and measurements shall be made:

a. Prior to the power pulse:

(1) Establish reference point temperature: T_{Xi}.

(2) Apply measurement current: I_M.

(3) Measure gate-source voltage drop: $V_{GSf(i)}$ (A measurement of the initial (T_J)).

b. Heating pulse parameters:

(1) Maintain measurement current: I_M.

(2) Apply drain-source heating voltage: V_H.

(3) Measure drain heating current: I_H.

(4) Allow heating condition to exist for the required heating pulse width: t_H.

(5) Measure reference point temperature: T_{Xf}, at the end of heating pulse width.

c. Post-power pulse measurements:

(1) Maintain measurement current: I_M.

(2) Measure gate-source voltage drop: $V_{GSf}(f)$ (A measurement of the final (T_J)).

(3) Determine time delay between the end of the power pulse and the completion of the $V_{GSf(f)}$ measurement as defined by the waveform of figure 3104-4.

5.4 Thermal resistance. The value of thermal resistance, θ_{JX}, is calculated from the following formula:

$$\theta_{JX} = \frac{\Delta T_J}{P_H} = \frac{K\,|V_{GSF(f)} - V_{GSf(i)}|}{(I_H)(V_H)}$$

This value of thermal resistance will have to be corrected if T_{Xf} is greater than TX_i. The correction consists of subtracting out the component of thermal resistance due to the heat flow path from the reference point (typically the device case) to the heat sink and the environment. This thermal resistance component has a value calculated as follows:

$$\theta_{X\text{-}HS} = \frac{\Delta T_X}{P_H} = \frac{(T_{Xf} - T_{Xi})}{(I_H)(V_H)}$$

Then:

$$\underbrace{\theta_{JX}\,|}_{\text{Corrected}} = \underbrace{\theta_{JX}\,|}_{\text{Calculated}} - \theta_{X\text{-}HS}$$

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An additional correction may be required because of the fast cooling of a typical MOSFET heat source area. This requires that the thermal resistance measurements be made for two different values of t_{MD}. Care shall be taken to ensure that the shorter of the chosen t_{MD} values does not lie within the non-thermal (i.e, electrical) switching transient region. Similarly, if the longer t_{MD} value is too large, the resultant value of θ_{JX} will be too small for an accurate measurement due to device cooling. The correction for the calculated thermal resistance is given below for test conditions in which I_M, V_H, and t_H remain the same for both tests.

$$\theta_{JX} = \theta_{JX} = \theta_{JX} \mid = \left| \frac{\theta_{JX}2 - \theta_{JX}1}{t_{MD1}^{1/2} - t_{MD2}^{1/2}} \right|$$

calculated value

6. Test conditions and measurements to be specified and recorded.

6.1 K factor calibration.

a. Specify the following test conditions:

(1) I_M current magnitude ___mA
(See applicable specification sheet for current value.)

(2) Initial junction temperature ___°C
(Normally +25°C ±5°C.)

(3) Final junction temperature ___°C
(Normally +100°C ±10°C.)

b. Record the following data:

(1) Initial $V_{GSf(i)}$ voltage ___mV

(2) Final $V_{GSf(f)}$ voltage ___mV

c. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_{J1} - T_{J2}}{V_{GSf1} - V_{GSf2}} \right| \ °C/mV$$

d. For die attachment evaluation, this step may not be necessary (see 4.1).

6.2 Thermal impedance measurements.

6.2.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___mA
(Shall be same as used for K factor calibration)

b. V_H drain-source heating voltage ___V

c. t_H heating time ___s

d. t_{MD} measurement time delay ___µs

e. t_{SW} sample window time ___µs

NOTE: The value of V_H is usually chosen to produce an I_H value that results in a P_H approximately two-thirds of the device rated power dissipation.

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6.2.2 Record data. Record the following data:

a. T_{Xi} initial reference temperature ___°C

b. T_{Xf} final reference temperature ___°C

c. I_H current during heating time ___A

6.2.2.1 ΔV_{GSf} data:

ΔV_{GSf} ___mV

6.2.2.2 V_{GSf} data:

a. $V_{GSf(i)}$ initial gate-source voltage ___V

b. $V_{GSf(f)}$ final gate-source voltage ___V

6.2.2.3 θ_{JX} data:

θ_{JX} ___°C/W

NOTE: T_X measurements are not required if the t_H value meets the requirements stated in 5.2.

6.2.3 Thermal impedance calculations. Using the data collected in 6.2.2 and the procedure and equations shown in 5.4, calculate the thermal resistance.

6.3 ΔV_{GSF} measurements for screening. These measurements are made for t_H values that meet the intent of 4.1 and the requirements stated in 5.2.

6.3.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___mA

b. V_H drain-source heating voltage ___V

c. t_H heating time ___s

d. t_{MD} measurement time delay ___µs

e. t_{SW} sample window time ___µs

NOTE: The value of V_H is usually chosen to produce an I_H value that results in a P_H equal to or greater than the values used for thermal impedance measurements.

6.3.2 Specified limits. Data from one or more of the following is compared to the specified limits:

6.3.2.1 ΔV_{GSf} data:

ΔV_{GSf} ___mV

6.3.2.2 V_{GSf} data:

a. $V_{GSf(i)}$ initial gate-source voltage ___V

b. $V_{GSf(f)}$ final gate-source voltage ___V

Compute ΔV_{SD} ___mV

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6.3.2.3 ΔT_J data. Optionally calculate ΔT_J if the K factor results (see 4. and 6.1) produce a σ greater than three percent of the average value of K and if the I_H variation between devices to be compared is relatively small.

$$\Delta T_J = K(\Delta V_{GSf})\,°C$$

NOTE: The test apparatus shall be capable of directly providing a computed value of ΔT_J.

6.3.2.4 CU data. Optionally calculate CU for comparison purposes if the K factor results (see 4. and 6.1) produce a σ less than three percent of the average value of K and if the I_H variation between devices to be compared is relatively large.

CU = comparison unit

CU = $\Delta V_{GSf}/I_H$ mV/A

NOTE: The test apparatus may be capable of directly providing a computed value of CU.

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METHOD 3105.1

MEASUREMENT METHOD FOR THERMAL RESISTANCE OF A BRIDGE RECTIFIER ASSEMBLY

1. Purpose. This test describes a means to cause current to flow alternately through the legs of a single-phase or three-phase bridge assembly under conditions to make it feasible to determine~~s~~ its effective thermal resistance. The bridge is operated under steady-state (I_O) conditions and the current in each leg is interrupted while readings are taken from which to calculate thermal resistance.

2. Symbols and definitions. The following symbols and terminology shall apply for the purposes of this test method:

a. V_F: The forward-biased junction voltage of the DUT used for (T_J) sensing. For bridge, this applies to individual legs (i.e., one ac to one dc terminal).

b. V_{F1}: The forward voltage at room temperature at I_{ref}.

c. V_{F2}: The forward voltage at I_{ref} and +100°C above that at V_{F1}.

d. $V_{F2}A$: The computed forward voltage at I_{ref} and at maximum rated T_J.

e. V_{F3}: The initial V_F value at I_{ref} before the application of heating power, with the device at rated case temperature.

f. V_{F4}: The final V_F value at I_{ref} after stabilization of temperatures due to the application of rated current at rated case temperature.

g. ΔV_F: The change in the TSP V_F, due to the application of heating power to the DUT in volts.

h. V_{FH}: The maximum forward voltage resulting from the application of I_O to the DUT.

i. I_O: The rated average current applied to the DUT.

j. I_{ref}: The measurement current used to forward-bias the temperature sensing diode junction for measurement of V_F.

k. TCVF: Voltage-temperature coefficient of V_F with respect to T_J at a fixed value of I_{ref} in V/°C.

l. T_J: The DUT junction temperature.

m. ΔT_J: The change in T_J caused by the application of I_O.

n. TSP: The temperature sensitive parameter (V_F).

o. t_{F4}: Step trace time.

p. T_N: Reference case temperature for measuring V_N, when N = 1, 2, 3, or 4.

q. $R_{\theta JX}$: Thermal resistance from device junction to a defined reference point (e.g., lead or ambient) in units of °C/W.

r. $R_{\theta JC}$: Thermal resistance from device junction to a defined reference point on the outside surface of the case in units of °C/W.

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3. Test circuit. The apparatus required for this test shall include the following, configured as shown on figures 3105-1 and 3105-2.

a. A source of 60 Hz, single or three-phase sine wave (AC) capable of being adjusted to the desired value of I_O and able to supply the V_{FH} value required by the DUT. The current source should be able to maintain the desired current to within ±2 percent during the entire time needed for temperature stabilization and measurements.

b. A constant current source to supply I_{REF} with sufficient compliance voltage range to turn on fully the junction of the diode leg being measured.

c. Anti-parallel fast recovery rectifier diodes with ratings exceeding I_O, to provide isolation of the high current source from I_{REF} during commutation of I_O between legs.

d. A voltage measurement circuit capable of accurately making the V_F measurements within the available time interval (when the anti-parallel diodes are not conducting), with millivolt resolution.

4. Procedure. Refer to figures 3105-1 and 3105-2, test circuits for single- and three-phase bridges.

a. With S1 open, and DUT at +20°C to +30°C (temperature T_1), read V_{F1} of each leg at current I_{REF}. Elevate the device temperature to +100°C above temperature T_1 (temperature T_2). Allow the device to stabilize until the junction temperature is at T_2. Read V_{F2} of each leg at I_{REF} current. Compute the TCVF of each leg as follows:

$$TCVF = (V_{F1} - V_{F2}) / +100°C$$

Compute the expected V_{F2A} at T_J = maximum rated as follows:

$$V_{F2A} = V_{F1} - [(TCVF) \times (T_{Jmax} - T_1)]$$

Determine the average TCVF and the standard deviation of the TCVF from the readings on each leg. If the standard deviation is less than or equal to three percent of the average value of TCVF, TCVF may be used for all devices. If the standard deviation is greater than three percent of the average value of TCVF, then the individual values of TCVF shall be used in determining the performance of the bridge.

b. With the device held at T_3, at or below rated case temperature of I_O, close S1 and read V_{F3} for each leg.

c. After closing S1, adjust the power source, the load resistor, or both to obtain the maximum rated I_O (either I_{O1} or I_{O2}, depending on the rated T_C selected) and readjust the case temperature to the chosen rated value. Allow the device to achieve stable junction temperatures (see note 1).

d. Measure V_{F4} (see figure 3105-2) for each leg at the same reference current (±1 percent) as in steps 4.a. and 4.b. (The instrumentation used to measure V_{F4} must have sufficient resolution to read it within 2 mV or 2 percent).

NOTE: If V_{F3} for the leg is greater than V_{F2}, T_J is less than T_{Jmax}.

e. Measure V_{FH} for each leg.

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f. Compute thermal resistance as follows:

(1) Compute $\Delta V_F = V_{F4} - V_{F3}$ for each leg.

(2) Compute $\Delta T_J = \frac{\Delta V_F}{TCVF}$ 1/

(3) Compute $R_{\theta JC}$ of the full bridge: $R_{\theta JC} = \frac{\Delta T_{JC}}{I_o \, x \, 2V_{FH}}$

Where: ΔT_J is the average of all legs. V_{FH} is the average of all legs and I_O is the rectified output current of the full bridge. 2/ 3/ 4/

5. Test condition to be specified.

I_O _____

T_C _____

I_{REF} _____

Frequency_____
(if other than 60 Hz)

6. Characteristics to be determined:

Steady-state thermal resistance. Unless otherwise specified, junction to care: _____°C/W.

1/ If, under power, the case is held to T_4, slightly above T_3, a corrected ΔT_J ($\Delta T_{J(corr)} = \Delta T_{JC} - (T_4 - T_3)$) should be used for step 4 f(2).

2/ Step 4 f(3) gives R_{th} for the bridge. The average per leg R_{th} for a single-phase bridge is four times the value; six times for a three-phase bridge (see 3/).

3/ If desired, R_{th} of individual legs may be computed from the individual values of ΔT_{JC} and V_{FH}.

4/ The power dissipated I_O x $2V_{FH}$ is a reasonable approximation.

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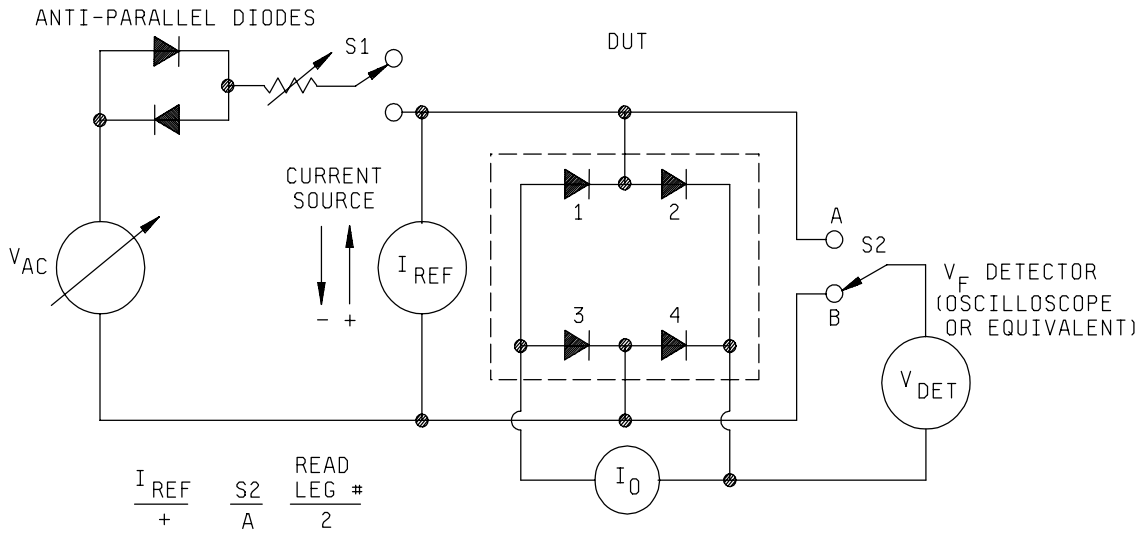

I_{REF}	S2	READ LEG #
+	A	2
+	B	3
−	B	4
−	A	1

NOTES:

1. All voltage measurements shall be made using leads Kelvin-connected directly to the bridge terminals.
2. V_{AC} is adjusted so that the V_{F4} step (t_{F4}) shown on figure 3105-3 is 100 μs ±50 μs and is clearly defined. A typical V_{AC} might be 10 volts peak. Bridges with parasitic inductive components shall adjust V_{AC} so that after the inductive ringing settles, the V_{F4} step on figure 3105-3 (t_{F4}) is 100 μs ±50 μs.

FIGURE 3105-1. Single-phase bridge.

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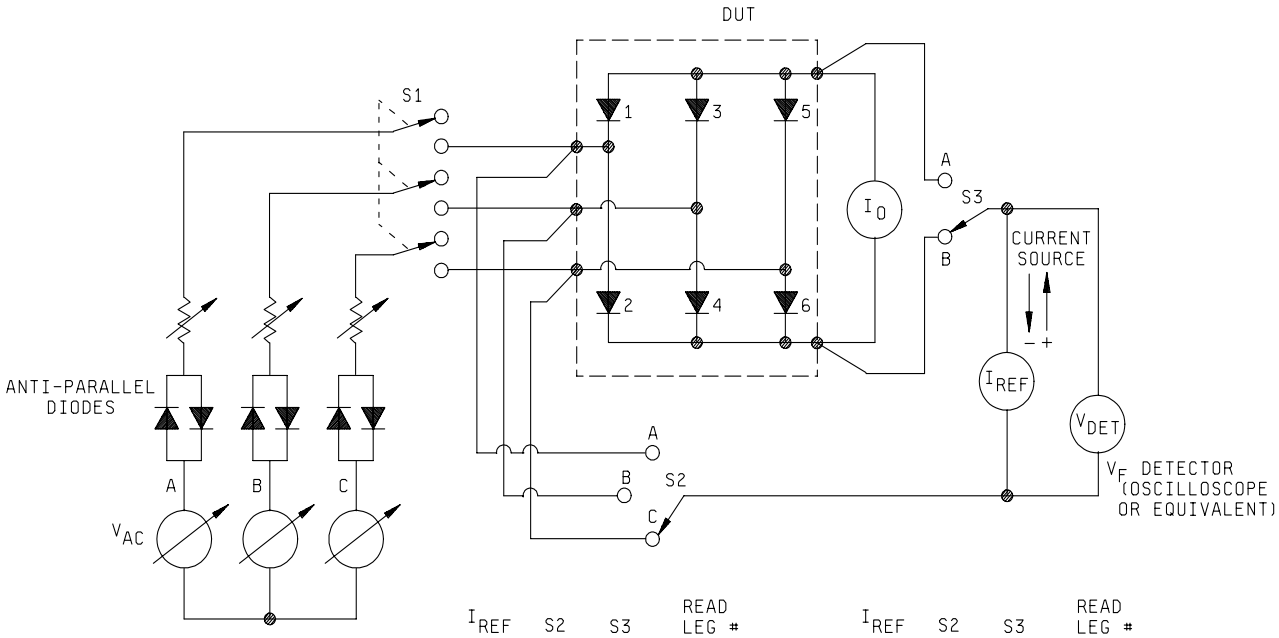

I_{REF}	S2	S3	READ LEG #
+	A	A	1
+	B	A	3
+	C	A	5

I_{REF}	S2	S3	READ LEG #
−	A	B	2
−	B	B	4
−	C	B	6

NOTES:

1. All voltage measurements shall be made using leads Kelvin-connected directly to the bridge terminals.
2. V_{AC} is adjusted so that the V_{F4} step (t_{F4}) shown on figure 3105-3 is 100 μs ±50 μs and is clearly defined. A typical V_{AC} might be 10 volts peak. Bridges with parasitic inductive components shall adjust V_{AC} so that after the inductive ringing settles, the V_{F4} step on figure 3105-3 (t_{F4}) is 100 μs ±50 μs.

FIGURE 3105-2. Three-phase bridge.

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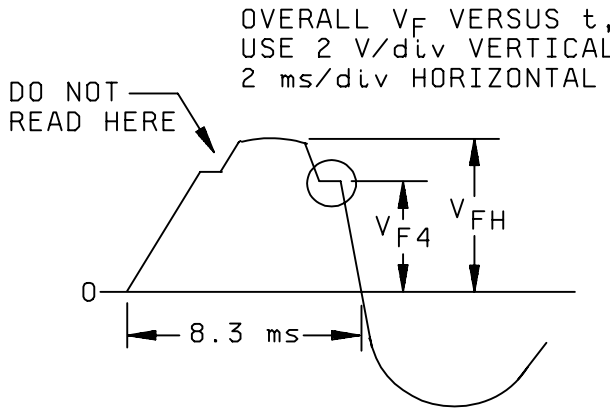
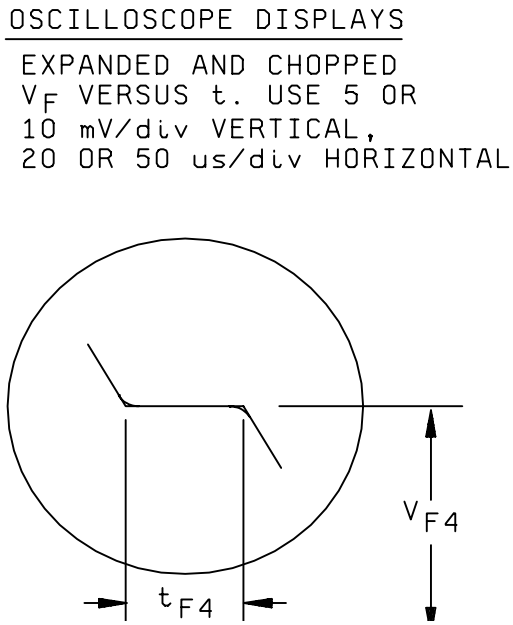


NOTE: V_{F4} step trace is provided when anti-parallel diodes in circuit briefly commutate off (the ac current passes through zero during each cooling cycle of individual bridge legs under ac test conditions.)



NOTES: 1. Polarity shown applies when I_{REF} is positive. The trace in inverted when I_{REF} is negative.

2. V_{AC} is adjusted so that the V_{F4} step (t_{F4}) shown on figure 3105-3 is 100 µs ±50 µs and is clearly defined. A typical V_{AC} might be 10 volts peak. Bridges with parasitic inductive components shall adjust V_{AC} so that after the inductive ringing settles, the V_{F4} step on figure 3105-3 (t_{F4}) is 100 µs ±50 µs.

FIGURE 3105-3. Oscilloscope displays.

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METHOD 3126

THERMAL RESISTANCE
(COLLECTOR CUTOFF CURRENT METHOD)

1. Purpose. The purpose of this test is to measure the thermal resistance of the device under the specified conditions. This method is particularly applicable to the measurement of germanium devices having relatively large thermal response times.

2. Test circuit. See figure 3126-1.

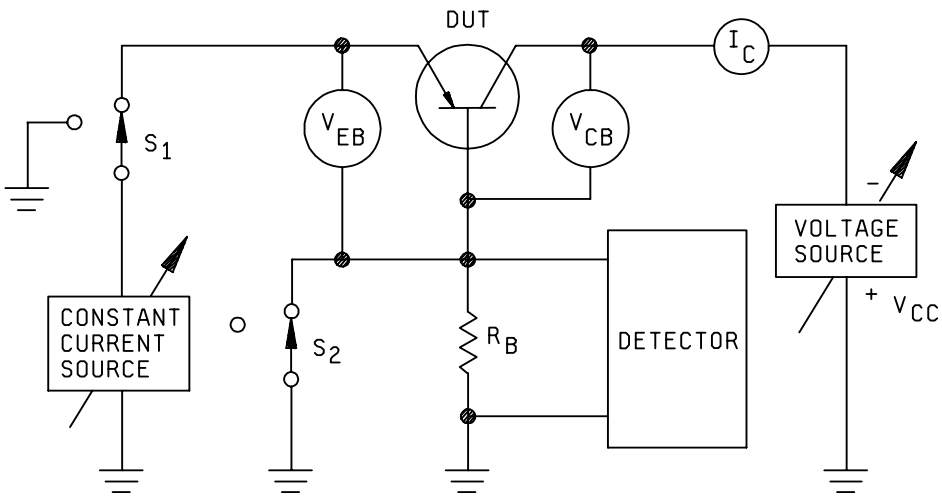

FIGURE 3126-1. Test circuit for thermal resistance (collector cutoff current method).

3. Procedure. Switches S_1 and S_2 are ganged and are operated such that the time they are closed (heat interval) is much larger than the time they are open (measurement interval). S_1 is arranged to open slightly before S_2 opens, and the interval between the opening of S_1 and S_2 is adjusted to be short compared to the thermal time constant of the device being measured. The length of the measurement interval should be short compared to the thermal response time of the transistor being measured. When both switches are open, the value of I_{CBO} is read as the drop across R_B. If the I_{CBO} varies during the measurement interval, the value immediately following the opening of S_2 should be read. A calibrated oscilloscope makes a convenient detector. Care should be taken that the collector voltage stays constant.

3.1 Measurement interval. The measurement is made in the following manner: The case, ambient, or other reference point is elevated to a high temperature T_2, not exceeding the maximum (T_J), and the cutoff current, I_{CBO}, read with the constant current source supplying no current. The reference temperature is then reduced to a lower temperature T_1, and power, P_1, is applied to heat the transistor, by increasing the current from the constant current source, until the same value of I_{CBO} is read as was read above.

$$\text{Then:} \quad \theta = \frac{T_2 - T_1}{P_1}$$

$$\text{Where:} \quad P_1 = (n)\,(I_C\ V_{CC} + I_E\ V_{EB})$$

$$n = \text{duty cycle} \left(\frac{t_{on}}{t_{total}}\right)$$

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4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test temperature (see 3.).

   b. Test voltages or currents (see 3.).

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METHOD 3131.5

STEADY-STATE THERMAL IMPEDANCE AND TRANSIENT THERMAL IMPEDANCE TESTING OF TRANSISTORS (DELTA BASE - EMITTER VOLTAGE METHOD)

1. Purpose. The purpose of this test is to determine the thermal performance of transistor devices. This can be done in two ways, steady-state thermal impedance or thermal transient testing. Steady-state thermal impedance (referred to as thermal resistance) determines the overall thermal performance of devices. A production oriented screening process, referred to as transient thermal impedance testing, is a subset of steady-state thermal impedance testing and determines the ability of the transistor chip-to-header interface to transfer heat from the chip to the header, and is a measure of the thermal quality of the die attachment. It is relevant to designs which use headers, or heat conducting plugs, with mass and thermal conductivity allowing effective discrimination of poor die attachments. This is particularly true with power devices. The method can be applied to small signal, power, switching, and Darlington transistors. This method is intended for production monitoring, incoming inspection, and pre-burn in screening applications. The measurement current (IM) shall be large enough to ensure that the Darlington output transistor is biased into the linear conduction mode of the temperature sensing measurement periods of the thermal test.

1.1 Background and scope for transient thermal impedance testing. Transient thermal impedance of semiconductor devices are sensitive to the presence of voids in the die attachment material between the semiconductor chip and package since voids impede the flow of heat from the chip to the substrate (package). Due to the difference in the thermal time constants of the chip and package, the measurement of transient thermal impedance can be made more sensitive to the presence of voids than can the measurement of steady-state thermal impedance. This is because the chip thermal time constant is generally several orders of magnitude shorter than that of the package. Thus, the heating power pulse width can be selected so that only the chip and the chip-to-substrate interface are heated during the pulse by using a pulse width somewhat greater than the chip thermal time constant but less than that of the substrate. Heating power pulse widths ranging from 1 to 400 ms for various package designs have been found to satisfy this criterion. This enables the detection of voids to be greatly enhanced, with the added advantage of not having to heat sink the device under test (DUT). Thus, the transient thermal impedance techniques are less time consuming than the measurement of thermal resistance for use as a manufacturing screen, process control, or incoming inspection measure for die attachment integrity evaluation.

2. Symbols and definitions. The following symbols and terminology shall apply for the purpose of this test method:

a. ΔT_J: The change in T_J caused by the application of P_H for a time equal to t_H.

b. ΔV_{BE}: The change in V_{BE}, (V_{BEi}-V_{BEf}) due to the application of heating power P_H to the DUT.

c. CU: The comparison unit, consisting of ΔV_{BE} divided by V_{BE}, that is used to normalize the transient thermal impedance for variations in power dissipation; in units of mV/V.

d. I_H: The collector current applied to the DUT during the heating period.

e. I_M: The measurement current applied to forward bias the junction for measurement of V_{BE}.

f. K: Thermal calibration factor equal to the reciprocal of VTC; in °C/mV.

g. P_H: The heating power applied to the DUT. $P_H = I_H . x V_{CE}$.

h. $R_{\theta JA}$: Steady-state. Thermal resistance from device junction to an ambient (world); in units of °C/W.

i. $R_{\theta JC}$: Steady-state. Thermal resistance from device junction to a point on the outside surface of the case immediately adjacent to the device chip; in units of °C/W.

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j. $R_{\theta JX}$: Steady-state. Thermal resistance from device junction to a defined reference point; in units of °C/W.

k. t_H: The duration of the P_H pulse.

l. ti: The time after application of the measurement current (IM) and before application of the P_H pulse.

m. T_J: The DUT T_J.

n. t_{MD}: Measurement delay time is the time from the end of the P_H pulse to the beginning of the sample window time (t_{SW}). Delay shall be sufficient in length to allow for attenuation of switching transients to occur. The delay time will vary according to the length of the cable to test fixture and associated fixture inductances.

o. TSP: The temperature sensitive parameter; V_{BE}.

p. t_{SW}: Sample window time during which final V_{BE} measurement is made. The value of t_{SW} should be small; and occur at precisely the conclusion of tMD. It can approach zero if an oscilloscope is used for manual measurements and no transient effects are present.

q. V_{BE}: The forward-biased base emitter junction voltage of the DUT used for T_J sensing.

V_{BEi}: The initial V_{BE} value during application of measurement current (IM) and before application of heating power.

V_{BEf}: The final V_{BE} value during the sample window time (t_{SW}) after application and subsequent removal of heating power.

r. V_{CE}: The voltage between the collector and emitter. V_{CE} is constant throughout the test.

s. VTC: Voltage-temperature coefficient of V_{BE} with respect to T_J at a fixed value of I_M; in mV/°C.

t. $Z_{\theta JC}$: Transient. Thermal impedance from device junction to a point on the outside surface of the case immediately adjacent to the device chip measured using time equal time constant of device; in units of °C/W.

u. $Z_{\theta JX}$: Transient. Thermal impedance from device junction to a time defined reference point; in units of °C/W.

3. Apparatus. The apparatus required for this test shall include the following, configured as shown on figure 3131-1, as applicable to the specified test procedure:

a. A constant current source capable of adjustment to the desired value of I_H and able to supply the V_{BE} value required by the DUT. The current source should be able to maintain the desired current to within ±2 percent during the entire length of heating time.

b. A constant current source to supply I_M with sufficient voltage compliance to turn the TSP junction fully on.

c. An electronic switch capable of switching between the heating period conditions and measurement conditions in a time frame short enough to avoid DUT cooling during the transition; this typically requires switching in the microsecond or tens of microseconds range.

d. A voltage measurement circuit capable of accurately making the V_{BEf} measurement within the time frame with millivolt resolution.

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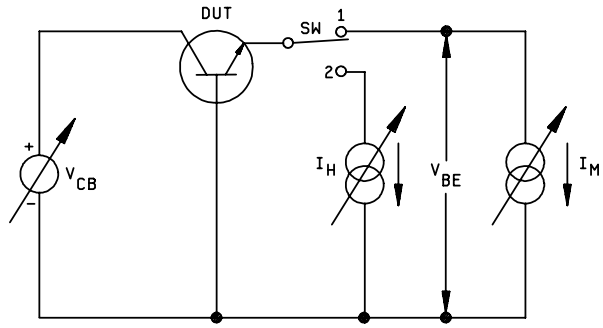

FIGURE 3131-1. Thermal impedance testing setup for transistors.

4. Test operation.

4.1 General description. The test begins with the adjustment of I_M and I_H to the desired values. The value of I_H is usually at least 50 times greater than the value of I_M. Then with the electronic switch in position 1, the value of V_{BEi} is measured. The switch is then moved to position 2 for a length of time equal to t_H and the value of V_{BE} is measured. Finally, at the conclusion of t_H, the switch is again moved to position 1 and the V_{BEf} value is measured within a time period defined by t_{MD} (or t_{MD} + t_{SW}, depending on the definitions stated previously). The two current sources are then turned off at the completion of the test.

4.1.2 Thermal resistance characterization of dual and quad bipolar transistors. Traditionally, thermal resistance has been called out on specification sheets without any clarification as to whether the values are for each element or all elements in parallel. While the assumption has been that the specifications for thermal resistance apply to all elements in parallel, there has been no procedure on how to do this. The thermal resistance test setup cannot directly parallel the transistors because the higher gain element will draw all of the current from the elements. Further complicating this scenario is the case of complimentary NPN-PNP pairs and quads. Circuitry necessary for measuring thermal resistance and thermal impedance is prohibitive. It is recommended that thermal resistance and thermal impedance be measured on each element individually while the other elements are un-powered. These individual readings cannot be combined in any way to yield the total rating. This means that there is no universal method to measure the dual or quad as a whole and the individual device specification shall not require such a measurement. Overall power rating can be derived from similar packages employing single elements.

4.1.3 Thermal resistance characterization of small emitter bipolar transistors. The accepted practice for measuring junction temperature for thermal impedance and thermal resistance measurements of BJTs is to employ the base-emitter (BE) junction as the temperature sensor. However, since the base area is always larger than the emitter area, some measurement errors can arise. When the ratio of emitter area (A_E) to base area (A_B) is greater than 0.5 (i.e. $A_E/A_B > 0.5$), this error is negligible, especially for long heating times. However, for small emitter BJT structures (low capacitance, high frequency, low current) this ratio can fall significantly below 0.5. For example, a BJT with two emitter elements sized each at 1x2 mils would have an emitter area of 4 mil^2 total. That same structure could have a base region of 6x6 mils for a base area of 36 mil^2 total. This makes A_E/A_B = 4/36 =0.11, a value considerably lower than the 0.5 guideline mentioned above. The problem with structures where A_E/A_B is below 0.5 is that you will be measuring a thermal response rather than a thermal impedance. A thermal response is defined as a measurement with no usable readings other that being able to be used for comparison. This measurement will no longer be able to tell the peak temperature of the emitter because the emitter region will be hotter than parts of the base and base contact region giving an average temperature rather than a peak temperature. This error is greatest for short measurement times where the radial temperature gradient is greatest and diminishes significantly for steady-state thermal resistance measurements where the entire chip has had a chance to heat up thereby reducing the error causing temperature gradient. The meaning of all this to the user and to the supplier is that, for small emitter area BJTs, only thermal response will be available for process monitor and not thermal impedance. Also, true thermal resistance may be higher than measured especially if the BJT is tested case-mounted rather than free-air. Where users require an accurate thermal impedance verses heating time curve, that curve will either have to be calculated or not be supplied at all. There is no currently accepted way in this test method to verify a BJT against a calculated curve.

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4.2 Notes.

a. Some test equipment may provide a ΔV_{BE} directly instead of V_{BEi} and V_{BEf}; this is an acceptable alternative. Record the value of ΔV_{BE}.

b. Some test equipment may provide $Z_{\theta JX}$ directly instead of V_{BEi} and V_{BEf} for thermal resistance calculations; this is an acceptable alternative. Record the value of $Z_{\theta JX}$.

c. Alternative waveforms, as may be generated by ATE using the general principles of this method, may be used upon approval of the qualifying activity.

d. Some test equipment allows you to set V_{CB} and not V_{CE}. This is acceptable provided that you measure V_{BE} at some point in the procedure and add that value to V_{CB} to obtain V_{CE}.

5. Acceptance limit.

5.1 General discussion. Variations in transistor characteristics from one manufacturer to another cause difficulty in establishing a single acceptance limit for all transistors tested to a given specification sheet. Ideally, a single acceptance limit value for ΔV_{BE} would be the simplest approach. However, different design, materials, and processes can alter the resultant ΔV_{BE} value for a given set of test conditions. Listed below are several different approaches to defining acceptance limits. The ΔV_{BE} limit is the simplest approach and is usually selected for screening purposes. Paragraphs 5.3 through 5.6 require increasingly greater detail or effort.

5.2 ΔV_{BE} limit. A single ΔV_{BE} limit is practical if the K factor and V_{BE} values for all transistors tested to a given specification sheet are nearly identical. Since these values may be different for different manufacturers, the use of different limits is likely to more accurately achieve the desired intent. (A lower limit does not indicate a better die bond when comparing different product sources.) The transistor specification sheet would list the following test conditions and measurement parameters:

a. I_H (in A).

b. t_H (in ms).

c. I_M (in mA).

d. t_{MD} (in µs).

e. t_{SW} (in µs).

f. ΔV_{BE} (maximum limit value, in mV).

5.3 ΔT_J limit. (Much more involved than ΔV_{BE}, but useful for examining questionable devices.) Since ΔT_J is the product of K (in accordance with 6 herein) and ΔV_{BE}, this approach is the same as defining a maximum acceptable T_J rise for a given set of test conditions.

5.4 CU limit. (Slightly more involved than ΔT_J.) The ΔT_J limit approach described above does not take into account potential power dissipation variations between devices. The V_{BE} value can vary, depending on chip design and size, thus causing the power dissipation during the heating time to be different from device to device. This variation will be small within a lot of devices produced by a single manufacturer but may be large between manufacturers. A CU limit value takes into account variations in power dissipation due to differences in V_{BE} by dividing the ΔV_{BE} value by V_{BE}.

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5.5 (K•CU) limit. (Slightly more involved but provides greater detail.) This is a combinational approach that takes into account both K factor and power dissipation variations between devices.

5.6 $Z_{\theta JX}$ limit. (For full characterization; not required for screening purposes, but preferred if the proper ATE is available.) The transient thermal impedance approach uses an absolute magnitude value specification that overcomes the problems associated with the other approaches. Transient thermal impedance is time dependent and is calculated as follows:

$$Z_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_{BE})}{(I_H)(V_H)} \right| {}^{\circ}\text{C/W}$$

5.7 $R_{\theta JX}$ limit. (For thermal resistance specification testing.) The thermal resistance to some defined point, such as the case, is an absolute magnitude value specification used for equilibrium conditions. The t_H heating time shall therefore be extended to longer times (typically 20 to 50 seconds). In the example of $R_{\theta JC}$ measurements, the case shall be carefully stabilized and monitored in temperature which requires an infinite heat sink for optimum results. The ΔT_J is the difference in T_J to the case temperature for the example of $R_{\theta JC}$.

$$R_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_{BE})}{(I_H)(V_H)} \right| {}^{\circ}\text{C/W}$$

5.8 General comment for transient thermal impedance testing. One potential problem in using the transient thermal impedance testing approach lies in trying to make accurate enough measurements with sufficient resolution to distinguish between acceptable and non-acceptable transistors. As the DUT current handling capability increases, the thermal impedance under transient conditions will become a very small value. This raises the potential for rejecting good devices and accepting bad ones. Higher I_H values shall be used in this case.

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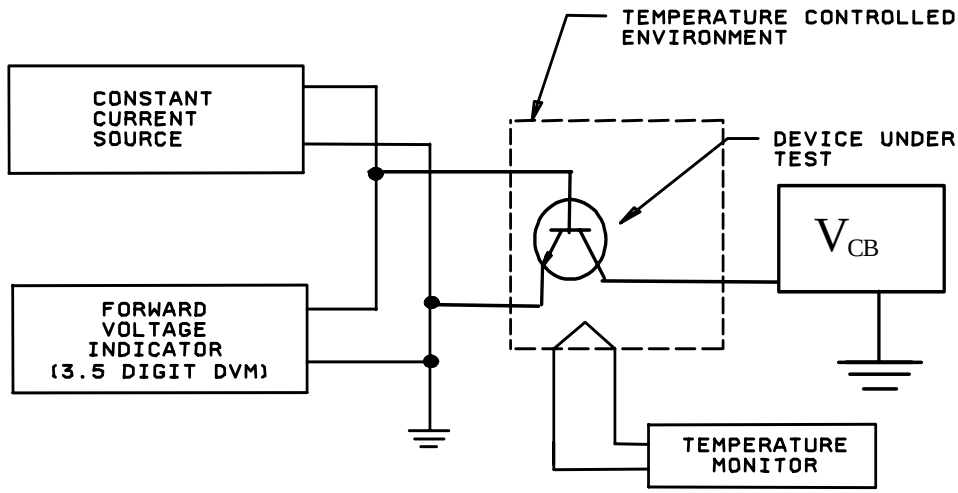
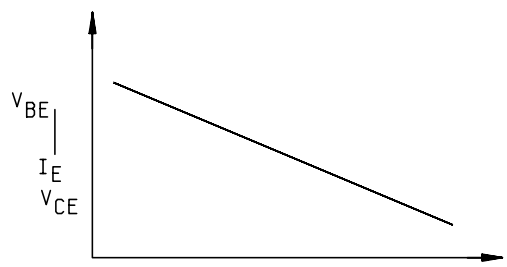
6. Measurement of the TSP V_{BE}. The calibration of V_{BE} versus T_J is accomplished by monitoring V_{BE} for the required value of I_M as the environmental temperature (and thus the DUT temperature), and is varied by external heating. It is not required if the acceptance limit is ΔV_{BE} (see 5.2), but is relevant to the other acceptance criteria (see 5.3 through 5.6). The magnitude of I_M shall be chosen so that V_{BE} is a linearly decreasing function over the normal T_J range of the device. I_M shall be large enough to ensure that the base-emitter junction is turned on but not large enough to cause significant self heating. An example of the measurement method and resulting calibration curve is shown on figure 3131-2.



Step 1: Measure V_{BE1} at T_{J1} using I_M

Step 2: Measure V_{BE2} at T_{J2} using I_M

Step 3: $K = \left| \frac{T_{J2} - T_{J1}}{V_{BE2} - V_{BE1}} \right| °C/mV$



NOTES:

1. I_M: Shall be large enough to overcome surface leakage effects but small enough not to cause significant self heating.

2. T_J: Is externally applied (e.g., via oven, liquid) environment.

FIGURE 3131-2. Example curve of V_{BE} versus T_J.

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A calibration factor K (which is the reciprocal of the slope of the curve on figure 3131-2) can be defined as:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{BE2} - V_{BE1}} \right| \ °C/mV$$

The K factor is used to calibrate the DUT such that the measured forward voltage drop corresponds to the temperature of the junction at a given bias condition. In order to ensure accurate results, the bias conditions used to determine the K factor shall be chosen such that the application is duplicated. Therefore, the results will be unique for each particular biasing condition and should be reestablished for different values of base or collector. This method should be used for each of the following conditions: Transient thermal impedance, burn-in, and life-tests. Verify actual TJ seen by a device in field applications.

NOTE: It is important that the range of temperatures that K-factor is measured over approximately correlates to the range of temperature used for thermal measurements. It is wise to characterize your product at least once over a broad temperature range using increments of 25°C.

It has been found experimentally that the K-factor variation for all devices within a given device type class is small. The usual procedure is to perform a K factor calibration on a 10 piece to 12 piece sample from a device lot and determine the average K and standard deviation (σ). If σ is less than or equal to 3 percent of the average value of K, then the average value of K can be used for all devices within the lot. If σ is greater than 3 percent of the average value of K, then all the devices in the lot shall be calibrated and the individual values of K shall be used in determining device acceptance. As an alternative to using individual values of K, the manufacture may establish internal limits unique to their product that ensures atypical product removal from the population (lot-to-lot and within-the-lot). The manufacturer shall use statistic techniques to establish the limits to the satisfaction of the Government.

7. Establishment of test conditions and acceptance limits. Thermal resistance measurements require that I_H be equal to the required value stated in the device specification sheet, typically at rated current or higher. Values for t_H, t_{MD}, and heat sink conditions are also taken from the device specification sheet. The steps shown below are primarily for transient thermal impedance testing and thermal characterization purposes.

The following steps describe how to set up the test conditions and determine the acceptance limits for implementing the transient thermal test for die attachment evaluation using the apparatus and definitions stated above.

7.1 Initial device testing procedure. The following steps describe in detail how to set up the apparatus described previously for proper testing of various transistors. Since this procedure thermally characterizes the transistor out to a point in heating time required to ensure heat propagation into the case (i.e., the $R_{\theta JX}$ condition), an appropriate heat sink should be used or the case temperature should be monitored.

Step 1: From a statistically valid sample, pick any one DUT to start the setup process. Set up the test apparatus as follows:

I_H = 1.0 A	(Or some other desired value near the DUT's normal operating current, typically higher for power transistors.)
t_H = 10 - 50 ms	Unless otherwise specified, for most devices rated up to 15 W power dissipation.
50 - 100 ms	Unless otherwise specified, for most devices rated up to 200 W power dissipation.
≥ 250 ms	For steady-state thermal impedance measurement. The pulse shall be shown to correlate to steady-state conditions before it can be substituted for steady-state condition.

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t_{MD} = 100 μs max — A different max value may be required by the specification or on power devices with inductive package elements which generate non-thermal electrical transients; unless otherwise specified, this would be observed in the t_3 region of figure 3131-3.

I_M = 10 mA — (Or some nominal value approximately two percent, or less, of I_H.)

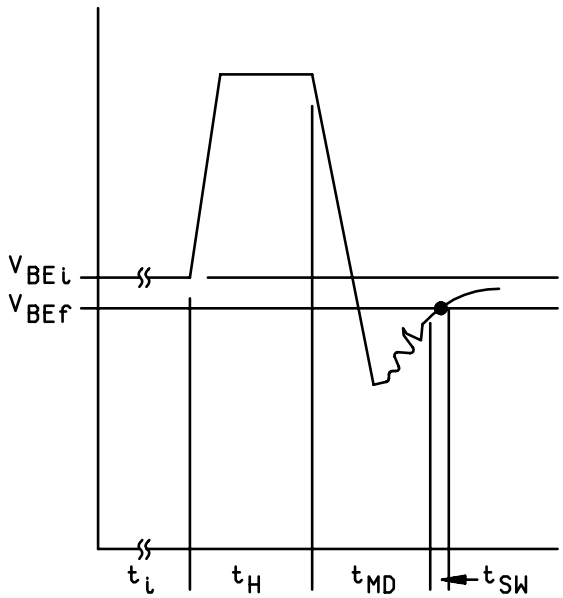

FIGURE 3131-3. Thermal impedance testing waveforms.

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Step 2: Insert device into the apparatus test fixture and initiate a test. (For best results, a test fixture that offers some form of heat sinking would be desirable. Heat sinking is not needed if either the power dissipation during the test is well within the DUT's free air rating or the maximum heating time is limited to less than that required for the heat to propagate through the case.)

Step 3: If ΔT_J is at least high enough to resolve thermal impedance/resistance to within 1 percent and the DUT does not exceed T_J(max), the applied power is likely appropriate. High power case-mounted DUTs will tend to have lower ΔT_J while air cooled DUTs may need the higher ΔT_J since their thermal resistance depends upon operating temperature.

If ΔT_J is less than specified above, return to 7.1, step 1 and increase heating power into device by increasing I_H.

If ΔT_J is greater than the safe junction operating temperature, it is required to reduce the heating power by returning to 7.1, step 1 and reducing I_H.

NOTE: The test equipment shall be capable of resolving ΔV_{BE} to within 5 percent. If not, the higher value of ΔV_{BE} shall be selected until the 5 percent tolerance is met. Two different devices can have the same T_J rise even when P_H is different, due to widely differing V_{BE}. Within a given lot, however, a higher V_{BE} is more likely to result in a higher T_J rise. For such examples, this screen can be more accurately accomplished using the CU value. As defined in 2.c herein, CU provides a comparison unit that takes into account different device V_{BE} values for a given I_H test condition.

Step 4: Test each of the sample devices and record the data detailed in 8.1.

Step 5: Select out the devices with the highest and lowest values of CU or $Z_{\theta JX}$ and put the remaining devices aside.

The ΔV_{BE} values can be used instead of CU or $Z_{\theta JX}$ if the measured values of V_{BE} are very tightly grouped around the average value.

Step 6: Using the devices from 7.1, step 5, collect and plot the heating curve data for the two devices in a manner similar to the examples shown on figure 3131-4.

Step 7: Interpretation of the heating curves is the next step. Realizing that the thermal characteristics of identical chips should be the same if the t_H is less than or equal to the thermal time constant of the chip, the two curves should start out the same for the low values of t_H. Non-identical chips (thinner or smaller in cross section) will have completely different curves, even at the smaller values of t_H. As the value of t_H is increased, thereby exceeding the chip thermal constant, heat will have propagated through the chip into the die attachment region. Since the heating curve devices of 7.1, step 5 were specifically chosen for their difference, the curves of figure 3131-4 diverge after t_H reaches a value where the die attachment variance has an affect on the device T_J. Increasing t_H further will probably result in a flattening of the curve as the heating propagates in the device package. If the device package has little thermal mass and is not well mounted to a good heat sink, the curve will not flatten very much, but will show a definite change in slope.

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Step 8: Using the heating curve, select the appropriate value of t_H to correspond to the inflection point in the transition region between heat in the chip and heat in the package.

If there are several different elements in the heat flow path: Chip, die attachment, substrate, substrate attach, and package, for example in a hybrid, there will be several plateaus and transitions in the heating curve. Appropriate selection of t_H will optimize evaluation sensitivity to other attachment areas.

Step 9: Return to the apparatus and set t_H equal to the value determined from 7.1, step 8.

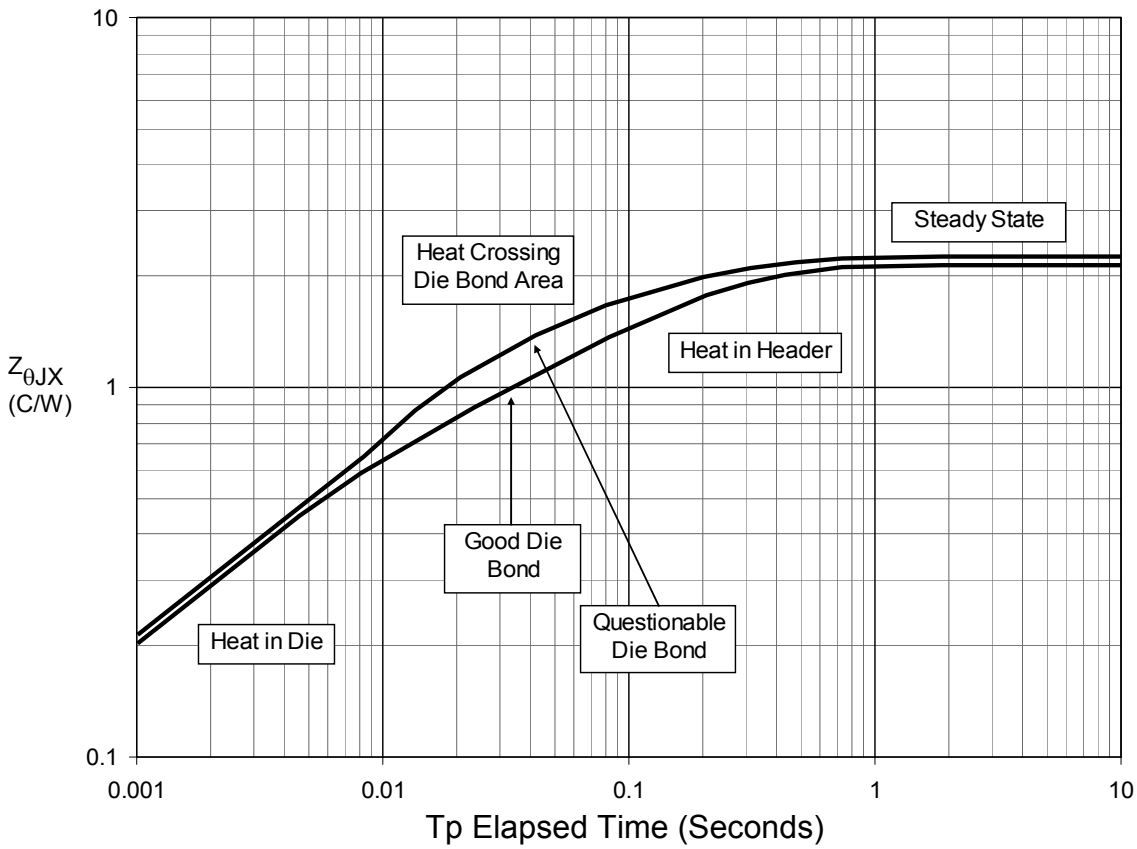

FIGURE 3131-4. Heating curves for two extreme devices.

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Step 10: Because the selected value of t_H is much less than that for thermal equilibrium, it is possible to significantly increase the P_H without degrading or destroying the device. The increased power dissipation within the DUT will result in higher ΔV_{BE} or CU values that will make determination of acceptable and non-acceptable devices much easier.

Step 11: The pass/fail limit, the cut-off point between acceptable and non-acceptable devices, can be established in a variety of ways:

a. Correlation to other die attachment evaluation methods, such as die shear and x-ray. While these two methods have little actual value from a thermal point of view, they do represent standardization methods as described in various standards.

b. Maximum allowable junction temperature variations between devices. Since the relationship between ΔT_J and ΔV_{BE} is about 0.5°C/mV for forward bias testing, or 0.25C/mV for Darlington transistors, the T_J spread between devices can be easily determined. The T_J predicts reliability. Conversely, the T_J spread necessary to meet the reliability projections can be translated to a ΔV_{BE} or CU value for pass/fail criteria.

To fully utilize this approach, it will be necessary to calibrate the devices for the exact value of the T_J to V_{BE} characteristic. The characteristic's slope, commonly referred to as K factor, is easily measured on a sample basis using a voltmeter, environmental chamber, temperature indicator, and a power supply setup as described in 6 herein. A simple set of equations yield the T_J once K and ΔV_{BE} are known:

$$\Delta T_J = (K)\ (\Delta V_{BE})$$

$$T_J = T_A + \Delta T_J$$

Where: T_A is the ambient or reference temperature. For thermal transient test conditions, this temperature is usually equivalent to case temperature (T_C) for case mounted devices.

c. From a statistically valid sample, the distribution of ΔV_{BE} or CU values should be a normal one with defective devices out of the normal range. Figure 3131-5 shows a ΔV_{BE} distribution for a sample lot of transistors. NOTE: The left-hand side of the histogram envelope is fairly well defined but the other side is greatly skewed to the right. This is because the left-hand side is constrained by the absolute best heat flow that can be obtained with a given chip assembly material and process unless a test method error is introduced. The other side has no such constraints because there is no limit as to how poorly a chip is mounted.

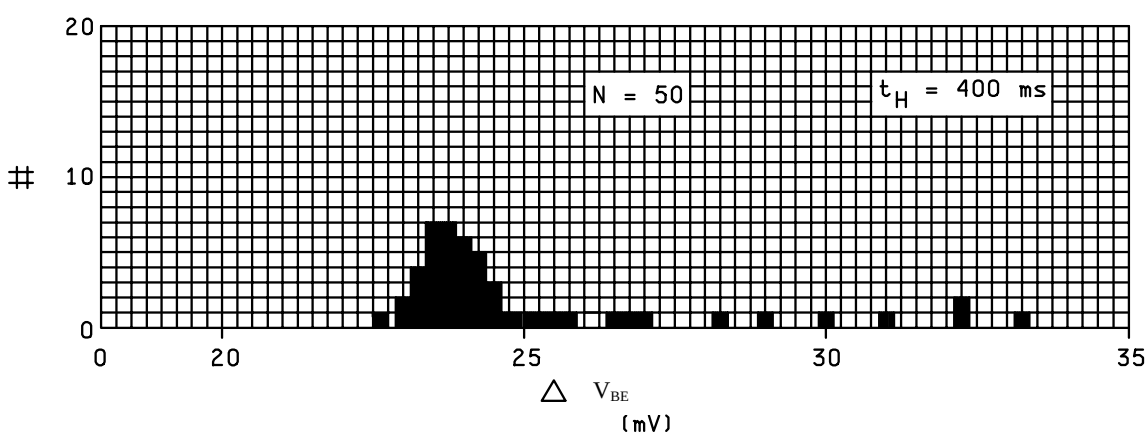

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FIGURE 3131-5. Typical ΔV_{BE} distribution.

The usual rule of thumb in setting the maximum limit for ΔV_{BE}, CU, or $Z_{\theta JX}$ is to use the distribution average value and three standard deviations (σ). For example:

$$|(\overline{\Delta V_{BE}})| = \Delta V_{BE} + X\sigma$$

high
limit

$$|(\overline{CU})| = CU + X\sigma$$

high
limit

$$|(\overline{Z_{\theta JX}})| = Z_{\theta JX} + X\sigma$$

high
limit

Where: X = 3 in most cases and $\overline{\Delta V_{BE}}$, $\overline{\Delta CU}$, and $\overline{\Delta Z_{\theta JX}}$ are the average distribution values.

The statistical data required is obtained by testing a statistically valid sample size of devices under the conditions of 7.1, step 11.

The maximum limit determined from this approach should be correlated to the transistor's specified thermal resistance. This will ensure that the ΔV_{BE} or CU limits do not pass DUTs that would fail the thermal resistance or transient thermal impedance requirements.

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Step 12: Once the test conditions and pass/fail limit have been determined, it is necessary only to record this information for future testing requirements of the same device in the same package. It is also recommended that a minimum limit is established to ensure a test method error or other anomaly is investigated.

Step 13: After the pass/fail limits are established, there shall be verification they correlate to good and bad bonded devices or the electrical properties such as surge.

The steps listed above are summarized in table 3131-I.

TABLE 3131-I. Summary of test procedure steps.

General description		Steps	Comments
A	Initial setup	1 through 4	Approximate instrument settings to find variations among devices in a statistically valid sample.
B	Heating curve generation	5 through 6	Using highest and lowest reading devices, generate heating curves.
C	Heating curve interpretation	7 through 9	Heating curve is used to find more appropriate value for t_H corresponding to heat in the die attachment area (for some other desired interface in the heat flow path).
D	Final setup	10	Heating power applied during t_H is increased in order to improve measurement sensitivity to variations among devices.
E	Pass-fail determination	11 through 12	A variety of methods is available such as JESD 34 for setting the fail limit; the statistical approach is the fastest and easiest to implement.
F	Verification	13	Mechanical / electrical correlation

7.2 Routine device thermal transient testing procedure. Once the proper control settings have been determined for a particular device type from a given manufacturing process or vendor, repeated testing of that device type simply requires that the same test conditions be used as previously determined. New device types, or the same devices manufactured with a different process, will require a repeat of 7.1 for proper thermal transient test conditions.

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8. Test conditions and measurements to be specified and recorded.

8.1 Transient thermal impedance-steady-state thermal impedance measurements.

8.1.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___ mA

b. I_H heating current ___ A

c. t_H heating time ___ ms

d. t_{MD} measurement time delay ___µs

e. t_{SW} sample window time __ µs

8.1.2 Data. Record the following data:

a. V_{BEi} initial forward voltage ___V

b. V_H heating voltage ___V

c. V_{BEf} final forward voltage ___V

NOTE: Some test equipment may provide a ΔV_{BE} instead of V_{BEi} and V_{BEf}; this is an acceptable alternative. Record the value of ΔV_{BE}.

Some test equipment may provide direct display of calculated CU or $Z_{\theta JX}$; this is an acceptable alternative. Record the value of CU or $Z_{\theta JX}$.

8.2 K factor calibration. (Optional for criteria 8.2.1.a or 8.2.1.b, mandatory for 8.2.1.c, 8.2.1.d, or 8.2.1.e.)

8.2.1 Test conditions. Specify the following test conditions:

a. I_M current magnitude ___mA

b. Initial junction temperature ___°C

c. Initial V_{BE} voltage ___mV

d. Final junction temperature ___°C
(See note in 6.0)

e. Final V_{BE} voltage ___mV

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8.2.2 K factor. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{BE2} - V_{BE1}} \right| \, °C/mV$$

K factor ___°C/mV

8.3 Specification limit calculations. One or more of the following should be measured or calculated, as stated on the device specification sheet (see 5.1):

a. ΔV_{BE} ___mV

b. CU ___mV/V

c. ΔT_J ___°C

d. K•CU ___°C/V

e. $Z_{\theta JX}$ ___°C/W

f. $R_{\theta JX}$ ___°C/W

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METHOD 3132

THERMAL RESISTANCE

(DC FORWARD VOLTAGE DROP, EMITTER BASE, CONTINUOUS METHOD)

1. Purpose. The purpose of this test is to measure the thermal resistance of the device under the specified conditions.

2. Test circuit. See figure 3132-1.

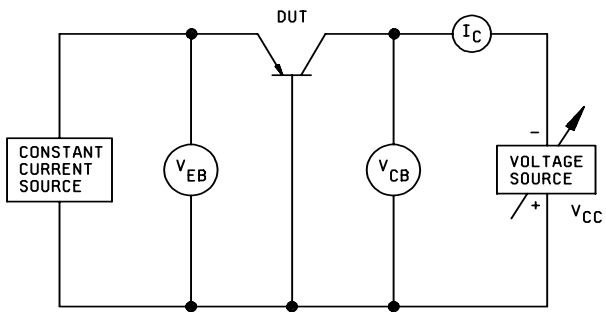

FIGURE 3132-1. Test circuit for thermal resistance (dc forward voltage drop, emitter base, continuous method).

3. Procedure. The measurement technique assumes that the forward emitter voltage drop varies with temperature. It further assumes that during the course of measurement, the variation in forward emitter voltage drop varies monotonically due to temperature and is much greater than that due to the variation with collector voltage.

3.1 Measurement. The measurement is made in the following manner: The case, ambient, or other reference point is elevated to a high temperature T_2, not exceeding the maximum-T_J. Current I_C is set to a value and a voltage applied to the collector base diode, V_2. The value of V_2 applied shall be low yet high enough so that the device is operating in a normal manner. V_{1EB} is read under these conditions. The reference temperature is reduced to a lower temperature T_1 and V_{CC} varied until the same value of V_{1EB} is read as was read above. The thermal resistance is then:

$$\theta = \frac{T_2 - T_1}{I_C (V_1 - V_2)}$$

Where: V_1 is the collector voltage applied at temperature T_1.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test temperatures.

b. I_C and V_2.

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METHOD 3136

THERMAL RESISTANCE

(FORWARD VOLTAGE DROP, COLLECTOR TO BASE, DIODE METHOD)

1. Purpose. The purpose of this test is to measure the thermal resistance of the device under the specified conditions. This method is particularly applicable to the measurement of germanium and silicon devices having relatively long thermal response times.

2. Test circuit. See figure 3136-1.

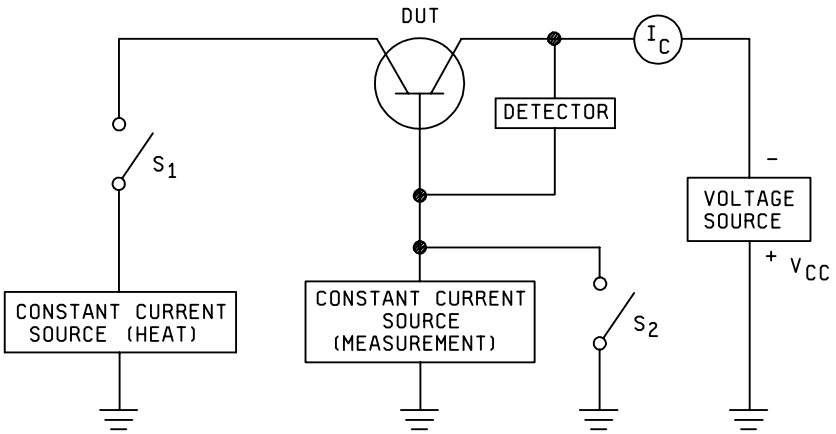

FIGURE 3136-1. Test circuit for thermal resistance (forward voltage drop, collector to base, diode method).

3. Procedure. Switches S_1 and S_2 are ganged switches and are so arranged that S_2 opens very shortly after S_1 opens and such that the delay between the openings is much shorter than the thermal response time of the device being measured. S_1 and S_2 should be closed (heat interval) for a much larger time than they are open (measurement interval) and the measurement interval should be short compared to the thermal response time of the device being measured.

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3.1 Measurement. The measurement is made in the following manner: The case, ambient, or other reference point is elevated to a high temperature T_2, not exceeding the maximum T_J, and the collector base voltage, V_{CB}, is read. This reading is made at the beginning of the measurement interval. An oscilloscope makes a convenient detector. The reference temperature is then reduced to a lower temperature, T_1. The heating power, P_1, is adjusted by adjusting the heating current source in the emitter circuit until the same value of V_{CB} is read as was read above. The value of Θ is calculated from the equation:

$$\theta = \frac{T_2 - T_1}{P_1}$$

Where: $P_1 = (n)\,(I_C\,V_{CC} + I_E\,V_{EB})$

$$and \;\; n = duty\,cycle\left[\frac{t_{on}}{t_{total}}\right]$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test temperature (see 3.1).

   b. Test voltages and currents (see 3.).

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METHOD 3141

THERMAL RESPONSE TIME

1. Purpose. The purpose of this test is to measure the time required for the junction to reach 90 percent of the final value of junction temperature change following application of a step function of power dissipation under specified conditions.

2. Apparatus. The apparatus used to determine the thermal response time shall be capable of demonstrating device conformance to the minimum requirements of the applicable specification sheet.

3. Procedure. The thermal response time shall be determined by measuring the time required for the T_J (as indicated by a precalibrated temperature sensitive electrical parameter) to reach 90 percent of the final value of T_J change caused by a step function in power dissipation when the device case or ambient temperature, as specified, is held constant.

4. Summary. The device case or ambient temperature shall be specified in the applicable specification sheet.

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METHOD 3146.1

THERMAL TIME CONSTANT

1. Purpose. The purpose of this test is to measure the time required for the junction to reach 63.2 percent of the final value of T_J change following application of a step function of power dissipation under specified conditions.

2. Apparatus. The apparatus used to determine the thermal time constant shall be capable of demonstrating device conformance to the minimum requirements of the applicable specification sheet.

3. Procedure. The thermal time constant shall be determined by measuring the time required for the T_J (as indicated by a precalibrated temperature sensitive electrical parameter) to reach 63.2 percent of the final value of T_J change caused by a step function in power dissipation, when the device case or ambient temperature, as specified, is held constant.

4. Summary. The device case or ambient temperature shall be specified in the applicable specification sheet.

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METHOD 3151

THERMAL RESISTANCE, GENERAL

1. Purpose. The purpose of this test is to measure the temperature rise per unit power dissipation of the designated junction above the case of the device or ambient temperature, under conditions of steady state operation.

2. Apparatus. The apparatus used to determine the thermal resistance shall be capable of demonstrating device conformance to the minimum requirements of the applicable specification sheet.

3. Procedure. The thermal resistance may be determined by:

   a. Measuring the junction power required to maintain the T_J constant (as indicated by a precalibrated temperature sensitive electrical parameter) when the case of the device or ambient temperature, as specified, is changed by a known amount.

   b. Measuring the T_J (as indicated by a precalibrated temperature sensitive electrical parameter) when the junction power is changed a known amount while the case of the device or ambient temperature, as specified, is held constant.

4. Summary. The characteristic being measured, $R_{\theta JC}$ or $R_{\theta JA}$ shall be specified in the applicable specification sheet.

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METHOD 3161.1

THERMAL IMPEDANCE MEASUREMENTS FOR VERTICAL POWER MOSFETs (DELTA SOURCE DRAIN VOLTAGE METHOD)

1. Purpose. The purpose of this test is to measure the thermal impedance of the MOSFET under the specified conditions of applied voltage, current, and pulse duration. The temperature sensitivity of the forward voltage of the source drain diode is used as the junction temperature indicator. This method is particularly suitable to enhancement mode, power MOSFET's having relatively long thermal response times. This test method may be used to measure the thermal response of the junction to a heating pulse, to ensure proper die mountdown to its case, or the dc thermal resistance, by the proper choice of the pulse duration and magnitude of the heating pulse. The appropriate test conditions and limits are detailed in 5 herein.

1.1 Symbols and definitions. The following symbols and terminology shall apply for the purpose of this test method:

I_H: Heating current through the drain.

I_M: Current in the source drain diode during measurement of the source drain voltage.

K: Thermal calibration factor, equal to reciprocal of VTC; in °C/mV.

P_H: Magnitude of the heating power pulse applied to DUT in watts; the product of I_H and V_H.

t_H: Heating time during which P_H is applied.

T_J: Junction temperature in degrees Celsius.

T_{Ji}: Junction temperature in degrees Celsius before start of the power pulse.

T_{Jf}: Junction temperature in degrees Celsius at the end of the power pulse.

t_{MD}: Measurement delay time is defined as the time from the removal of heating power (P_H) to the start of the V_{SD} measurement.

t_{SW}: Sample window time during which final V_{SD} measurement is made.

T_X: Reference temperature in degrees Celsius.

T_{Xi}: Initial reference temperature in degrees Celsius.

T_{Xf}: Final reference temperature in degrees Celsius.

$V_{GS(M)}$: Gate source voltage applied during the initial and final measurement periods.

V_H: Heating voltage between the drain and source.

V_{SD}: Source drain diode voltage in millivolts.

V_{SDi}: Initial source drain voltage in millivolts.

V_{SDf}: Final source drain voltage in millivolts.

VTC: Voltage temperature coefficient of V_{SD} with respect to T_J; in mV/°C.

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$Z_{\theta JX}$: Transient junction-to-reference point thermal impedance in degrees Celsius/watt. $Z_{\theta JX}$ for specified power pulse duration is:

$$Z_{\theta JX} = \frac{(T_{jf} - T_{ji} - \Delta T_X)}{P_H}$$

Where: ΔT_X = Change in reference point temperature during the heating pulse (see 4.2 and 4.4). For short heating pulses, e.g., die attach evaluation, this term is normally negligible).

2. Apparatus. The apparatus required for this test shall include the following, as applicable, to the specified test procedure:

a. A thermocouple for measuring the case temperature at a specified reference point. The recommended reference point shall be located on the case under the heat source. Thermocouple material shall be copper-constantan (type T) or equivalent. The wire size shall be no larger than AWG size 30. The junction of the thermocouple shall be welded to form a bead rather than soldered or twisted. The accuracy of the thermocouple and its associated measuring system shall be ±0.5°C. Proper mounting of the thermocouple to ensure intimate contact to the reference point is critical for system accuracy.

b. A controlled temperature environment capable of maintaining the case temperature during the device calibration procedure to within ±1°C over the temperature range of +23°C to +100°C, the recommended temperatures for measuring K factor.

c. A K factor calibration setup, as shown on figure 3161-1, that measures V_{SD} for a specified value of I_M in an environment in which temperature is both controlled and measured. A temperature controlled, circulating fluid bath may be used. The current source shall be capable of supplying I_M with an accuracy of ±1 percent. The voltage source shall be capable of supplying a stable $V_{GS(M)}$ in the range of -1 to -5 V (opposite polarity for p-channel devices). This voltage is applied in such a way as to turn the DUT off (i.e., gate negative with respect to source for n-channel device). The voltage measurement of V_{SD} shall be made using Kelvin contacts and with voltmeters capable of 1 mV resolution. The device-to-current source wire size shall be sufficient to handle the measurement current (AWG size 22 stranded is typically used for up to 100 mA).

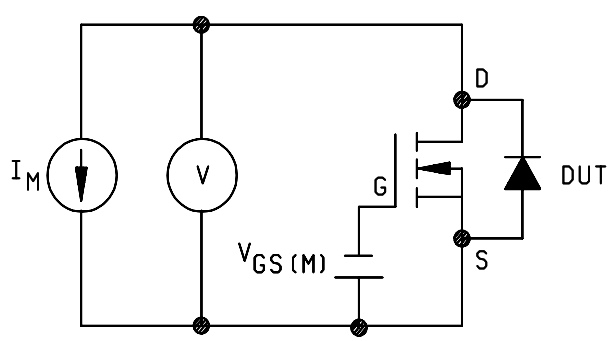

FIGURE 3161-1. K-factor calibration setup.

d. A test circuit used to control the device and to measure the temperature using the forward voltage of the source drain diode as the temperature sensing parameter as shown on figure 3161-2. Polarities shown are for n-channel devices but the circuit may be used for p-channel types by reversing the polarities of the voltage and current sources.

e. Suitable sample-and-hold voltmeter or oscilloscope to measure source drain forward voltage at specified times. V_{SD} shall be measured to within 5 mV, or within 5 percent of (V_{SDi} - V_{SDf}), whichever is less.

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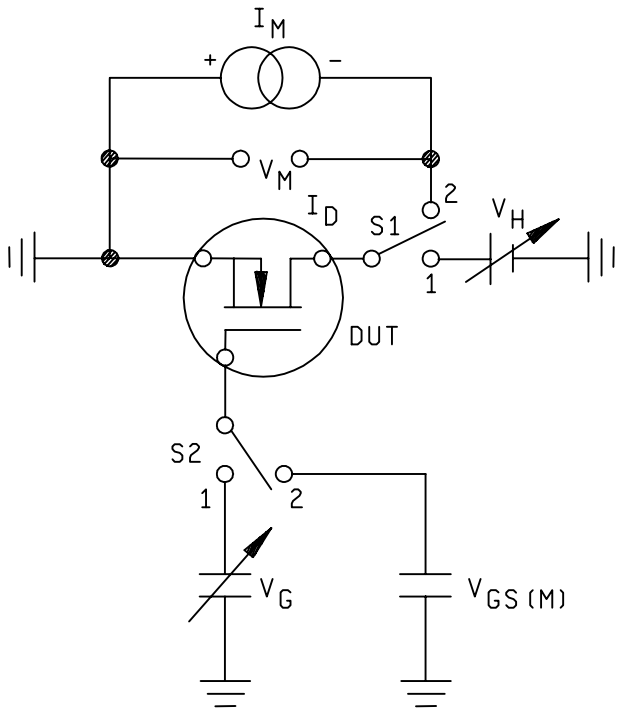

NOTES:

1. The circuit consists of the DUT, three voltage sources, a current source, and two electronic switches. During the heating phase of the measurement, switches S1 and S2 are in position 1. The values of V_G and V_D are adjusted to achieve the desired values of I_D and V_{DS} for the P_H heating condition.
2. To measure the initial and post-heating pulse junction temperatures of the DUT, switches S1 and S2 are each switched to position 2. This puts the gate at the measurement voltage level $V_{GS(M)}$ and connects the current source I_M to supply forward measurement current to the source drain diode. The polarity of the current source is such that the voltage applied to the MOSFET source and drain are opposite to those employed during normal MOSFET operation. Figures 3161-3 and 3161-4 show the waveforms associated with the three segments of the test.

FIGURE 3161-2. Thermal impedance measurement circuit (source drain diode method).

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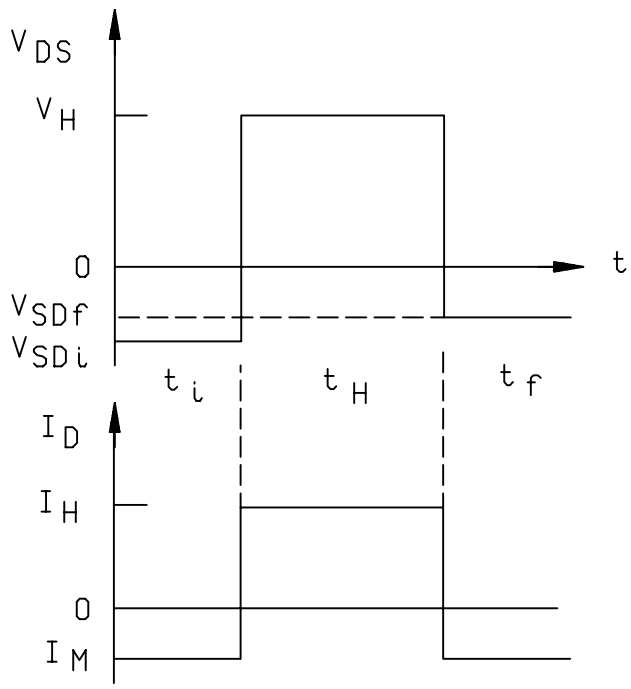

FIGURE 3161-3. Device waveforms during the three segments of the thermal transient test.

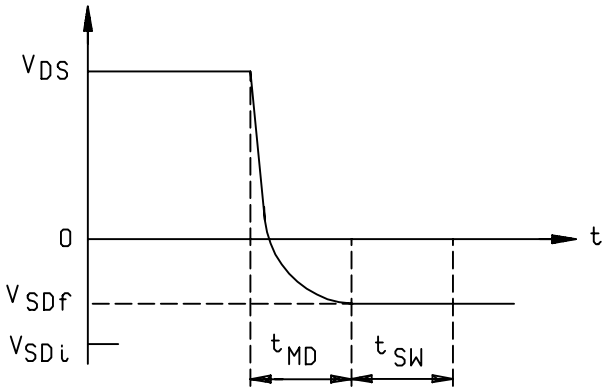

FIGURE 3161-4. Second V_{SD} measurement waveform.

NOTE: The value of t_{MD} is critical to the accuracy of the measurement and shall be properly specified in order to ensure measurement repeatability. Note that some test equipment manufacturers include the sample-and-hold window time t_{SW} within their t_{MD} specification.

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3. Measurement of the TSP. The required calibration of V_{SD} versus T_J is accomplished by monitoring V_{SD} for the required value of I_M as the heat sink temperature (and thus the DUT temperature) is varied by external heating. The magnitude of I_M shall be chosen so that V_{SD} is a linearly decreasing function over the expected range of T_J during the power pulse. I_M shall be large enough to ensure that the source drain junction is turned on but not so large as to cause any significant self heating. (This will normally be 10 mA for small power devices and up to 100 mA for large ones.) The $V_{GS(M)}$ value shall be large enough to decouple the gate from controlling the DUT; typical values are in the 1 to 5 V range. An example calibration curve is shown on figure 3161-5.

3.1 Measurement of die attachment integrity. When screening to ensure proper die attachment integrity within a given lot or in a group of same type number devices of one manufacturer, this calibration step is not required. In such cases, the measure of thermal response may be ΔV_{SD} for a short heating pulse, and the computation of ΔT_J or $Z_{\theta JX}$ is not necessary. (For this purpose, t_H shall be 10 ms for TO-39 size packages and 100 ms for TO-3 size packages.)

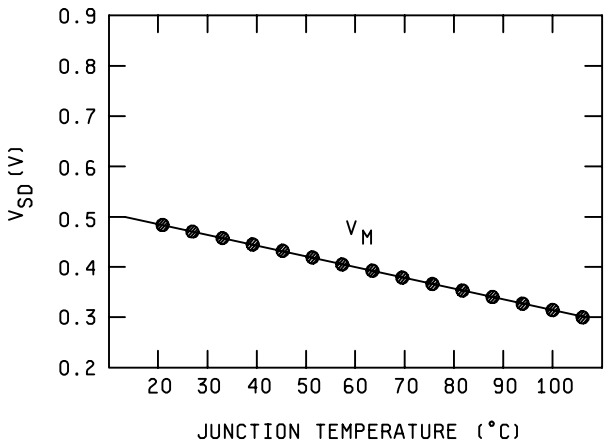

FIGURE 3161-5. Example curve of V_{SD} versus T_J.

3.2 K factor calibration. A K factor calibration (which is the reciprocal of VTC or the slope of the curve on figure 3161-4) can be defined as:

$$K = \frac{1}{VTC} = \left| \frac{T_{J1} - T_{J2}}{V_{SD1} - V_{SD2}} \right| \, °C/mV$$

It has been found experimentally that the K factor variation for all devices within a given device type class is small. The usual procedure is to perform a K factor calibration on a 10 to 12 piece sample from a device lot and determine the average K and standard deviation (σ). If σ is less than or equal to three percent of the average value of K, then the average value of K can be used for all devices within the lot. If σ is greater than three percent of the average value of K, then all the devices in the lot shall be calibrated and the individual values of K shall be used in thermal impedance calculations or in correcting ΔV_{SD} values for comparison purposes.

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4. Test procedure.

4.1 Calibration. K factor shall be determined according to the procedure outlined in 3 herein, except as noted in 3.1.

4.2 Reference point temperature. The reference point is usually chosen to be on the bottom of the transistor case directly below the semiconductor chip in a TO-204 metal can or in close proximity to the chip in other styles of packages. Reference temperature point location shall be specified and its temperature shall be monitored using the thermocouple as stated in 2.a herein during the preliminary testing. If it is determined that T_X increases by more than +5°C of measured junction temperature rise during the power pulse, then either the heating power pulse magnitude shall be decreased, the DUT shall be mounted in a temperature controlled heat sink, or the calculated value of thermal impedance shall be corrected to take into account the thermal impedance of the reference point to the cooling medium or heat sink. Temperature measurements for monitoring, controlling, and correcting for reference point temperature changes are not required if the t_H value is low enough to ensure that the heat generated within the DUT has not had time to propagate through the package. Typical values of t_H for this case are in the 10 to 500 ms range, depending on DUT package type and material.

4.3 Thermal measurements. The following sequence of tests and measurements shall be made:

a. Prior to the power pulse:

(1) Establish reference point temperature (T_{Xi}).

(2) Apply measurement current (I_M).

(3) Apply gate source measurement voltage ($V_{GS(M)}$).

(4) Measure source drain voltage drop (V_{SDi}) (a measurement of the initial junction temperature).

b. Heating pulse parameters:

(1) Apply drain source heating voltage (V_H).

(2) Apply drain heating current (I_H) as required by adjustment of gate source voltage.

(3) Allow heating condition to exist for the required heating pulse duration (t_H).

(4) Measure reference point temperature (T_{Xf}) at the end of heating pulse duration.

(NOTE: T_X measurements are not required if the t_H value meets the requirements stated in 4.2.)

c. Post-power pulse measurements:

(1) Apply measurement current (I_M).

(2) Apply gate source measurement voltage ($V_{GS(M)}$).

(3) Measurement source drain voltage drop (V_{SDf}) (a measurement of the final junction temperature).

(4) Time delay between the end of the power pulse and the completion of the V_{SDf} measurement as defined by the waveform on figure 3161-4 in terms of $t_{MD} + t_{SW}$.

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4.4 Thermal impedance. The value of thermal impedance ($Z_{\Theta JX}$) is calculated from the following formula:

$$Z_{\theta JX} = \frac{\Delta T_J}{P_H} = \left| \frac{K\ (V_{SDf} - V_{SDi})}{(I_H)\ (V_H)} \right| \ °C/W$$

This value of thermal impedance will have to be corrected if T_{Xf} is greater than T_{Xi} by +5°C. The correction consists of subtracting out the component of thermal impedance due to the thermal impedance from the reference point (typically the device case) to the cooling medium or heat sink. T_X measurements are not required if the t_H value meets the requirements stated in 4.2 herein. This thermal impedance component has a value calculated as follows:

$$Z_{\theta X\text{-}HS} = \frac{\Delta T_X}{P_H} = \frac{(T_{xf} - T_{xi})}{[(I_H)(V_H)]}$$

Where: HS = cooling medium or heat sink (if used).

Then: $Z_{\theta JX}\,|_{\text{Corrected}} = Z_{\theta JX}\,|_{\text{Calculated}} - Z_{\theta X\text{-}HS}$

NOTE: This last step is not necessary for die attach evaluation (see 3.1 herein).

5. Test conditions and measurements to be specified and recorded.

5.1 K factor calibration.

5.1.1 Conditions data. Specify the following test conditions:

a. Measuring current (I_M) (see applicable specification sheet).

b. Gate-source voltage ($V_{GS(M)}$) (in the range of 0 V to -6 V).

c. Initial junction temperature (T_J): +25°C ±5°C.

d. Final junction temperature (T_{Jf}): +100°C ±10°C.

5.1.2 Record data. Record the following data:

a. Initial V_{SD} voltage.

b. Final V_{SD} voltage.

5.1.3 Calculation data. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_J 1 - T_J 2}{V_{SD} 1 - V_{SD} 2} \right| °C/mV$$

5.1.4 Die attach procedure. K factor calibration (see 5.1) may not be necessary for die attachment evaluation (see 3.1).

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5.2 Thermal impedance measurements.

5.2.1 Conditions data. Specify the following test conditions in the applicable specification sheet.

a. Measuring current (I_M) (shall be same as used for K factor calibration).

b. Drain heating current (I_H).

c. Heating time (t_H).

d. Drain source heating voltage (V_H).

e. Measurement time delay (t_{MD}).

f. Sample window time (t_{SW}).

g. Gate-source voltage ($V_{GS(M)}$) (shall be same as used for K factor calibration).

(NOTE: I_H and V_H are usually chosen so that P_H is approximately two-thirds of device rated power dissipation).

5.2.2 Record data. Record the following data:

a. Initial reference temperature (T_{Xi}).

b. Final reference temperature (T_{Xf}).

c. T_X measurements are not required if the t_H value meets the requirements stated in 4.2.

d. Calculate thermal impedance using the procedure and equations shown in 4.4.

5.2.2.1 ΔV_{SD} data. This parameter can either be read directly from suitable test instrumentation or calculated by taking the difference between initial and final values of V_{SD} (i.e., $\Delta V_{SD} = |V_{SD(i)} - V_{SD(f)}|$.)

5.2.3 Thermal resistance measurements. This is a thermal impedance measurement for the condition in which the heating time (t_H) has been applied long enough to ensure that the temperature drop from the device junction to the case reference point in accordance with 2.a has reached equilibrium and no longer increases for greater values of t_H. In practical measurements, this condition can be assumed to exist when the rate of junction temperature change matches the rate of case temperature change.

5.3 Thermal response ΔV_{DS} measurements for screening. These measurements are made for t_H values that meet the intent of 3.1 and the requirements stated in 4.2.

5.3.1 Conditions data. Specify the following test conditions in the applicable specification sheet:

a. Measuring current (I_M).

b. Drain heating current (I_H).

c. Heating time (t_H).

d. Drain source heating voltage (V_H).

e. Measurement time delay (t_{MD}).

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f. Sample window time (t_{SW}).

g. Gate-source voltage ($V_{GS(M)}$) (shall be the same as used if and when K factor calibration is performed (see 5.3.2.1b herein)).

NOTE: The values of I_H and V_H are usually chosen equal to or greater than the values used for thermal impedance measurements.

5.3.2 Specified limits. The following data is compared to the specified limits:

5.3.2.1 ΔV_{SD} data.

a. Same as 5.2.2.1 herein.

b. Optionally calculate ΔT_J for comparison or screening purposes, or both, if the K factor results (see 3 herein and 5.1 herein) produce a σ greater than three percent of the average value of K.

$$\Delta T_J = K\ (\Delta V_{SD})\ \text{in °C}$$

6. Summary. The following conditions shall be specified in the applicable specification sheet:

6.1 Thermal impedance.

a. I_M measuring current.

b. I_H drain heating current.

c. t_H heating time.

d. V_H drain source heating voltage.

e. t_{MD} measurement time delay.

f. t_{SW} sample window time.

6.2 Thermal response ΔV_{SD} measurement.

a. I_M measuring current.

b. I_H drain heating current.

c. t_H heating time.

d. V_H drain source heating voltage.

e. t_{MD} measurement time delay.

f. t_{SW} sample window time.

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7. Tutorial guidelines. Thermal response, thermal impedance, and thermal resistance measurements require that I_H and V_H not to exceed the rated specified values and t_H for I_H and V_H not to exceed the specified safe-operating area (SOA) stated in the device specifications. Values of I_M, t_{MD} conditions are also taken from the device specifications.

The steps shown below are guidelines of how to reach the proper test conditions and determine the acceptance limits, primarily for thermal transient testing and thermal characterization purposes.

7.1 Characterizing thermal resistance and thermal impedance. The following steps describe in detail how to set up the apparatus stated in above sections to achieve the thermal resistance and thermal impedance characterizations on MOSFET devices.

a. Step 1 - K-factor calibration: using apparatus 2.c herein, best with circulating bath and Kelvin cable, on ten devices. I_M = 10 mA for most MOSFET (or 5 mA for smaller power devices). Temperatures start from 150ºC and cool down to 25ºC (25 points). K-factors are individually calculated and analyzed for possible usage of average value in all calculations of thermal impedances and resistances. The linear relationship of ΔV_{SD} verses T_J can expressed as calculated slope (K-factor) and offset. These data can be performed automatically by some test equipment and can be kept to traceable device serial numbers.

b. Step 2 - Measurement-delay-time (t_{MD}) characterization: With above K-factor data, on ten devices V_H = 12 V for devices with rated breakdown voltage of beyond 30 V. (V_H = 10 V for devices with rated breakdown voltage of 30 V or lower). I_M = 10 mA for most MOSFET (or 5 mA for smaller power devices). t_H = 10 ms and I_H = adjusted to achieve ΔT_J of about 90ºC to 100ºC (not to exceed the rated SOA). t_{MD} = set at each 10 µsec., 20 µsec., 30 µsec., 50 µsec., 100 µsec., 200 µsec. and 320 µsec.

The measured ΔV_{SD} verses square-root of t_{MD} can be plotted, as shown on figure 3161-6 herein, to show the optimum 30 µsec. t_{MD} as well as added T_J-factor for 0 µsec. The added T_J-factor will be used to calculated true T_J.

Measurement-delay-time (t_{MD}) optimization can be performed automatically by some test equipment and can be kept to traceable device serial numbers.

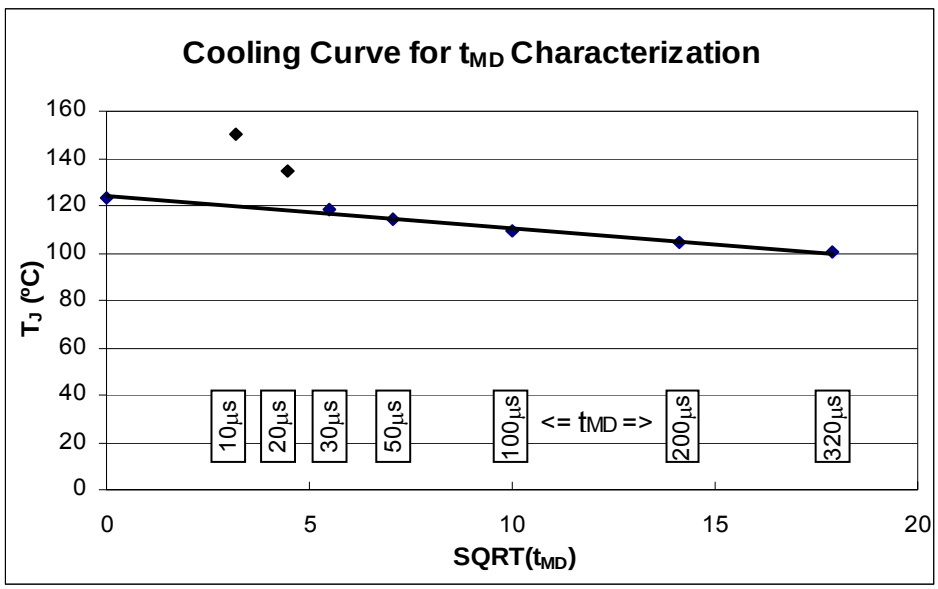

FIGURE 3161-6. Cooling curve.

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c. Step 3 - Thermal Resistance Characterization: with device in temperature-stable environment (liquid-flowed heat-sink, closed still-air chamber or forced-air chamber) and thermal-couple contacted to specified referent point (lead, case, pad, printed circuit board, or heat-sink). V_H = 12 V for devices with rated breakdown voltage of beyond 30 V. (V_H = 10 V for devices with rated breakdown voltage of 30 V or lower). I_M = 10 mA for most MOSFET (or 5 mA for smaller power devices). I_H = adjusted (initially on first device) to achieve T_J of about 90ºC at steady-state (long) t_H. K-factor and t_{MD} = individual values to each device serial number or single value (from above). Use additional controls on equipment to minimize power oscillation and waveform ringing or transients. The ΔV_{SD} measurement will be converted to ΔT_J and R_{th} using individual K-factor and added T_J-factor (for 0 µsec. t_{MD}) with referent temperature measurement. The measured thermal resistances of ten devices will be statistically analyzed to set the final specification (rated RthJC, R_{thJA}, R_{thJPcb}, $R_{thJSink}$ limits). Average plus 4 (Cpk = 1.33) to 4.5 (Cpk = 1.5), sigma should be used to derive the maximum rated limits.

d. Step 4 - Thermal impedance / heating CURVE Characterization: with same set-up in thermal resistance prior to running heating curve, perform the 5-msec. Thermal impedance while adjusting heating V_H and I_H for minimized ringing and transient waveforms. I_H is typically selected 1.5 Amps. higher than the final I_H of above Rth characterization. Power V_H x I_H is typically selected for ΔT_J about 20ºC. For each t_H, ΔV_{SD} measurement will be converted to ΔT_J and Z_{th} using individual K-factor and added T_J-factor (for 0 µsec. t_{MD}) with referent temperature measurement.

Example of heating curve and thermal model in both semi-log and log-log scales, see figure 3161-7:
The “inflection point”, defined for transition between thermal interfaces, are more visibly shown in log-log graph than in semi-log graph.

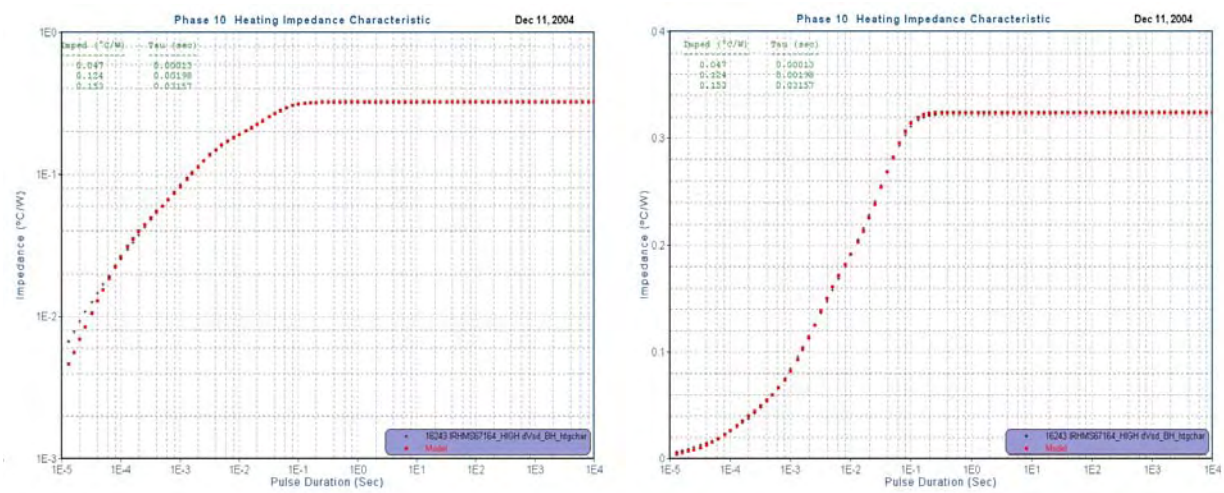

FIGURE 3161-7. Heating curve and thermal model example.

Thermal impedance curves for various different duty cycles can also be simulated from the model and added to the specifications.

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7.2 Optimizing production test conditions for die-attach thermal response or thermal impedance: The following steps describe in detail how to set up the apparatus stated in above sections (production equipment) to achieve proper production test conditions for die-attach thermal response and impedance on MOSFET devices.

a. Step 1 - Selection of two extreme devices: Use the following guidelines to select proper conditions and apparatus: V_H = 12 V for devices with rated breakdown voltage of beyond 30 V. (V_H = 10 V for devices with rated breakdown voltage of 30 V or lower). I_H = (0.66 x rated power) / (above V_H) or adjusted for 195 to 255 mV ΔV_{SD} (about 100ºC ΔT_J). t_H = 10ms for TO-205AF (TO-39), LCC18 and TO-276AA (SMD-.5). 20 ms for TO-276AB (SMD-1) and TO-276AC (SMD-2). 50 ms for TO-257AA, TO-254AA, and TO-204AA (TO-3). I_M = 10 mA for most MOSFET (Or 5 mA for smaller power devices). t_{MD} = 30 µs from above characterization. Larger value may be required on power devices with high inductive package elements which generate non-thermal electrical transients; unless otherwise specified, this would be observed in the t_f region of figure 3161-3. k = value from measurements of above K-factor calibration (at above I_M condition). Record the ΔV_{SD} measurements of above conditions for 20 to 25 devices, correlated with X-ray results of die-attachment. One device with highest ΔV_{SD} value (best with X-ray failure) and one device with lowest ΔV_{SD} value (best die attachment) are selected for test and generate heating curves.

b. Step 2 - Thermal impedance / heating curve characterization: On two extreme devices follow Step 4 of 7.1 herein to generate the heating curve for each of the two extreme devices selected in accordance with 7.2.a herein (superimposed in one graph).

The thermal impedance curves for both Highest and lowest delta-VSD devices, as well as the curves for average and average+4sigma values, are displayed on figure 3161-8. The final thermal impedance specification is typically scaled from average curve, with ratio factor of final RthJC value (which is round-off from average+4.Sigma RthJC value) to average RthJC value.

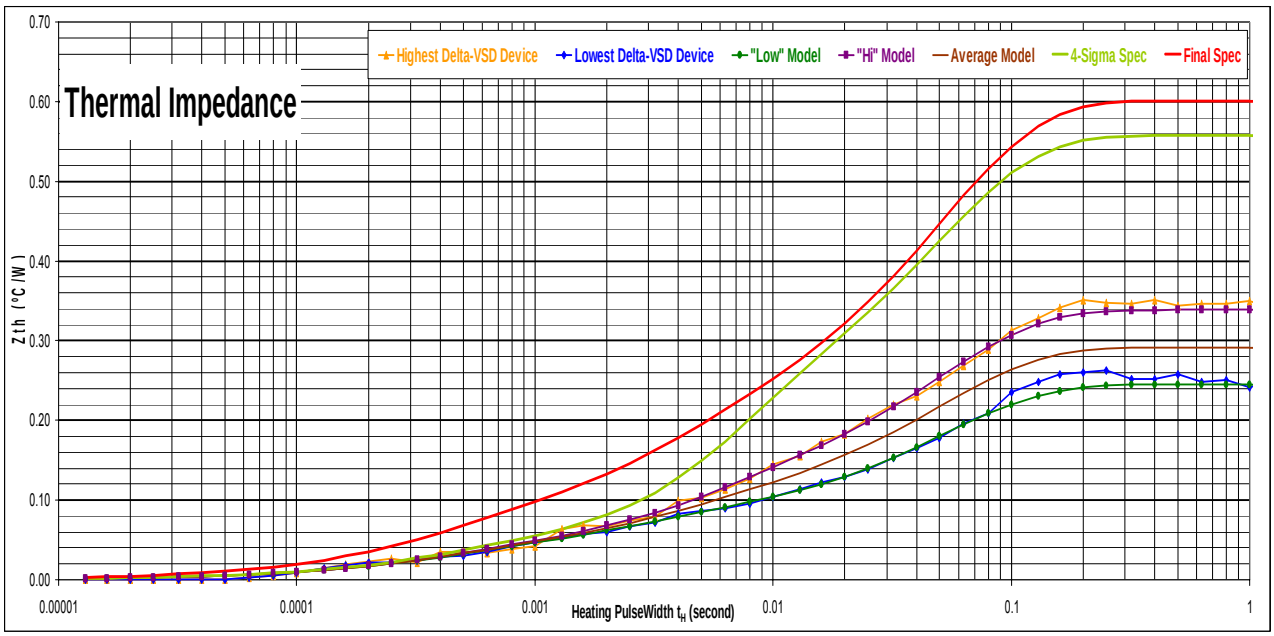

FIGURE 3161-8. Thermal impedance curves.

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c. Step 3 - Heating curve interpretation: For proper selection of die-attach thermal response t_H:
At heating time t_H less than or equal thermal time constant of identical chips, the thermal characteristics are the same. As t_H is increased (exceeding the chip thermal constant) and the heat propagated through the chip into the die attachment region, the curves of the specially selected extreme devices diverge (changes in slope), starting from time point where the die attachment variance has an affect on device junction temperature. As t_H is increased further, the curve somewhat flattened out (more flattening with higher thermal mass), with same slope for identical package. With several different elements in heat flow path (chip, die attachment, substrate, substrate attachment, package, package attachment, and printer circuit board / heatsink), several plateaus and transitions will be shown in the heating curve. Proper selection of extreme devices (correlating to X-ray inspection results) would provide better differentiation in attachment areas on heating curves.

Using heating curves and 7.2.c herein, select appropriate die attachment t_H to correspond to the immediate point in the region beyond the die attachment area.

7.3 Deriving statistical-process-control (SPC) limits for production die-attach thermal response. The following steps describe in detail how to derive proper SPC limits for 100 percent production testing of die-attach thermal response or thermal impedance on MOSFET devices.

a. Step 1 - Data collection and data types: (first production lots and subsequent production lots). Using above optimized test conditions, thermal data should be recorded for setting limit from minimum 30 devices sampling of first five production lots and from five to Ten devices sampling from each subsequent production lot.
These data can be ΔV_{SD} or ΔT_J [=ΔV_{SD} x K-factor] or CU [=ΔV_{SD} / P_H] or ZthJX [=(ΔV_{SD} x K-factor / P_H).+T_{ref}].

(1) A single ΔV_{SD} limit is practical if the K-factor values for all devices (of the same type) tested to a given specification are nearly identical (see 3.2 herein). Different device type (from different manufacturer) should have different limit with its unique conditions specified.

(2) When a single K-factor can not be used (see 3.2 herein), the ΔT_J (or T_J) single limit is practical to take into account the individual device K-factor.

(3) Other single limits of CU (if identical K-factor but individual P_H), K.CU (if individual K-factor and individual P_H) and ZthJX (absolute magnitude with individual K-factor, P_H and T_{ref}) have the same significance as ΔT_J (or T_J) single limit, since P_H and T_{ref} are identical and insignificant to MOSFET.

Thus, for MOSFET, the significant data types are ΔV_{SD} and ZthJX (or ΔT_J or T_J).

b. Step 2 - Statistical analysis and limit setting: The data shall be statistically analyzed to establish the pass/fail limit (the cut-off point between acceptable and non-acceptable devices) for each initial lot, as well as derived to final SPC limits.

For each of the first five production lots, the statistical analysis of sample data should be shown in a single-lot histogram with upper SPC limit (UCL) and lower SPC limit (LCL) resulted from average plus three standard deviations and average minus three standard deviations, respectively. In this example, figure 3161-9, the single lot will be tested to LCL of 166 mV and UCL of 177 mV.

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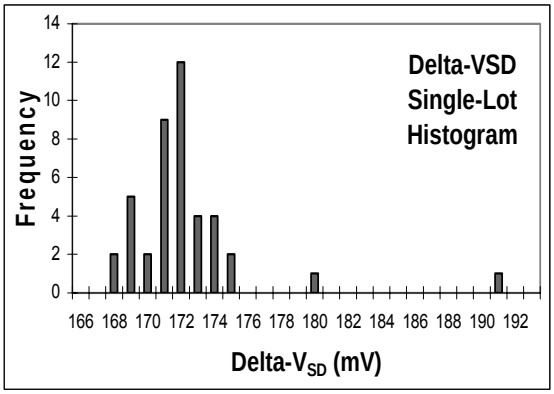
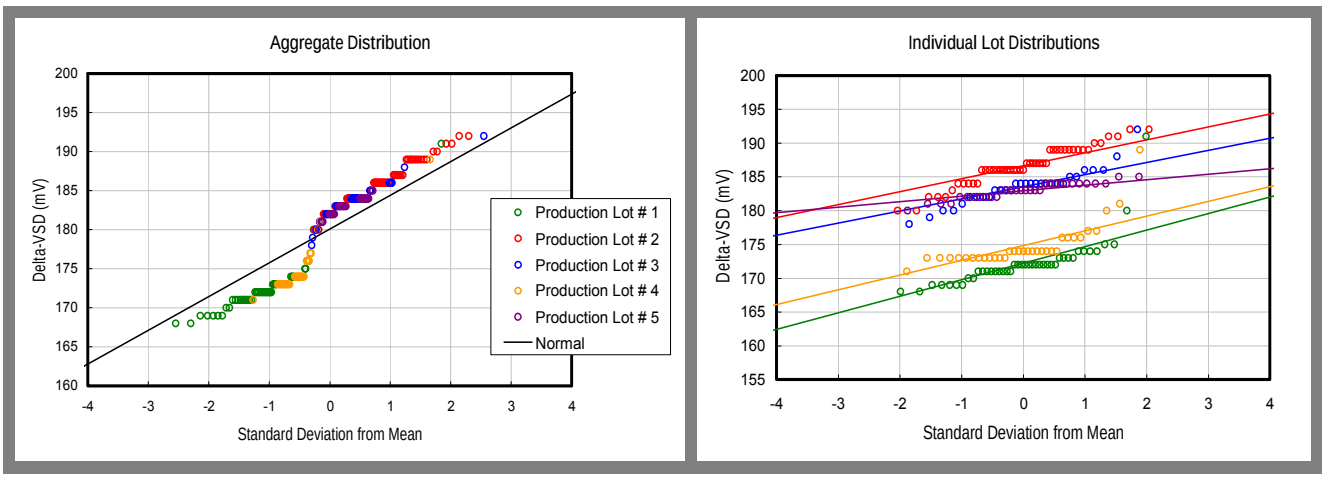


Average	171.6	mV
Sigma	1.8	mV
Mean-3Sigma	166.2	mV
Mean+3Sigma	176.9	mV

FIGURE 3161-9. Delta VSD single lot histogram.

Very high ΔV_{SD} in some devices can be confirmed of unacceptance limit with results from X-ray, SonaScanning or die shear.

For setting of final SPC limits, the statistical analysis of combined sample data from five production lots should be shown in a summary table (inverse normalization graph optional) as shown in figure 3161-10 herein.



		All	Production Lot # 1	Production Lot # 2	Production Lot # 3	Production Lot # 4	Production Lot # 5
	n =	184	42	47	30	33	32
	R^2 =	0.936	0.621	0.957	0.895	0.617	0.926
Mean	μ =	180.076087	172.2142857	186.6382979	183.5333333	174.8181818	182.9375
Standard Deviation	σ =	6.481134785	3.679446633	2.877389607	2.687561814	3.273516319	1.216486214
Mean - 4 Standard Deviation	$\mu - 4\sigma$ =	154.1515478	157.4964992	175.1287394	172.7830861	161.7241165	178.0715551
Mean + 4 Standard Deviation	$\mu + 4\sigma$ =	206.0006261	186.9320722	198.1478563	194.2835806	187.9122471	187.8034449
	σ / μ =	3.60%	2.14%	1.54%	1.46%	1.87%	0.66%

FIGURE 3161-10. Summary table and sample data from five production lots.

In this example, all succeeding production lots (after fifth production lot) will be tested to final lower SPC limit of 154 mV and final upper SPC limit of 206 mV, the calculated mean ±4 sigma values.

7.4 Process change control for thermal response/impedance/resistance. At any time that production die attach process (temperature profile) changes or related material property (compositions or finshes) changes, new thermal resistance and thermal impedance shall be re-characterized for new defined specifications, as well as new SPC limits shall be re-established from data of devices sampling from new production lots.

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METHOD 3181

THERMAL RESISTANCE FOR THYRISTORS

1. Purpose. The purpose of this test is to measure the thermal resistance of thyristors under specified conditions.

2. Test circuit. See figure 3181-1.

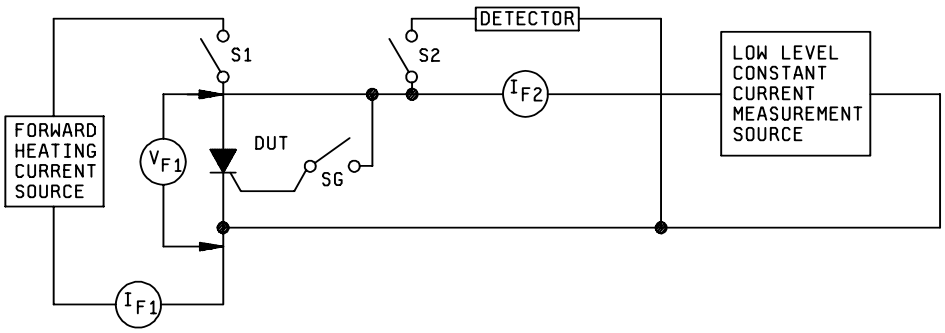

FIGURE 3181-1. Thermal resistance test circuit.

3. Procedure. S1 is closed for a much longer interval (heat) than it is opened (measurement). The measurement interval should be short compared to the thermal response time of the device being measured. The constant measurement current is a small current (of the order of a few milliamperes) and so selected that the magnitude of V_{F1} changes appropriately with the device material (silicon approximately 2 mV/°C) and junction temperature. The heating current source is adjustable.

3.1 Measurement. The measurement is made in the following manner. The case ambient or other reference point is elevated to a high temperature, T_2, not exceeding the maximum junction temperature and the forward voltage drop (V_{F1}) read with the heating source supplying no current (i.e., the forward voltage (V_{F1}) is to be read at the start of the measurement interval). An oscilloscope makes a suitable detector. At T_2 there will be a small power dissipated in the device due to the measurement current source. The reference is then reduced to a lower temperature (T_1), and power (P_1) is applied to heat the device by increasing the current from the constant current source until the same value of V_{F1} is read as was read above. However, if P_1 is calculated as the heating power contributed by the heating current source only, the equation:

$$\theta = \frac{T_2 - T_1}{P_1} \; gives\, \theta \; accurately$$

Where: $P_1 = V_{F1}\, I_{F1}$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test temperatures (see 3.1).

b. Test voltages and currents (see 3.1).

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3200 Series

Low frequency tests

Unless otherwise specified, the measurements shall be made at the electrical test frequency, 1,000 ±25 Hz. At 1,000 Hz, the reactive components may not be negligible.

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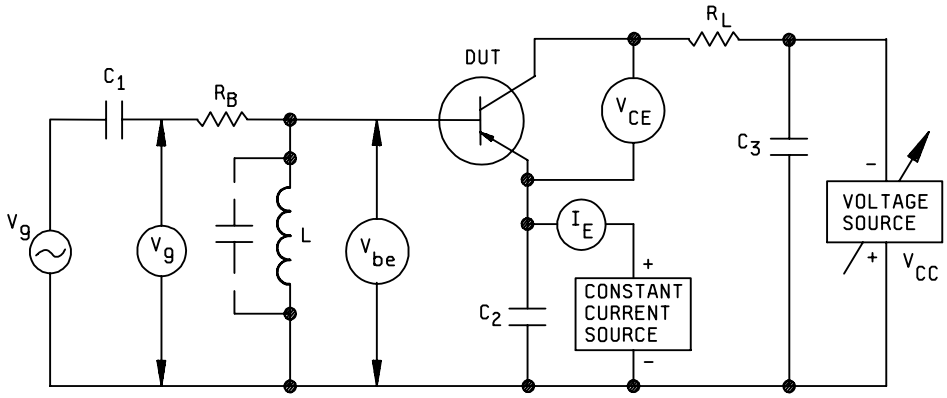
METHOD 3201.1

SMALL-SIGNAL, SHORT-CIRCUIT INPUT IMPEDANCE

1. Purpose. The purpose of this test is to measure the input impedance of the device under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common emitter configuration. For other parameters the circuit and procedure should be changed accordingly. See figure 3201-1.



NOTE: The biasing circuit shown is for purposes of illustration only. Other stable biasing circuits may be used (see 3).

FIGURE 3201-1. Test circuit for small-signal, short-circuit input impedance.

3. Procedure. The capacitors C_1, C_2, and C_3 shall present short-circuits at the test frequency in order to effectively couple and bypass the test signal. The inductance L shall be resonated with a capacitor and the combination shall have a large impedance compared with h_{ie} at the test frequency. R_L shall be a short-circuit compared with the output impedance of the device. V_g and V_{be} are measured on high-impedance ac voltmeters after setting the specified values of I_E and V_{CE}.

$$Then: \; h_{ie} = \frac{V_{be}}{I_b}, where \; I_b = \frac{V_g - V_{be}}{R_B}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test frequency (see 3.).

b. Test voltages and currents (see 3.).

c. Parameter to be measured.

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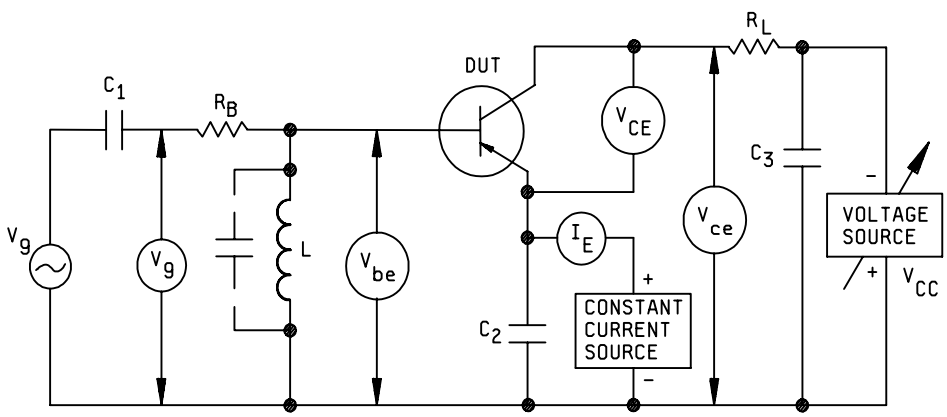
METHOD 3206.1

SMALL-SIGNAL, SHORT-CIRCUIT FORWARD-CURRENT TRANSFER RATIO

1. Purpose. The purpose of this test is to measure the forward-current transfer ratio of the device under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common emitter configuration. For other parameters the circuit and procedure should be changed accordingly. See 3206.1.



NOTE: The biasing circuit shown is for purposes of illustration only. Other stable biasing circuits may be used (see 3).

FIGURE 3206-1. Test circuit for small-signal, short-circuit forward-current transfer ratio.

3. Procedure. The capacitors C_1, C_2, and C_3 shall present short-circuits at the test frequency in order to effectively couple and bypass the test signal. The inductance L shall be resonated with a capacitor and the combination shall have a large impedance compared with h_{ie} at the test frequency. R_L shall be a short-circuit compared with the output impedance of the device. V_g, V_{be}, and V_{ce} shall be measured on high-impedance ac voltmeters after setting the specified values of I_E and V_{CE}.

$$Then: \; h_{fe} = \frac{I_c}{I_b}, where: \; I_c = \frac{V_{ce}}{R_L} \; and \; I_b = \frac{V_g - V_{be}}{R_B}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test frequency (see 3.).

b. Test voltage and currents (see 3.).

c. Parameter to be measured.

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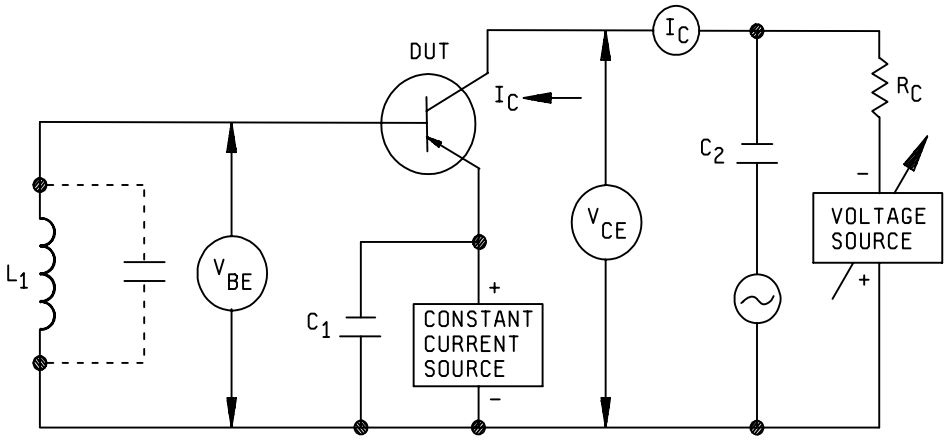
METHOD 3211

SMALL-SIGNAL, OPEN-CIRCUIT REVERSE-VOLTAGE TRANSFER RATIO

1. Purpose. The purpose of this test is to measure the reverse-voltage transfer ratio of the device under the specified conditions.

2. Test circuit. The circuit and procedures shown are for common emitter configuration. For other parameters the circuit and procedure should be changed accordingly. See figure 3211-1



NOTE: The biasing circuit shown is for purposes of illustration only. Other stable biasing circuits may be used (see 3).

FIGURE 3211-1. Test circuit for small-signal, open-circuit reverse-voltage transfer ratio.

3. Procedure. Inductance L_1 shall be resonated with a capacitor and the combination shall have a large impedance compared with h_{ic} at the test frequency. The capacitors C_1 and C_2 shall present short-circuits at the test frequency in order to effectively couple and bypass the test signal. Voltmeters V_{be} and V_{ce} shall be high impedance voltmeters. Thus, after applying the specified test voltages and currents:

$$h_{re} = \frac{V_{be}}{V_{ce}}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test frequency (see 3.).

b. Test voltages and currents (see 3.).

c. Parameter to be measured.

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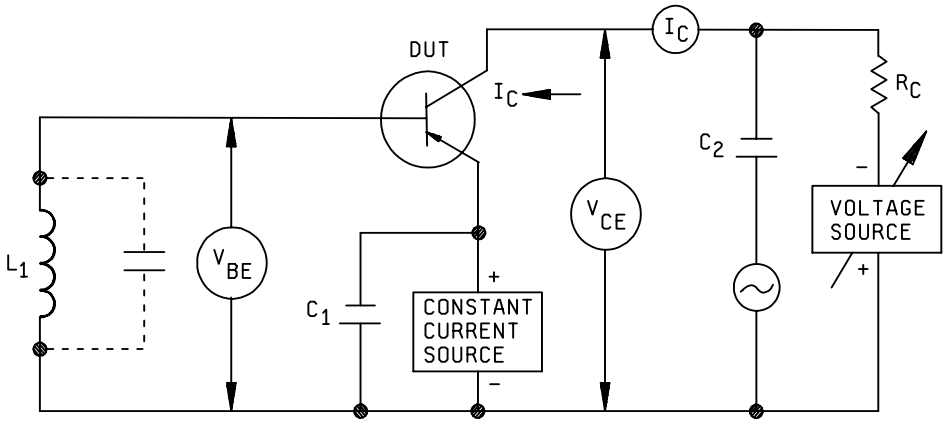
METHOD 3216

SMALL-SIGNAL, OPEN-CIRCUIT OUTPUT ADMITTANCE

1. Purpose. The purpose of this test is to measure the output admittance of the device under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common emitter configuration. For other parameters the circuit and procedure should be changed accordingly. See figure 3216-1.



NOTE: The biasing circuit shown is for purposes of illustration only. Other stable biasing circuits may be used (see 3).

FIGURE 3216-1. Test circuit for small-signal, open-circuit output admittance.

3. Procedure. Inductance L_1 shall be resonated with a capacitor and the combination shall have a large impedance compared with h_{ie} at the test frequency. The capacitors C_1 and C_2 shall present short-circuits at the test frequency in order to effectively couple and bypass the test signal. Voltmeters V_{be} and V_{ce} shall be high impedance voltmeters. Then:

$$h_{oe} = \frac{I_c}{V_{ce}}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test voltages and currents (see 3.).

b. Test frequency (see 3.).

c. Parameter to be measured.

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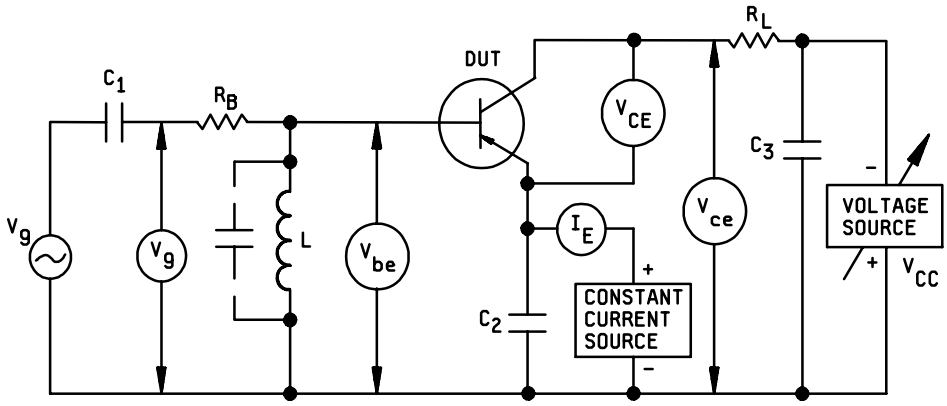
METHOD 3221

SMALL-SIGNAL, SHORT-CIRCUIT INPUT ADMITTANCE

1. Purpose. The purpose of this test is to measure the input admittance of the device under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common emitter configuration. For other parameters the circuit and procedure should be changed accordingly. See figure 3221-1.



NOTE: The biasing circuit shown is for purposes of illustration only. Other stable biasing circuits may be used (see 4.3.4).

FIGURE 3221-1. Test circuit for small-signal, short-circuit input admittance.

3. Procedure. The capacitors C_1, C_2, and C_3 shall present short circuits at the test frequency in order to effectively couple and bypass the test signal. The inductance L shall be resonated with a capacitor and the combination shall have a large impedance compared with h_{ie} at the test frequency. R_L is optional and shall be a short-circuit compared with the output impedance of the device. V_g and V_{be} are measured on high-impedance ac voltmeters.

$$Then: \; h_{ie} = \frac{V_{be}}{I_b}$$

$$Thus: \; Y_{ie} = \frac{1}{h_{ie}}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test frequency (see 3.).

b. Test voltages and currents (see 3.).

c. Parameter to be measured.

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METHOD 3231

SMALL-SIGNAL, SHORT-CIRCUIT OUTPUT ADMITTANCE

1. Purpose. The purpose of this test is to measure the output admittance of the device under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common emitter configuration. For other parameters the circuit and procedure should be changed accordingly. See figure 3231-1.

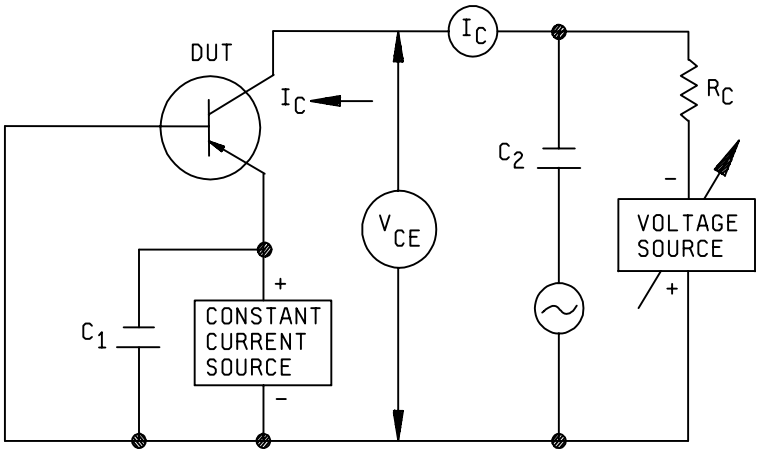

FIGURE 3231-1. Test circuit for small-signal short-circuit output admittance.

3. Procedure. The capacitors C_1 and C_2 shall present short-circuits at the test frequency in order to effectively couple and bypass the test signal. Resistor R_C is not zero but chosen for any convenient value.

Then: $$y_{oe} = \frac{I_c}{V_{ce}}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test frequency (see 3.).

b. Test voltages or currents (see 3.).

c. Parameter to be measured.

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METHOD 3236

OPEN-CIRCUIT OUTPUT CAPACITANCE

1. Purpose. The purpose of this test is designed to measure the open-circuit output capacitance of the device under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common base configuration. For other parameters the circuit and procedure should be changed accordingly. See figure 3236-1.

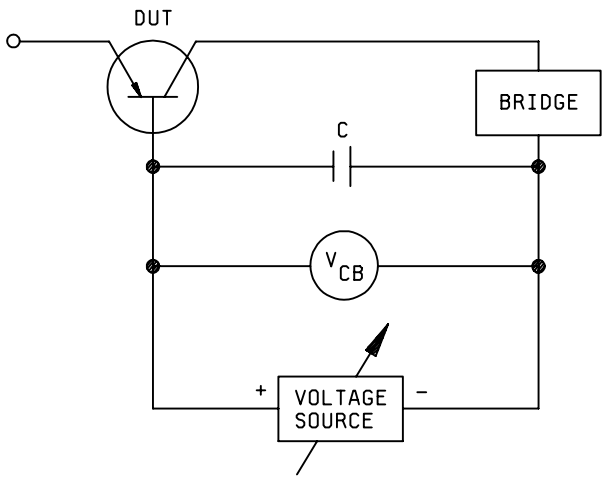

FIGURE 3236-1. Test circuit for open-circuit output capacitance.

3. Procedure. The bridge should have low dc resistance between its output terminals and should be capable of carrying the specified collector current without affecting the desired accuracy of measurement. The emitter should be open-circuited to ac and the frequency of measurement shall be as specified. Capacitor C should be sufficiently large to provide a short-circuit at the test frequency.

3.1 Measurement. The capacitance reading instrument is nulled with the circuitry connected, thereby eliminating errors due to the stray capacitances of the circuit wiring. The device to be measured is inserted into the test socket, is properly biased, and the output capacitance is measured.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test voltages or currents (see 3.).

b. Measurement frequency (see 3.).

c. Parameter to be measured.

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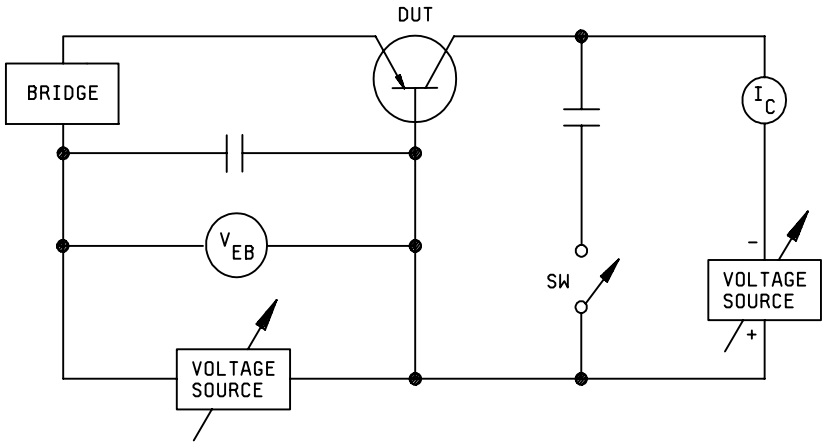
METHOD 3240.1

INPUT CAPACITANCE
(OUTPUT OPEN-CIRCUITED OR SHORT-CIRCUITED)

1. Purpose. The purpose of this test is to measure the shunt capacitance of the input terminals of the device under the specified conditions.

2. Test circuit. See figure 3240-1.



NOTE: For other configurations, the circuit may be modified in such a manner that it is capable of demonstrating device conformance to the minimum requirements of the applicable specification sheet.

FIGURE 3240-1. Test circuit for input capacitance (output open-circuited or short-circuited).

3. Procedure. The bridge should have a low dc resistance between the input terminals and should be capable of carrying the required emitter current without effecting the desired accuracy of measurement. The specified voltages or voltage and current shall be applied to the terminals; an ac small-signal shall be applied to the input terminals. Switch SW shall be opened or closed depending upon whether the output is intended to be ac open-circuited or ac short-circuited. The input capacitance shall then be measured. The capacitance reading instrument is nulled with the circuitry connected, thereby eliminating errors due to stray capacitances and circuit wiring.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test voltages or currents (see 3.).

   b. Test frequency (see 3.).

   c. Whether output is to be open-circuited or short-circuited.

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METHOD 3241

DIRECT INTERTERMINAL CAPACITANCE

1. Purpose. The purpose of this test is to measure the direct interterminal capacitance between specified terminals using specified electrical biases.

2. Apparatus. A direct capacitance bridge or resonance method may be used to determine the value of the direct interterminal capacitance.

3. Procedure. The direct interterminal capacitance may be determined by using method A or method B as follows.

3.1 Method A. The specified voltage shall be applied between specified terminals: an ac small-signal shall be applied to the terminals and the direct interterminal capacitance shall be measured. The lead capacitance beyond .5 inch (12.70 mm) from the body seat shall be effectively eliminated by suitable means such as test socket shielding. The abbreviations and symbols used are defined as follows:

C_{cb}(dir): Collector to base interterminal direct capacitance.

C_{eb}(dir): Emitter to base interterminal direct capacitance.

C_{ce}(dir): Collector to emitter interterminal direct capacitance.

3.2 Method B. A suitable resonance method can be utilized to measure the following two-terminal capacitances:

C_1: Capacitance between collector terminal and ground, with base and emitter terminals grounded.

C_2: Capacitance between the base terminal and ground, with collector and emitter terminals grounded.

C_3: Capacitance between the collector and base terminals strapped together and ground, with the emitter terminal grounded.

The direct interterminal capacitance can then be calculated from the following relationship:

$$C_{cb}(dir) = \frac{C_1 + C_2 - C_3}{2}$$

The direct interterminal capacitance for other configurations may be determined by suitable modifications of the above procedure. Such modifications shall be capable of demonstrating device conformance to the minimum requirements of the applicable specification sheet.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Terminal arrangement.

b. DC biasing conditions.

c. Test voltage or current.

d. Measurement frequency.

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METHOD 3246.1

NOISE FIGURE

1. Purpose. The purpose of this test is to measure the noise figure of the device under the specified conditions.

2. Apparatus. An average responding rms calibrated indicator shall be used in addition to other suitable apparatus to measure the noise figure of the diode.

3. Procedure. The voltage and current specified in the applicable specification sheet shall be applied to the terminals, and the noise figure shall then be measured at the frequency specified in the applicable specification sheet (normally 1,000 Hz) with an input resistance of 1,000 A and as referred to a 1 Hz bandwidth.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test voltage or current.

   b. Test frequency.

   c. Load resistance.

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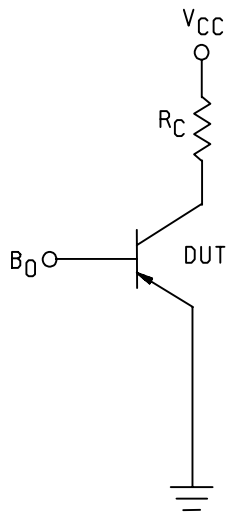
METHOD 3251.1

PULSE RESPONSE

1. Purpose. The purpose of this test is to measure the pulse response (t_d, t_r, t_s, and t_f) of the device under the specified conditions.

2. Test circuit. See figures 3251-1 and 3251-2.



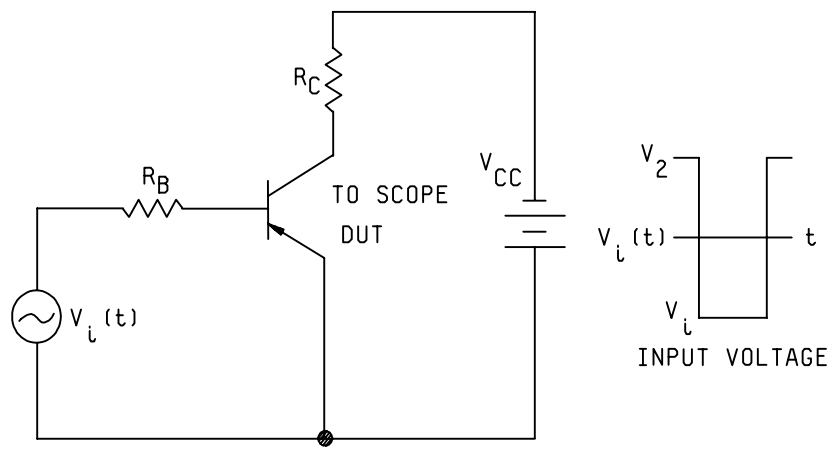


FIGURE 3251-1. Test circuit for pulse response, test condition A.

FIGURE 3251-2. Test circuit for pulse response, test condition B.

3. Procedure. The pulse response of the device shall be measured using test condition A or B.

3.1 Test condition A. The device shall be operated in the common emitter configuration as shown on figure 3251-1 with the collector load resistance (R_C) and collector supply voltage (V_{CC}) specified. When measuring delay or rise time, $I_{B(0)}$ and $I_{B(1)}$ or $V_{BE(1)}$ shall be specified. When measuring storage or fall time, $I_{B(1)}$ or $V_{BE(1)}$ and $I_{B(2)}$ or $V_{BE(2)}$ shall be specified. The input transition and the collector voltage response detector shall have rise and response fall times such that doubling these responses will not affect the results greater than the precision of measurement. The current and voltages specified shall be constant. Stray capacitance of the circuit shall be sufficiently small so that doubling it does not affect the test results greater than the precision of measurement.

$I_{B(0)}$ = prior off state base current.

$V_{BE(0)}$ = prior off state base to emitter voltage.

$I_{B(1)}$ = on state base current.

$V_{BE(1)}$ = on state base to emitter voltage.

$I_{B(2)}$ = post off state base current.

$V_{BE(2)}$ = post off state base to emitter voltage.

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3.2 Test condition B. The device shall be operated in the test circuit shown on figure 3251-2 (constant current drive) with the voltages and component values as specified. The pulse or square-wave generator and scope shall have rise and fall response times such that doubling these responses will not affect the results greater than the precision of measurement.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test condition (A or B).

b. Collector load resistance (R_C) and collector supply voltage (V_{CC}) for A.

c. Base resistance (R_B) collector load resistance (R_C), and collector supply voltage (V_{CC}) for B.

d. Test voltages or currents (see 3.).

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METHOD 3255

LARGE-SIGNAL POWER GAIN

1. Purpose. The purpose of this test is to measure the ratio of ac output power to the ac input power (usually specified in dB) under specified large-signal conditions.

2. Test circuit. The test circuit shall be as specified in the applicable specification sheet.

3. Procedure. The procedure shall be as specified in the applicable specification sheet.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

   a. Test voltages and currents.

   b. Test frequency (if other than 1,000 Hz).

   c. Test circuit.

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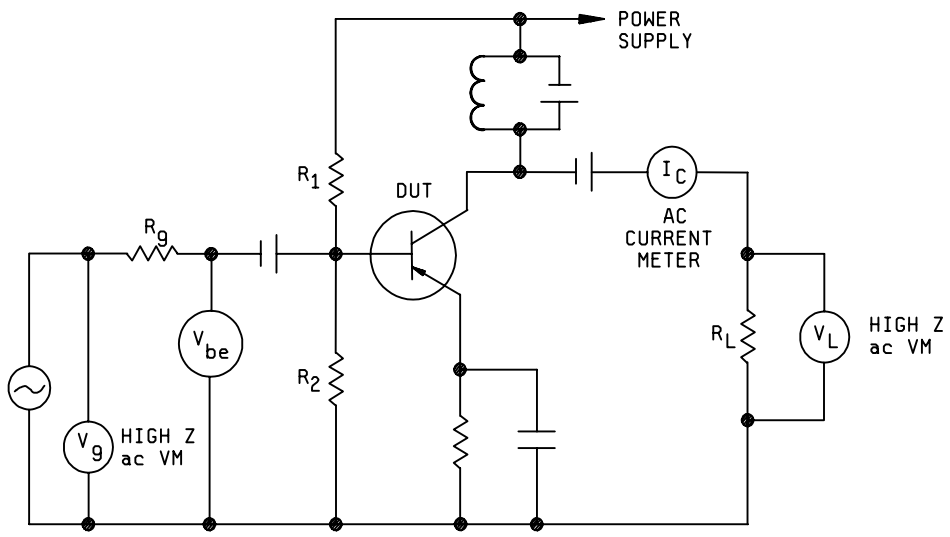
METHOD 3256

SMALL-SIGNAL POWER GAIN

1. Purpose. The purpose of this test is to measure the ratio of the ac output power to the ac input power under the specified conditions (usually specified in dB) for small-signal power gain.

2. Test circuit. See figure 3256-1.



NOTE: For other configurations, the circuit should be modified in such a manner that the circuit is capable of demonstrating device conformance to the applicable specification sheet.

FIGURE 3256-1. Test circuit for small-signal power gain.

3. Procedure. The specified voltage(s) and current(s) should be applied to the terminals; an ac small-signal should be applied to the input terminals of the specified circuit. The resistors R_1 and R_2 should have values larger than the h_{ie} of the device. The phase angle 1 between the input current and V_{be} shall be considered to be 0, if the specified test frequency is less than the extrapolated unity gain frequency (f_t) of the device.

Then, for common emitter:

$$P_{ge} = 10 \log \frac{P_{out}}{P_{in}}$$

$$Where, P_{in} = (V_{be})(i_b) \cos \theta$$

$$i_b = \frac{V_g - V_{be}}{R_g}$$

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$$P_{out} = (i_c)^2 (R_L) \; or \; \frac{(V_L{}^2)}{R_L}$$

$$Thus, \; P_{ge} = 10 \log \frac{(i_c)^2 (R_L)}{(V_{be})\left(\frac{V_g - V_{be}}{R_g}\right)} \quad or$$

$$10 \log \frac{\frac{V_L{}^2}{R_L}}{V_{be}\left(\frac{V_g - V_{be}}{R_g}\right)}$$

For other configurations, modifications to the procedure should be made in such a manner that it is capable of demonstrating device conformance to the applicable specification sheet.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test circuit.

   b. Test voltage(s) and current(s).

   c. Test frequency (if other than 1,000 Hz).

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METHOD 3261.1

EXTRAPOLATED UNITY-GAIN FREQUENCY

1. Purpose. The purpose of this test is to determine the extrapolated unity-gain frequency (gain-bandwidth product) of the device under the specified conditions.

2. Test circuit. The test circuit employed in determining the extrapolated unity-gain frequency shall be that which is used for measuring the magnitude of the common emitter small-signal, short-circuit forward-current transfer ratio. (See method 3306.)

3. Procedure. The magnitude of the common emitter short-circuit forward-current transfer ratio shall be determined at the specified frequency with the specified bias voltages and currents applied. The product of the specified signal frequency (f) and the measured common emitter small-signal, short-circuit forward-current transfer ratio (h_{fe}) is the extrapolated unity gain frequency (f_t).

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test current and voltage.

   b. Test frequency.

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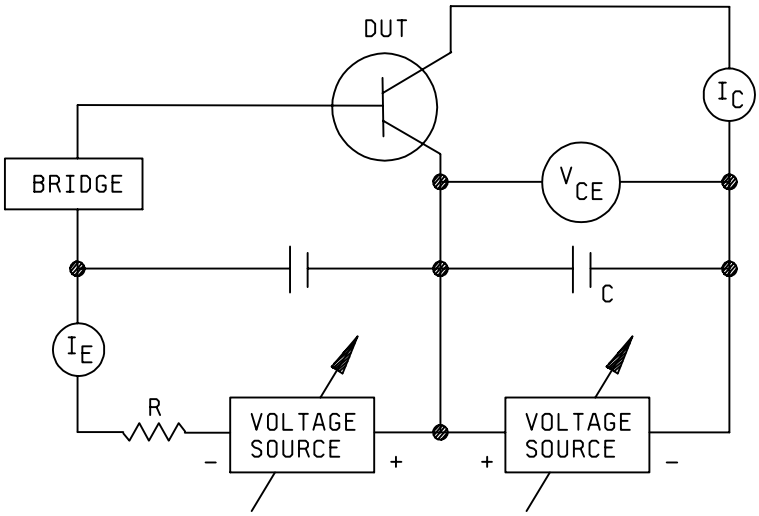
METHOD 3266

REAL PART OF SMALL-SIGNAL, SHORT-CIRCUIT INPUT IMPEDANCE

1. Purpose. The purpose of this test is to measure the resistive component of the small-signal, short-circuit input impedance of the device under the specified conditions.

2. Test circuit. See figure 3266-1.



NOTE: The circuit shown is used for measuring the common emitter real part of the small-signal, short-circuit input impedance. For other device configurations, the above circuitry should be modified in such a manner that it is capable of demonstrating device conformance to the minimum requirements of the applicable specification sheet.

FIGURE 3166-1. Test circuit for real part of small-signal short-circuit input impedance.

3. Procedure. The voltage and current specified shall be applied to the terminals. An ac small-signal of the frequency specified shall be applied to the input terminals and the output terminals shall be ac short-circuited. The real part of the input impedance shall then be measured.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test voltage and current.

b. Test frequency.

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3300 Series

High frequency tests

Care shall be taken that, in designing the circuit and transistor mounting, adequate shielding and decoupling are provided and that series inductances in circuits are negligible.

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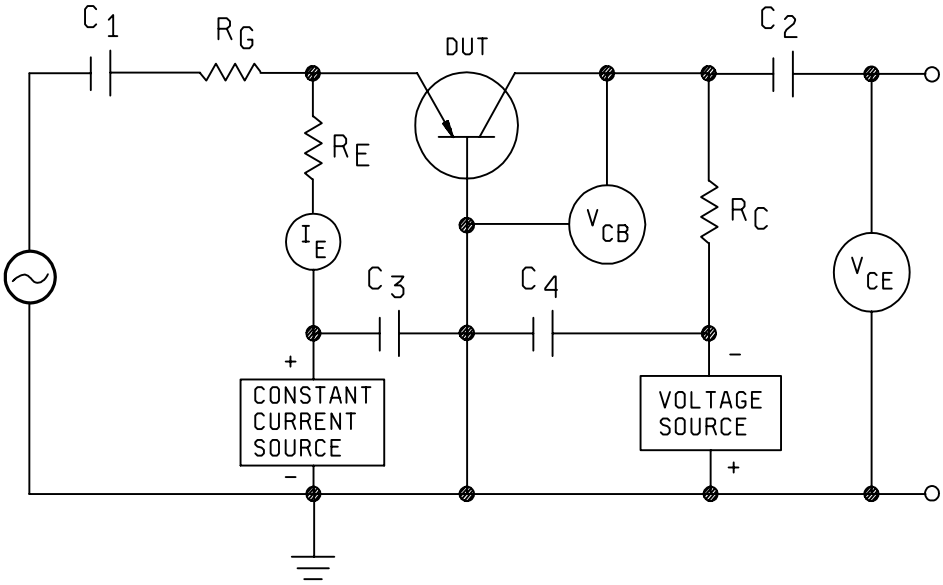
METHOD 3301

SMALL-SIGNAL, SHORT-CIRCUIT, FORWARD-CURRENT TRANSFER RATIO
CUT OFF FREQUENCY

1. Purpose. The purpose of this test is to measure the forward-current transfer ratio cut off frequency under the specified conditions.

2. Test circuit. The circuit and procedure shown are for common base configuration. For other parameters the circuit and procedure should be changed accordingly.



NOTE: Normal VHF circuit precautions should be taken. At frequencies higher than 10 MHz, the use of this circuit may lead to excessive errors. The biasing circuit shown is for the purposes of illustration only and any stable biasing circuit may be used.

FIGURE 3301-1. Test circuit for small-signal, short-circuit forward-current transfer ratio cutoff frequency.

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3. Procedure. The voltages and currents shall be as specified. Resistors R_G and R_E shall be large to present open-circuits to h_{ib}. Resistor R_C shall be small to present a short-circuit to h_{ob}. Capacitors C_1, C_2, C_3, and C_4 shall present short-circuits at the test frequency to effectively couple and bypass the test signal.

a. The circuitry shall be frequency independent. This can be checked by removing the device from the circuit and shorting between emitter and collector with no bias voltages applied. Care should be taken to ensure that the generator has a sufficiently pure waveform and that the high-impedance voltmeter is adequately sensitive to enable the measurement to be made at a low enough signal level to avoid the introduction of harmonics by the device.

b. The generator is set to a frequency at least 30 times lower than the lowest cut off frequency limit and the low frequency h_{fb} is measured. The frequency is then increased until the magnitude of h_{fb} has fallen to $1/\sqrt{2}$ of its low frequency value. This is the cut off frequency.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test voltages and currents (see 3.).

b. Parameter to be measured.

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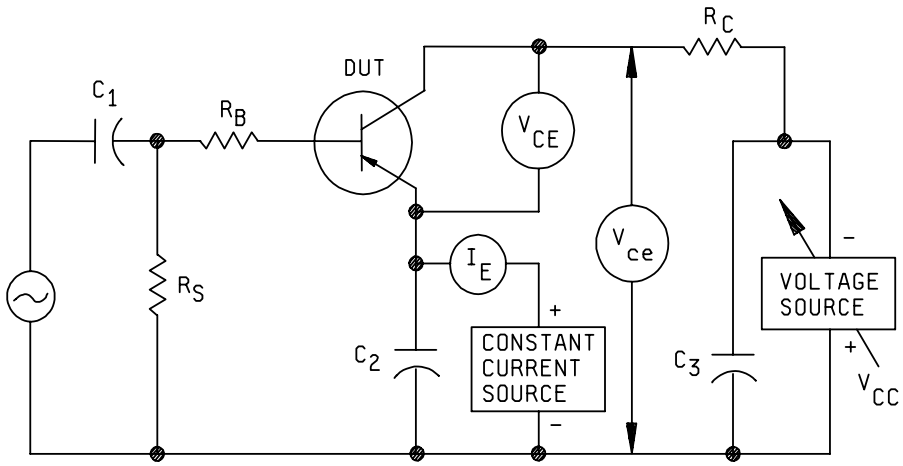
METHOD 3306.4

SMALL-SIGNAL, SHORT-CIRCUIT FORWARD-CURRENT TRANSFER RATIO

1. Purpose. The purpose of this test is to measure the forward-current transfer ratio under the specified conditions.

2. Test circuit. The circuit (see figure 3306-1) and procedure shown are for common emitter configuration. For other parameters the circuit and procedure should be changed accordingly.



NOTE: The biasing circuit shown is for purpose of illustration only. Other stable biasing circuits may be used.

FIGURE 3306-1. Test circuit for small-signal, short-circuit forward-current transfer ratio.

3. Procedure. Capacitors C_1, C_2, and C_3 shall present short-circuits in order to effectively couple and bypass the test signal at the frequency of measurement. The value of R_B shall be sufficiently large to provide a constant current source. Resistor R_C shall be a short-circuit compared to the output impedance of the device. With the device removed from the circuit, a shorting link is placed between the base and collector and the output voltage of the signal generator is adjusted until a reading of one (in arbitrary units) is obtained on the high-impedance ac voltmeter, V_{ce}. With the device in the circuit and biased as specified, the reading on voltmeter V_{CE} is now equal to the magnitude of (h_{fe}). (NOTE: Care must be taken to assure that the output signal is not clipped.)

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Measurement frequency.

b. Test voltages and currents.

c. Parameter to be measured.

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METHOD 3311

MAXIMUM FREQUENCY OF OSCILLATION

1. Purpose. The purpose of this test is to measure the maximum frequency of oscillation for the device under the specified conditions.

2. Test circuit. The circuit utilized for the maximum frequency of oscillation test shall be as specified in the applicable specification sheet.

3. Procedure. The voltage(s) and current(s) specified shall be applied to the device in the circuit specified, and the circuit resonant frequency shall be increased until oscillation ceases. The frequency at which oscillation ceases is the maximum frequency of oscillation.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test circuit.

   b. Test voltage(s) and current(s).

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METHOD 3320

RADIO FREQUENCY (RF) POWER OUTPUT, RF POWER GAIN, AND COLLECTOR EFFICIENCY

1. TEST CONDITION A

1.1 Purpose. The purpose of this test is to measure the RF power output, RF power gain, and collector efficiency of a transistor under actual operating conditions in a specific RF amplifier test circuit. Test condition A shall be valid for devices operating at RF power levels greater than 10 dBm when tested in the frequency range between 10 MHz and 2 GHz.

1.2 Apparatus. All referenced equipment may be replaced by equivalents suitable for the frequency of test. The equipment setup shall be as shown on figures 3320-1 and 3320-2.

1.3 Procedure. The test fixture shall be disconnected and directional couplers number 1 and number 2 shall be directly connected using a minimum number of connectors. The RF switch shall be set to the output position C and the frequency and RF power source adjusted to the specific conditions by monitoring the frequency counter and RF power meter respectively. The RF switch shall be set to position A and the variable attenuator adjusted to obtain the identical reading as power out in position C. The test fixture shall be reconnected with the DUT inserted and the dc power supply adjusted to the specified voltage. The circuit output tuning shall be adjusted for maximum power gain and circuit input tuning for minimum reflected power. (The RF switch shall be alternated between power in, reflected power, and power out while tuning and this procedure shall be repeated as many times as necessary to obtain minimum reflected power and maximum power out.) The power in level shall be checked before taking the final measurement. If input reflected power calibration is required, the above procedure shall be repeated with directional coupler number 1 reversed and switch position A changed to switch position B.

NOTE: Minimum reflected power is defined as minimum reading obtained with switch in position 'B' and maintaining power in.

1.3.1 Measurements.

1.3.1.1 Power output. Power output (P_{out}) is measured by adjusting the RF power source to obtain the specified forward input power and reading the output power in watts.

1.3.1.2 Power input. Power input (P_{in}) is measured by adjusting the RF power source to obtain the specified forward output power and reading the input power in watts.

1.3.1.3 Power gain. Power gain (G_p) is measured by adjusting the RF power source to the value of P_{in} which produces the specified P_{out}. P_{in} and P_{out} shall be observed and the gain (in dB) determined as follows:

$$G_P = 10 \log \frac{P_{out}}{P_{in}}$$

1.3.1.4 Collector efficiency. Collector efficiency (η) is measured by adjusting the RF source to the specified P_{in} (or P_{out}) and reading P_{out}. The collector efficiency shall be computed as follows:

$$\eta(\%) = \frac{P_{out}(W)}{P_{in}(W)} X\ 100 = \frac{P_{out}(W)}{I_C\ X\ V_{CC}} X\ 100$$

Where: I_C = collector current

V_{CC} = collector supply voltage

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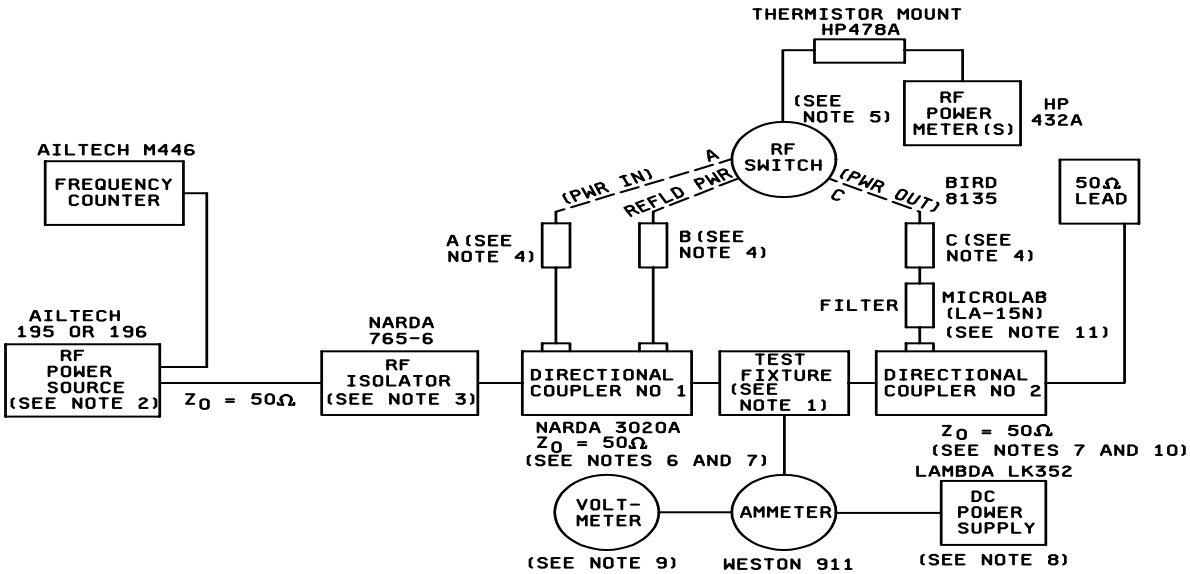

FIGURE 3320-1. Test equipment setup.

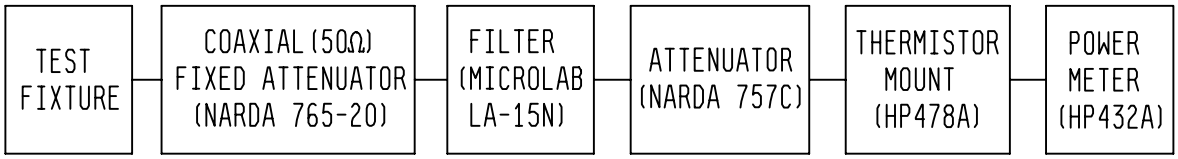

FIGURE 3320-2. Alternate test equipment setup.

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NOTES:

1. Test fixture is the circuit as described in the applicable applicable specification sheet (circuit layout and components quality are critical).
2. RF power source shall be a unit capable of generating desired power level at desired frequency with a harmonic and spurious content ≥ 20 dB below operating frequency level of 100 MHz to 1 GHz.
3. The RF isolator shall be a device (e.g., pad, circulator) capable of establishing ≥ 20 dB of isolation between RF power source and test fixture. (A resistive attenuator shall be used for out-of-band isolation.)
4. Variable attenuators (or fixed, if calibrated): Attenuators are set so that the actual power into and out of test fixture are known. Attenuation on directional coupler number 2 shall be calibrated against a known working standard either by means of a calibration chart or suitable adjustment if variable. Attenuation at position A of directional coupler number 1 shall be calibrated or adjusted so that actual power at test fixture is known. Attenuation at position B shall be adjusted to establish sensitivity needed to measure reflected power (normally 10 dB less than the attenuation at position A).
5. RF switch may be eliminated if additional power meters are used.
6. More than one directional coupler may be used in place of coupler number 1. If more than one coupler is used, the power in and reflected power position may be interchanged.
7. The directional couplers shall have a minimum directivity of 30 dB and a nominal 20 dB coupling attenuation except where test level sensitivities require 10 dB or less attenuation.
8. The dc power supply shall be RF decoupled at the test fixture.
9. Voltmeter readings shall be sensed at test fixture, not at power supply.
10. Coupler number 2 and 50 Ω load may be replaced by coaxial fixed attenuators (Narda) and a power meter (HP 432A). Power meter may be separate or connected to the one shown on the other side through port C of the RF switch (see figure 3320-2).
11. If harmonic or subharmonic contents less than 20 dB down from the desired signal are present and could influence the measured output power, a suitable filter (low pass, band pass, or high pass) shall be employed between the attenuator(s) and power meter used for output power measurement.

FIGURE 3320-2. Alternate test equipment setup - Continued.

1.4 Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test voltage (and current, if applicable).

b. Test frequency.

c. Power input (or output).

d. Test circuit with critical parts and layout specified.

e. Parameter to be measured.

2. TEST CONDITION B

2.1 Purpose. The purpose of this test is to measure the RF power output, RF power gain, and collector efficiency of a transistor under actual operating conditions in a specific RF amplifier test circuit. Test condition B shall be valid for devices operating at RF power levels greater than 0 dBm when tested in the frequency range between 100 MHz and 10 GHz.

2.2. Apparatus. All referenced equipment may be replaced by equipment of equal or superior capability. A typical equipment setup is as follows (see figures 3320-3, 3320-4, and 3320-5). All components shall be suitable for the frequency range of measurement.

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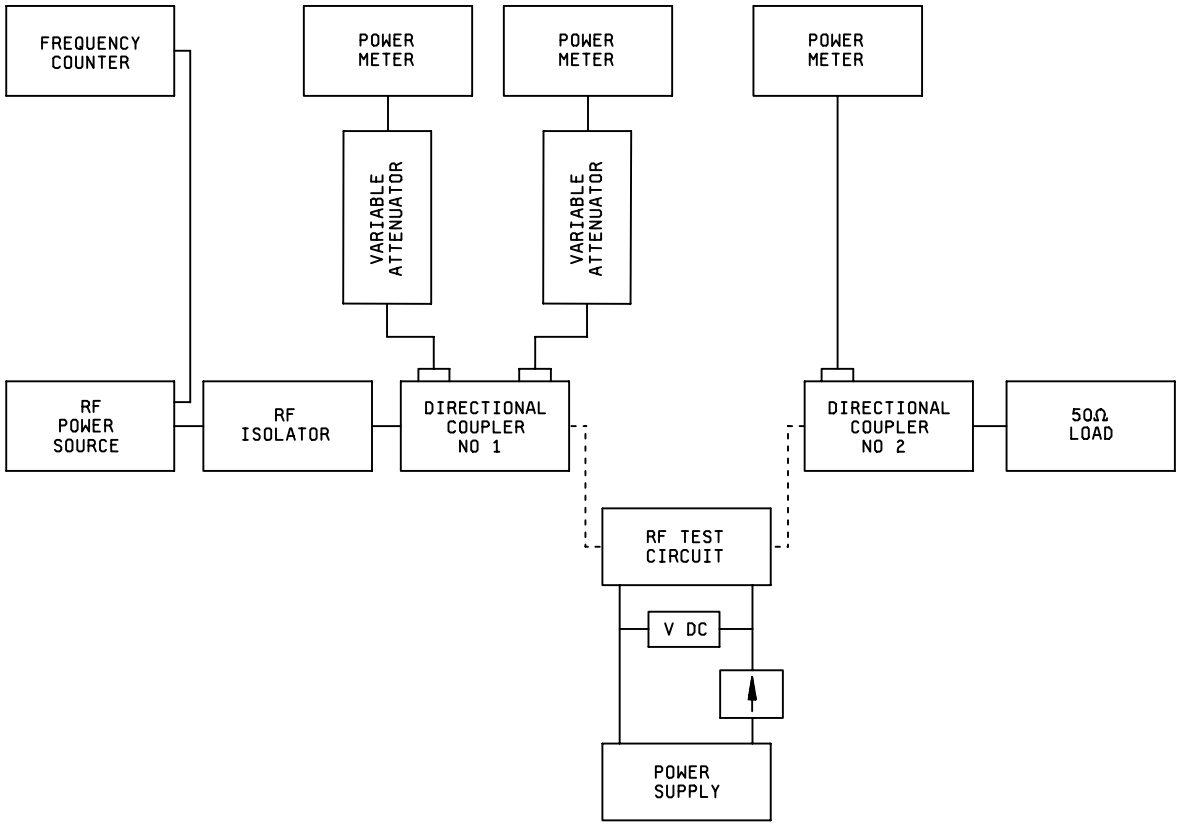

FIGURE 3320-3. RF test setup.

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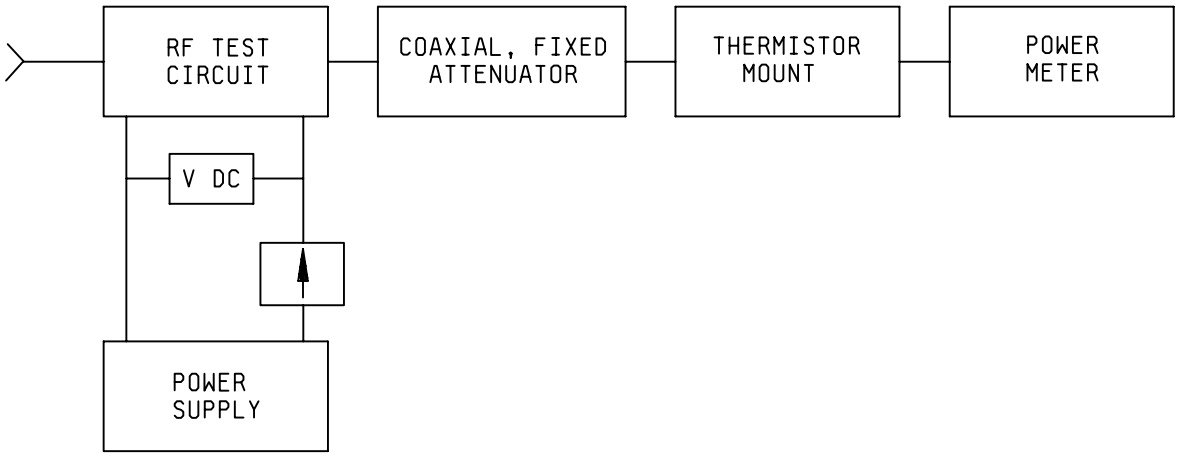

FIGURE 3320-4. Alternate output setup.

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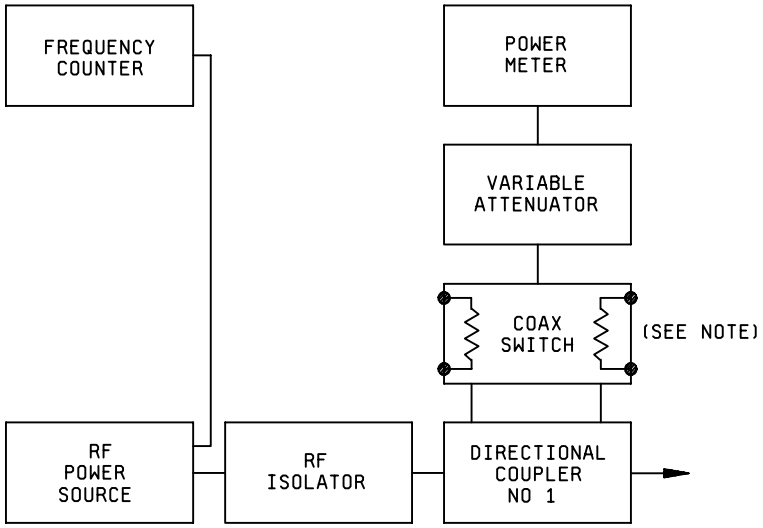

NOTE: The unswitched port automatically terminates the alternate coupler port in 50 Ω when using the coax switch specified in the equipment list.

FIGURE 3320-5. Alternate input setup.

NOTES:

1. The test fixture referred to in this test method is the circuit which is described in the applicable specification sheet (circuit layout and component quality are critical).
2. The RF power source shall be a unit capable of generating desired power levels at the frequency of interest. All harmonics and spurious content shall be at least 26 dB below the output level. When necessary, a suitable filter (low pass or band pass) should be used between the RF source and the isolator to reduce the second harmonic. A similar filter should be used in the output circuit between the coupler and the power meter unless the harmonic levels of the DUT are less than 26 dB below the measurement level. If the filter is to be used, its insertion loss should be calibrated and accounted for at the measurement frequency.
3. Coupler number 2 and the 50 Ω load may be replaced by a coaxial fixed attenuator and a power meter (see figure 3320-4). If employed, the output low pass filter should be placed between the attenuator and power meter.
4. The two power meters connected to coupler number 1 may be replaced by one power meter and a good quality coaxial transfer switch. (The use of such switches is discouraged at frequencies above 4 GHz unless precautions are taken to account for RF losses (see figure 3320-5).) These switches are designed for use in 50 systems. The unswitched port is automatically terminated internally with 50 Ω and loads the alternate coupler port.
5. The RF isolator shall be a device (e.g., pad, circulator) capable of establishing ≥ 20 dB of isolation between RF power source and test fixture.
6. The directional couplers shall have a minimum directivity of 30 dB and a nominal 20 dB coupling attenuation except where test level sensitivities require 10 dB or less attenuation. (Greater accuracy results from using the highest coupling possible, consistent with the measurement.)
7. The dc power supply shall be RF decoupled at the test fixture.
8. Voltmeter readings shall be sensed at the test fixture, not at power supply.
9. A calibrated wavemeter may be used in lieu of the frequency counter specified on figure 3320-3.

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2.3 Equipment list. (All referenced equipment may be replaced by equipment of equal or superior quality.)

Equipment	Manufacturer	Model
CW source	As desired	1/
Isolator	Addington Labs	1/
Dual directional coupler	NARDA	3022
Variable attenuator	Merrimac	Au-25A5
Average power meter	Hewlett-Packard	432 A
Coax switch	Hewlett-Packard	33311 B/C
Fixed attenuator	NARDA	766-20
L.P. filter	Microlab FXR	1/
Power supply	Hewlett-Packard	6296 A
RF test fixture	(See applicable specification sheet)	
Voltmeter	Meter-mod Instruments	420 R
Ammeter	Meter-mod Instruments	420 R

2.4 Test procedure.

2.4.1 RF setup calibration procedure.

a. With the RF test setup as on figure 3320-3 and with the test fixture removed, hook up the output of coupler number 1 to the input of coupler number 2 (attenuation of directional coupler number 2 shall be calibrated against a known working standard either by means of calibration chart or suitable adjustment if variable).

b. Set the frequency of the source as indicated by the readout of the frequency counter or a dip in the power level when using an in-line wavemeter.

c. Adjust the variable attenuator on the source by decreasing the attenuator until the desired power level is observed on the output power meter (apply correction factor if necessary to correct for coupler number 2 or output attenuator error).

d. Observe the input power meter, and adjust the attenuator associated with this meter until it reads the same power output as the output power meter in . (If using the alternate input setup on figure 3320-5, calibrate with coaxial switch in the forward position.)

e. Disconnect the output coupler and power meter from the circuit so that the output of coupler number 1 is open-circuited. Adjust the attenuator associated with the reflected power meter until it reads the same as the forward meter. With a calibrated short on the input of the coupler, observe the difference in reflected power between an open-circuit condition and a short. Adjust the reflected power variable attenuator for an average between the open and short-circuit readings. (If using the alternate input setup on figure 3320-5, the reflected power port is automatically calibrated when the forward power is calibrated if both ports of the coupler are balanced.)

1/ Model depends on frequency of test: See manufacturer's catalog for correct model number.

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f. Increase the input attenuator until power output is zero (calibration completed).

g. If multiple frequency testing is required repeat through 1f for each frequency, noting the variable attenuator and power source settings for each specified frequency. All equipment must be returned to the noted settings during test at each specified frequency point.

2.4.2 RF testing.

a. Make certain the dc power supply is off.

b. With the RF test setup on figure 3320-3 or with alternate circuits of figures 3320-4 and 3320-5, and with the test fixture in place, clamp a device in the test fixture.

c. Switch on the dc power supply. Precautions should be observed to prevent voltages exceeding the specified test level.

d. Adjust the attenuator at the source until the input power reads the appropriate power.

e. Observe the output power, reflected power, and collector current (record, if necessary).

f. Increase the attenuator at the source until the input power reads zero.

g. Repeat through as required, with the previously noted power source and attenuator settings, if other test frequencies are required.

h. Switch off the dc power supply.

i. Remove the device from the test fixture.

2.5 Data required (measurements).

a. Power output (P_{out}) is measured by adjusting the RF power source as outlined in to obtain the specified forward input power and reading the output power in watts.

b. Power input (P_{in}) is measured by adjusting the RF power source to obtain the specified forward output power and reading the input power in watts.

c. Power gain (Gp) is calculated from the measured RF data. P_{in} and P_{out} shall be observed and the gain (in dB) determined as follows:

$$G_p = 10 \log \frac{P_{out}}{P_{in}}$$

d. Collector efficiency (η) is calculated from the measured RF and dc data. The collector efficiency shall be computed as follows:

$$\eta(\%) = \frac{P_{out}(W)}{P_{in}(dc-w)} X\ 100 = \frac{P_{out}(W)}{I_C\ X\ V_{CC}} X\ 100$$

Where: I_C = Collector current

V_{CC} = Collector supply voltage

e. Reflected power may be observed directly from the power meter if the setup is calibrated as specified in . Even though reflected power may not be part of the RF specifications, it is included here because it is an indication as to how much of the input is actually reaching the device. Good practice dictates that, where possible, the external circuit should be adjusted from minimum reflected power.

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2.6 Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test voltage (and current if applicable).

b. Test frequency.

c. Power input or power output.

d. Test circuit with critical parts and layout specified.

e. Parameter(s) to be measured.

f. Parameter(s) to be calculated.

g. RF test fixture.

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3400 Series

Electrical characteristics tests for MOS field-effect transistors

Circuits are shown for n-channel field-effect transistors in one circuit configuration only. They may readily be adapted for p-channel devices and for other circuit configurations.

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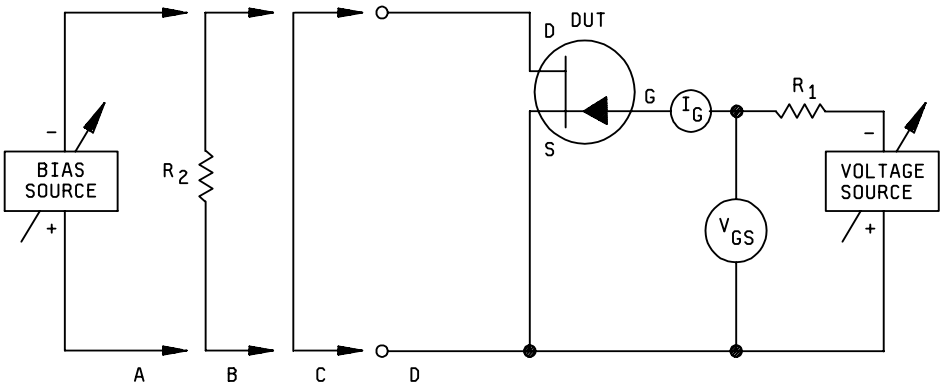
METHOD 3401.1

BREAKDOWN VOLTAGE, GATE-TO-SOURCE

1. Purpose. The purpose of this test is to determine if the breakdown voltage of the field-effect transistor or IGBT under the specified conditions is greater than the specified minimum limit. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3401-1.



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 3401-1. Test circuit for breakdown voltage, gate-to-source.

3. Procedure. The resistor R_1 is a current-limiting resistor and should be of sufficiently high resistance to avoid excessive current flowing through the device and current meter. The voltage shall be gradually increased, with the specified bias condition (condition A, B, C, or D) applied, from zero until either the minimum limit for $V_{(BR)GSX}$ or the specified test current is reached.1/ The device is acceptable if the minimum limit for $V_{(BR)GSX}$ is reached before the test current reaches the specified value. If the specified test current is reached first, the device shall be considered a failure.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test current (see 3.).

   b. Bias condition:

      A: Drain-to-source: Reverse bias (specify bias voltage).

      B: Drain-to-source: Resistance return (specify resistance of R_2).

      C: Drain- to-source: Short-circuit.

      D: Drain-to-source: Open-circuit.

1/ $V_{(BR)GSX}$: Breakdown voltage, gate-to-source, with the specified bias condition applied from drain-to-source.

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METHOD 3402

MOSFET GATE EQUIVALENT SERIES RESISTANCE

1. Purpose. The purpose of this test is to determine the Gate Equivalent Series Resistance (ESR) of MOSFET devices. This can be done in two ways, using either manual test circuit or LCR test equipment. This test method provides a mean to ensure switching consistency of power MOSFET. ESR combined with gate charge measurements provide an alternative to high-current high-speed measurements where device fast switching characteristics are over-masked by test circuit stray elements.

1.1 Background. High-speed switching measurements of power semiconductor devices are sensitive and dependent to the stray elements (capacitive, inductive and resistive impedances) of the test circuit. As a result, switching data of identical devices have difficult time reaching reasonable agreement. The ESR by design directly relates to die gate processing such as polysilicon doping level, metallization, contact resistance, all of which affect high-speed performance. Since big process variation usually results in an ESR increase in significant magnitude, the ESR test method provide an alternative for the industry to reach agreement on high speed switching measurements.

2. Definitions. The following symbols and terminology shall apply for the purpose of this test method:

a. R_g Gate equivalent series resistance (ESR)

b. f Test frequency

c. C_g Effective gate capacitance

d. C_{iss} Input capacitance (small-signal common-source, short-circuit)

e. L Test circuit inductance

3. Condition A. This is the test in which a LCR Meter is used with the C_{iss} test circuit. The test frequency is fixed at 1 MHz and the Rg & Cg of MOSFET device-under-test are calculated by the impedance analyzer.

3.1 The apparatus required for this test condition shall include the following, configured as shown on figure 3402-1, as applicable to the specified test procedure:

a. C_{iss} Test Circuit, as shown in Figure 3402-1. Capacitors C1 and C2 present short circuits at the test frequency; L1 and L2 present high ac impedance at test frequency for isolation; Bridge has low dc resistance between its output terminals and capable of carrying test current without affecting the desired accuracy of measurement.

b. A LCR Meter capable to supply the sine wave signal with magnitude up to 1 Volt and frequency of MHz (1MHZ typical) and to measure series resistance and series capacitance

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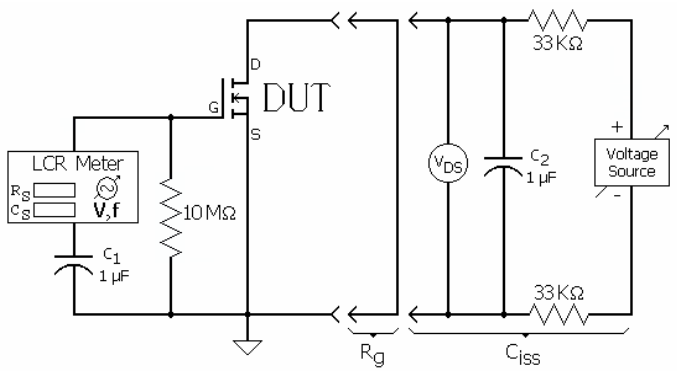

FIGURE 3402-1. Gate ESR testing setup for MOSFETs – Condition B.

3.2 Procedure. The test begins with applying 1MHZ sine wave voltage of less than 1V and measuring stray capacitances of test circuit and socket in both Drain and Source OPEN mode as well as SHORT mode (short Drain and Source contacts prior to this measurement). Insert MOSFET device-under-test and record R_S (C_S optional) measurements.

3.3 Summary. The following conditions & limit shall be specified in detail specification for Condition A:

a. Test frequency (in MHz), typical 1MHz.

b. Gate ESR, as R_S from LCR meter (in Ohms).

c. Effective gate capacitance, as C_S from LCR meter (pico-Farad), optional

4. Condition B. This is the test in which an external inductor is added in series with Rg & Cg of MOSFET device-under-test. The test frequency is then adjusted to get capacitive and inductive impedances cancelled out and thus pure resistance Rg can be measured.

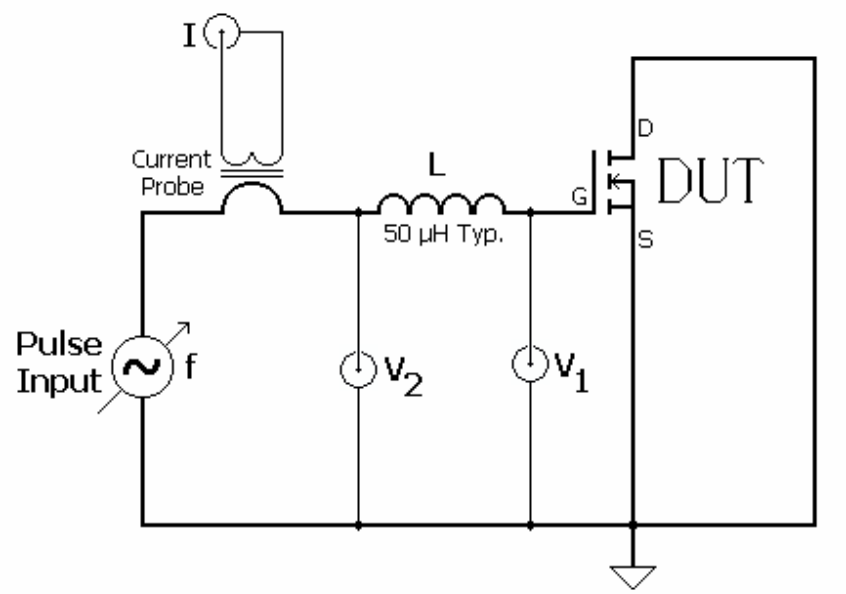

FIGURE 3402-2. Gate ESR testing setup for MOSFETs – Condition A.

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4.1 The apparatus required for this test condition shall include the following, configured as shown on figure 3402-2, as applicable to the specified test procedure:

a. Gate ESR Test Circuit, as shown in Figure 3402-2

b. A function generator source capable to supply the sine wave signal with magnitude up to 1 Volt and frequency of MHz (1MHZ typical).

c. Current Probe capable of high-frequency measurements

d. Oscilloscope capable of high-frequency measurements

4.2 Procedure. The test begins with applying 1 MHz sine wave voltage of less than 1 Volt. V_1 voltage is monitored not to exceed the rated VGS (typical ±20V). Adjust the test frequency until the source output voltage V_2 waveform and source output current I waveform are in phase. The MOSFET Gate ESR measurement can then be calculated from below formula:

$$R_g = \frac{V_2}{I}$$

4.3 Notes.

a. The effective Gate Capacitance can also be calculated with below formula

$$C_g = \frac{1}{(2\pi f)^2 \times L}$$

b. The inductor in the circuit is normally 50 μH in value; however, if the gate resistance (or capacitance) is very high then the proper inductor value can be estimated with below formula

$$L = \frac{1}{2 \times \left(2\pi 10^6\right)^2 \times C_{iss}}$$

4.4 Summary. The following conditions & limit shall be specified in detail specification for Condition A:

a. Test frequency (in MHz), about 1MHz.

b. Series inductor value (in micro-Henry), if not 50 μH.

c. Gate ESR (in Ohms).

d. Effective gate capacitance (pico-Farad), optional

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5. General note.

a. Even though the Gate ESR together with Gate Charges helps better representing MOSFET in high speed applications and circuit simulations, the lumped R_g and effective C_g presentation does have its limitation. Some power MOSFET die in latest technology do not have symmetrical or uniform connecting conductances from Gate and Source terminations to each individual cell or stripe structures. The switching responses from the lumped R_g and effective C_g model may not be true responses. The correct series resistor and parallel capacitor model in these cases suggests a somewhat test frequency dependence in lumped R_g measurement.

b. Because of DC Bias & AC Bias Dependencies of Cg, the DC voltage induced from AC Bias applying through LRC Series Resonant Circuitry would cause Cg to be changed. The measured Rg with Condition B at resonant frequency thus somewhat dependent of input signal

Series Resonant Frequency: $W_O = \frac{1}{\sqrt{L C_g}}$

Series Resonant Characteristic Impedance: $Z_O = \sqrt{\frac{L}{C}}$

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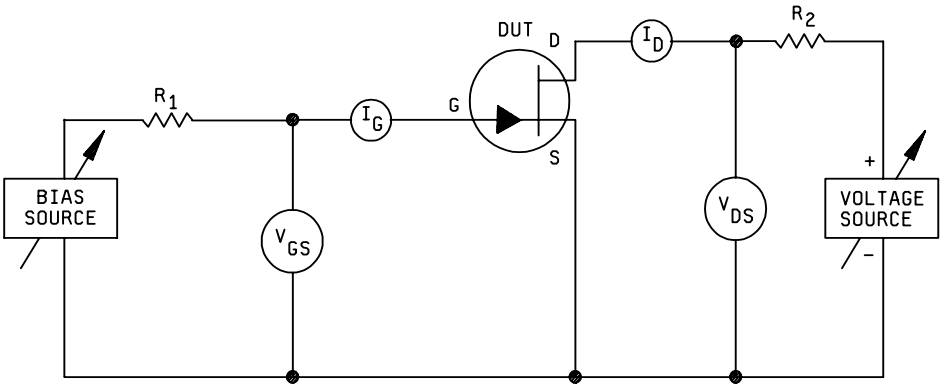
METHOD 3403.1

GATE-TO-SOURCE VOLTAGE OR CURRENT

1. Purpose. The purpose of this test is to measure the gate-to-source voltage or current of the field-effect transistor or IGBT under the specified conditions. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3403-1.



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 3403-1. Test circuit for breakdown voltage, gate-to-source.

3. Procedure. The voltage source and bias source shall be adjusted to bring V_{DS} and I_D to their specified values. The voltage V_{GS} or current I_G may then be read.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test voltages and currents (see 3.).

   b. Parameter to be measured.

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METHOD 3404

MOSFET THRESHOLD VOLTAGE

1. Purpose. The purpose of this test establishes the means for measuring MOSFET threshold voltage. This method applies to both enhancement-mode and depletion-mode MOSFETs, and for both silicon-on-sapphire and bulk-silicon MOSFETs. It is for use primarily in evaluating the response of MOSFETs to ionizing radiation, and for this reason the test differs from conventional methods for measuring threshold voltage.

1.1 Definition.

MOSFET threshold voltage, $V_{GS(TH)}$: The gate-to-source voltage at which the drain current is reduced to the leakage current, as determined by this test method.

2. Apparatus. The apparatus shall consist of a suitable ammeter, voltmeters, and voltage sources. The apparatus may be manually adjusted or, alternatively, may be digitally programmed or controlled by a computer. Such alternative arrangements shall be capable of the same accuracy as specified below for manually adjusted apparatus.

2.1 Ammeter (A_1). The ammeter shall be capable of measuring current in the range specified with a full scale accuracy of ±0.5 percent or better.

2.2 Voltmeters (V_1 and V_2). The voltmeters shall have an input impedance of 10 mΩ or greater and have a capability of measuring 0 V to 20 V with a full scale accuracy of ±0.5 percent or better.

2.3 Voltage sources (V_{GS} and V_{DS}). The voltage sources shall be adjustable over a nominal range of 0 V to 20 V, have a capability of supplying output currents at least equal to the maximum rated drain current of the device to be tested, and have noise and ripple outputs less than 0.5 percent of the output voltage.

3. Procedure.

WARNING: The absolute maximum values of power dissipation, drain-to-source voltage, drain current, or gate-to-source voltage specified is either the applicable acquisition document or the manufacturer's specifications shall not be exceeded under any circumstances.

3.1 N-channel devices.

3.1.1 Test circuit for n-channel devices. The test circuit shown on figure 3404-1 shall be assembled and the apparatus turned on. With the voltage sources V_{DS} and V_{GS} set to 0 volts, the MOSFET to be tested shall be inserted into the test circuit. The gate-to-source polarity switch shall be set to the appropriate position, and voltage source V_{GS} shall be set 1.0 V negative with respect to the anticipated value of threshold voltage $V_{GS(TH)}$. Voltage source V_{DS} shall be adjusted until voltmeter V_2 indicates the specified drain-to-source voltage V_{DS}. The current I_D, indicated by ammeter A_1, and the gate-to-source voltage V_{GS}, indicated by voltmeter V_1, shall be measured and recorded.

3.1.2 Measurement for n-channel devices. The measurement shall be repeated at gate-to-source voltages which are successively 0.25 volts more positive until either the maximum gate-to-source voltage or maximum drain current is reached. If the gate-to-source voltage reaches 0 volts before either of these limits has been reached, the gate-to-source polarity switch shall be changed as necessary and measurements shall continue to be made at gate-to-source voltages which are successively 0.25 volts more positive until one of these limits has been reached.

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3.2 P-channel devices.

3.2.1 Test circuit for p-channel devices. The test circuit shown on figure 3404-2 shall be assembled and the apparatus turned on. With the voltage sources V_{GS} and V_{DS} set to 0 volts, the MOSFET to be tested shall be inserted into the test circuit. The gate-to-source polarity switch shall be set to the appropriate position, and voltage source V_{GS} shall be set 1.0 V positive with respect to the anticipated value of threshold voltage $V_{GS(TH)}$. Voltage source V_{DS} shall be adjusted until voltmeter V_2 indicates the specified drain-to-source voltage V_{DS}. The current I_D, indicated by ammeter A_1, and the gate-to-source voltage V_{GS}, indicated by voltmeter V_1, shall be measured and recorded.

3.2.2 Measurement for p-channel devices. The measurement shall be repeated at gate-to-source voltages are successively 0.25 volts more negative until either the maximum gate-to-source voltage or maximum drain current is reached. If the gate-to-source voltage reaches 0 volts before either of these limits has been reached, the gate-to-source polarity switch shall be changed as necessary and measurements shall continue to be made at gate-to-source voltages which are successfully 0.25 volts more negative until one of these limits has been reached.

3.3 Leakage current measurement. Using method 3415, the leakage current shall be measured.

3.3.1 Drain-to-source voltage. The drain-to-source voltage shall be as specified in 4.b.

3.3.2 Gate-to-source voltage. The gate-to-source voltage shall be five volts different from the anticipated threshold voltage in the direction of reduced drain current.

3.4 Gate-to-source voltage graph. The gate-to-source voltage, V_{GS}, shall be plotted versus the square-root of the drain current minus the leakage current, $\sqrt{I_D - I_L}$. At the point of maximum slope, a straight line shall be extrapolated downward. The threshold voltage ($V_{GS(TH)}$) is the intersection of this line with the gate-to-source voltage axis. Examples are shown on figure 3404-3.

3.5 Report. As a minimum, the report shall include the device identification, the test date, the test operator, the test temperature, the drain-to-source voltage, the range of gate-to-source voltage, the leakage current, and the threshold voltage.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test temperature. Unless otherwise specified, the test shall be performed at ambient.

b. Drain-to-source voltage.

c. Maximum drain current.

d. Range of gate-to-source voltage.

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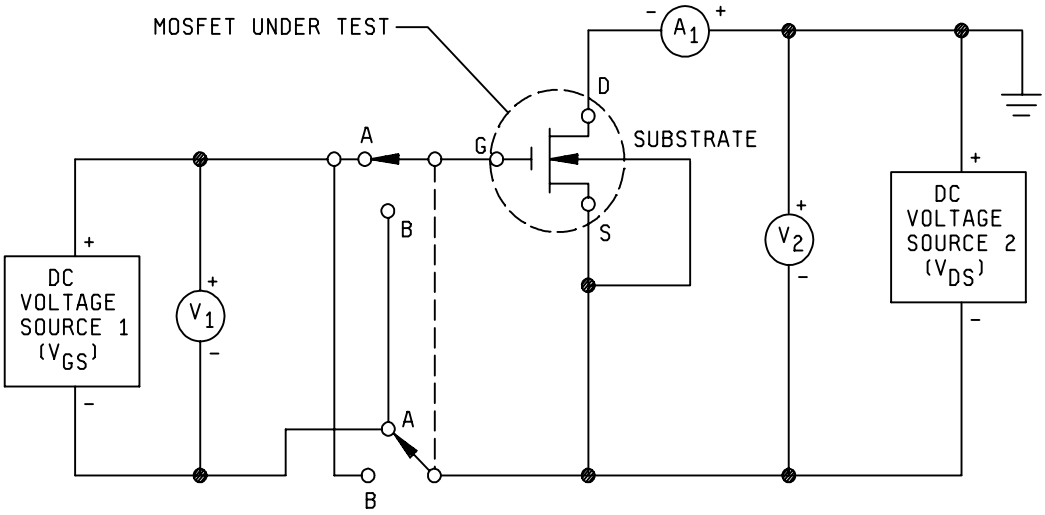

NOTE: Gate-to-source polarity switch set at:
A for enhancement mode.
B for depletion mode.

FIGURE 3404-1. Test circuit for n-channel MOSFETs.

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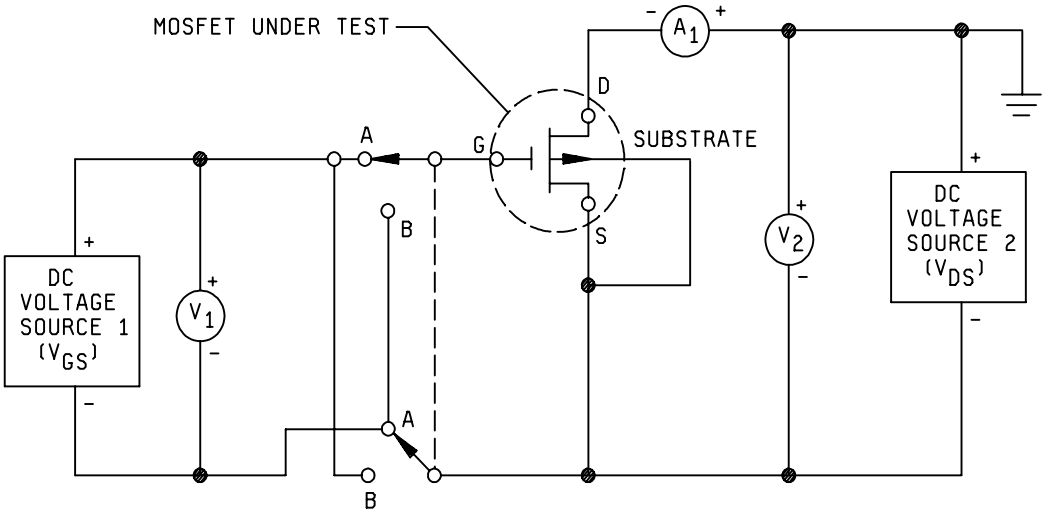

NOTE: Gate-to-source polarity switch set at:
A for enhancement mode.
B for depletion mode.

FIGURE 3404-2. Test circuit for p-channel MOSFETs.

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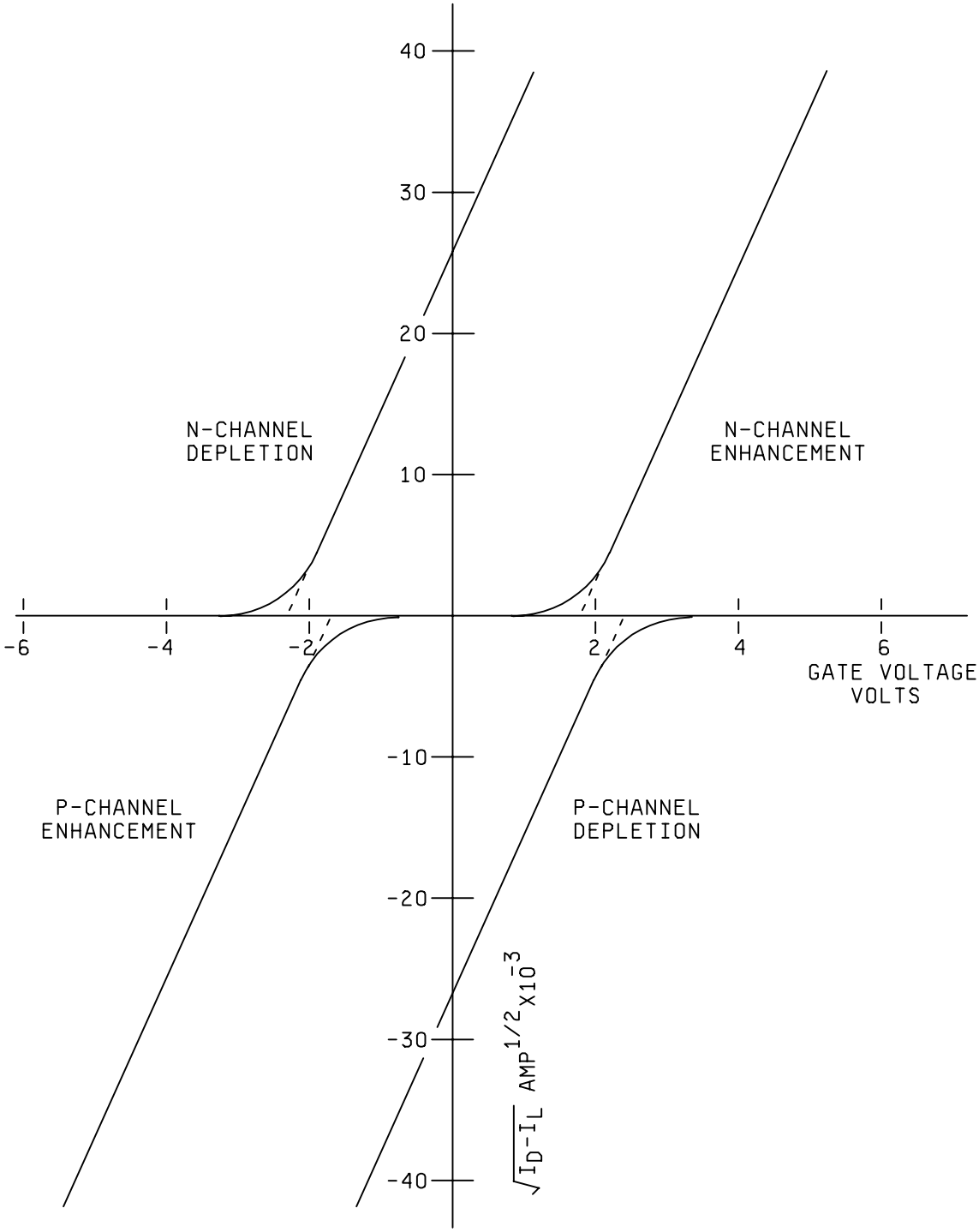

FIGURE 3404-3. Examples of curves.

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METHOD 3405.1

DRAIN-TO-SOURCE ON-STATE VOLTAGE

1. Purpose. The purpose of this test is to measure the drain-to-source voltage of the field-effect transistor or IGBT at the specified value of drain current. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3405-1.

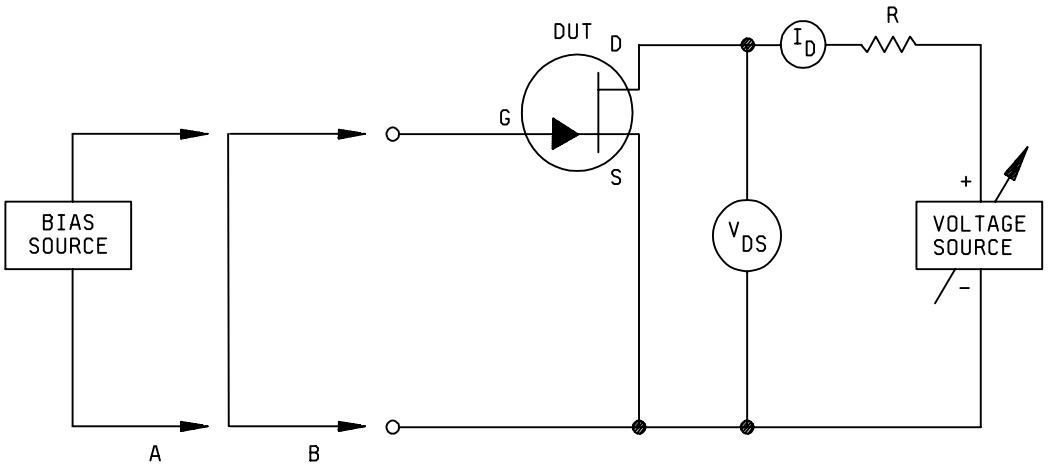

FIGURE 3405-1. Test circuit for drain-to-source on-state voltage.

3. Procedure. The specified bias condition shall be applied between the gate and source and the voltage source shall be adjusted to bring I_D to the specified value. The voltage V_{DS} may then be read.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test current (see 3.).

b. Gate-to-source bias condition:

A: Voltage-biased (specify bias voltage and polarity).

B: Short-circuited.

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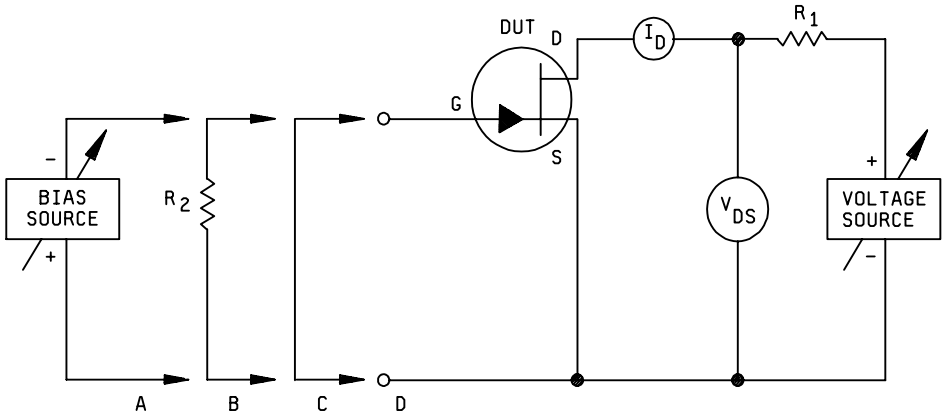
METHOD 3407.1

BREAKDOWN VOLTAGE, DRAIN-TO-SOURCE

1. Purpose. The purpose of this test is to determine if the breakdown voltage of the field-effect transistor or IGBT under the specified conditions is greater than the specified minimum limit. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3407-1.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 3407-1. Test circuit for breakdown voltage, drain-to-source.

3. Procedure. The resistor R_1 is a current-limiting resistor and should be of sufficiently high resistance to avoid excessive current flowing through the device and current meter. The voltage shall be gradually increased from zero, with the specified bias condition (condition A, B, C, or D) applied, until either the minimum limit for $V_{(BR)DSX}$ 1/ or the specified test current is reached.1/ The device is acceptable if the minimum limit for $V_{(BR)DSX}$ is reached before the test current reaches the specified value. If the specified test current is reached first, the device shall be considered a failure.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test current (see 3.).

b. Bias condition:

A: Gate-to-source: Reverse bias. (Specify bias voltage.)

B: Gate-to-source: Resistance return. (Specify resistance of R_2.)

C: Gate-to-source: Short-circuit.

D: Gate-to-source: Open-circuit.

1/ $V_{(BR)DSX}$: Breakdown voltage, drain-to-source, with the specified bias condition applied from gate-to-source.

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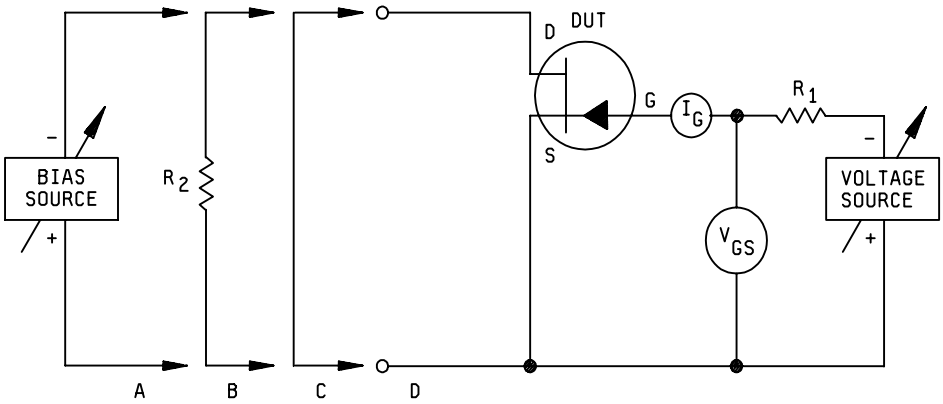
METHOD 3411.1

GATE REVERSE CURRENT

1. Purpose. The purpose of this test is to measure the gate reverse current of the field-effect transistor or IGBT under the specified conditions. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3411-1.



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the volt meter readings shall be corrected for the drop across the ammeter.

FIGURE 3411-1. Test circuit for gate reverse current.

3. Procedure. The specified dc voltage shall be applied between the gate and the source with the specified bias condition (condition A, B, C, or D) applied to the drain. The measurement of current shall be made at the specified ambient or case temperature.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test voltage (see 3.).

b. Test temperature if other than +25°C ±3°C ambient (see 3.).

c. Bias condition:

A: Drain-to-source: Reverse bias. (Specify bias voltage.)

B: Drain-to-source: Resistance return. (Specify resistance of R_2.)

C: Drain-to-source: Short-circuit.

D: Drain-to-source: Open-circuit.

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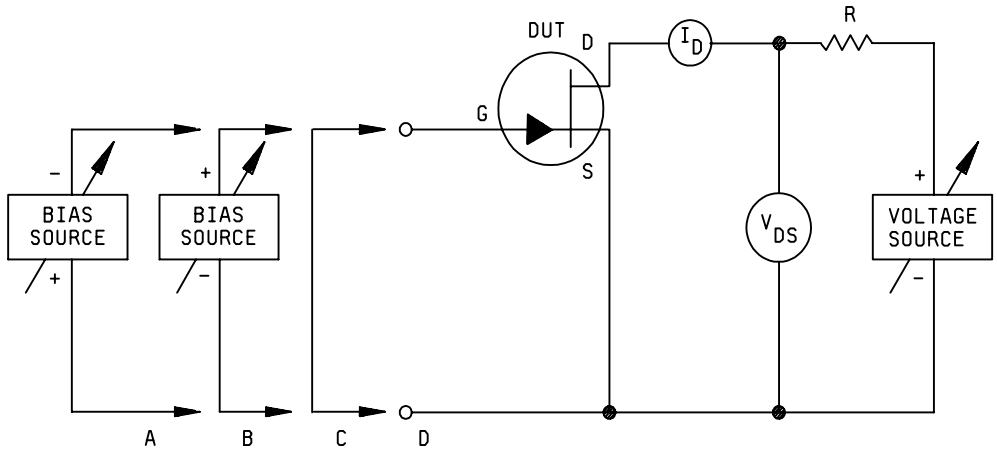
METHOD 3413.1

DRAIN CURRENT

1. Purpose. The purpose of this test is to measure the drain current of the field-effect transistor or IGBT under the specified conditions. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3413-1.



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the volt meter readings shall be corrected for the drop across the ammeter.

FIGURE 3413-1. Test circuit for drain current.

3. Procedure. The specified voltage shall be applied between the drain and source with the specified bias condition (condition A, B, C, or D) applied to the gate. The measurement of current shall be made at the specified ambient or case temperature.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test voltage (see 3.).

b. Test temperature if other than +25°C ±3°C ambient (see 3.).

c. Parameter to be measured.

d. Bias condition:

A: Gate-to-source: Reverse bias. (Specify bias voltage.)

B: Gate-to-source: Forward bias. (Specify bias voltage.)

C: Gate-to-source: Short-circuit.

D: Gate-to-source: Open-circuit.

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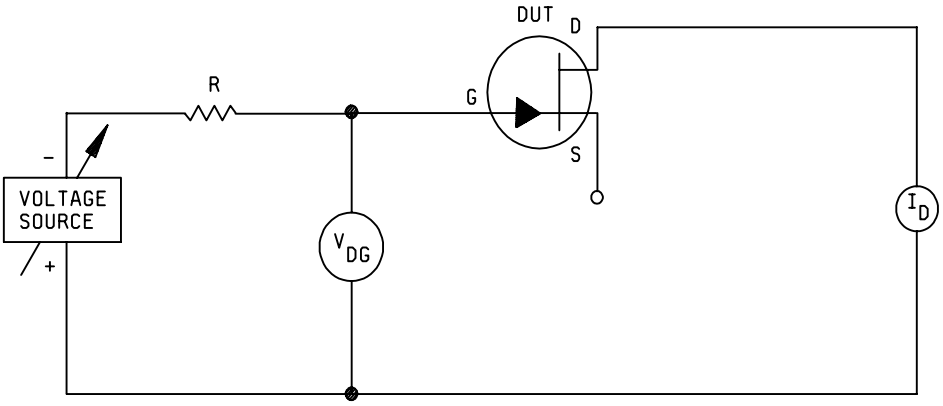
METHOD 3415.1

DRAIN REVERSE CURRENT

1. Purpose. The purpose of this test is to measure the drain reverse current of the field-effect transistor or IGBT under the specified conditions. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3415-1.



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the volt meter readings shall be corrected for the drop across the ammeter.

FIGURE 3415-1. Test circuit for drain reverse current.

3. Procedure. The specified dc voltage shall be applied between the drain and the gate. The measurement of current shall be made at the specified ambient or case temperature.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test voltage (see 3.).

b. Test temperature if other than +25°C ±3°C ambient (see 3.).

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METHOD 3421.1

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

1. Purpose. The purpose of this test is to measure the resistance between the drain and source of the field-effect transistor or IGBT under the specified static condition. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test circuit. See figure 3421-1.

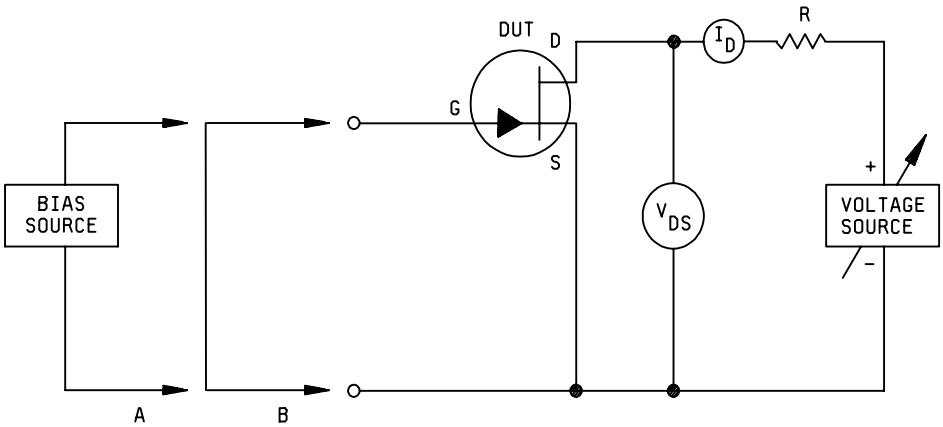

FIGURE 3421-1. Test circuit for static drain-to-source on-state resistance.

3. Procedure. The specified bias condition shall be applied between the gate and source and the voltage source shall be adjusted so that the specified current is achieved. The drain-to-source voltage shall then be measured.

$$Then: \; r_{DS(on)} = \frac{V_{DS}}{I_D}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test currents.

b. Gate-to-source bias condition:

A: Voltage-biased (specify bias voltage and polarity).

B: Short-circuited.

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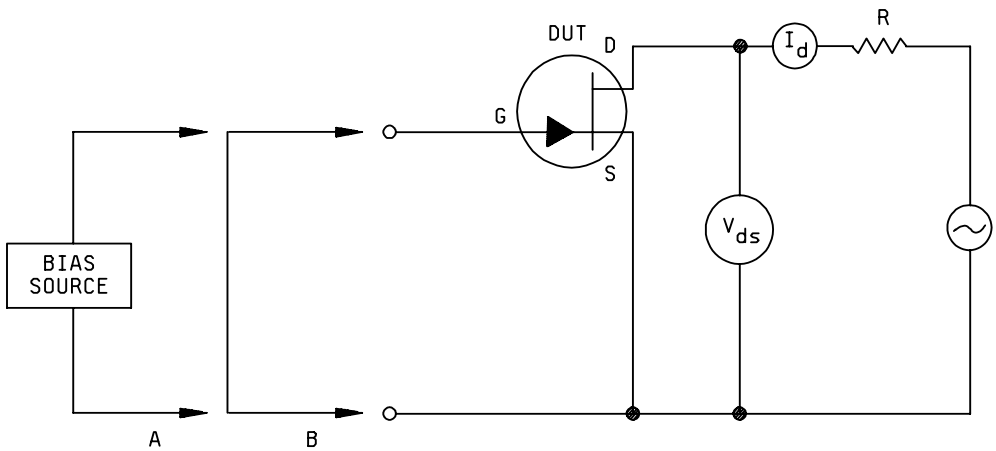
METHOD 3423

SMALL-SIGNAL, DRAIN-TO-SOURCE ON-STATE RESISTANCE

1. Purpose. The purpose of this test is to measure the resistance between the drain and source of the field-effect transistor under the specified small-signal conditions.

2. Test circuit. See figure 3423-1.



NOTE: The ac voltmeter shall have an input impedance high enough that halving it does not change the measured value within the required accuracy of the measurement.

FIGURE 3423-1. Test circuit for small-signal, drain-to-source on-state resistance.

3. Procedure. The specified bias condition shall be applied between the gate and the source and an ac sinusoidal signal current, I_d, of the specified rms value shall be applied.

$$Then: \; r_{ds(on)} = \frac{V_{ds}}{I_d}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test current (see 3.).

b. Test frequency.

c. Gate-to-source bias condition:

A: Voltage-biased (specify bias voltage and polarity).

B: Short-circuited.

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METHOD 3431

SMALL-SIGNAL, COMMON-SOURCE, SHORT-CIRCUIT, INPUT CAPACITANCE

1. Purpose. The purpose of this test is to measure the input capacitance of the field-effect transistor under the specified small-signal conditions.

2. Test circuit. The circuit and procedure shown on figure 3431-1 are for common-source configuration. For other configurations, the circuit and procedure should be changed accordingly.

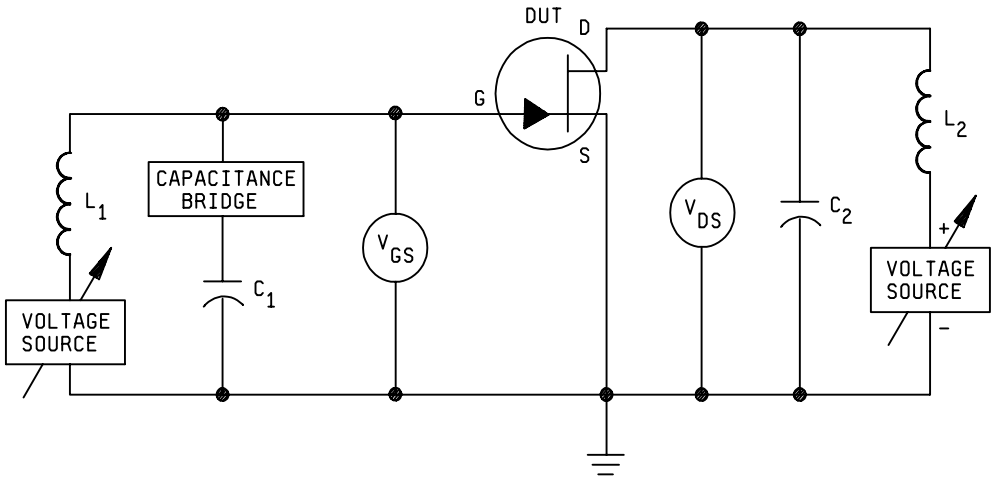

FIGURE 3431-1. Test circuit for small-signal, common-source, short-circuit, input capacitance.

3. Procedure. The capacitors C_1 and C_2 shall present short-circuits at the test frequency. L_1 and L_2 shall present a high ac impedance at the test frequency for isolation. The bridge shall have low dc resistance between its output terminals and should be capable of carrying the test current without affecting the desired accuracy of measurement.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test voltages and currents.

b. Measurement frequency.

c. Parameter to be measured.

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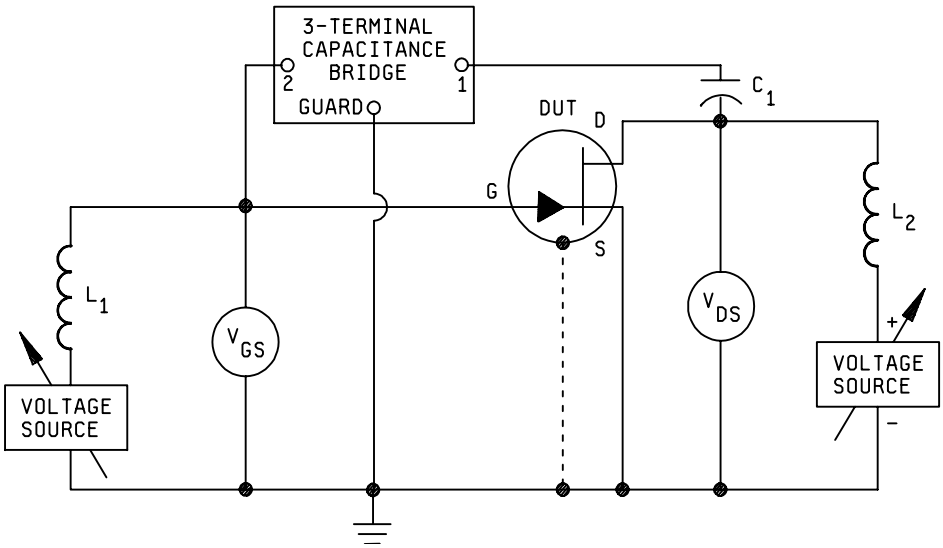
METHOD 3433

SMALL-SIGNAL, COMMON-SOURCE, SHORT-CIRCUIT, REVERSE TRANSFER CAPACITANCE

1. Purpose. The purpose of this test is to measure the reverse transfer capacitance of the field-effect transistor under the specified conditions.

2. Test circuit. The circuit and procedure shown on figure 3433-1 are for common-source configuration. For other configurations, the circuit and procedure should be changed accordingly. Terminal 2 of bridge shall be the terminal with an ac potential closest to the ac potential of the guard terminal so as to provide an effective short-circuit of the input.



NOTE: The dotted connection between the case and ground shall be used for devices in which the case is not internally electrically connected to any element. If the case is internally electrically connected to any element, the dotted connection shall not be used.

FIGURE 3433-1. Test circuit for small-signal, common-source, short-circuit, reverse transfer capacitance.

3. Procedure. The capacitor C_1 shall present a short-circuit at the test frequency. L_1 and L_2 shall present a high ac impedance at the test frequency for isolation. The bridge shall have low dc resistance between its output terminals and should be capable of carrying the test current without affecting the desired accuracy of measurement.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test voltages and currents.

b. Measurement frequency.

c. Parameter to be measured.

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METHOD 3453

SMALL-SIGNAL, COMMON-SOURCE, SHORT-CIRCUIT, OUTPUT ADMITTANCE

1. Purpose. The purpose of this test is to measure the output admittance of the field-effect transistor under the specified small-signal conditions.

2. Test circuit. The circuit and procedure are shown on figure 3453-1 for common-source configuration. For other configurations, the circuit and procedure should be changed accordingly.

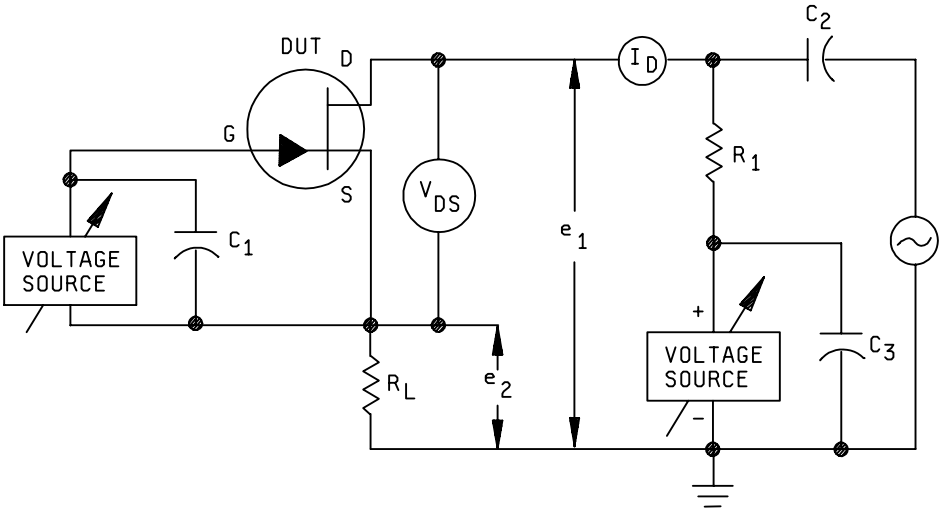

FIGURE 3453-1. Test circuit for small-signal, common-source, short-circuit, output admittance.

3. Procedure. The capacitors C_1, C_2, and C_3 shall present short-circuits at the test frequency in order to effectively couple and bypass the test signal. R_1 and R_L shall be short-circuits compared with the output impedance of the device. After setting the specified dc conditions, the V_{DS} meter shall be disconnected from the circuit while measuring e_1 and e_2. The voltages e_1 and e_2 shall be measured with high-impedance ac voltmeters.

$$\textit{Then:}\quad y_{os} = \frac{I_d}{e_1 - e_2} \qquad \textit{Where:}\quad I_d = \frac{e_2}{R_L} \qquad \textit{Thus:}\quad y_{os} = \frac{\frac{e_2}{R_L}}{e_1 - e_2}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test frequency.

b. Test voltages and currents.

c. Parameter to be measured.

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METHOD 3455

SMALL-SIGNAL, COMMON-SOURCE, SHORT-CIRCUIT, FORWARD TRANSADMITTANCE

1. Purpose. The purpose of the test is to measure the forward transadmittance of the field-effect transistor under the specified small-signal conditions.

2. Test circuit. The circuit and procedure shown on figure 3455-1 are for common-source configuration. For other configurations, the circuit and procedure should be changed accordingly.

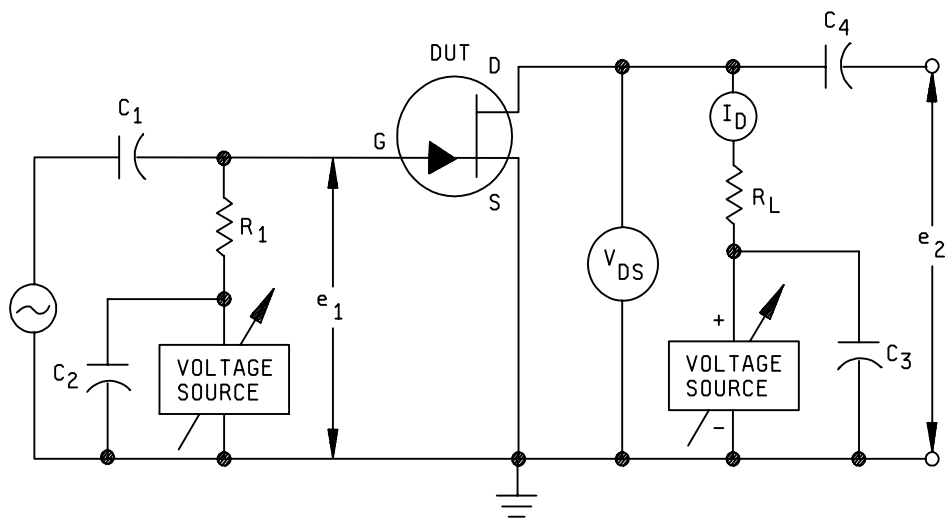

FIGURE 3455-1. Test circuit for small-signal, common-source, short-circuit, forward transadmittance.

3. Procedure. The capacitors C_1, C_2, C_3, and C_4 shall present short-circuits at the test frequency in order to effectively couple and bypass the test signal. R_1 shall be a short-circuit compared with the input impedance of the device. R_L shall be a short circuit compared with the output impedance of the device. The voltages e_1 and e_2 shall be measured with high-impedance ac voltmeters.

$$\text{Then: } y_{fs} = \frac{I_d}{e_1} \quad \text{Where: } I_d = \frac{e_2}{R_L} \quad \text{Thus: } y_{fs} = \frac{\frac{e_2}{R_L}}{e_1} = \frac{e_2}{e_1 \bullet R_L}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test frequency.

b. Test voltages and currents.

c. Parameter to be measured.

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METHOD 3457

SMALL-SIGNAL, COMMON-SOURCE, SHORT-CIRCUIT, REVERSE TRANSFER ADMITTANCE

1. Purpose. The purpose of the test is to measure the reverse transfer admittance under the specified small-signal conditions.

2. Test circuit. The circuit and procedure shown on figure 3457-1 are for common-source configuration. For other configurations, the circuit and procedure should be changed accordingly.

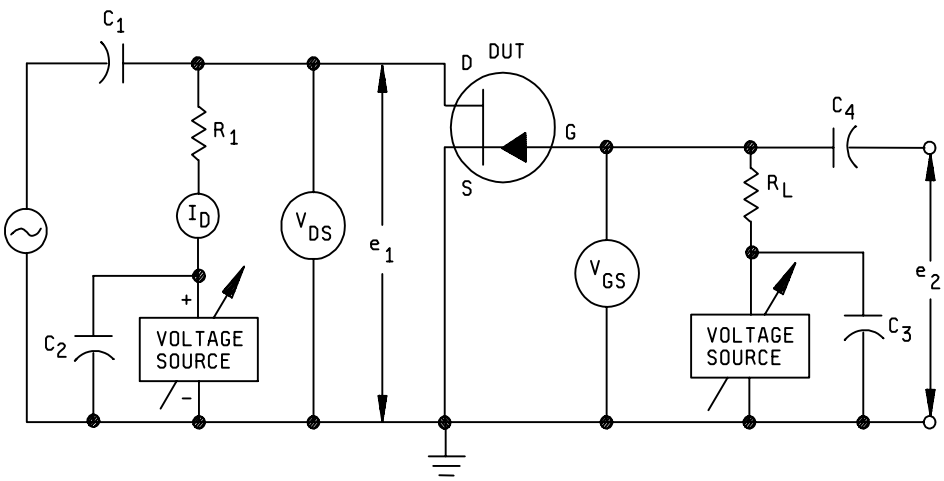

FIGURE 3457-1. Test circuit for small-signal, common-source, short-circuit, reverse transfer admittance.

3. Procedure. The capacitors C_1, C_2, C_3, and C_4 shall present short-circuits at the test frequency in order to effectively couple and bypass the test signal. R_1 shall be impedance matched to the generator. R_L shall be a short-circuit compared with the input impedance of the device. The rms voltages e_1 and e_2 shall be measured with high-impedance ac voltmeters.

V_{DS} shall be adjusted to the specified value, then the gate voltage supply shall be adjusted so that V_{GS} or I_D equals the specified value, and the voltages e_1 and e_2 shall be measured.

$$\text{Then:}\quad y_{rs} = \frac{I_g}{e_1} \qquad \text{Where:}\quad I_g = \frac{e_2}{R_L}$$

$$\text{Thus:}\quad y_{rs} = \frac{\frac{e_2}{R_L}}{e_1} \quad \text{or} \quad y_{rs} = \frac{e_2}{e_1\ R_L}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test frequency.

b. Test voltages and currents.

c. Parameter to be measured.

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METHOD 3459

PULSE RESPONSE FIELD-EFFECT TRANSISTOR (FET)

1. Purpose. The purpose of this test is to measure the pulse response ($t_{d(on)}$, t_r, $t_{d(off)}$, and t_f) of the field-effect transistor under the specified conditions.

2. Test circuit. The test circuit shall be as shown in the applicable specification sheet.

3. Procedure. The FET shall be tested in the specified circuit. $V_{in(on)}$, $V_{in(off)}$, pulse generator impedance, all circuit components, and supply voltages shall be as specified in figure 3459-1.

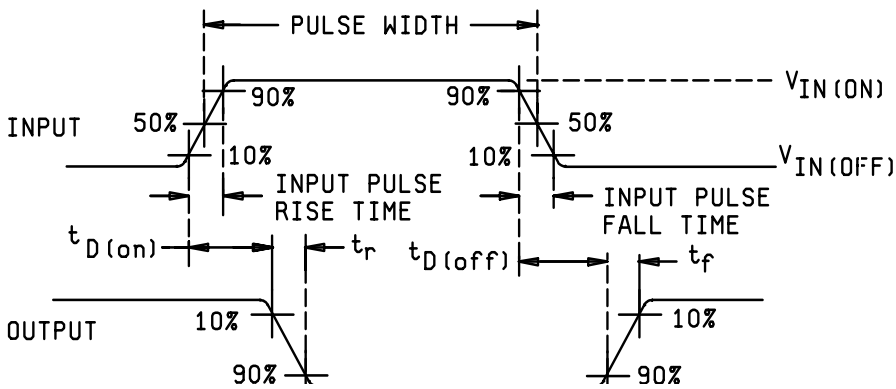

FIGURE 3459-1. Pulse characteristics.

Pulse characteristics are defined on figure 3459-1. The rise time, fall time, duty cycle or pulse repetition rate, and pulse width of the input waveform, together with the input resistance, capacitance, and response time of the response detector shall all be such that halving or doubling these parameters will not affect the results of the measurement greater than the precision of measurement.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Input pulse levels $V_{in(on)}$ and $V_{in(off)}$.

b. Output impedance of pulse generator.

c. Circuit with all components.

d. All supply voltages.

e. Parameters to be measured.

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METHOD 3461

SMALL-SIGNAL, COMMON-SOURCE, SHORT-CIRCUIT, INPUT ADMITTANCE

1. Purpose. The purpose of this test is to measure the input admittance of the field-effect transistor under the specified small-signal conditions.

2. Test circuit. The circuit and procedure shown on figure 3461-1 are for common-source configuration. For other configurations, the circuit and procedure should be changed accordingly.

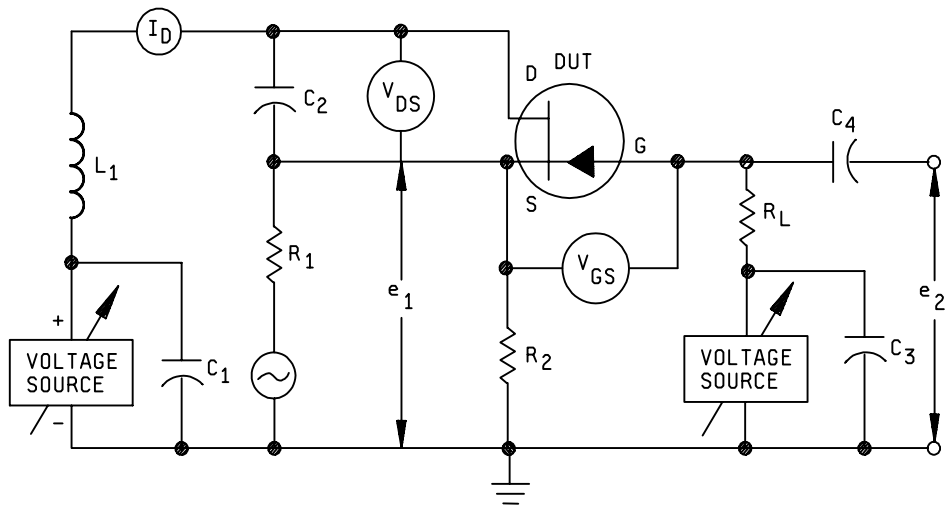

FIGURE 3461-1. Test circuit for small-signal, common-source, short-circuit, input admittance.

3. Procedure. The capacitors C_1, C_2, C_3, and C_4 shall present short-circuits at the test frequency in order to effectively couple and bypass the test signal. R_1 facilitates the adjustment of e_1. Its use is optional. R_2 shall be such that dc biasing is possible. R_L shall be a short-circuit compared with the input impedance of the device. V_{DS} shall be adjusted to the specified value, then the gate voltage supply shall be adjusted so that V_{GS} or I_D equals the specified value, and the voltages e_1 and e_2 shall be measured.

$$\textit{Then:}\quad y_{is} = \frac{I_g}{e_1 - e_2} \qquad \textit{Where:}\quad I_g = \frac{e_2}{R_L}$$

$$\textit{Thus:}\quad y_{is} = \frac{\frac{e_2}{R_L}}{e_1 - e_2} \quad \textit{or} \quad y_{is} = \frac{e_2}{R_L\,(e_1 - e_2)}$$

$$e_1 \textit{ must be greater than } e_2\textit{; therefore, } y_{is} = \frac{e_2}{R_L\ e_1}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test frequency.

b. Test voltages and currents.

c. Parameter to be measured.

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METHOD 3469

REPETITIVE UNCLAMPED INDUCTIVE SWITCHING

1. Purpose. This purpose of this test method is to determine the repetitive inductive avalanche switching capability of power devices.

2. Scope. This method is intended as an endurance test for any power switching device designed and specified with repetitive avalanche capability.

3. Circuitry. The circuit shall be designed so that all stray reactances are held to a minimum. The inductor L shall be of a fast response type.

4. Symbols and definitions. The following symbols and terminology apply to this test method:

a. E_{AR}: Repetitive avalanche energy, minimum.

b. E_{on}: On-state energy.

c. f: Frequency.

d. I_{AR}: Repetitive avalanche current, maximum.

e. L: Load inductance in accordance with DUT.

f. P_D: Power dissipation of device.

g. $R_{\theta JC}$: Thermal resistance from junction-to -case.

h. R_S: Stray circuit resistance.

i. t_{av}: Time in avalanche.

j. T_C: Case temperature.

k. T_J: Junction temperature.

l. $T_{J(max)}$: The maximum specified junction temperature.

m. $V_{(BR)}$: Breakdown or avalanche voltage of device.

n. V_{DD}: Power supply voltage.

5. Procedure.

5.1 Screening. The DUT must be screened prior to avalanche and meet all specified parameters.

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5.2 Calculations. The energy delivered to the DUT can be calculated as follows:

a. $$E_{AR} = \frac{\dfrac{L * I_{AR^2} * V_{(BR)}}{\left[V_{(BR)} - V_{DD}\right]}}{2}$$

$$NOTE: \quad R_S = 0, \text{ where, } V_{(BR)} = \frac{LI_{AR^2}}{t_{AV}}$$

b. $$E_{AR} = V_{(BR)} \; I_{AR} \left(\frac{L}{R_S}\right) ln \left[\frac{I_{AR} \; R_S}{(V_{BR} - V_{DD}) + 1}\right]$$

NOTE: $R_S \neq 0$

5.2.1 Energy delivered. The actual energy delivered to the DUT can vary depending on the real value of R_S. Since this is test circuit dependent, the actual energy delivered must be verified by observing the voltage across the DUT and current through the DUT waveforms. Empirically record the $V_{(BR)}$, I_{AR}, and t_{av}. Then calculate:

$E_{AR} = 1/2 \; V_{(BR)} I_{AR} \; t_{av}$.

If this empirically derived value is not greater than or equal to the specified minimum E_{AR} value, the circuit must be compensated until it is.

5.3 Junction temperature. T_J during the test must be held constant to T_J (max) +0°C -10°C, based on the case temperature of the DUT and the $R_{\theta JC}$ or the junction temperature as determined using a TSP. The power dissipated in the DUT is equal to the sum of the on-energy and the avalanche-energy multiplied by the frequency. The E_{on} in most cases can be neglected.

So: $P_D = f * (E_{AR} + E_{on})$

$T_J = P_D * R_{\theta JC} + T_C$

The case temperature of the DUT will be measured at a specified reference point under the heat source. It is also possible to measure the temperature of the heat sink at a specified reference point provided that an accurate value of the thermal resistance case-to-heat-sink-reference-point is known. The measured junction temperature based on measurements of a TSP may also be substituted for the junction temperature calculated from case temperature.

5.4 Number of pulses. The DUT will be avalanched for a specified minimum number of pulses at specified conditions. Upon completion the specified device parameters will be tested.

6. Summary. Unless otherwise specified in the applicable specification sheet, the following parameters shall be as follows:

a. E_{AR}: (Repetitive avalanche energy (joules)).

b. I_{AR}: (Repetitive avalanche current (amperes)).

c. T_J: +150°C +0°C, -10°C.

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d. t_{av}: 2 μs minimum, 2 μs maximum.

e. f: 500 Hz, minimum.

f. N: 3.6×10^8 minimum number of pulses.

$$L = \left[\frac{2\ E_{AR}}{(I_{DI})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]\ nH\ minimum$$

Supply voltage ±50 V.

7. Failure criteria. The DUT shall be within all specified parameter limits at the completion of the test. As a minimum, V_{BR} shall be greater than or equal to rated breakdown voltage and applicable leakage currents.

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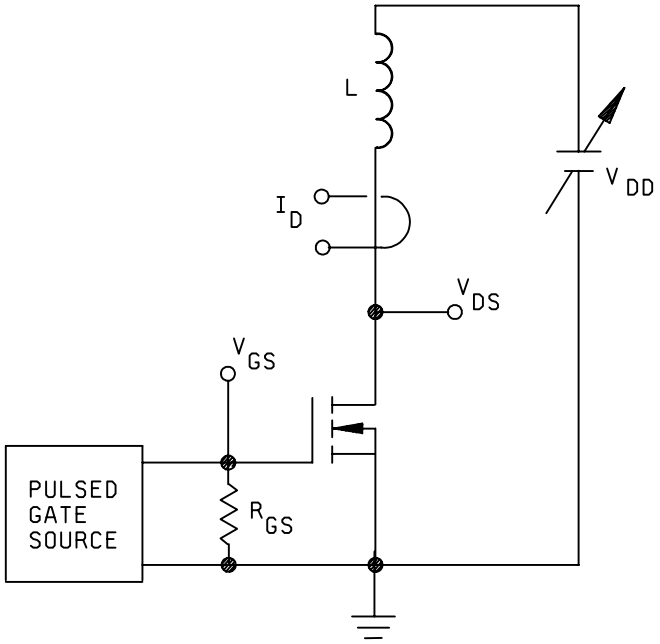
METHOD 3470.2

SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING

1. Purpose. The purpose of this method is applicable to power MOSFETs and IGBT. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E. The purpose of this test method is to screen out weak devices which otherwise may result in costly equipment failures. This is accomplished by providing a controlled means of testing the capability of a power MOSFET or IGBT to withstand avalanche breakdown while turning off with an unclamped inductive load under specified conditions. The device capability is a strong function of the peak drain current at turn-off and the circuit inductance. Since no voltage clamping circuits or devices are employed, essentially, all of the energy stored in the inductor must be dissipated in the DUT at turn-off. It is not the intent of this test method to closely duplicate actual application conditions where device temperatures may approach maximum rated value, repetition rates may be 10 to 100 kHz, and voltage transients are usually only a few microseconds in duration. However, experience has shown that failures in actual applications can be greatly reduced or eliminated if devices are tested for avalanche operation under defined circuit conditions at very low repetition rates and at room ambient temperature.

2. Test procedures. The specified value of inductance L shall be connected into the circuit (see figures 3470-1 and 3470-2). The gate pulse shall be applied to the device at the specified repetition rate. The V_{DD} supply voltage shall be applied. The gate pulse width shall be adjusted as necessary until the specified drain current I_D is reached. Test failures are defined as those devices which fail catastrophically.



NOTE: The test circuit, shown for n-channel devices, is also applicable for p-channel devices with appropriate changes in polarities and symbols.

FIGURE 3470-1. Unclamped inductive switching circuit.

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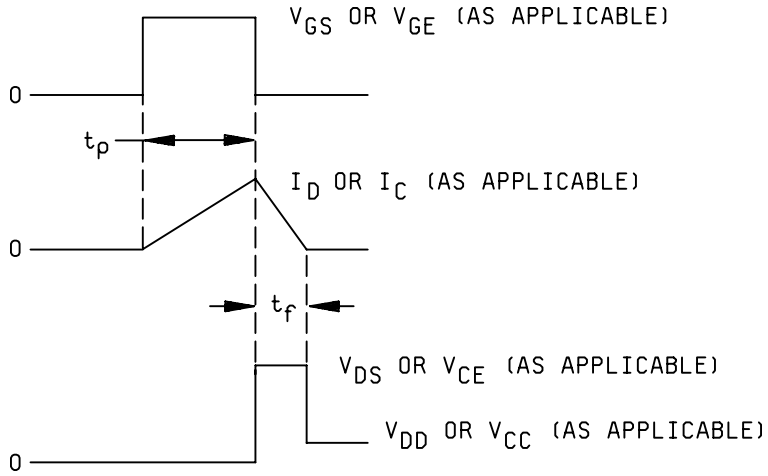

NOTES: The following notes are provided in the interest of achieving comparable results from various test circuits employed to perform this test.

a. Air core inductors are recommended for this test to avoid the possibility of core problems. If iron core inductors are used, care must be taken such that core saturation is not changing the effective value to the inductance L which will lead to non-repeatable test results.
b. The resistance of the inductor must be controlled since I^2R losses in the inductor will decrease the percentage of $LI^2/2$ stored energy transferred to the DUT. The relationship $R = 0.015\ (V_{DS}/I_D)$ applies for one percent of the stored energy being dissipated in the resistance. For two percent loss, $R = 2\ (.015)\ (V_{DS}/I_D)$ or (V_{CE}/I_C). The resistance loss shall be limited to two percent maximum, if not compensated by the equipment.
c. The gate-to-source resistor shall be closely connected to the test device. The gate-to-source resistor shall be a low enough value that the switching performance of the device does not affect the test and the inductor in the drain circuit determines the current waveform. The design of the pulsed gate source must be such that R_{GS} or R_{GE} is the effective gate-to-source resistance during the t_f portion of the test.
d. The repetition rate and duty cycle of the test shall be chosen so that device average junction temperature rise is minimal. Limits of one pulse per second or 0.5 percent duty cycle are recommended. The device peak junction temperature shall not exceed maximum rated value.
e. If the V_{DD} or V_{CE} power supply remains in series with the inductor during the t_f interval, then the energy transferred to the DUT may be considerably higher than $LI^2/2$. If the gate pulse width is adjusted so that V_{CC} or $V_{DD} < 0.1\ V_{DS}$ or V_{CE} then the contribution of the power supply will be less than 10 percent of the stored $LI^2/2$ energy.

FIGURE 3470-2. Unclamped inductive switching power pulse.

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3. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Minimum peak current (I_D).

   b. Peak gate voltage (V_{GS}).

   c. Unless otherwise specified, gate to source resistor (R_{GS}) = 25 Ω to 50 Ω.

   d. Initial case temperature (T_C).

   e. Inductance (L).

   f. V_{DD}.

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METHOD 3471.2

GATE CHARGE

1. Purpose. The purpose of this test is to measure the gate charge (Q_g) of power MOSFETs and IGBT. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

1.1 Definitions.

a. Test 1: $Q_{g(th)}$ is the gate charge that shall be supplied to reach the minimum specified gate-source threshold voltage. It establishes line loci through the origin of a Q = f(V_{gs}) graph that is invariant with I_D, V_{DD}, and T_J. It establishes a relationship with capacitance, i.e.,

$$C_{GS} = \frac{Q_{g(th)}}{V_{g(th)}} = \frac{Q_{gs}}{V_{GP}}$$

b. Test 2: $Q_{g(on)}$ is the gate charge that shall be supplied to reach the gate-source voltage specified for the device $r_{DS(on)}$ measurement.

c. Test 3: $Q_{gm(on)}$ is the gate charge that shall be supplied to the device to reach the maximum rated gate-source voltage. $Q_{gm(on)}$ and $Q_{g(on)}$ establish line loci on a Q = f(V_{gs}) graph that may be considered invariant with I_D and T_J. The slope of the loci is invariant with V_{DD}, while the intercept with the Q axis is variant with V_{DD}.

d. Test 4: V_{GP} is the gate voltage necessary to support a specified drain current. V_{GP}, and, I_D is a point on the device gate voltage, drain current transfer characteristic. V_{GP} is variant with I_D and T_J. It may be measured one of two ways:

(1) Using a dc parameter test set employing a circuit similar to that described in method 3474 for SOA setting $V_{DD} > V_{GS}$.

(2) Using a gate charge test circuit employing a constant I_D drain load.

e. Test 5: Q_{gs} is the charge required by C_{GS} to reach a specified I_D. It is variant with I_D and T_J. It is measured in a gate charge test circuit employing a constant drain current load.

f. Test 6: Q_{gd} is the charge supplied to the drain from the gate to change the drain voltage under constant drain current conditions. It is variant with V_{DD} and may be considered invariant with I_D and T_J. It can be related to an effective gate-drain capacitance (i.e., $C_{rss} = Q_{gd}/V_{DD}$). The effective input capacitance is: $C_{iss} = C_{GS} + C_{rss}$.

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2. Test procedure.

a. The gate charge test is performed by driving the device gate with a constant current and measuring the resulting gate source voltage response. Constant gate current scales the gate-source voltage, a function of time, to a function of coulombs. The value of gate current is chosen so that the device on-state is of the order of 100 μs.

The resulting gate-source voltage waveform is nonlinear and is representative of device behavior in the low to mid-frequency ranges. The slope of the generated response reflects the active device capacitance ($C_g = dQ_g / dV_{GS}$) as it varies during the switching transition. The input characteristic obtained from this test reflects the chip design while avoiding high frequency effects.

b. Figure 3471-1 is the test circuit schematic for testing an n-channel device. Polarities are simply reversed for a p-channel device.

c. Figure 3471-2 is an example of a practical embodiment of figure 3471-1. It illustrates a gate drive and instrument circuit that will test n-channel and p-channel devices.

d. The circuit has I_g programmability ranging from microamperes to milliamperes. For very large power MOSFET devices, the output I_g can be extended to tens of milliamperes by paralleling additional CA3280 devices.

e. The circuit provides an independent gate voltage clamp control to prevent voltage excursions from exceeding test device gate voltage ratings.

f. The CA3240E follower ensures that the smallest power devices will not be loaded by the oscilloscope. (R_{in} = 1.5 T Ω, I_{IN} = 10 pA, C_{IN} = 4 pF).

g. Gate charge is to be measured starting at zero gate voltage to a specified gate voltage value.

h. The magnitude of input step constant gate current I_g should be such that gate propagation and inductive effects are not evident. Typically this means the device on-state should be of the order of 100 μs.

i. The dynamic response, source impedance, and duty factor of the pulsed gate current generator are to be such that they do not materially affect the measurement.

j. Typically, the instrument used for a gate charge measurement is an oscilloscope with an input amplifier and probe. The switching response and probe impedance are to be such that they do not materially affect the measurement. Too low a probe resistance relative to the magnitude of I_g can significantly increase the apparent Q_g for a given V_{GS}. Too high a value of probe capacitance relative to the device C_{iss} will also increase the apparent Q_g for a given V_{GS}.

$$I_g = \frac{C_g \; dV_{GS}}{dt}, \; Q_g = C_g \; V_{GS}.$$

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3. Summary. Figure 3471-3 illustrates the waveform and tests 1 through 4, condition A. Figure 3471-4 illustrates the waveform for tests 2, 4, 5, and 6, condition B. Only four of the six tests need be performed since the results of the remaining two are uniquely determined and may be calculated. Either condition A or condition B may be used.

3.1 Condition A.

3.1.1 Test 1, $Q_{g(th)}$.

a. Case temperature (T_C): +25°C.

b. Drain current: $I_D \geq 100$ mA.

c. Off-state drain voltage (V_{DD}): Between 50 percent and 80 percent of the device's rated drain-source breakdown voltage.

d. Load resistor (R_L): Equal to V_{DD}/I_D.

e. Gate current (I_g): Constant gate current such that the transition from off-state to on-state or on-state to off-state is of the order of 50 μs. The value of I_g varies with die size and ranges from 0.1 mA to 5 mA.

f. Gate-to-source voltage ($V_{g(th)\ min}$): The minimum rated gate-source threshold voltage.

g. Minimum off-state gate charge ($Q_{g(th)}$): A minimum and maximum limit shall be specified.

3.1.2 Test 2, $Q_{g(on)}$.

a. T_C, I_D, V_{DD}, R_L, I_g: Same as test 1 in 3.1.1.

b. V_{GS}: The gate-source voltage specified for the $r_{DS(on)}$ test, $V_{(on)}$.

c. On-state gate charge ($Q_{g(on)}$): A minimum and maximum limit shall be specified.

3.1.3 Test 3, $Q_{gm(on)}$.

a. T_C, I_D, V_{DD}, R_L, I_g: Same as test 1 in 3.1.1.

b. V_{GS}: The maximum rated gate-source voltage, $V_{(max)}$.

c. Maximum on-state gate charge ($Q_{gm(on)}$): A minimum and maximum limit shall be specified.

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3.1.4 Test 4, V_{GP}. This test is to be performed on a dc parameter test set.

a. I_D: The continuous rated drain current at T_C = +25°C.

b. $V_{DS} > V_{GS}$: Normally $V_{DD} \approx 3\ V_{GS}$ is satisfactory.

c. The pulse width and duty factor are such that they do not materially affect the measurement.

d. V_{GP} shall be specified as a maximum and minimum.

e. T_C: +25°C.

3.1.5 Test 5, Q_{gs}; test 6, Q_{gd}. No tests are required. The calculations in terms of the results of tests 1 through 4 are as follows:

a. $$Q_{gs} = Q_{g(th)} \left[\frac{V_{GP}}{V_{g(th)\min}} \right]$$

b. Determine the fully on-state charge slope:

$$m = \left[\frac{V_{(\max)} - V_{(on)}}{Q_{gm(on)} - Q_{g(on)}} \right]$$

c. Determine the V_{gs} axis intercept:

$$b = V_{(on)} - m\ Q_{g(on)}.$$

d. $$Calculate\, Q_{gd}:\ Q_{gd} = \left[\frac{(V_{GP} - b)}{m} \right] - Q_{gs}$$

3.2 Condition B.

3.2.1 Test 2, $Q_{g(on)}$.

a. Case temperature (T_C): +25°C.

b. On-state drain current (I_D): The continuous rated drain current at T_C = +25°C.

c. Off-state drain voltage (V_{DD}): Between 50 percent and 80 percent of the device's rated drain-source breakdown voltage.

d. The drain load shall be such that the drain current will remain essentially constant.

e. Gate current (I_g): Same as in 3.1.1 test 1 .

f. Gate-to-source voltage $V_{(on)}$: Same as in 3.1.1 test 1 .

g. On-state gate charge ($Q_{g(on)}$): A minimum and maximum limit shall be specified.

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3.2.2 Test 4, V_{GP}.

a. T_C, I_D, V_{DD}, Load, I_g: Same as in 3.2.1, test 2 .

b. V_{GP}: This is the gate plateau voltage where Q_{gs} and Q_{gd} are measured. This voltage is essentially constant during the drain voltage transition when Q_{gd} is supplied from the gate to the drain under constant I_g, and, I_D conditions.

3.2.3 Test 5, Q_{gs}.

a. T_C, I_D, V_{DD}, Load, I_g: Same as in 3.2.1, test 2 .

b. V_{GS}: Equal to V_{GP} at the specified I_D.

c. Q_{gs}: A minimum and maximum limit shall be specified.

3.2.4 Test 6, Q_{gd}.

a. T_C, I_D, V_{DD}, Load, I_g: Same as in 3.2.1, test 2 .

b. V_{GS}: Equal to V_{GP} at the specified I_D.

c. Q_{gs}: A minimum and maximum limit shall be specified.

3.2.5 Test 1, $Q_{g(th)}$; test 3, $Q_{gm(on)}$. No tests are required. The calculations in terms of the results of test 2, 4, 5, and 6 are as follows:

a. $$Q_{g(th)} = Q_{gs}\left[\frac{V_{g(th)}\min}{V_{GP}}\right]$$

b. Determine the fully on-state charge slope:

$$m = \left[\frac{V_{(on)} - V_{GP}}{Q_{g(on)} - Q_{gs} - Q_{gd}}\right]$$

c. Determine the V_{gs} axis intercept:

$$b = V_{(on)} - m\,Q_{g(on)}$$

d. Calculate $Q_{gm(on)}$:

$$Q_{gm(on)} = \frac{[V_{(\max)} - b]}{m}$$

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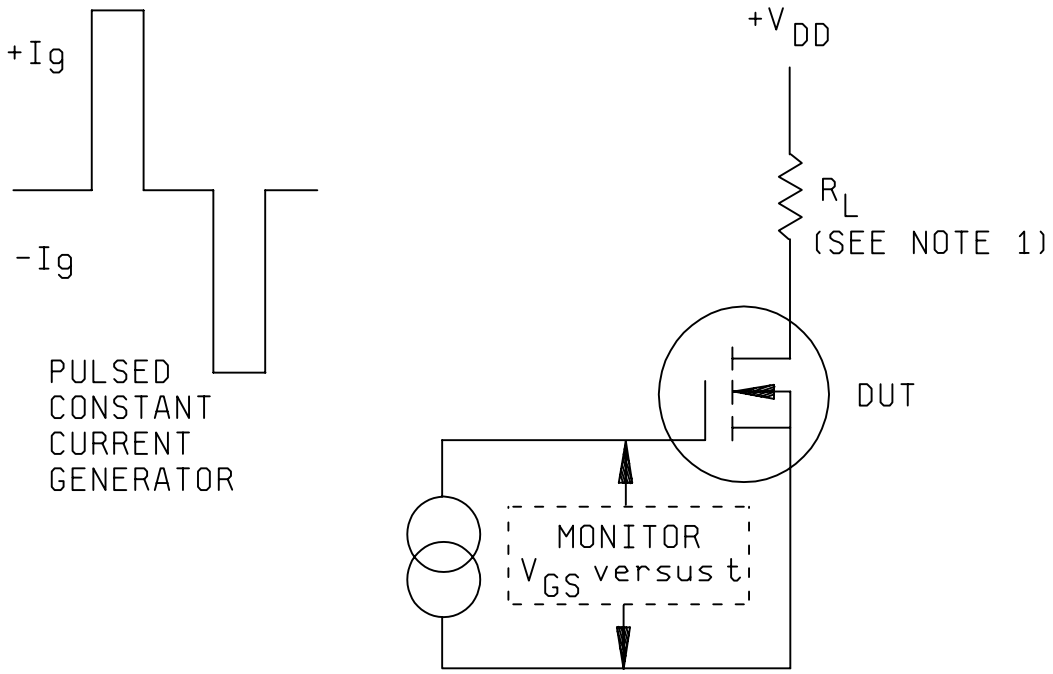

NOTES:
1. Condition B requires a constant drain current regulator.
2. $I_g \times t = Q_g$.

FIGURE 3471-1. Pulsed constant current generator.

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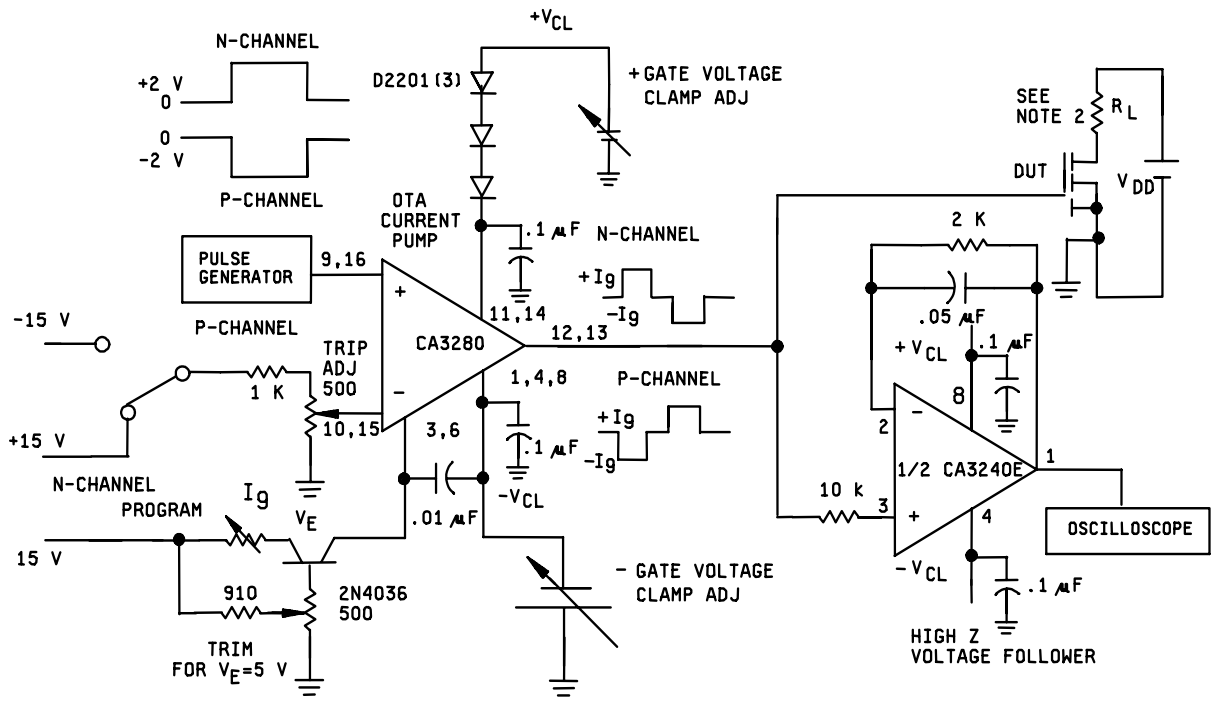

NOTES:

1. This test method provides gate voltage as a monotonic function of gate charge. Charge or capacitance may be unambiguously specified at any gate voltage. Gate voltage assuring that the device is well into the on-state will result in very reproducible measurements. For a given device, the gate charges at these voltages are independent of drain current and a weak function of the off-state voltage.
2. Condition B requires a constant current drain regulator.

FIGURE 3471-2. Practical gate charge test circuit.

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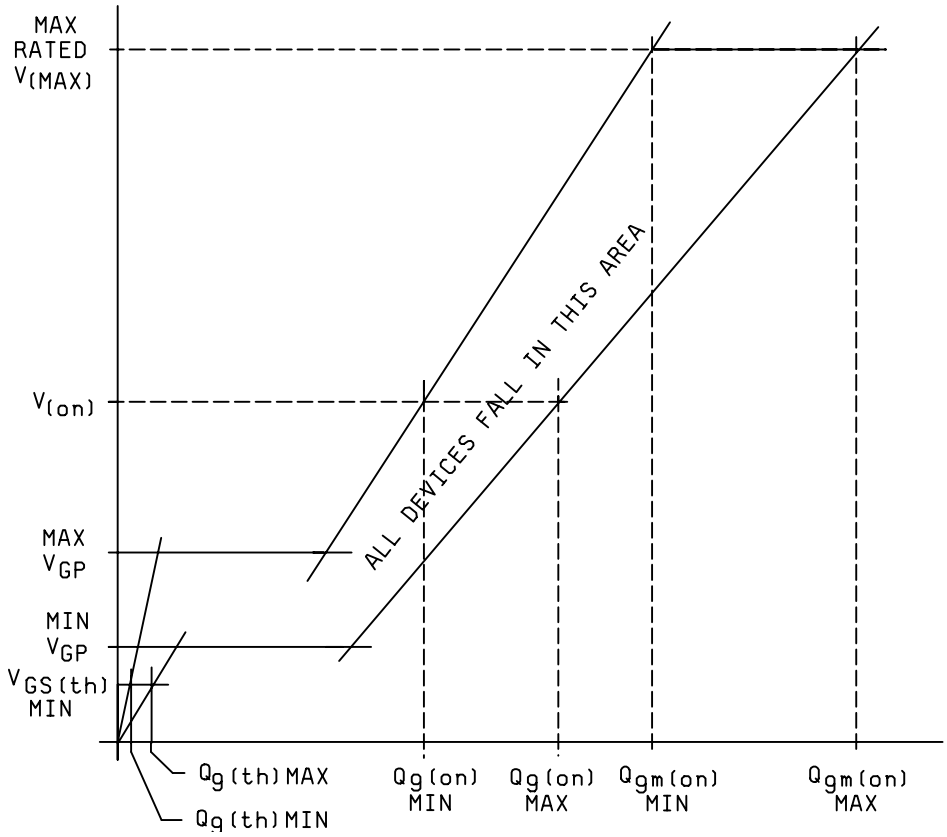

NOTES:

1. $Q_g = I_g t$.
2. V_{GP} is measured by a dc test, same I_D, $V_{DS} >> V_{GP}$ (see 3.1.4).
3. $V_{(max)}$ and $V_{(on)}$ are specified voltages for charge measurements $Q_{gm(on)}$ and $Q_{g(on)}$.
4. $V_{GS(th)}$ min is a specified voltage for measuring $Q_{g(th)}$.

FIGURE 3471-3. Gate charge characterization showing measured characteristics.

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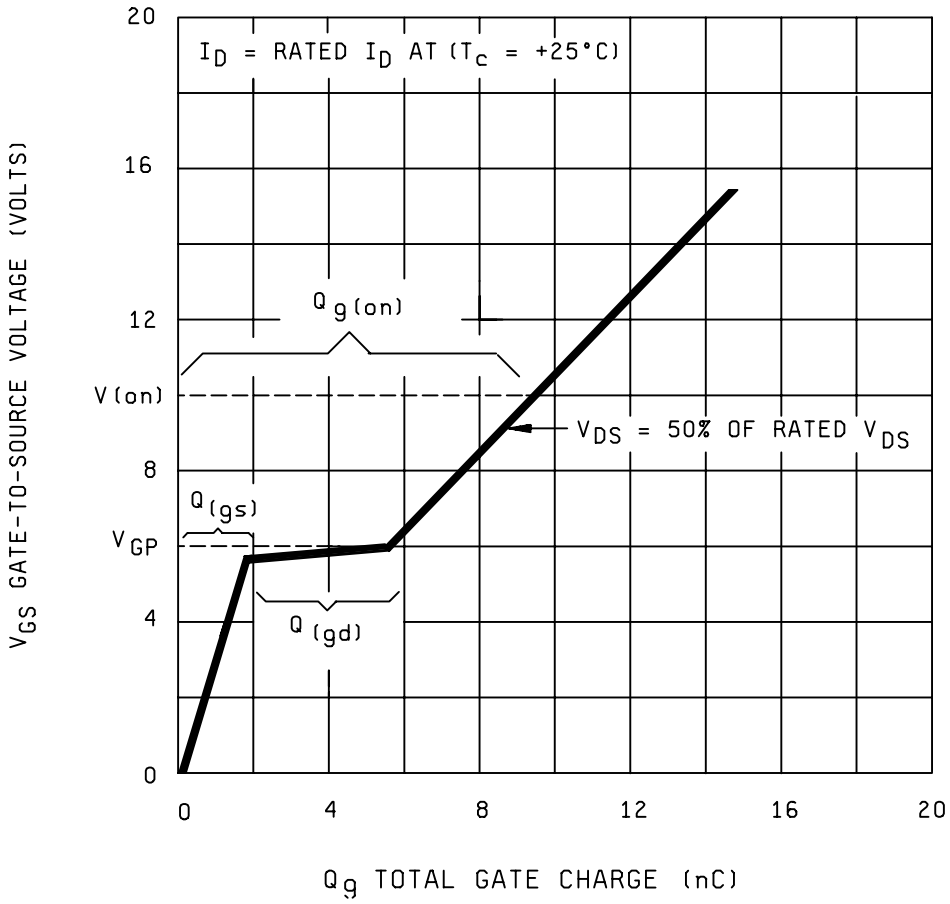

FIGURE 3471-4. Gate charge, condition B.

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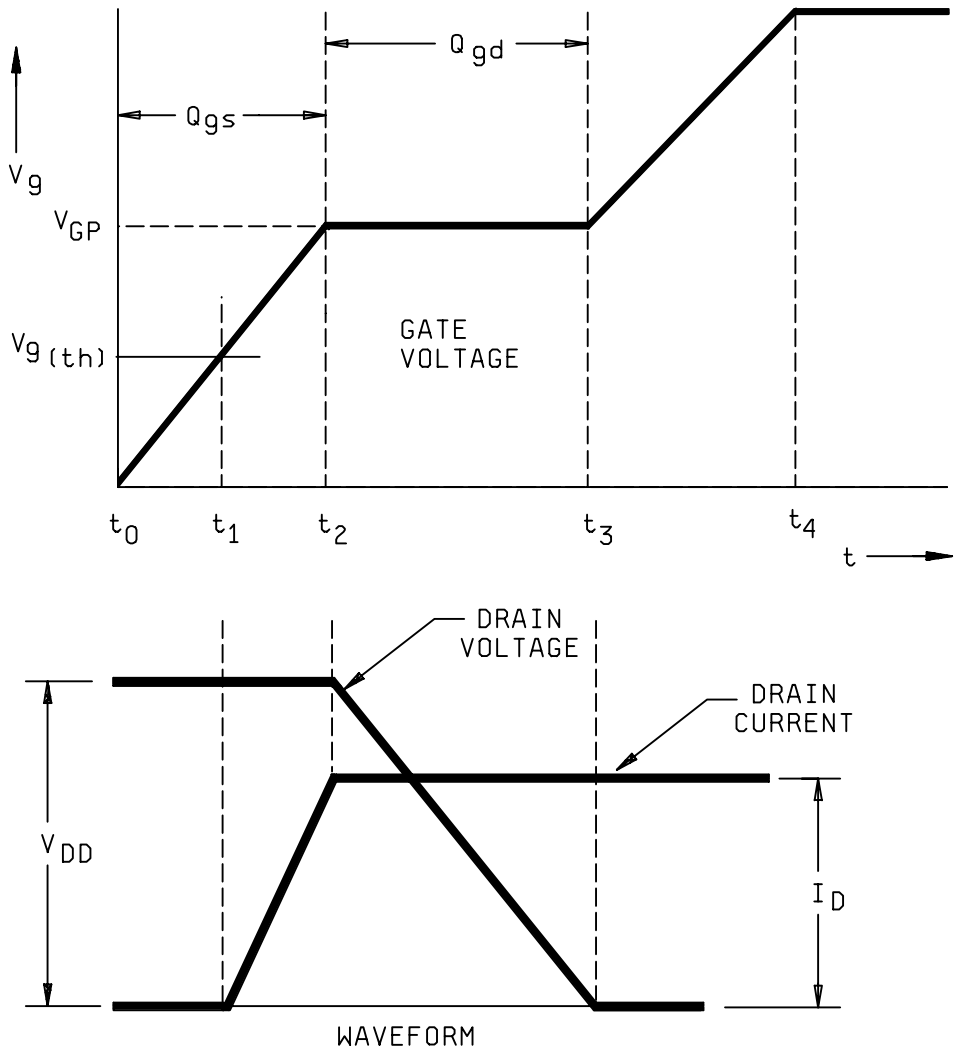

FIGURE 3471-5. Idealized gate charge waveforms, condition B.

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METHOD 3472.2

SWITCHING TIME TEST

1. Purpose. The purpose of this test is to measure the pulse response ($t_{d(on)}$, t_r, $t_{d(off)}$, t_f) of power MOSFET or IGBT devices under specified conditions. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Test procedure. Monitor V_{GS} and V_{DS} versus time using the following notes and precautions. Refer to figures 3472-1 through 3472-4 for clarification.

2.1 Notes and precautions.

a. This method presumes that good engineering practice will be employed in the physical construction of the test circuit, i.e., short leads, good ground plane, minimum gate-to-drain mutual inductance, and appropriate high speed generators and instruments.

b. The value of R_{GS} or R_{GE} includes instrumentation resistive loading. R_{GEN} and R_{GS} R_{GE} should be low enough in value that gate propagation effects are evident.

c. The value of L_{DST} or L_{CET}, C_{GST} or C_{GET}, and C_{DST} or C_{CET} are understood to include those of the test fixture, circuit elements, instrumentation and any added values, exclusive of the DUT. L_{DST} or L_{CET} shall not exceed 100 nH nor shall (C_{DST} or C_{CET}) or (C_{GST} or C_{GET}) exceed 100 pF. Devices with small die may need smaller values of L_{DST} or L_{CET}, C_{DST} or C_{CET}, and C_{GST} or C_{GET}. L_{DST}, C_{DST}, and C_{GST} need not be measured when using figure 3472-3 and figure 3472-4. When $r_{CS(on)}$ or $r_{DS(on)}$ is measured at a V_{GS} or V_{GE} of less than 10 V, then figure 3472-3 and figure 3472-4 do not apply.

d. Gate circuit inductance need not be specified. With the DUT removed, the gate-source voltage waveform should be free of anomalies that could materially affect the measurement. Inductance is difficult to measure accurately in a well designed test fixture. The gate drive common should be Kelvin connected to the device source lead.

e. Passive circuit elements referred to in this method are lumped parameter representations whose values would be those obtained through the use of an RLC bridge using a 1 MHz test frequency.

f. Voltage and current sources are to be interpreted as effective idealizations of active elements.

g. The phrase "affect the measurement" is intended to mean that doubling a value will not affect results greater than the precision of measurement.

h. The turn-off drain voltage overshoot should not be allowed to exceed the device rated drain-source breakdown voltage. Drain circuit ringing begins when the inductive time constant is 25 percent of the capacitive time constant. Ringing is particularly serious when testing low voltage high current devices at high speeds. When the ratio $L_{DST}/R^2 L(C_{DST} + C_{OSS})$ exceeds 10, test conditions may have to be adjusted to ensure that device breakdown is not reached.

i. The instrument used for switching parameter measurement is an oscilloscope with input amplifiers and probes. The affect on rise and fall times can be estimated by the following relationship:

$$(\text{measurement rise time})^2 = (\text{actual rise time})^2 + (\text{amplifier rise time})^2 + (\text{probe rise time})^2$$

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j. When two channels with probes are involved in a measurement (turn-on and turn-off delays), the relative channel probe delays should not materially affect the measurement. Simultaneous viewing the same waveform using the two channel/probes is an effective means of estimating errors.

k. Unless otherwise specified, half rated drain voltage and rated drain current are mandatory conditions for measuring switching parameters.

l. When measuring rise time, $V_{GS(on)}$ shall be as specified on the input waveform. When measuring fall time $V_{GS(off)}$ shall be specified on the input waveform. The input transition and drain voltage response detector shall have rise and fall response times such that doubling these responses will not affect the results greater than the precision of measurement. The current shall be sufficiently small so that doubling it does not affect test results greater than the precision of measurement.

3. Test circuit and waveform: See figures 3472-1, 3472-2, 3472-3, and tables 3472-I and 3472-II.

TABLE 3472-I. Switching time circuit parts list.

Part	No.	Value or size	Manufacturer	PIN
On-board supply	1	15 volts	Datel	UPM 15/100-A
Voltage regulator	1	TO-220 package	National	LM317
Timer	1	8-pin DIP package	National	LM555
Drivers	1	50 V, Hex1, p-channel	I.R.C.	IRFD9010
	1	100 V, Hexz, n-channel	I.R.C.	IRFD1ZO
	2	50 V, Hex2, p-channel	I.R.C.	IRFD9020
	2	50 V, Hex2, n-channel	I.R.C.	IRFD020
Resistors 1/	2	4.95 KΩ, .25 W, ±1 percent	Dale	CMF604951FT0
	1	220 Ω, 0.5 W, ±1 percent	Dale	CMF602200FT0
	1	5 KΩ variable	Dale	724, 5 K, ±10 percent
	1	2.2 MΩ, .25 W, ±1 percent	Dale	CMF602204FT0
	1	360 Ω, .25 W, ±1 percent	Dale	CMF603600FT0
	1	100 Ω, .25 W, ±1 percent	Dale	CMF601000FT0
Capacitors	14	1 μF, 50 V, ±10 percent	Mallory	M30R105K5
	10	.82 μF, 600 V, ±10 percent	CRC	B55F824KXC
	7	.15 μF, 50 V, ±10 percent	Mallory	M30R154K5
	4	.01 μF, 50 V, ±10 percent	Mallory	M10R103K5
	2	22 pF, 600 V, ±5 percent	AVX	AQ14BG220JU
	1	100 pF, 100 V, ±10 percent	Sprague	TST10
	1	100 μF, 450 V, -10 percent, +5 percent	Sprague	53D101F450JS6
	1	.01 μF, 600 V, ±5 percent	Sprague	715P10356KD3
DUT socket	1	TO-3	Loranger	3128-032-4225
BNC	3	PC board mount	Pomona Elect.	4578
Transformer	1	Torroidal core	Micrometals	T5-12
Banana plugs	2	Standard uninsulated	Pomona	3267
Circuit board 2/	1	10.5" x 7.50"		

1/ All resistors are metal-film.
2/ A .062 inch (1.57 mm) double-sided board with 3 ounces copper and 60/40 tin-lead of .0003 inch (0.008 mm) thickness.

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TABLE 3472-II. Switching time circuit, component layout list. 1/ 2/

Label	Component	Value
R1	Resistor	220 Ω
R2	Variable resistor	5 KΩ
R3	Resistor	2.2 MΩ
R4	Resistor	360 Ω
R5	Resistor	100 Ω
R6	Gate resistor	Varies
R7	Drain resistor	Varies
C1, C2, C4, C26	Capacitor 50 V	.01 μF
C3-C10, C12, C14	Capacitor	1 μF
C16, C18, C20, C22	Capacitor	1 μF
C11, C13, C15, C17	Capacitor	.15 μF
C19, C21, C23	Capacitor	.15 μF
C25	Capacitor	100 pF
C27, C29	Capacitor	22 pF
C28	Capacitor 600 V	.01 μF
C30	Capacitor	100 μF
C31-C40	Capacitor	.82 μF
Q1	MOSFET (4 pin DIP)	IRFD9010
Q2, Q3	MOSFET (4 pin DIP)	IRFD9020
Q4	MOSFET (4 pin DIP)	IRFD1ZO
Q5, Q6	MOSFET (4 pin DIP)	IRFD020
Q7	Regulator (TO220)	LM317
Q8	Timer (8-pin DIP)	LM555
T1	Iso. transformer	T5-12

1/ Figure 3472-3 board layout is an artist's view for an n-channel TO-3 package. The following company will provide the circuit boards or a drawing of the exact board layout for a TO-3 as well as other packages such as the TO-39, TO-61, and TO-66:

a. Integrated Technology Corporation
1228 N. Stadem Drive
Tempe, AZ 85281

2/ L_{DST}, C_{DST}, and C_{GST} need not be measured when using these circuit boards derived from figures 3472-3 and 3472-4.

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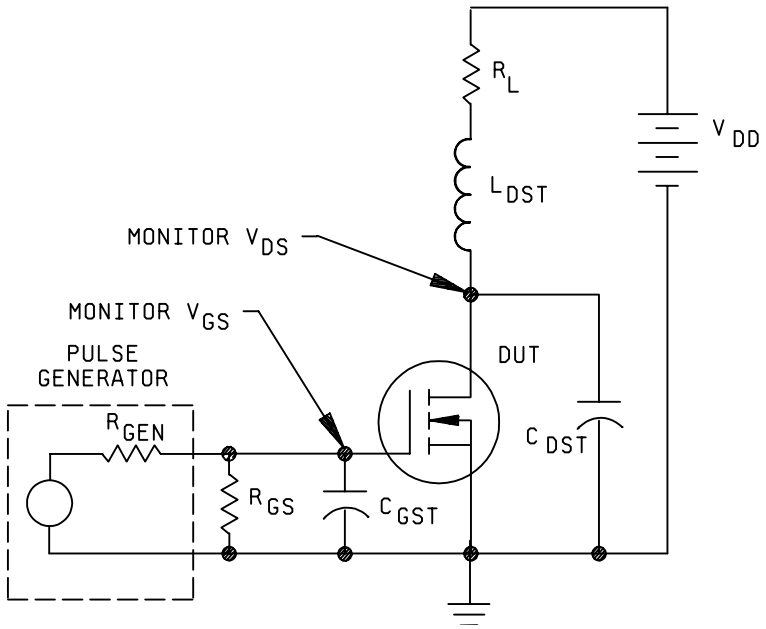

FIGURE 3472-1. Switching time test circuit.

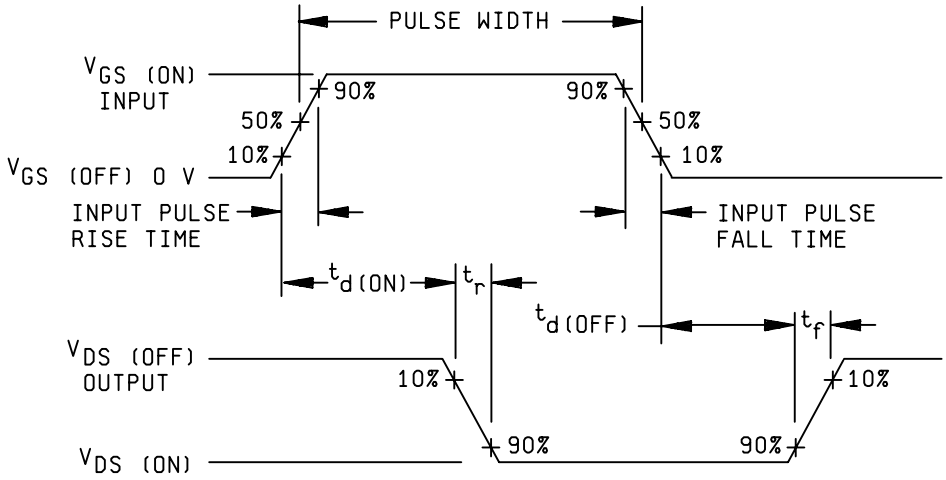

FIGURE 3472-2. Switching time waveforms.

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TOP LAYER

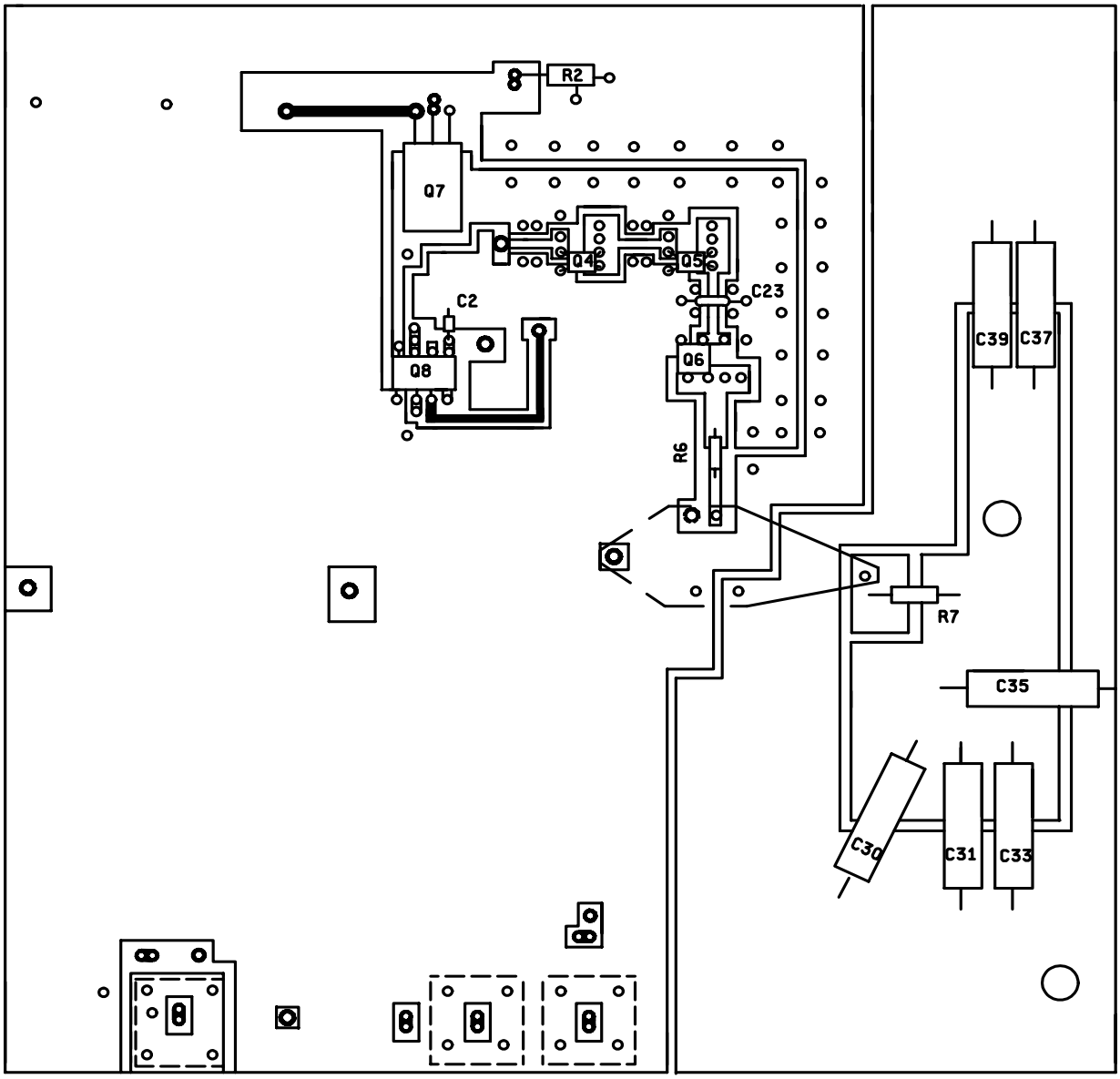

FIGURE 3472-3. Board layout.

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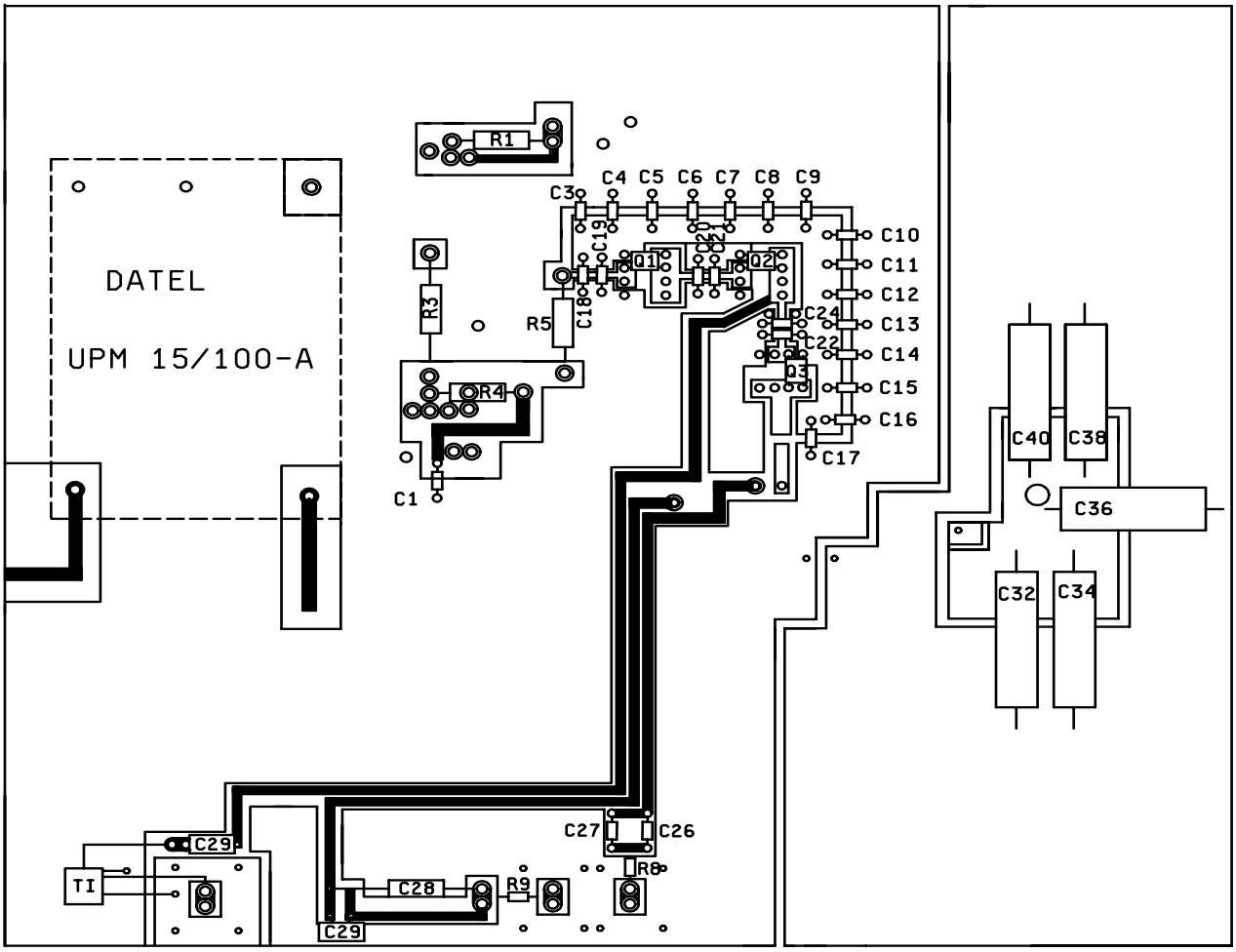

FIGURE 3472-3. Board layout - Continued.

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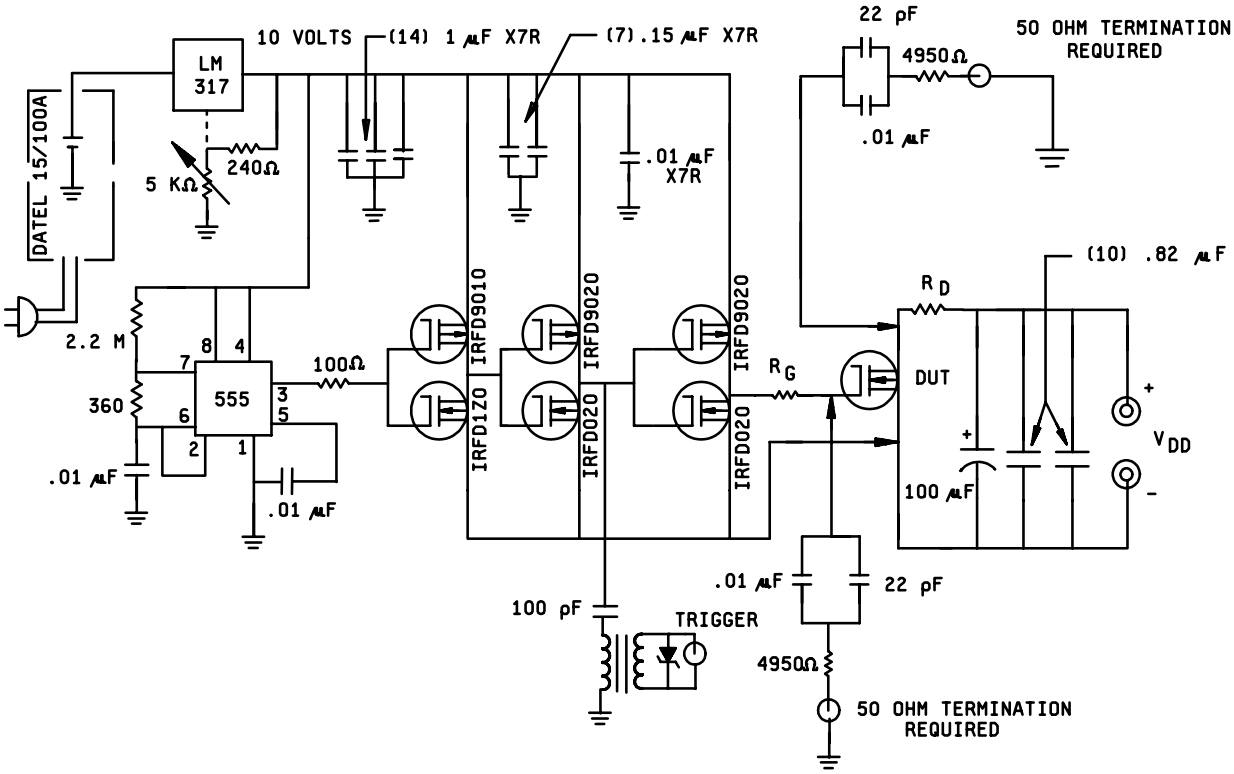

FIGURE 3472-4. Stand alone switching circuit.

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4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. T_C: Unless otherwise specified, case temperature = +25°C.

   b. I_D: On-state drain current (see 4.1.a.).

   c. V_{DD}: Off-state drain voltage (see 4.1.a. and 4.1.b.).

   d. R_L: Nominally equal to V_{DD}/I_D (see 4.1.b.).

   e. V_{GS}: On-state gate voltage (see 4.1.c.).

   f. R_{GS}: Gate-to-source resistance.

   g. R_{GEN}: Resistance looking back into the generator.

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METHOD 3473.1

REVERSE RECOVERY TIME (t_{rr}) AND RECOVERED CHARGE (Q_{rr}) FOR POWER MOSFET (DRAIN-TO-SOURCE) AND POWER RECTIFIERS WITH $t_{rr} \leq 100$ ns

1. Purpose. The purpose of this test is to determine the time required for the DUT to switch off when a reverse bias is applied after the DUT has been forward biased and to determine the charge recovered under the same conditions.

2. Test conditions.

2.1 Test condition A, reverse recovery time (t_{rr}). Monitor diode current versus time. If the DUT is a power MOSFET, the gate lead must be shorted to the source lead. Use the following notes and precautions as a guide. Refer to figures 3473-1 through 3473-3 for clarification.

2.1.1 Notes and precautions.

a. This method presumes that good engineering practice will be employed in the construction of the test circuit, i.e., short leads, good ground plane, minimum inductance of the measuring loop, and minimum self-inductance (L_1) of the current sampling resistor (R_4). Also, appropriate high speed generators and instruments will be employed.

b. The measuring-loop inductance (L_{LOOP}, see figure 3473-1) represents the net effect of all inductive elements, whether lumped or distributed, i.e., bonding wires, test fixture, circuit board foil, and inductance of energy storage capacitors. The value of L_{LOOP} should be 100 nH or less. The reason for controlling this circuit parameter is that it, combined with diode characteristics, determines the value of t_b.

c. The turn-off reverse-voltage overshoot shall not be allowed to exceed the device rated breakdown voltage. Ringing and overshoot may become a problem with $R_{LOOP} < 2(L/C)^{1/2}$; where $L = L_{LOOP}$. That is another reason for minimizing L_{LOOP}.

d. Regarding breakdown voltage, $-V_4$ should be kept as specified.

e. The self-inductance of the current-sample resistor R_4 (see figure 3473-1) shall be kept low relative to t_a because the observed values of t_a and I_{RM} increase with increasing self-inductance. Since the value of R_4 is not specified, the recommended maximum inductance is expressed as a time constant (L_1/R_4) with a maximum value of t_a(minimum)/10, where t_a(minimum) is the lowest t_a value to be measured. This ratio was chosen as a practical compromise and would yield an observed t_a which is 10 percent high ($\Delta t_a = L_1/R_4$). The I_{RM} error is a function of the L_1/R_4 time constant and di/dt. For a di/dt of 100A/µs the observed I_{RM} would also be 10 percent high. $\Delta I_{RM} = L_1/R_4$ di/dt.

f. The di/dt of 100A/µs was chosen so as to provide reasonably high signal levels and still not introduce the large I_{RM} errors caused by higher di/dt.

g. The forward current (I_F) used for this test shall be as specified at T = +25°C.

h. The values of t_a, t_b, and I_{RM} are to be measured and recorded separately. $t_{rr} = t_a + t_b$.

i. The forward current value must be specified, otherwise the t_a and I_{RM} values have little useful meaning.

j. The forward current generator consisting of Q_1, Q_2, R_1, and R_2 may be replaced with any functionally equivalent circuit. Likewise the current ramp generator consisting of Q_3, Q_4, R_3, and C_1.

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2.2 Test condition B, reverse recovered charge (Q_{rr}). This method is direct reading and therefore does not require an oscilloscope. Use the following notes and precautions as a guide. Refer to figures 3473-4 and 3473-5 for clarification.

2.2.1 Notes and precautions.

a. This method presumes that good engineering practice will be employed in the construction of the test circuit, i.e., short leads, good ground plane, minimum inductance of the measuring loop. Also, appropriate high speed generators and instruments will be employed.

b. The measuring-loop inductance (L_{LOOP}, see figure 3473-4) represents the net affect of all inductive elements in the loop, whether lumped or distributed, i.e., DUT bonding wires, test fixture, circuit board foil, and inductive component of energy storage capacitors. The value of L_{LOOP} should be 100 nH or less.

c. The turn-off reverse-voltage overshoot shall not be allowed to exceed the device rated breakdown voltage. Ringing and overshoot may become a problem when $R_{LOOP} < 2(L/C)^{1/2}$; where $L = L_{LOOP}$.

d. Regarding breakdown voltage, $-V_4$ should be kept as specified.

e. The di/dt of 100A/μs was chosen as a compromise between having reasonably high signal levels for the faster devices and the need to keep the reverse voltage as low as possible. Higher di/dt requires a higher reverse voltage to overcome the drop across L_{LOOP}.

f. The forward current (I_F) used for this test shall be as specified at +25°C.

g. The capacitor C_2 (see figure 3473-4) shall be large enough so that there is no appreciable voltage drop across it. Reducing its value by 50 percent shall not change the reading by more than the required measurement accuracy.

h. The current meter across C_2 should have as low a resistance as possible. Doubling the resistance shall not change the reading by more than the required measurement accuracy. A good compromise may be a digital ammeter with a full scale drop of 0.2 volt. If the reverse bias supply is 30 volts, the maximum meter potential differences is then less than one percent of supply voltage.

i. The recommended pulse repetition rate is 1 kHz ±5 percent.

j. The forward current generator consisting of Q_1, Q_2, R_1, and R_2 may be replaced by any functionally equivalent circuit. Likewise the reverse current ramp generator consisting of Q_3, Q_4, R_3, and C_1.

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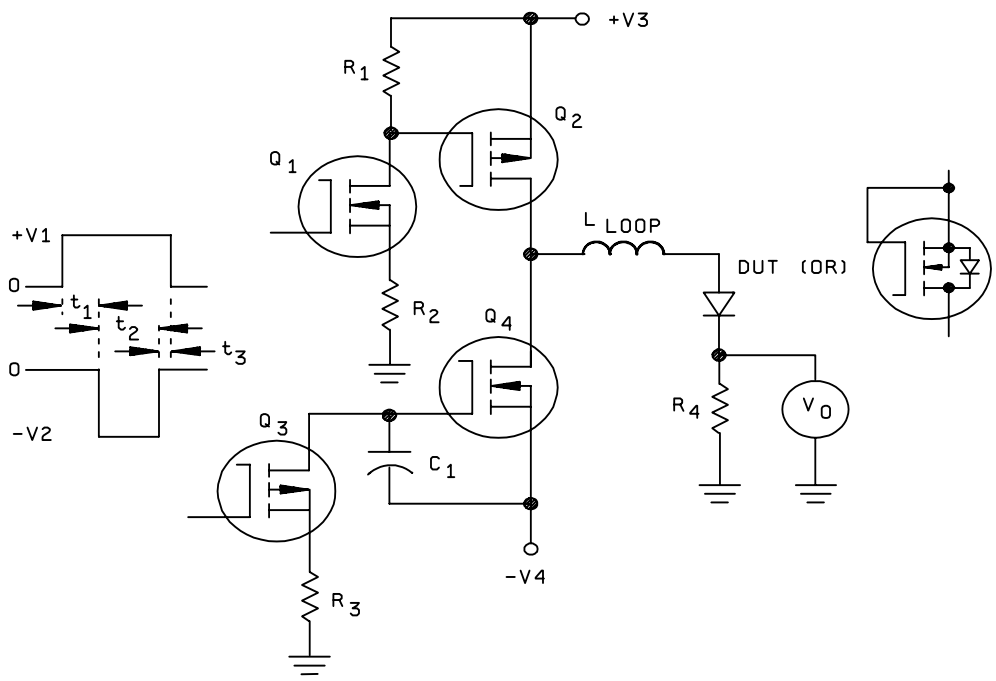

$t_1 >= 5\ t_a$ (max)
$t_2 > t_{rr}$
$t_3 > 0$

$$\frac{L_1}{R_4} <= \frac{t_a(\min)}{10}$$

NOTES:

1. V1 amplitude controls forward current (I_f).
2. V2 amplitude controls di/dt.
3. L_1 is self inductance of R_4.
4. t_a (max) is longest t_a to be measured.
5. t_a (min) is shortest t_a to be measured.

FIGURE 3473-1. t_{rr} test circuit.

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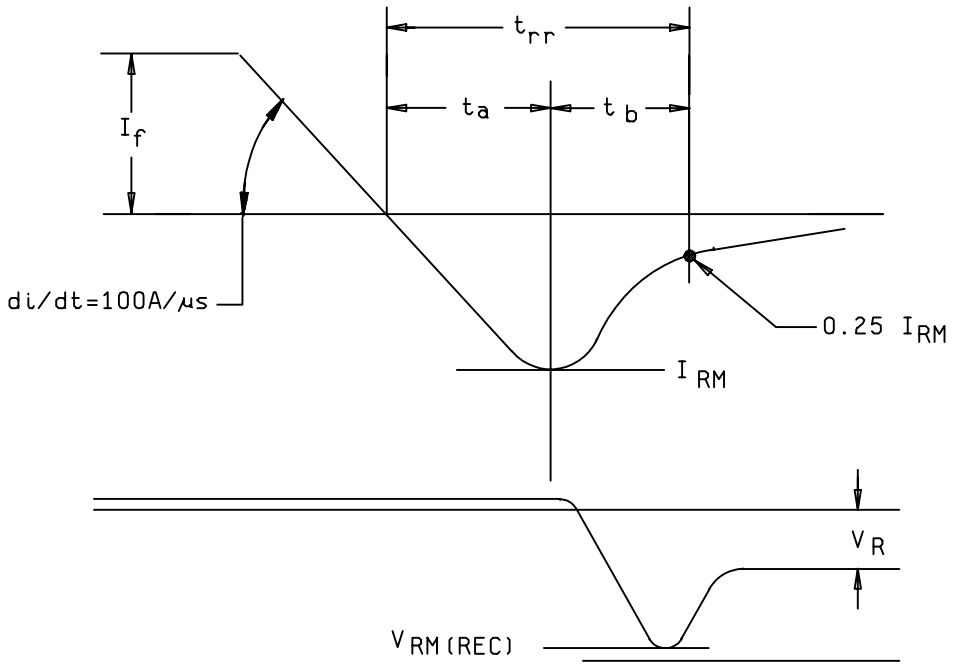

FIGURE 3473-2. Generalized reverse recovery waveforms.

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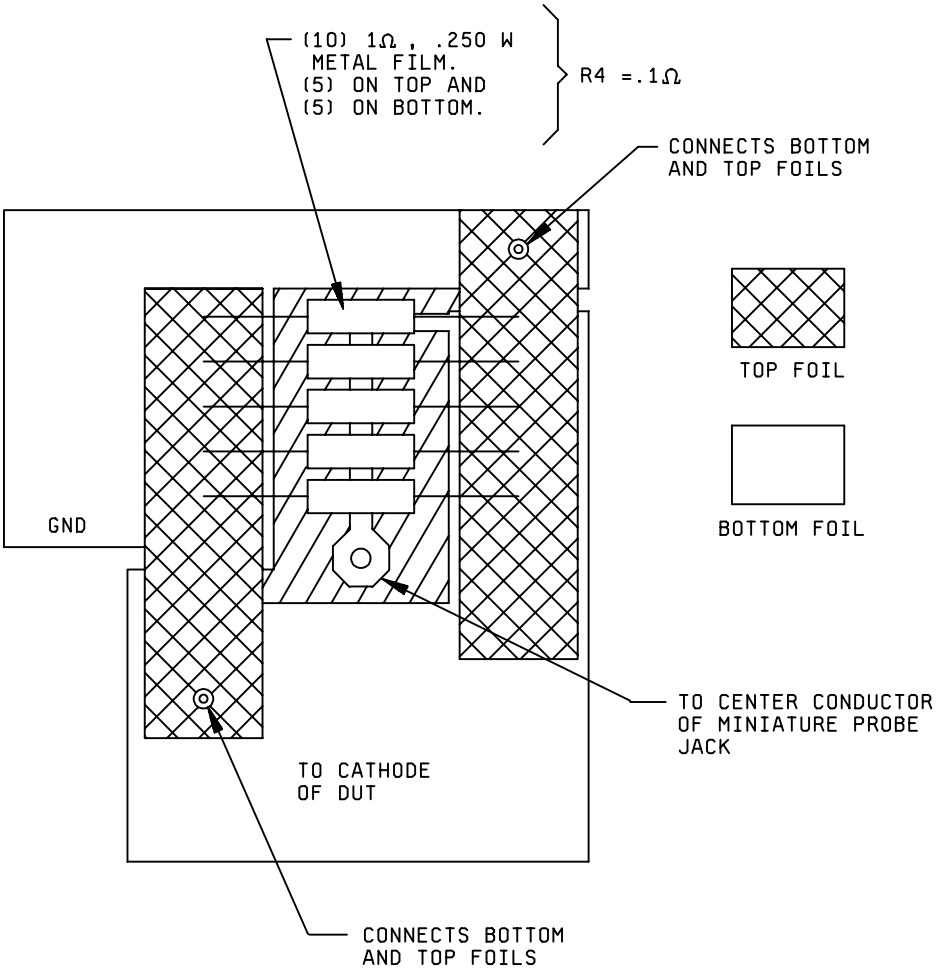

NOTE: Bottom resistor current flow is in opposite direction of top resistor current flow, providing magnetic field cancellation. Sense lead to center conductor of probe jack exits at right angle to resistor axes and is located between the resistor layers; five on the top layer and five on the bottom layer.

FIGURE 3473-3. Suggested board layout for low L_1/R_4.

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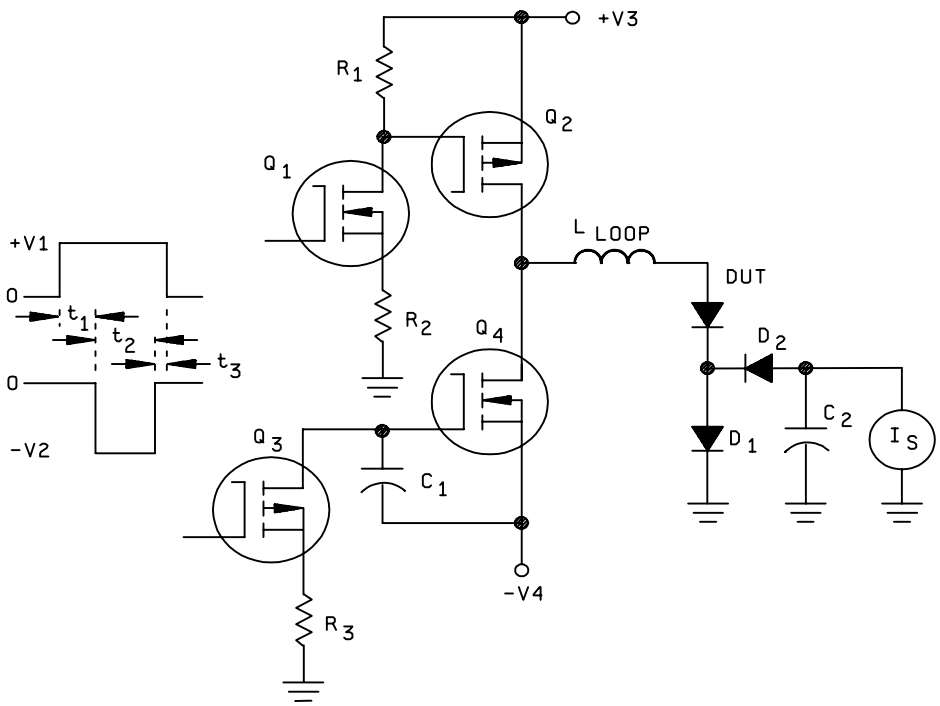

NOTES:

1. D_1 provides forward current path to ground.
2. D_2 steers reverse signal current into integrating capacitor (C_2).
3. V1 amplitude controls forward current (I_f).
4. V2 amplitude controls di/dt.
5. t_1 > = 5 t_a (max); t_a (max) is the highest t_a to be measured.
6. $t_2 > t_{rr}$.
7. $t_3 > 0$.
8. D1 is a low voltage Schottky rectifier.
9. D2 must have a much lower recovered charge than the value being measured.
10. $Q_{rr} = I_S$ PRR; where PRR is pulse repetition rate.
11. di/dt = 100 A/µs.

FIGURE 3473-4. Q_{rr} test circuit.

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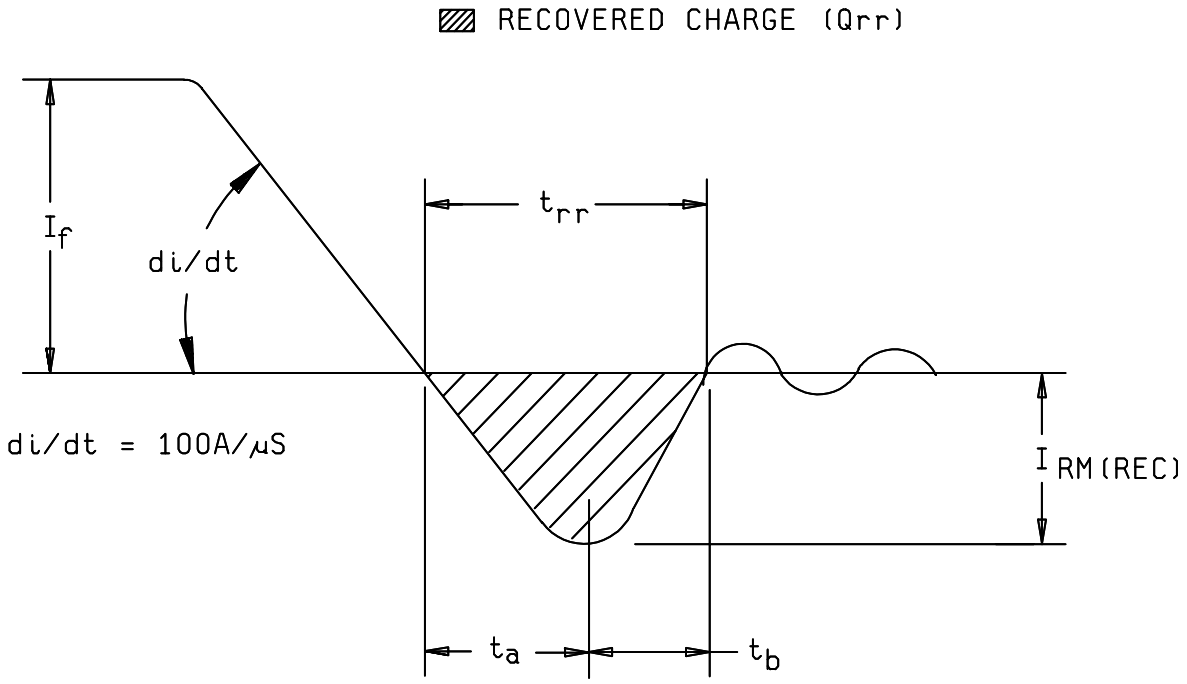

FIGURE 3473-5. Typical t_{rr} waveform (for mnemonic reference only).

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3. Summary. Unless otherwise specified in the applicable specification sheet, the following conditions shall be as follows.

a. T_C: Case temperature = +25°C.

b. I_F: As specified at +25°C.

c. di/dt: 100A/μs.

d. $-V_4$: Reverse-ramp power supply voltage.

e. V_{DD}: As specified.

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METHOD 3474.1

SAFE OPERATING AREA FOR POWER MOSFETs OR INSULATED GATE BIPOLAR TRANSISTORS

1. Purpose. The purpose of this test is to verify the boundary of the SOA as constituted by the interdependency of the specified voltage, current, power, and temperature in a temperature stable circuit. Deliberate consideration is given to the problem of unavoidable case temperature rise during the test. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

1.1 Symbols and definitions. The following symbols and terminology shall apply for the purpose of this test method:

a. D_F: Linear derating factor (W/°C).

b. I_D: Test current (amperes).

c. P_D: Test power dissipation (watts).

d. P_{DM}: Maximum rated power dissipation (watts).

e. $R_{\theta CS}$: Case to heat sink thermal resistance (K/watt).

f. $R_{\theta JC}$: Junction to case thermal resistance (K/watt).

g. $R_{\theta SA}$: Heat sink to ambient thermal resistance (K/watt).

h. T_A: Ambient temperature (°C).

i. T_C: Case temperature (°C).

j. T_{CR}: Rated SOA case temperature (°C).

k. T_J: Junction temperature (°C).

l. T_{JM}: Maximum rated junction temperature (°C).

m. t_p: Test pulse duration (seconds).

n. T_S: Heat sink temperature (°C).

o. V_{DD}: Test power supply voltage (volts).

p. V_{DS}: Drain to source voltage (volts).

2. Test circuit. See figure 3474-1. Circuit polarities shall be reversed for p-channel devices.

a. R_S shall be a Kelvin contact resistor of five percent tolerance.

b. Operational amplifier shall have a speed and accuracy such that the errors it produces will contribute less than a five percent error to the measurement.

c. Precision voltage source shall have an accuracy of five percent.

d. S1 shall have adequate speed and characteristics such that the accuracy of the measurement will not be affected by more than five percent.

e. V_{DD} shall be maintained to within five percent.

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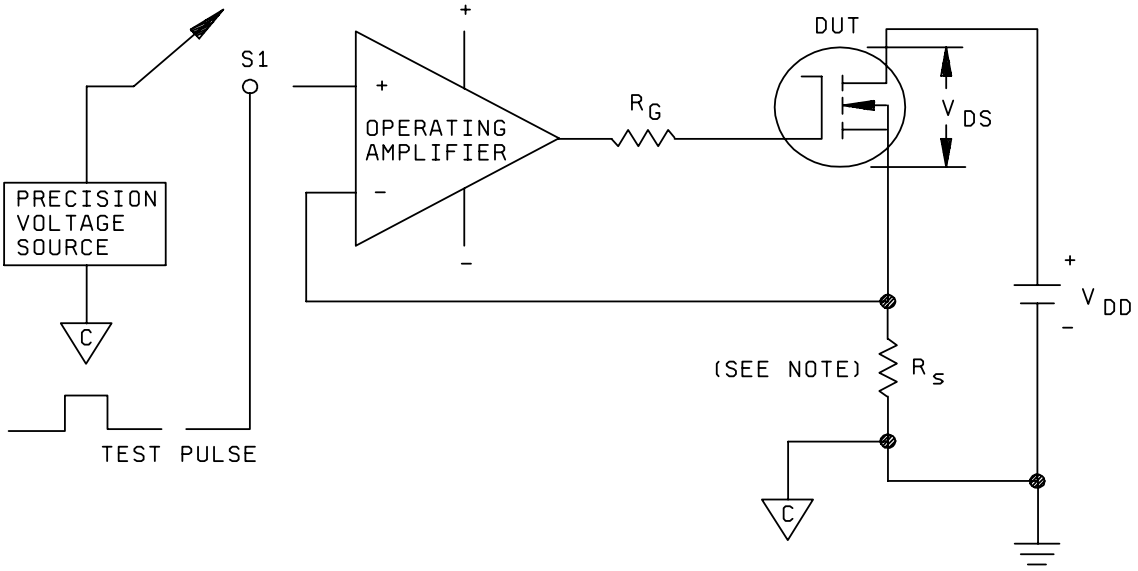
f. t_p shall be maintained to within five percent.

g. Total test accuracy shall be maintained to within 10 percent.

h. R_G shall be selected to eliminate parasitic oscillations.



NOTE: Low inductance resistor.

FIGURE 3474-1. SOA test circuit.

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3. Procedure. Set the precision voltage source to I_D x R_S. Applied V_{DD} to the circuit. Close S1 for t_p seconds.

4. Summary. In any practical application, the junction temperature during an SOA test can be calculated by adding all of the temperature drops in the system to the ambient temperature:

$R_S \leq$ (maximum rated gate voltage) I_D not to exceed (.2 x maximum rated V_{DS})/I_D
$T_J = T_A + \Delta$sink to ambient + Δcase to sink + Δjunction to case

$$I_D = \frac{(P_{DM} - (T_C - T_{CR}) \times D_F)}{V_{DS}}$$

Under a controlled set of conditions, such as those that are encountered in an SOA test, the case temperature can be measured and therefore known as a constant. This simplifies the expression substantially:

$T_J = T_C + \Delta$junction to case
$T_J = T_C + P_D \times R_{\theta JC}$

By substituting in the maximum rated junction temperature and rearranging the terms, the maximum power dissipation for this condition can be calculated:

$$P_D \frac{(T_{JM} - T_C)}{R_{\theta JC}}$$

If a case temperature of T_{CR}°C was chosen for the purpose of specifying the device SOA, then a derating factor D_F can be determined:

$$D_F = \frac{P_{DM}}{(T_{JM} - T_{CR})}$$

P_{DM} can be any P_{DM} from the SOA curves for that particular device type, either dc or pulsed. The maximum power dissipation for any case temperature can now be readily calculated and used in an SOA test

$P_D = P_{DM} - (T_C - T_{CR}) \times D_F$

Unless otherwise specified in the applicable specification sheet, the following conditions shall be as follows.

a. V_{DS} = as specified.

b. I_D = as calculated above.

c. +20°C $\leq T_C \leq$ +45°C.

d. t_p shall be that which corresponds with the SOA curve being used.

e. $D_F = \frac{P_{DM}}{(T_{JM} - T_{CR})}$.

f. R_S = as calculated above.

g. P_{DM} shall be a value chosen from one of the SOA curves for that particular device either dc or pulsed.

h. $V_{DD} = V_{DS} + I_D \times R_S$.

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METHOD 3475.1

FORWARD TRANSCONDUCTANCE (PULSED DC METHOD) OF POWER MOSFETs OR INSULATED GATE BIPOLAR TRANSISTORS

1. Purpose. The purpose of this establishes a basic test circuit for the purpose of establishing forward transconductance (g_{FS}) using pulsed dc for the test conditions to enable measurements above the small signal (g_{FS}) output current levels. The described method is adaptable to ATE where large ac test currents are often impractical. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Procedure. The gate-source voltage (V_{GS1}) is applied as necessary to achieve a specified drain-source current. I_{D1} shall be five percent minimum less than the value of I_D used in specifying $r_{DS(on)}$ (normally 50 percent of rated dc current). The gate-source voltage (V_{GS1}) is then decreased to achieve a second drain-source current (I_{D2}). I_{D2} shall be five percent minimum below the I_{D1} used in specifying $r_{DS(on)}$. The drain-source voltage (V_{GS2}) shall remain equal to the value specified for establishing I_{D2}.

Calculation:

$$g_{FS} = \frac{I_{D1} - I_{D2}}{\Delta V_{GS}}$$

Where: $\Delta V_{GS} = V_{GS1} - V_{GS2}$

NOTE: ΔV_{GS} should not be set lower than 0.05 volt or test equipment accuracy can adversely affect measurement. I_{D1} and I_{D2} can be adjusted such that ΔV_{GS} is $\geq$ 0.1 volt. In all cases I_{D1} and I_{D2} should be adjusted so they are equally above and below specified current. The formula below can be used as initial reference point:

If:

$$\Delta V_{GS} = \frac{I_{D1} - I_{D2}}{G_{FS}}$$

then:

$$\frac{I_{D1} - I_{D2}}{2} = \Delta I_D \, desired$$

The previous calculations can be used in establishing minimum ΔV_{GS} desired to achieve highest accuracy.

3. Test circuit. See figure 3475-1.

4. Summary. Unless otherwise specified in the applicable specification sheet, the following conditions shall be as follows.

a. I_{D1} = 0.5 I_D continuous at T_C = +25°C x 1.05 minimum.

b. I_{D2} = 0.5 I_D continuous at T_C = +25°C x 0.95 minimum.

c. V_{DS} = 4 $r_{DS(on)}$ x 0.5 I_D continuous or as necessary to be in the active region.

d. $\Delta V_{GS} \geq$ 0.1 volts.

e. $r_{DS(on)}$ as specified.

f. Pulse width $\leq$ 300 μs.

g. Unless otherwise specified, (T_C) = (temperature of case) = +25°C.

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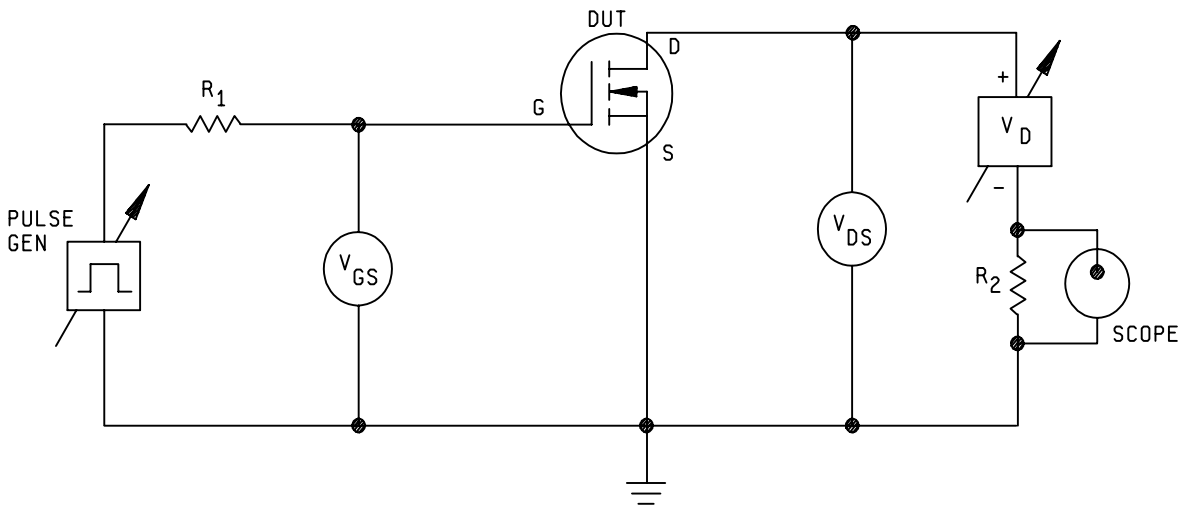

NOTES:

1. Pulse the device according to 4.3.2.2 of MIL-STD-750. Resistor R_1 shall be used to damp spurious oscillations that can occur (approximately 100 Ω).
2. The device used for circuit illustration is an n-channel, enhancement-mode FET. The methodology described is not limited solely to this type of device. For all other field effect devices where the power ratings are such that the dc method is the preferred method, the parameter symbols need only indicate the appropriate voltage or current polarity.
3. When performing this test on a nonheat-sinked part, the following caution is applicable. The implementation of this test requires the use of repeated incremental steps of gate voltage, while measuring drain current. The number of steps and the duration of each step result is cumulative energy which may thermally overstress the part if it is not heat-sinked. A stepped program to perform this test will result in higher power dissipation during test of a unit requiring a high gate drive voltage than during test of a unit requiring a lesser gate drive voltage.
4. R_2 is a noninductive, current sensing resistor and is normally ≤ 0.1 Ω.

FIGURE 3475-1. Forward transconductance circuit.

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METHOD 3476

TEST PROCEDURE FOR MEASURING DV/DT DURING REVERSE RECOVERY OF POWER MOSFET TRANSISTORS

1. Purpose. The purpose of this test is to define a way for verifying the diode recovery stress capability of power MOSFET transistors. The focus is on simplicity and practicality.

2. Scope. This test covers all power transistors which have an internal diode capable of commutating current generated during reverse recovery.

3. Symbols and definitions.

a. di/dt: Rate of change of diode current while in reverse-recovery mode, recorded as maximum value.

b. Driver: A device is used in the lower portion of a half H bridge (see figure 3476-1) and is an equivalent to the DUT.

c. dv/dt: Rate of change of reapplied diode voltage, as measured as maximum value of inflection.

d. I_{DSS}: Zero gate voltage drain current.

e. I_{FM}: Maximum body diode forward current.

f. I_{GSS}: Reverse gate current, drain shorted to source.

g. $L_{(LOAD)}$: Load inductor. Shall be of a large enough value that the decay of current during the forward conduction of the DUT is less than five percent of I_{FM}.

h. $R_{DS(ON)}$: Static drain-source on-state resistance.

i. R_{DUT}: Gate-to-source circuit resistance at DUT.

j. R_G: Gate drive impedance.

k. T_j: Semiconductor junction temperature.

l. t_{rr}: Reverse recovery time.

m. $V_{(BR)DSS}$: Breakdown voltage drain-source.

n. V_{DD}: Supply voltage.

o. V_{DS}: Drain-source voltage.

p. V_{GEN}: Gate generator voltage (volts) for drive transistors.

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4. Circuit. Basic circuitry for testing this parameter is shown on figure 3476-1. Idealized waveforms are shown on figure 3476-2. Snubbers may not be used. Stray capacitance and inductance, especially in the source of the drive transistor, shall be minimized.

The basic principle of the circuit may not be altered; that is, the lower half H bridge device must be equivalent to the DUT. The circuit may operate continuously or single shot, as long as the required test conditions are achieved. Gate drive to the driver may be any Thevenin equivalent of that specified.

To test continuously or single shot, the electrical sequence is similar.

a. Drive is turned on until current in $L_{(LOAD)}$ is higher than I_{FM}.

b. Driver is turned off until current in DUT reaches I_{FM}. The minimum time for DUT forward conduction is 5 μs or 10 times the rated maximum t_{rr}, whichever is greater.

c. If testing repetitively, go back to 4.a. Else, driver is turned on for the reverse recovery period of the device plus a minimum additional one microsecond. The DUT shall be monitored for V_{DS} collapse during this additional time period and gate drive to the driver transistor may be removed at any time a failure is encountered.

If the device operates with a low repetition rate, the device may not be exposed to sufficient energy to cause a catastrophic failure. The circuit must be equipped to either cause catastrophic failure or generate a failure signal in the event of a collapse of V_{DS} during voltage recovery.

5. Specification details. The specification may take the form of a single point tabular specification, a graphical representation, or both. Ideally, a device will have both. This will allow for easy comparison of devices with the tabular specification, but still have the detail of the graph available to the designer.

a. A tabular specification will define a single point of operation. The following must be specified in the applicable specification sheet.

(1)	di/dt Reverse current change rate	_____	A/μsec.
(2)	V_{GEN} Gate generated voltage	_____	V
(3)	I_{FM} Maximum forward current	_____	A
(4)	V_{DD} Supply voltage	_____	V
(5)	T_j Junction temperature	_____	°C
(6)	dv/dt Reverse voltage change rate limit	_____	V/ns maximum

b. A graphical representation could take several different forms; for example: R_G versus I_{FM}, di/dt versus dv/dt, or I_{FM} versus V_{DS}. An example of R_G versus I_{FM} is shown on figure 3476-3.

6. Acceptance criteria. If a specification requires that this test be performed for verification of a maximum limit, then the device V_{DS} must not collapse during or after reverse recovery and (in addition) shall pass any specified parametric limits, as a minimum: $V_{(BR)DSS}$, I_{GSS}, I_{DSS}, and $R_{DS(ON)}$.

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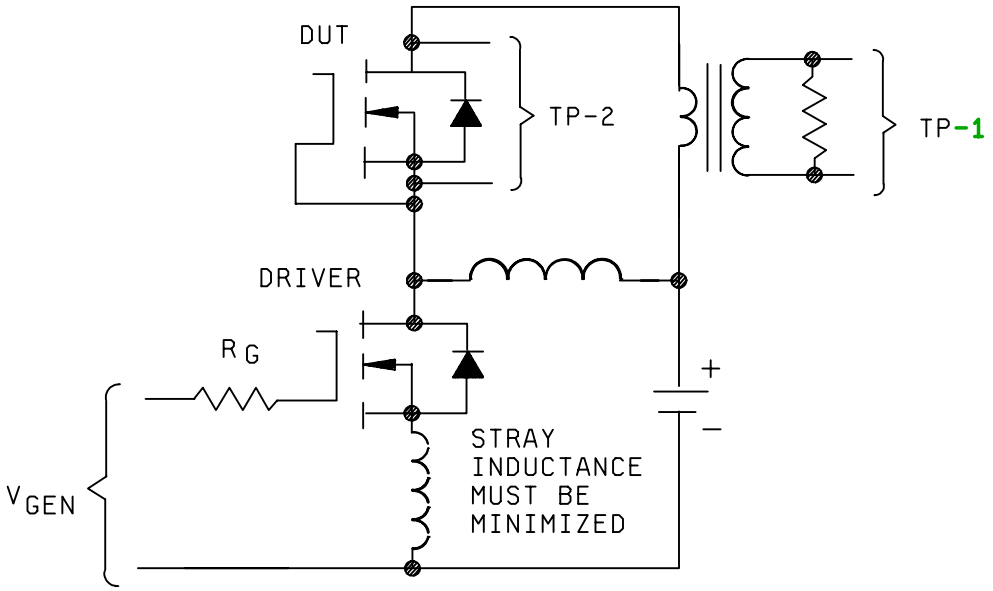

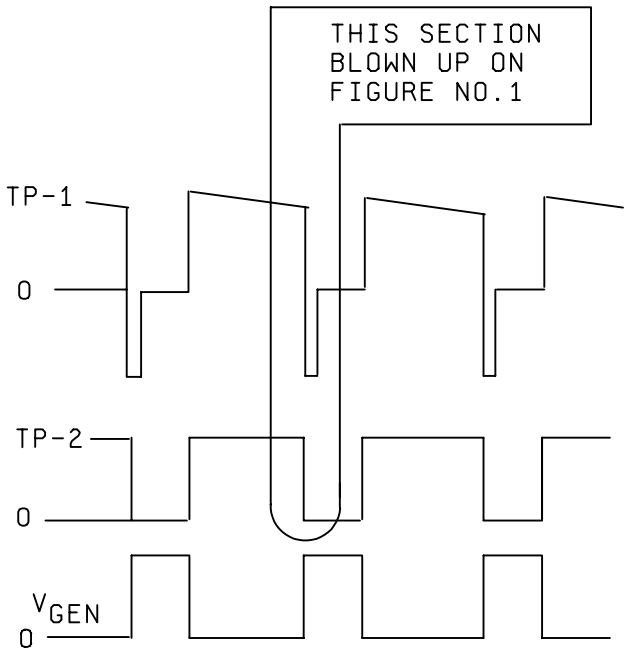

FIGURE 3476-1. Body diode test circuit.

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di/dt and dv/dt

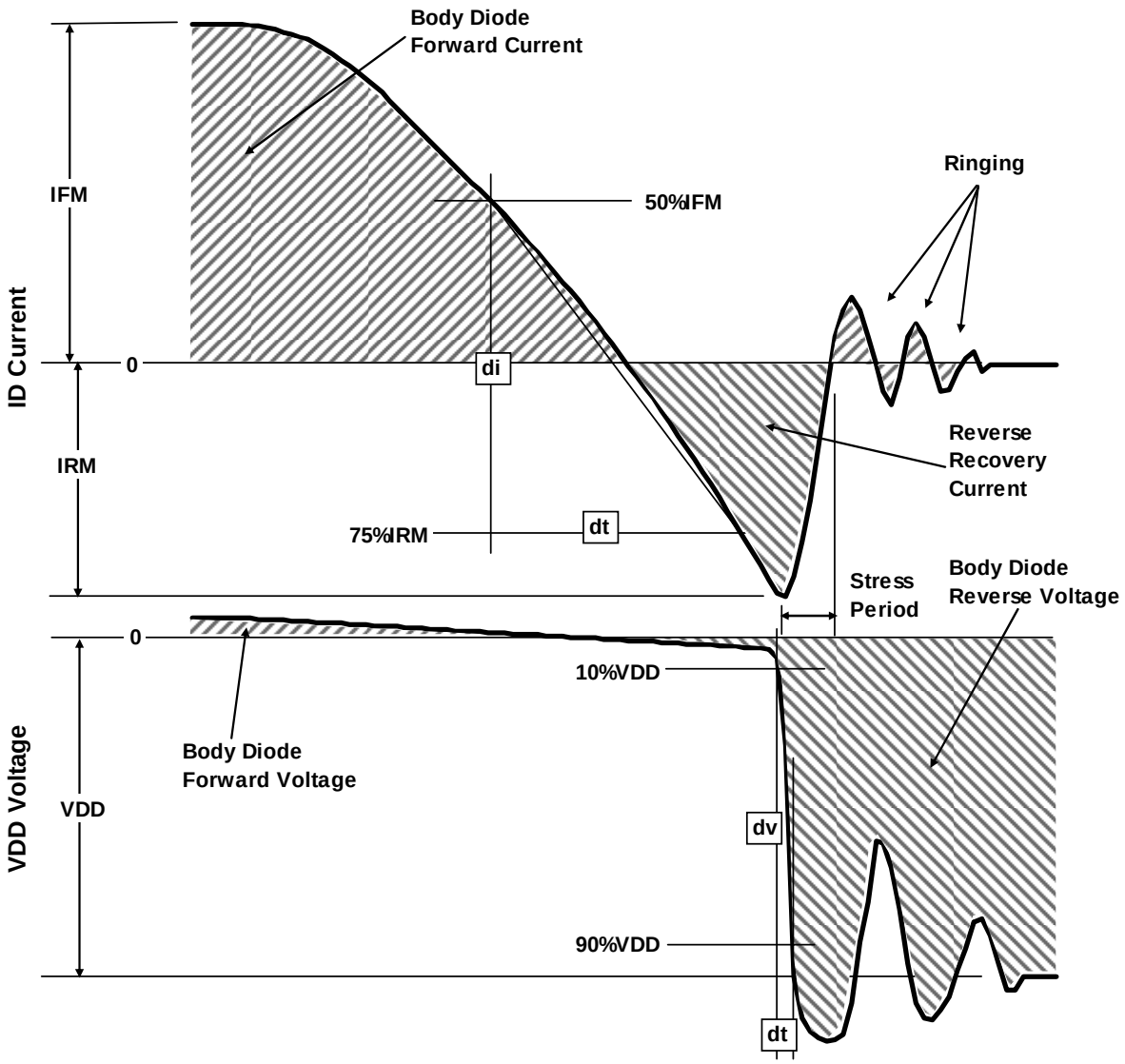

FIGURE 3476-2. Body diode waveforms.

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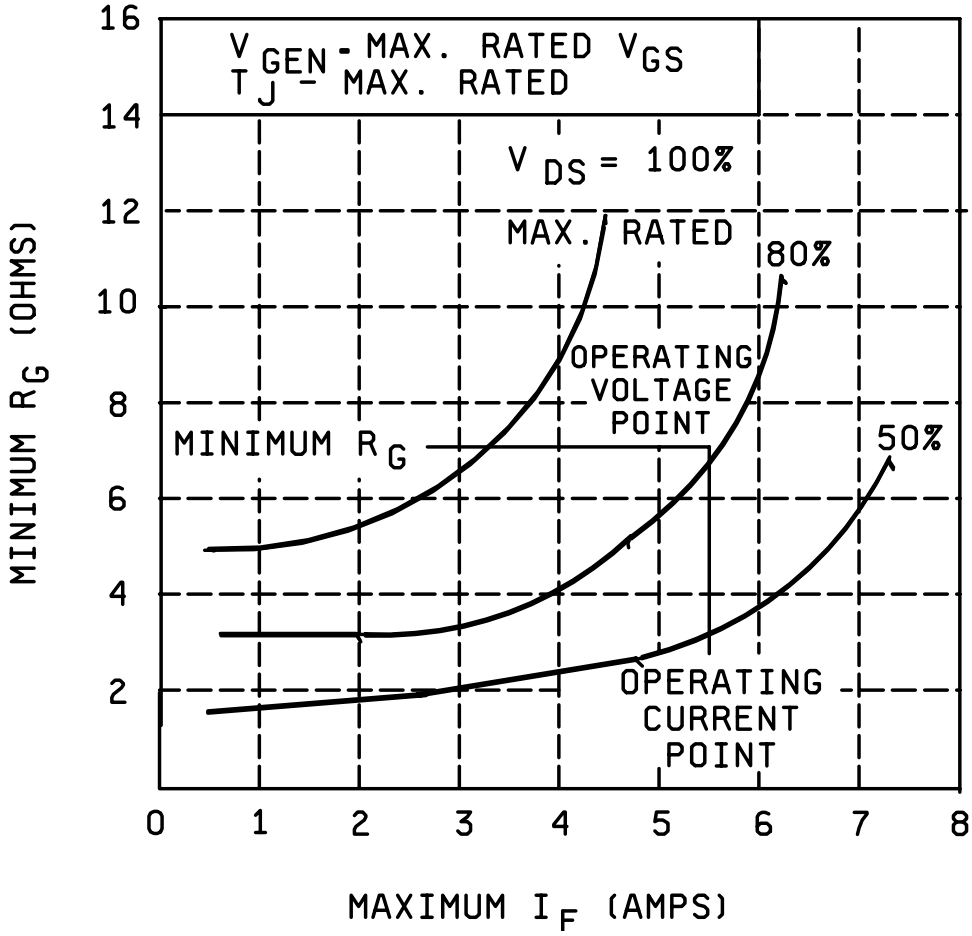

FIGURE 3476-3. Example of graphic representation.

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METHOD 3477.1

MEASUREMENT OF INSULATED GATE BIPOLAR TRANSISTOR TOTAL SWITCHING LOSSES AND SWITCHING TIMES

1. Purpose. This test defines the basic test circuitry and waveform definitions by which to measure the total switching losses of an IGBT.

2. Scope. This method applies only to measurements of IGBT devices without an integral diode.

3. Symbols and definitions. The following symbols and terminology shall apply for the purposes of this test method:

a. $V_{(BR)CES}$: Collector/emitter breakdown voltage.

b. I_{CE}: Test current.

c. V_{GE}: Gate to emitter voltage.

d. R_G: Gate drive series resistance.

e. V_{CL}: Clamp voltage (80 percent rated $V_{(BR)CES}$).

f. t0: Time point where V_{CE} is at 10 percent of the specified gate drive.

g. t1: Time point where I_{CE} = 5 percent I_{CE} (maximum).

h. t2: Time point where V_{CE} = 5 percent V_{CL} when V_{CE} is decreasing.

i. t3: Time point where V_{CE} = 5 percent V_{CL} when V_{CE} is increasing.

j. t4: t3 + 5 μs.

k. $t_{d(on)}$: Turn on delay time.

l. t_r: Rise time.

m. $t_{d(off)}$: Turn off delay time.

n. t_f: Fall time.

o. W_{ON}: Turn on switching losses.

p. W_{OFF}: Turn off switching losses.

q. W_{TOT}: Total switching losses.

r. T_j: Semiconductor junction temperature.

s. V_G: Gate drive voltage.

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4. Circuitry. Figure 3477-1 shows the basic test circuit. The circuit has to satisfy two fundamental requirements.

a. The circuit reflects the losses that are attributed to the IGBT only and is independent from those due to other circuit components, like the freewheeling diode.

b. The operation of the circuit shown on figure 3477-1 is as follows:

(1) The driver IGBT builds the test current in the inductor. When it is turned off, current flows in the zener. At this point, the switching time and switching energy test begins, by turning on and off the DUT. In its switching, the DUT will see the test current that is flowing into the inductor and the voltage across the zener, without any reverse recovery component from a freewheeling diode. This test can exercise the IGBT to its full voltage and current without any spurious effect due to diode reverse recovery.

(2) Input drive duty cycle should be chosen such that T_j is not affected. Control of T_j is best done using external methods.

5. Method. Figure 3477-2 shows the DUT current and voltage waveforms and test points.

5.1 Energy loss during turn on. During turn on, the energy loss is defined as follows in equation (1).

(1) $$W_{ON} = \int_{t1}^{t2} i_{CE} \bullet V_{CE}\, dt \;\; joules/pulse$$

Refer to figure 3477-2 for t1 and t2

5.2 Energy loss during turn off. During turn off, the energy loss is defined as follows in equation (2).

(2) $$W_{ON} = \int_{t4}^{t3} i_{CE} \bullet V_{CE}\, dt \;\; joules/pulse$$

Refer to figure 3477-2 for t3 and t4

5.3 Total switching loss. The total switching loss is the sum of equations (1) and (2).

$W_{TOT} = W_{ON} + W_{OFF}$ joules/pulse

5.4 Switching time measurements. Switching time measurements, while not the preferred method of delineating between devices, may be determined using the measurements below and as seen on figure 3477-2.

a. $t_{d(on)}$: The interval measured from the 10 percent point of the rising input pulse V_g and the 10 percent rise of the output current I_C.

b. t_r: The interval measured from the 10 percent to the 90 percent point of the rising output current I_C.

c. $t_{d(off)}$: The interval measured from the 90 percent point of the falling input pulse V_g to the 90 percent point of the falling output current I_C.

d. t_f: The interval measured from the 90 percent to the 10 percent point of the falling output current I_C.

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6. Equipment. A modern high speed digitizing system is recommended. The measurement of W_{ON} or W_{OFF} is accomplished by accessing the output V(t) and I(t) waveforms, digitizing them, and transmitting the data to a computer where W_{ON} or W_{OFF} is calculated and the results displayed. Two factors of importance must be considered.

a. Sample spacing must be short, relative to transition times for accurate and repeatable results.

b. The relative V(t), I(t) channel delay must be known and accounted for in the computer program that does the point by point multiplication and summation that determines either W_{ON} or W_{OFF} (see figure 3477-2).

7. Specifications.

a. V_{CL}: Clamp voltage ____ V

b. I_{CE}: Maximum test current A ____ A

c. V_{GE}: Gate to emitter voltage ____ V

d. R_G: Gate resistance ____ Ω

e. T_j: Junction temperature ____ °C

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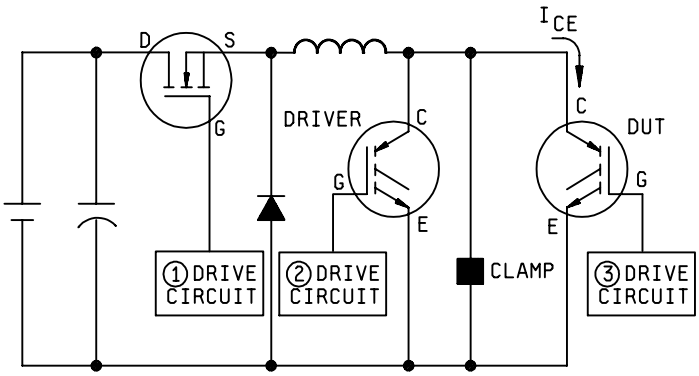

FIGURE 3477-1. Test circuit.

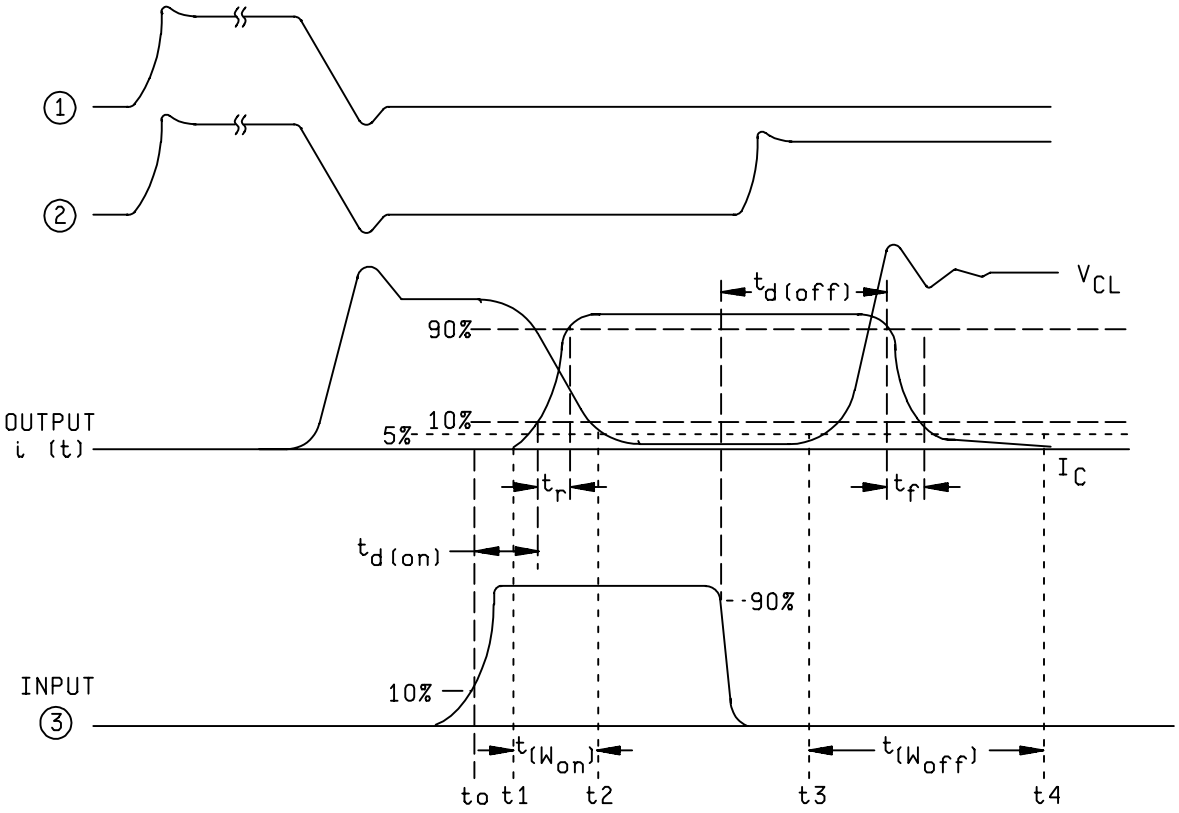

FIGURE 3477-2. Typical clamped inductive waveforms.

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METHOD 3478

POWER TRANSISTOR ELECTRICAL DOSE RATE

1. Purpose. The purpose of this test method establishes a baseline methodology for characterizing high-voltage transistors to high gamma dose rate radiation and for establishing electrical criteria to evaluate key test fixture parameters. From this data, a valid comparison can then be made between the device's response and its radiation data. Since power transistors are susceptible to radiation-induced burnout/damage, this test method should be considered a destructive test. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Symbols and definitions. The following symbols and terminology shall appl for the purposes of this test method.

a. Power transistor burnout: Burnout is defined as a condition that renders the power transistor nonfunctional, usually a result of current-induced avalanche and second breakdown. Identification is accomplished by observing the drain current during irradiation and by verifying the device's performance after irradiation.

b. Symbols and terms.

di/dt: Change in current with respect to time (amperes per second).

dv/dt: Change in voltage with respect to time (volts per second).

I_{ds}: Measured current flowing into drain (amperes).

FWHM: Full-width half-max pulse width.

L_s: Calculated stray inductance observed by the DUT's response (henrys).

PW: Radiation pulse width defined by the full-width half-max (FWHM) measurement (seconds).

RC: Time constant equal to the resistance times capacitance

R_s: Calculated stray resistance observed by the DUT's response (ohms).

V_{ds}: Applied measured drain-to-source voltage (volts).

V_{gs}: Applied measured gate-to-source voltage (volts).

3. Test plan. A detailed test plan shall be prepared specifying, as a minimum, the following information.

a. Identify device types to be tested.

b. Identify number of samples.

c. Test fixture characteristics of stray R_s and L_s, based upon previous data or calculations (see 5.8).

d. Electrical characterization required in accordance with applicable specification sheet before and after the radiation event.

e. Electrical parameters to be monitored.

f. Complete description of test system (e.g., schematics, flow charts).

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4. Apparatus.

4.1 Instrumentation. Instrumentation required to monitor and test the device to high gamma dose rate radiation will generally consist of the following types of equipment.

a. Curve tracer.

b. Digital or analog voltmeter.

c. DC current probe.

d. Digital or analog current meter.

e. Digitizer or storage scope.

f. High-voltage power supply.

4.2 Holding fixture. The holding fixture may be mandated by the test facility. Coordination between users and facility is an absolute necessity. The fixture shall be capable of interfacing the power and signal lines between the test board and DUT, as well as, collimating the radiation beam to expose only the DUT.

4.3 Test fixture. The test board shall be constructed to meet the following requirements.

a. Construction: Circuit layout and construction are critical. Circuit layout and construction shall be optimized to minimize stray L_S and R_S effects presented to the DUT. Applicable gauge wires, ground planes, and materials shall be used to minimize these effects of stray inductance and resistance. Wire lengths shall be kept to an absolute minimum.

   CAUTION: Wire lengths connecting the DUT in excess of four inches (101.60 mm) should be re-evaluated to determine shortest possible wire length.

b. Components: Circuit components shall be chosen to optimize performance. Capacitors shall have high Q ratings reflecting high di/dt. The test circuit shall have multiple capacitors in parallel, minimizing the parasitic resistance presented by each capacitor while obtaining the required dv/dt response. DC current probes shall be passive having minimal ac insertion resistance. The current probe shall also be capable of measuring a large current without saturating its magnetic core.

c. DUT package: Circuit and device parameters will dictate the power transistor response to high gamma dose rate radiation. The DUT shall be tested in the same package type that will be used in the system. If a different package type is used, then electrical, mechanical, and thermal properties of that package need to be considered and their effects accounted for in the test results.

d. Test circuit: Schematically, test circuits are as shown on figure 3478-1 and representative waveforms are depicted on figure 3478-2. Components and wiring shall not be placed directly in the radiation beam. An isolation resistor shall be placed between the stiffening capacitors and high-voltage power supply, minimizing its interaction with the DUT response. The resistor value will depend on the RC time constant required to isolate interaction. Biasing of the gate shall be accomplished using an RC filtering or ballasting resistor network (see figure 3478-1a or 3478-1b), unless it is connected directly to the common source (see figure 3478-1c).

   CAUTION: Peak currents in excess of 1,000 amperes with di/dt in excess of 1,000 amperes per microsecond are possible.

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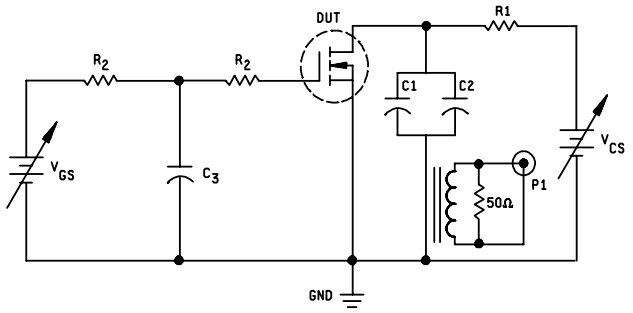


FIGURE 3478-1a. Gate bias configuration 1.

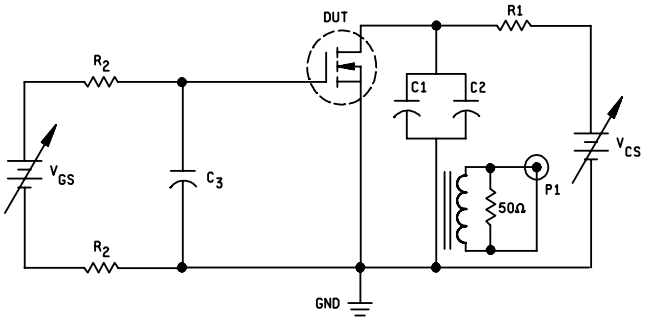
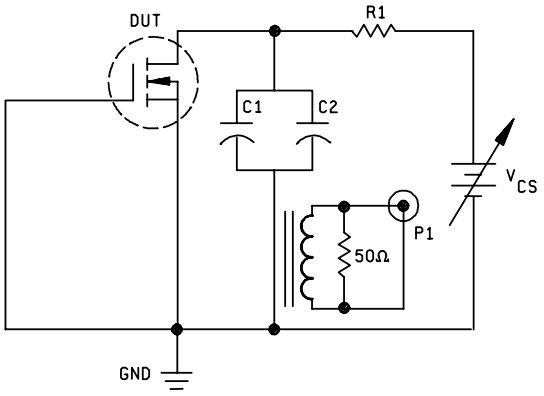


FIGURE 3478-1b. Gate bias configuration 2.



NOTES:

1. C1: Consists of several small capacitors (typically .1 μF).
2. C2: Consists of several large capacitors (typically 200 μF).
3. R1: Drain isolation resistor (typically > 1 kΩ).
4. R2: Gate filter resistor (typically 1 kΩ).
5. C3: Gate filter capacitance (typically 0.1 μF).
6. P1: Current probe (Pearson Model +11 or similar).

FIGURE 3478-1c. No gate bias configuration 3.

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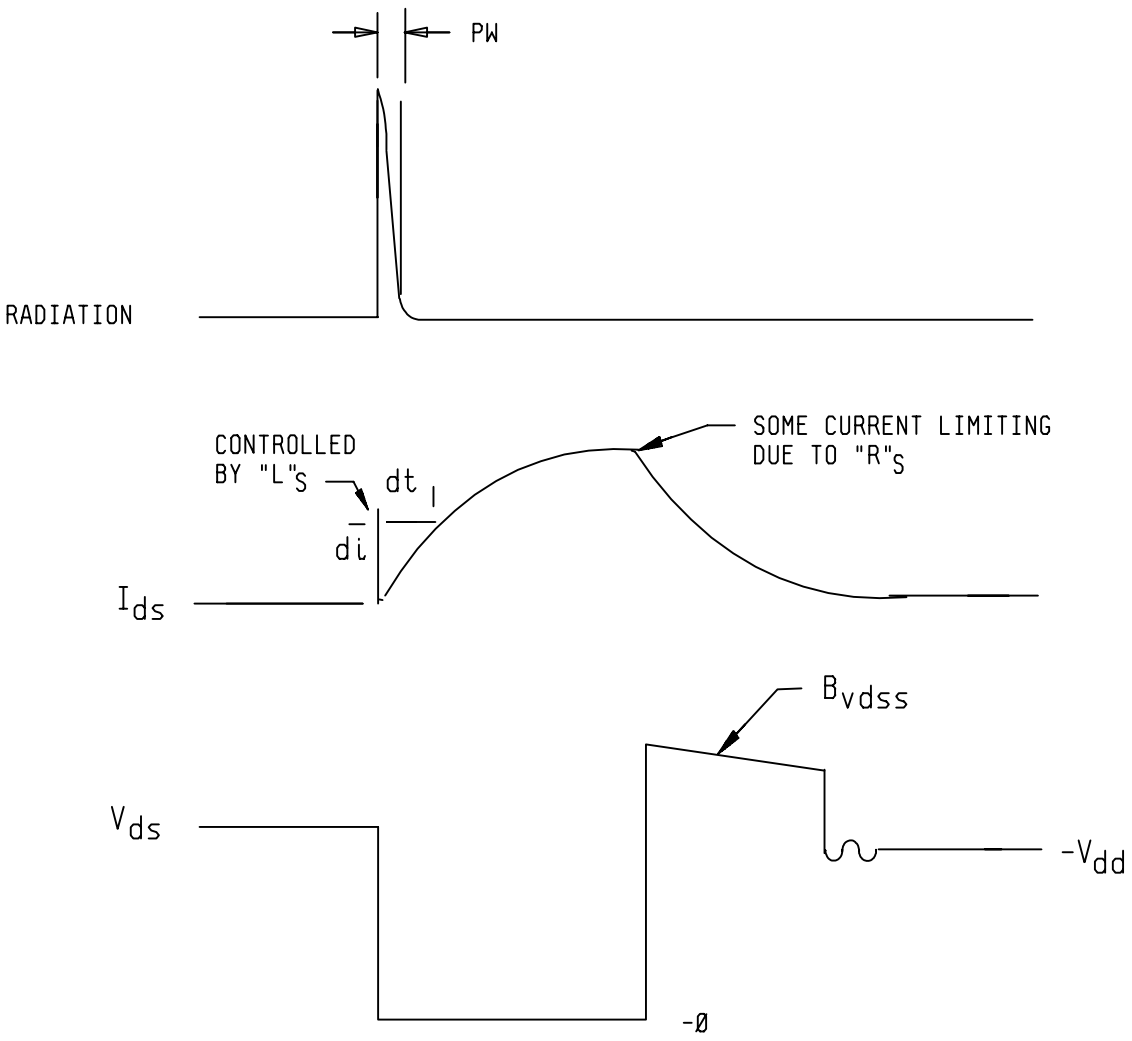

FIGURE 3478-2. Actual test waveforms.

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5. Procedure. Two essential requirements are outlined in this procedure that allow a meaningful analysis of a device's radiation response as compared to data obtained on a different test fixture.

a. In 5.1 through 5.7, the procedure to characterize power transistors to high gamma dose rate radiation and what data to collect and record are described.

b. In 5.8, there is a description for a technique to extract key electrical parameters, L_S and R_S, allowing the test fixture to be characterized using the above radiation data.

5.1 Sample size. A minimum of five samples per device type shall be tested to determine the dose rate response of each power transistor type. All devices shall meet the electrical specifications required for that particular device type before initial exposure.

5.2 Identification. In all cases, each test sample shall be individually marked to ensure that the test data can be traced to its corresponding test sample.

5.3 Radiation source.

a. The radiation source shall be either a flash x-ray or a LINAC.

b. The facility/source shall be capable of varying the dose rate levels to characterize the device's response to various dose rates.

c. The minimum pulse width shall be performed using a 20 to 50 ns pulse width (FWHM).

5.4 Dosimetry. Dosimetry shall be used to measure the actual dose in rad(Si) of the radiation pulse. Any dosimetry technique that meets ASTM standards (ASTM F526-77) may be used.

5.5 Waveform recording. The voltage, V_{ds}, and test current, I_{ds}, shall be monitored before, during, and after each irradiation. Voltage in excess of the maximum input voltage of the recording device shall be attenuated.

5.6 Test conditions. The DUT shall be biased with the specified test conditions and verified for each irradiation. Drain and gate current shall be monitored before, during, and after each exposure. The capacitive load across the drain/source shall maintain the drain bias voltage, V_{ds}, during the exposure within $\pm$10 percent of that specified. The test shall not be repeated until the stiffening capacitors have sufficiently recharged. All tests shall be performed at the required ambient temperature.

CAUTION: Some transistors may require a gate bias to turn the DUT off after the radiation event.

5.7 Test setup/sequence.

a. Tune LINAC/flash x-ray to desired pulse width and dose rates and perform initial beam dosimetry.

b. Install holding fixture and test system circuitry.

c. Insert DUT (precharacterized in accordance with applicable specification sheet).

d. Apply and verify test voltage to gate (V_{gs}).

e. Apply and verify test voltage to drain (V_{ds}).

f. Connect monitors to appropriate recorders.

g. Expose DUT to desired dose rate.

h. Record photocurrent (I_{ds}) and V_{ds} response.

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i. Record test information: Test conditions V_{ds} and V_{gs}; actual dose rate, accumulated total dose, date, and other information pertinent to test.

j. Verify survivability of test device: Check electrical parameters to determine any damage.

k. Repeat with new test conditions: Different V_{ds}, dose rate, or V_{gs}.

5.8 Determination of stray inductance/resistance. Knowing the stray components, L_s and R_s, will provide a technique to compare test data from different test fixtures and packages. L_s and R_s will limit the amount of current flow and the peak current observed by the DUT.

a. Using the recorded photocurrent waveforms, the quantitative values of the stray resistance, R_s, and inductance, L_s, can be extracted for that test fixture and package.

CAUTION. The stray fixture components may change with exposure to radiation, testing, or time.

b. Determine the inductance, L_s, from the relationship:

$$\left(\frac{di}{dt}\right) = \left(\frac{V_{ds}}{L_s}\right)$$

and

$$L_s = \frac{V_{ds}}{\left(\frac{di}{dt}\right)}$$

The calculated inductance will be influenced by the series resistance; and, therefore, the value of the di/dt response shall be based upon the change in primary photocurrent between its 0 percent to 10 percent response. The L_s value shall be determined from this experimental data.

c. Determine the resistance, R_s, from the relationship:

$$I_{ds} = \left(\frac{V_{ds}}{R_s}\right) * \left[1 - \left(\exp - \left((t * \frac{R_s}{L_s}\right)\right)\right]$$

The calculated resistance should be determined from the peak primary photocurrent response and its corresponding time. Using iterative calculations, R_s shall be determined within ±5 percent based upon this experimental data.

6. Documentation. Test records shall be maintained by the experimenter. Test records shall include the following:

a. Part type, item, and lot identification.

b. Date of test and operator's name.

c. Identification of radiation source and pulse width.

d. Description of test system and circuit.

e. Description of dosimetry techniques and circuits.

f. Test bias conditions.

g. Recorded voltage current waveforms.

h. Minimum dose rate V_{ds} to induce burnout.

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i. Maximum dose rate V_{ds} not to induce burnout.

j. Device leakage currents before and after irradiation.

k. Recorded waveforms of pulse shape intensity.

l. Accumulated total dose.

m. Ambient test temperature.

n. Calibration records and serial numbers, if required.

o. DC electrical measurements after radiation event.

6.1 Reporting. This documentation shall be used to prepare a summary describing the test system, data, results, and analysis. The summary shall include a description of the device, dc electrical parameters before and after testing, a statistic summary indicating the sample mean and standard deviation of each device type, plots of photocurrent versus dose rate at a specified V_{ds} and V_{gs}, calculations for stray L_s and R_s for the test fixture for each device type or package type, and a general synopsis of the test results.

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METHOD 3479

SHORT-CIRCUIT WITHSTAND TIME

1. Purpose. The purpose of this test finds out the length of time a device can survive a short-circuit condition. In some circuits, such as motor drives, it is necessary for a semiconductor device to withstand a short-circuit condition for short periods of time. During such a condition, the current in the device is dependent on the gain of the device and the level of the drive supplied. It is important for the designer to know how long a device can survive a short-circuit condition with a given drive level. Fault detect circuits can be designed to react within this time period. In some cases the junction temperature may exceed the maximum rating. If it does, the rating shall be nonrepetitive with a limit on the maximum number of events over the lifetime of the device. Otherwise, it will be a repetitive rating. In the case of a nonrepetitive rating, the manufacturer shall perform adequate reliability testing so as to ensure the validity of this rating. For performance specifications, the controlling document shall mandate such tests.

2. Scope. This test covers all power semiconductors or hybrids that can be turned off with a control terminal and which are intended for use as switching devices. Power MOSFETs, IGBTs, and bipolar transistors are examples of these devices.

3. Symbols and definitions. The following symbols and terminology shall apply for the purposes of this test method:

a. Drive: One of the following:

V_{DRIVE} = Nominal drive voltage (volts).

I_{DRIVE} = Nominal drive current (amperes).

This value must be maintained to within ±5 percent of the specified value. In a graphical representation, various levels of drive may be specified, as shown on figure 3479-3. The speed of turn-off shall be such that avalanching the DUT is prevented.

b. L_S: Stray inductance of the output circuit (see figure 3479-1) shall be kept as low as is practical. In order to verify this, the maximum value of L_S shall be a condition of the test called out on the applicable specification sheet of the device (see figure 3479-2). L_S = V dt/di during the first 10 percent of the output current waveform.

c. R_{DRIVE}: The output impedance of the drive circuitry.

d. T_j: Junction temperature (°C). Its starting value shall be specified, and controlled to five percent at the beginning of the test.

e. t_{sc}: Short-circuit withstand time (seconds). Measured between the time the device drive rises above 50 percent of its peak value and when it falls below 50 percent of its peak value.

f. V_{SC}: Nominal short-circuit voltage (volts). Shall be maintained between +5 percent and -10 percent of the specified value during the test.

4. Circuitry. Electrical test circuitry is as shown on figure 3479-1. Drive circuitry must be appropriate for the device being tested, whether voltage or current driven. Care must be taken to minimize stray inductance in the output circuit in order to avoid limiting the current during the test, or avalanching the device during turn-off at the end of the test.

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4.1 Procedure for measurement of short-circuit withstand time (see figure 3479-2).

a. t0: Apply test voltage.

b. t1: Apply drive signal.

c. t2: Device drive reaches 50 percent of maximum value.

d. t3: Remove drive signal.

e. t4: Device drive falls to 50 percent of maximum value.

f. t5: Remove test voltage.

5. Acceptance criteria. DC electrical test shall be conducted before and after the test. Exactly which parameters are to be measured will be device dependent, and shall be called out on the applicable specification sheet.

6. Specification. Tabular specification shall be as follows.

t_{SC} short-circuit withstand time	_____ μs at:
(1) V_{SC} short-circuit voltage	_____ V
(2) Drive voltage (or current)	_____ V (or A)
(3) T_j junction temperature	_____ °C
(4) R_{DRIVE} output impedance	_____ Ω
(5) L_S stray inductance	_____ nH

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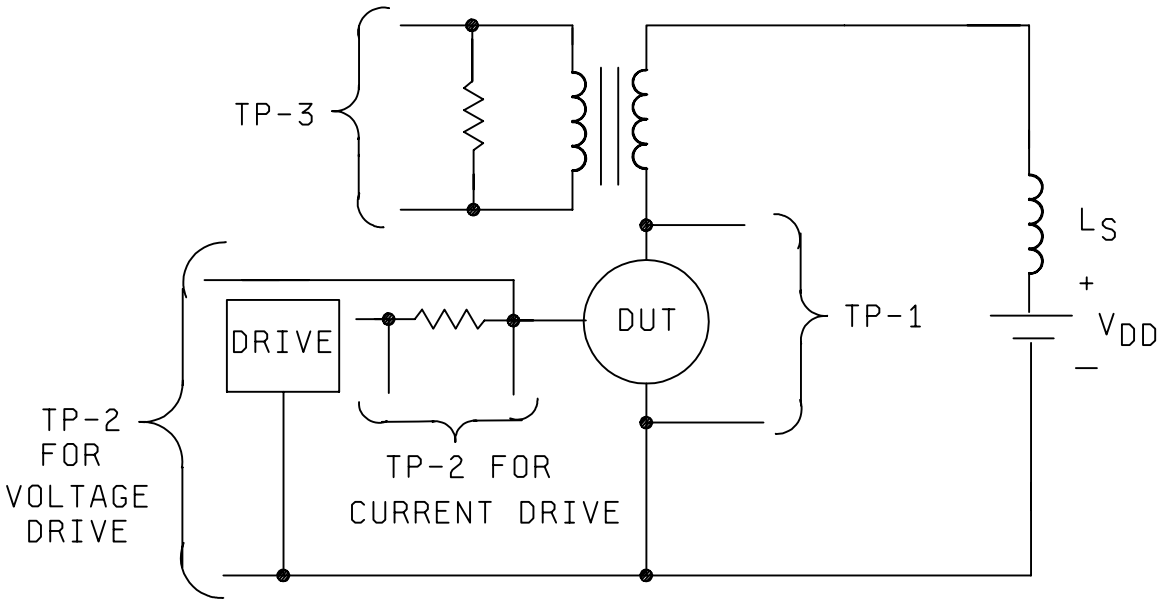

FIGURE 3479-1. Test circuit.

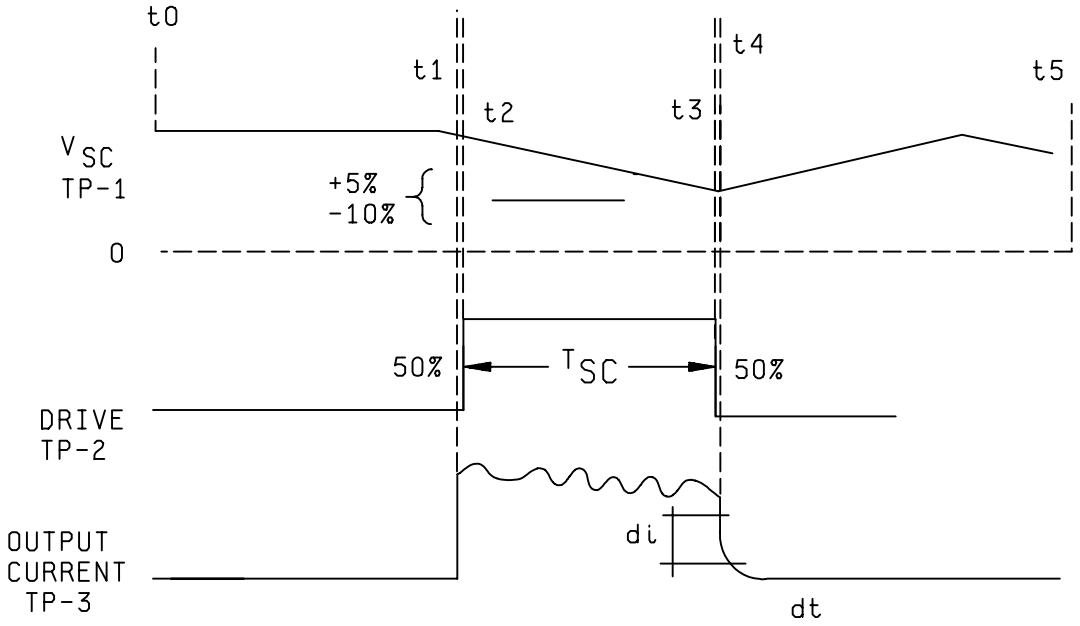

FIGURE 3479-2. Short-circuit withstand time waveform.

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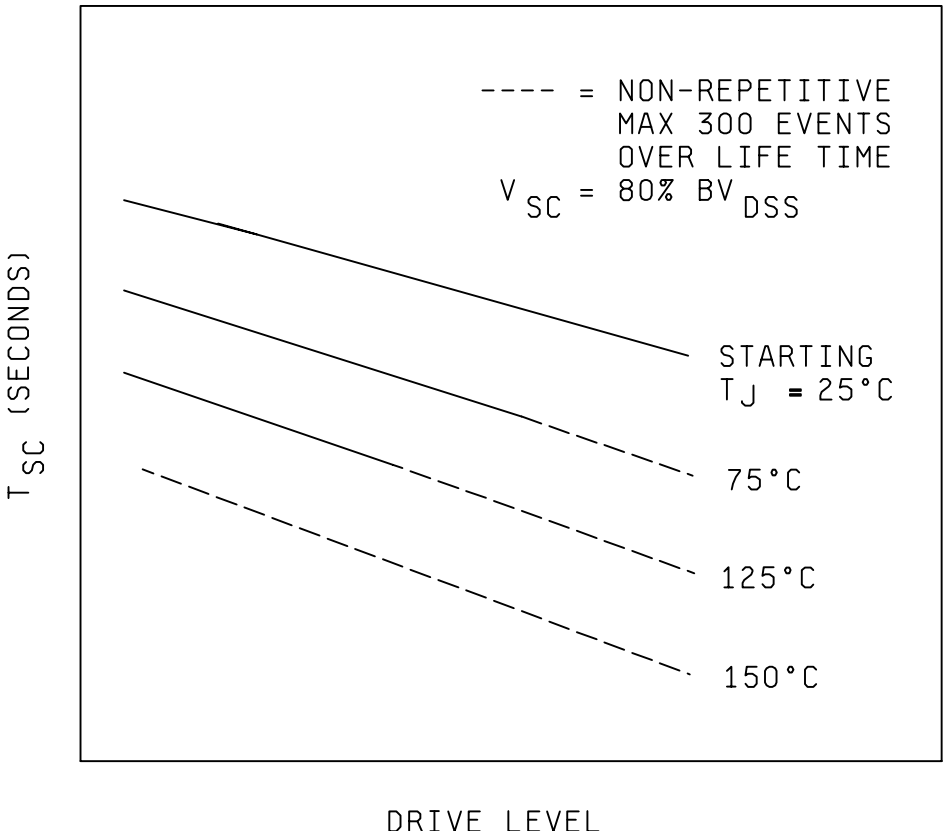

FIGURE 3479-3. Sample graphical specification.

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METHOD 3490

CLAMPED INDUCTIVE SWITCHING SAFE OPERATING AREA FOR MOS GATED POWER TRANSISTORS

1. Purpose. The purpose of this test is to define a method for verifying the inductive switching SOA for MOS gated power transistors and to assure devices are free from latch up.

2. Scope. This test includes all power MOSFETs and IGBTs used in switching applications for power supplies and motor controls.

3. Circuitry. As shown on figure 3490-1, a simple inductive load circuit is employed. Drive circuitry applies a voltage to the DUT to achieve a specified current. The turn-off dv/dt is controlled by a gate resistor. A clamping diode or suppression device is used to limit the maximum voltage which occurs during turn-off. The clamping device shall be located as close as possible to the DUT to minimize voltage spikes due to stray inductance L_S. For inductive load waveform see 3490-2.

4. Symbols and definitions. The following symbols and terminology shall apply for the purposes of this test method:

a. dv/dt: Change in voltage during turn-on and turn-off measured between 75 percent and 25 percent of total clamp voltage during turn-off.

b. I_L: Load current through inductor and DUT.

c. L: Series inductance.

d. L_S: Stray series inductance due to layout of circuit.

e. R_g: Resistor in series with the gate which is used to limit turn-off dv/dt during switching.

f. T_A: Ambient temperature (°C): Temperature used to heat the DUT.

g. T_C: Case temperature (°C): Temperature of the DUT as measured on the exterior of the package as close as possible to the die location.

h. T_J: Junction temperature (°C): Shall not exceed maximum rating of the DUT.

i. t_p: Pulse width between turn-on and turn-off of DUT.

J. V_{CC}: Collector supply voltage, dc.

K. V_{CES}: Collector to emitter voltage gate shorted to emitter.

l. V_{CF}: Clamping voltage.

m. V_{DM}: Maximum off-state voltage measure at the DUT which is caused by stray inductance between the DUT and the voltage suppressor. V_{DM} is due to L di/dt generated during turn-off.

n. V_{DSS}: Source-to-drain voltage gate shorted to source.

o. V_G: Drive voltage from a voltage source used to turn-on and turn-off the MOS DUT to achieve a specified current.

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5. Specification conditions. The following conditions shall be as specified in the applicable specification sheet.

   a. V_{CC}: V.

   b. V_{CF}: V.

   c. I_L: A.

   d. $T_C = T_A$: °C.

   e. L: mH.

   f. t_p: µs.

   g. dv/dt: V/µs minimum.

   h. N: Number of pulses.

6. Acceptance criteria.

   a. No degradation of blocking voltage at the end of test shall be permitted.

   b. Latch-up or reduction of I_L shall not be observed.

   c. DUT shall meet group A, subgroup 2 limits of the applicable specification.

7. Comments and recommendations.

   a. Gate resistor or gate drive source shall be as close as possible to the DUT to minimize oscillations during turn-off.

   b. Gate resistor valve or gate drive is selected to assure minimum peak dv/dt is achieved.

   c. V_{CF} clamping device should be as close as possible to the DUT to minimize voltage over shoot. A general guideline is V_{CF} should not exceed 110 percent of V_{DM} and shall be less than avalanche breakdown of DUT.

   d. L should be selected to assure peak current is reached. The I_C will not be reached if too large of an inductor is used.

   e. Safety precautions should be taken when testing high voltage devices and rules and regulations for handling high voltage devices should be followed.

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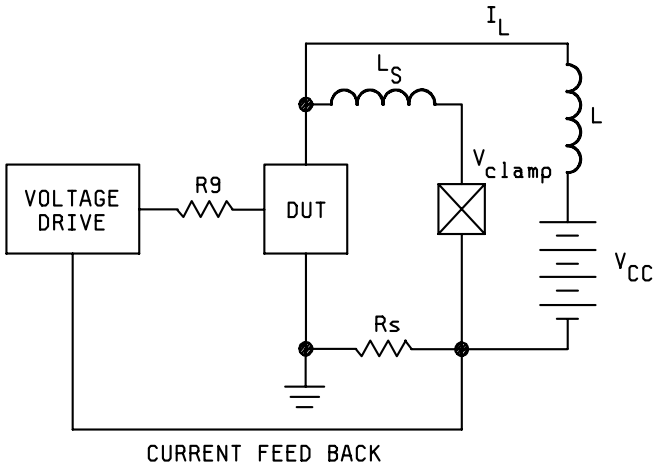
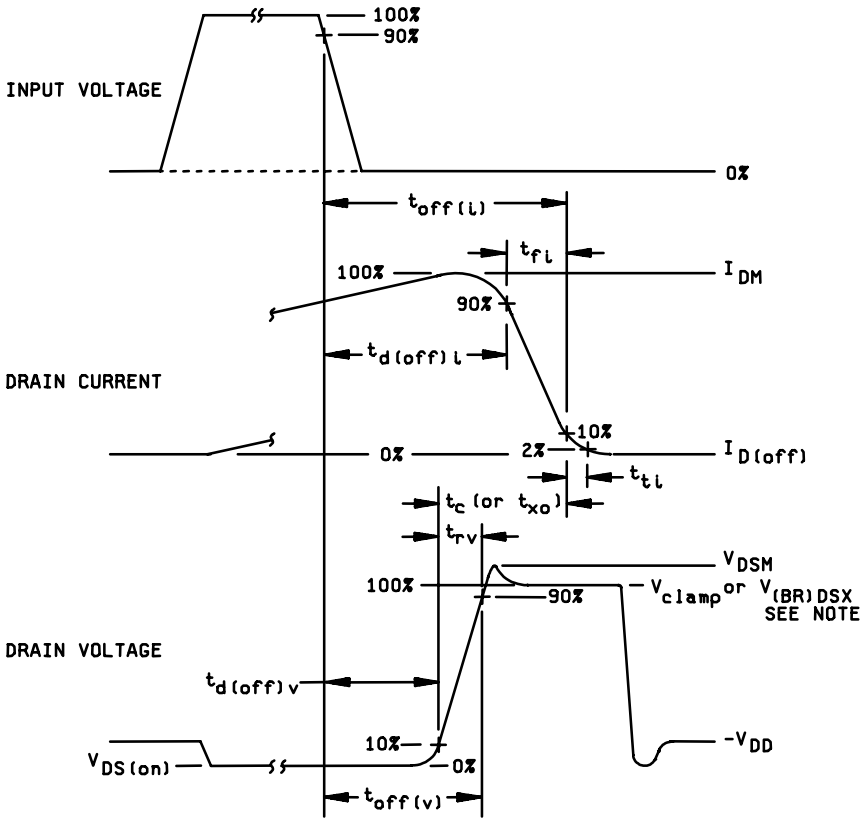


FIGURE 3490-1. Inductive load circuit.



NOTES:

1. V_{clamp} (in a clamped inductive-load switching circuit) or $V_{(BR)DSX}$ (in an unclamped circuit) is the peak off-state.
2. Drain and source references for MOSFETs are equivalent to collector and emitter references for IGBTs.

FIGURE 3490-2. Inductive load waveform.

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3500 Series

Electrical characteristics tests for Gallium Arsenide transistors

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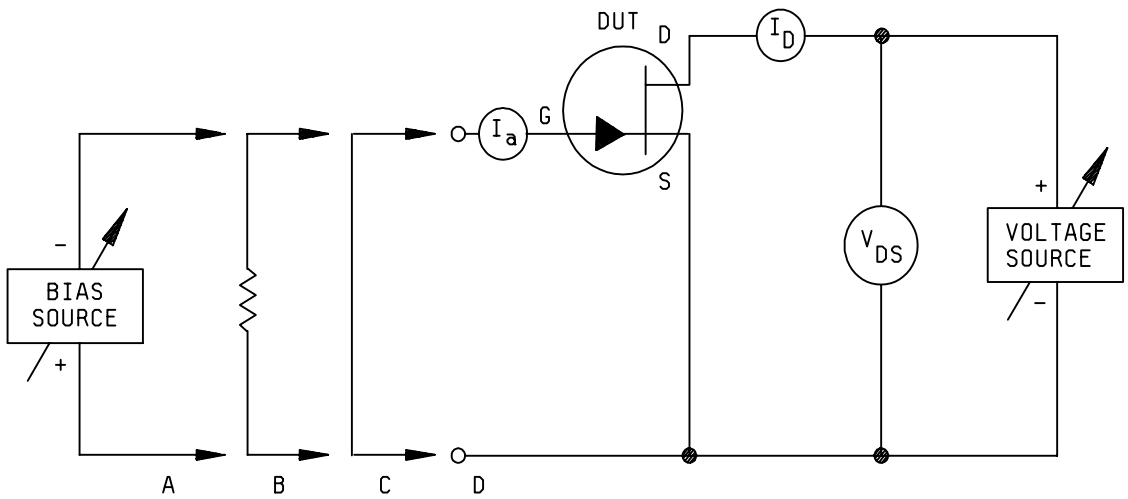
METHOD 3501

BREAKDOWN VOLTAGE, DRAIN-TO-SOURCE

1. Purpose. The purpose of this test is to determine if the breakdown voltage of the gallium arsenide field-effect transistor under the specified conditions is greater than the specified minimum limit.

2. Test circuit. See figure 3501-1.



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 3501-1. Test circuit.

3. Procedure. A negative (reverse) voltage shall be applied to the gate, with the specified bias condition (condition A) applied, then a positive voltage applied to the drain. The device is acceptable if the gate current is less than the maximum specified with the voltage bias conditions on the gate and drain as specified in the applicable specification sheet. 1/ With the specified gate and drain voltages, if the specified maximum gate current is exceeded, the device shall be considered a failure.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test current (see 3).

b. The bias condition is gate-to-source and drain-to-source - reverse bias (specify bias voltages).

1/ I_q Breakdown voltage as determined by maximum. Allowed gate current, with the specified bias condition applied from gate-to-source and drain-to-source.

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METHOD 3505

MAXIMUM AVAILABLE GAIN OF A GaAs Field effect transistor (FET)

1. Purpose. The purpose of this method establishes a basic test circuit for the purpose of determining the associated gain of a gallium arsenide field-effect transistor (FET).

2. Procedure. Configure the test setup as shown on figure 3505-1. First apply the gate voltage (V_{GS}) then apply the drain voltage (V_{DS}). Adjust the gate voltage so that the FET is biased at the specified operating point as noted in the applicable specification sheet, such as I_{DS} = 50 percent of I_{DSS}. Adjust the input and output tuners so that the transistor exhibits maximum output power and near maximum gain; that is, the transistor's gain must not be compressed more than 2 dB. The input power level is then reduced by at least 10 dB. At this reduced input signal level, the small signal gain is defined as G0.

Calculation:

G_{1dB} = G0 - 1.0 dB (associated gain at the 1 dB compression point).

The gain of the FET (output power/input power in dB) is recorded as the input power is increased in 1 dB increments. When the measured gain of the FET is less than or equal to G_{1dB}, as calculated above, the output power is recorded and this value represents the 1 dB compression point (P_{1dB}) power level and is used in determining the pass/fail status of the DUT in accordance with the value specified in the detail specification.

3. Test circuit. See figure 3505-1.

4. Summary. Unless otherwise specified in the applicable specification sheet, the following condition shall be as follows: T_C = (Temperature of case) = +25°C.

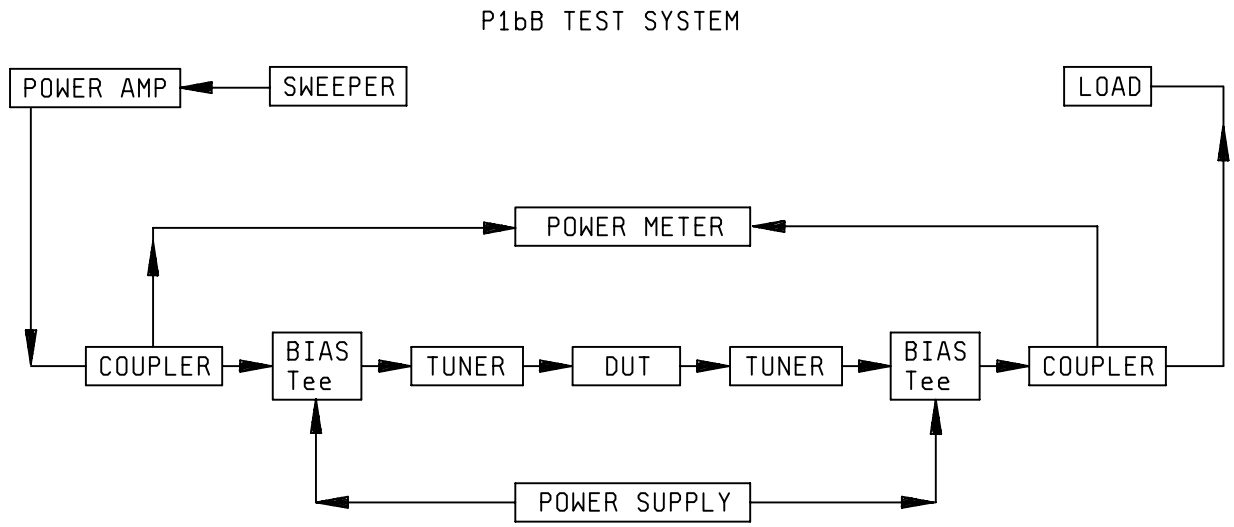

FIGURE 3505-1. Test circuit.

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METHOD 3510

1 dB COMPRESSION POINT OF A GaAs Field effect transistor (FET)

1. Purpose. The purpose of this method establishes a basic test circuit for the purpose of determining the 1 dB compression point of a gallium arsenide FET.

2. Procedure. Configure the test setup as shown on figure 3510-1. To prevent damage to the DUT, first apply the gate voltage (V_{GS}) then apply the drain voltage (V_{DS}). Adjust the gate voltage so the FET is biased at the specified operating point as noted in the applicable specification sheet, such as I_{DS} = 50 percent of I_{DSS}. Adjust the input power to the level and frequency given in the applicable specification sheet; adjust the input and output tuners so the transistor exhibits maximum output power while its gain remains within 2 dB of the manufacturer's specified minimum gain for the part and while the gate current remains within the range specified in the applicable specification sheet. The gate current shall also remain within the range specified in the applicable specification sheet. The input power level is then reduced by 10 dB or some greater amount specified in the applicable specification sheet. At this reduced input signal level, the small signal gain is defined as G0.

Calculation: G_{1dB} = G0 = 1.0 dB.

The gain of the FET (output power/input power in dB) is recorded as the input power is increased in increments of 1 dB decreasing to 0.25 dB, or smaller, as G_{1dB} is approached. When the gain of the FET is less than or equal to G_{1dB}, as calculated above, the output is recorded and this value represents the 1 dB compression point (P_{1dB}) and is used in determining the pass/fail status of the DUT in accordance with the value specified in the applicable specification sheet.

3. Test circuit. See figure 3510-1.

4. Summary. Unless otherwise specified in the applicable specification sheet, the following condition shall be as follows: (T_C) = (Temperature of case) = +25°C.

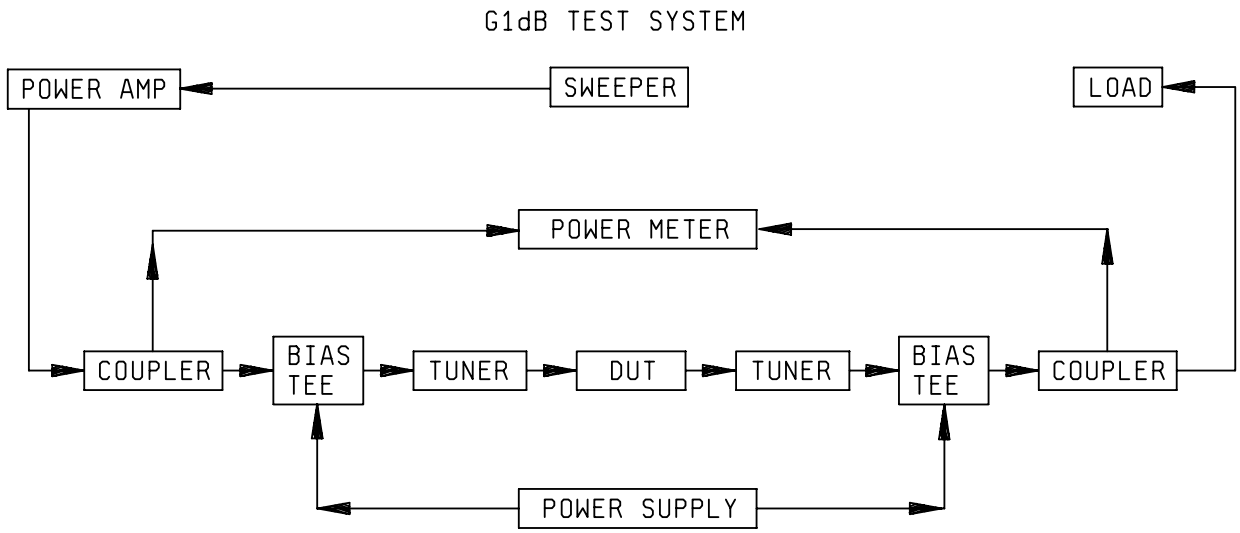

FIGURE 3510-1. Test system.

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METHOD 3570

GaAs Field-effect transistor (FET) FORWARD GAIN (Mag S21)

1. Purpose. The purpose of this method establishes a basic test method, test setup, and procedure for measuring the forward gain (magnitude of S21) of GaAs FETs.

2. Procedure. Configure and calibrate the test setup as shown on figure 3570-1. To prevent damage to the DUT, first apply the gate voltage (V_{GS}) and then apply the drain voltage (V_{DS}) to the bias levels specified in the applicable specification sheet. Adjust the gate voltage so that the DUT is biased at the specified operating point, such as I_{DS} = 50 percent of I_{DSS}. Record the DUTs magnitude of S21 (in dB) using the network analyzer as shown on figure 3570-1.

3. Test circuit. See figure 3570-1.

4. Summary. Unless otherwise specified in the applicable specification sheet, the following condition shall be as follows: (T_C) = (Temperature of case) = +25°C.

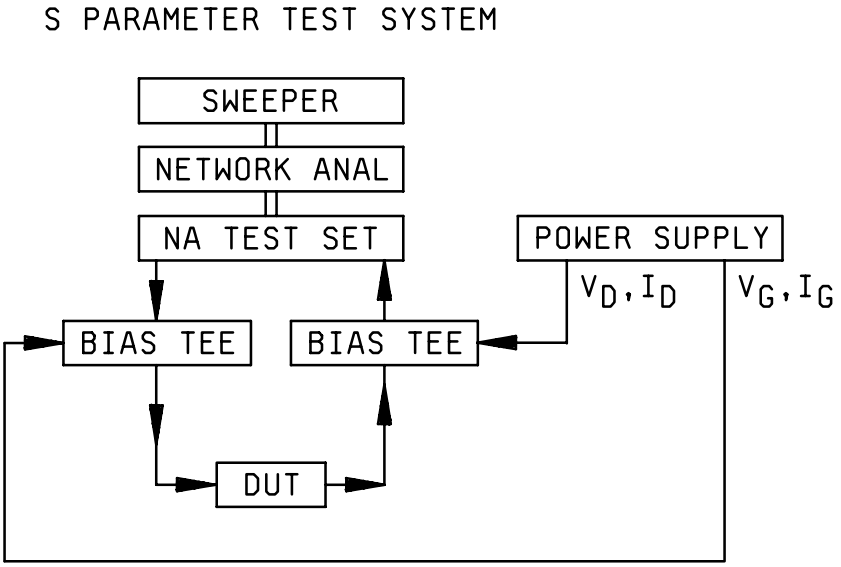

FIGURE 3570-1. Parameter test system.

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METHOD 3575

FORWARD TRANSCONDUCTANCE

1. Purpose. The purpose of this method establishes a basic test circuit for the purpose of establishing forward transconductance gm for gallium arsenide field-effect transistors.

2. Procedure. The gate-to-source voltage (V_{g1}) is applied as necessary to achieve the specified drain-to-source current (I_{DS1}). The gate-to-source voltage is reduced gradually or increased gradually by 0.050 volts (V_{g2}) and the drain-to-source current is measured (I_{DS2}). The transconductance (gm) is calculated using the following formula:

Calculation:

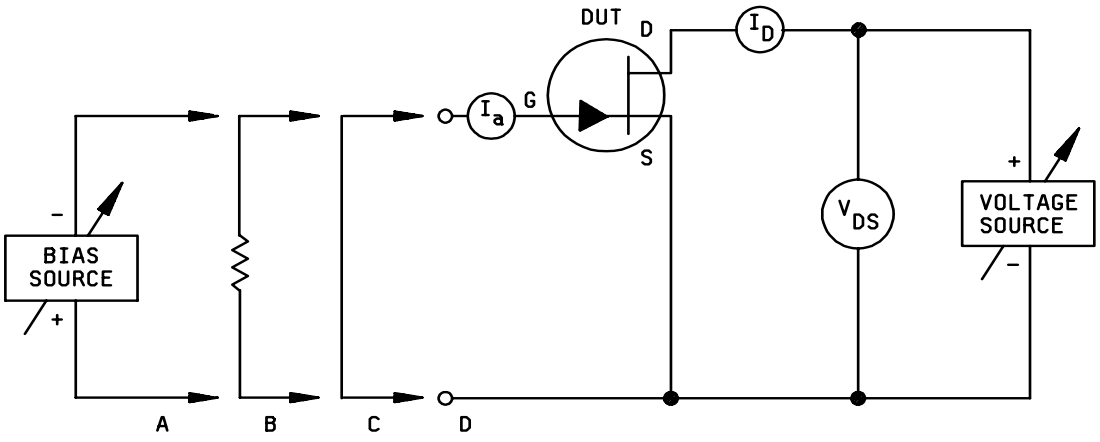
$$gm = \left| \frac{I_{d1} - I_{d2}}{0.050} \right|$$

3. Test circuit. See figure 3575-1.

4. Summary. Unless otherwise specified in the applicable specification sheet, the following conditions shall be as follows:

a. I_{D1} = 0.5 I_{DSS} ±10 percent I_{DSS}.

b. Unless otherwise specified, T_C = (temperature of case) = +25°C.



NOTE: The ammeter shall present essentially a short circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 3575-1. Forward transconductance circuit.

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4000 Series

Electrical characteristics test for diodes

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METHOD 4000

CONDITION FOR MEASUREMENT OF DIODE STATIC PARAMETERS

1. Purpose. The purpose of this test is for measuring a temperature-sensitive static parameter under conditions such that the product of the applied voltage and current at the test point produces a power dissipation level that will cause significant heating of the junction, the measured result may be subject to errors due to thermal or transient effects. In order to avoid such errors, the measurement should be made under defined conditions.

2. Steady-state dc measurements. When making measurements under conditions of steady-state dc, a condition of thermal equilibrium may be considered to have been achieved if halving the time between the application of power and the taking of the reading causes no error in the indicated results within the required accuracy of measurement. For these purposes very long pulses or step functions may be considered as steady-state dc. When appropriate, the mounting conditions (T_L or T_C) or the thermal resistance (reference point to ambient $R_{\theta CA}$ or $R_{\theta LA}$) shall be specified.

3. Pulse measurements. When a measurement is made under pulse conditions, the point of measurement after the start of the pulse shall be chosen such that it is long enough to charge interconnecting test cable capacitance, avoid electrical transient effects, and short enough to avoid heating effects. This can be ensured if halving the minimum selected time, or doubling the maximum selected time, will not produce errors beyond the defined accuracy of the measurement. The pulse measurement may be intended to correlate to a steady-state dc measurement, provided that a correlation has been established.

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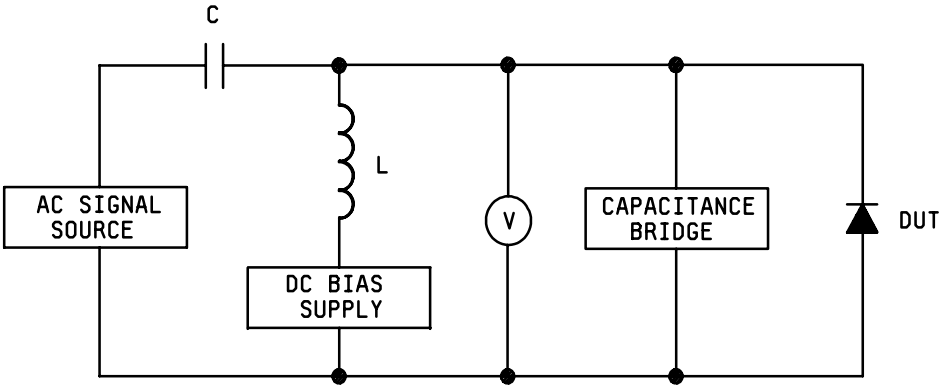
METHOD 4001.1

CAPACITANCE

1. Purpose. The purpose of this test is to measure the capacitance across the device terminals under specified dc bias and ac signal voltages.

2. Test circuit. See figure 4001-1.



NOTE: Both dc bias and ac signal sources may be incorporated in the capacitance bridge. The dc bias source should be properly isolated, preferably with an inductance L in series and have negligible capacitance compared to the DUT. The reactance of C must be negligible compared to the reactance of the DUT, at the frequency of measurement. Impedance of voltmeter should be at least 10 times that of the DUT.

FIGURE 4001-1. Test circuit for capacitance.

3. Procedure. The dc voltage source shall be adjusted to the specified bias voltage. The ac small signal voltage shall be adjusted to the specified frequency for the capacitance measurement. The bridge shall be nulled and adjusted for zero capacitance reading just prior to insertion of the DUT to eliminate error from external circuitry.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. DC bias voltage.

b. Test frequency.

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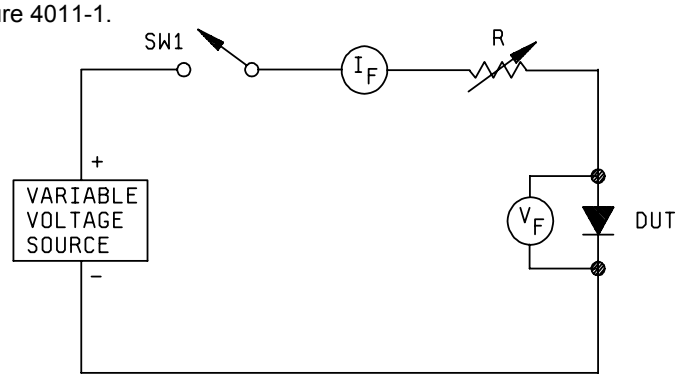
METHOD 4011.4

FORWARD VOLTAGE

1. Purpose. The purpose of this test is to measure the voltage across the device when a specified current flows through the device in the forward direction.

2. Test circuit. See figure 4011-1.



NOTE: When specified, switch SW1 shall consist of either an electronic switch or a pulse generator to provide pulses of short-duty cycle to minimize device heating. When pulse techniques are used, suitable peak-reading methods shall be used to measure the parameters of pulse amplitude, frequency, duty cycle, and pulse width. When dc techniques are used, device thermal equilibrium shall be achieved before the measurement is made.

FIGURE 4011-1. Test circuit for forward voltage.

3. Procedure.

3.1 DC method. The specified test current (I_F) shall be adjusted by varying either the variable voltage source or the resistor (R). The value of I_F shall be measured using an ammeter. The forward voltage (V_F) shall be measured using a dc voltmeter. The voltmeter connections shall be made at specified points on the device and always within the current connection points.

3.2 Pulse method. An oscilloscope shall be used to measure the pulse characteristics. The pulse generator or electronic switch shall be adjusted to achieve the specified amplitude, frequency, and pulse width values. Device current (I_F) may be determined by measuring the voltage drop across a known value of resistor (R) where:

$$I_F = \frac{V\ peak\ X\ duty\ cycle}{R}$$

After adjusting pulse level to correct value for required I_F, measure forward voltage V_F.

3.3 Curve tracer method. A Tektronix Model 576 or equivalent curve tracer shall be used. The device shall be tested by applying a positive voltage to the anode and limiting the current to within the manufacturer's ratings for I_F. The forward voltage may be determined by observing the curve tracer waveform at the specified I_F.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. Test current (I_F).

b. Forward voltage (V_F).

c. Duty cycle and pulse width, when pulse techniques are used.

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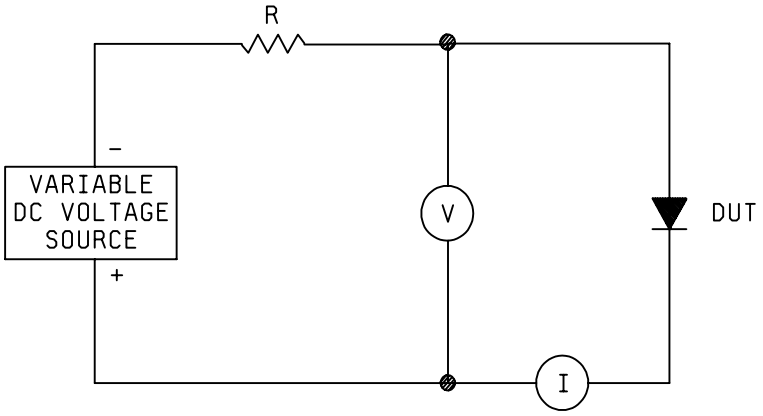
METHOD 4016.4

REVERSE CURRENT LEAKAGE

1. Purpose. The purpose of this test is to measure the reverse current leakage through a device at a specified reverse voltage using a dc method or an ac method, as applicable.

2. DC method.

2.1 Test circuit. See figure 4016-1.



NOTE: To assure accurate measurement of reverse leakage current, the voltage drop across the ammeter shall be subtracted from the measured value of reverse voltage. Resistor (R) shall be chosen to limit the current flow in the event the device goes into reverse breakdown.

FIGURE 4016-1. Test circuit for reverse current leakage (dc method).

2.2 Procedure.

2.2.1 Reverse current. The dc voltage shall be adjusted to the specified value by voltmeter (V) and the reverse current (I_R) shall be measured by current meter (I).

3. AC method.

3.1 Test circuit. See figure 4016-2.

*NOTE: The resistor R is a selectable value within the curve tracer.

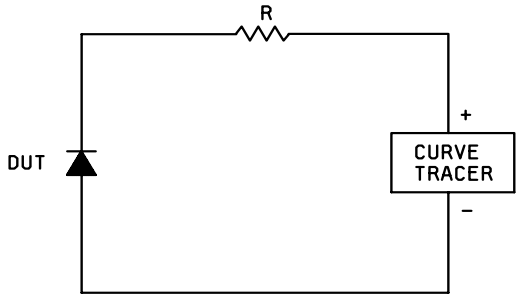


FIGURE 4016-2. Test circuit for reverse current leakage (ac method).

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3.2 Procedure.

3.2.1 Reverse current. A Tektronix 576-curve tracer or equivalent shall be used to apply voltage in the reverse direction only. The curve tracer supply shall be adjusted to obtain the specified peak reverse voltage across the device. Current and voltage shall be measured on the curve tracer.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. DC or ac method.

b. Test voltage (dc method) or peak reverse voltage (ac method).

c. Thermal resistance of minimum heat dissipater on which device is mounted in °C/W (where applicable).

d. Thermal equilibrium or pulse condition such as specified in EIA-320-A. (If pulse test is not specified, thermal equilibrium dc test method correlation will be applicable. This may include pulse measurement intended to correlate to steady-state dc measurement as described in EIA-320-A.)

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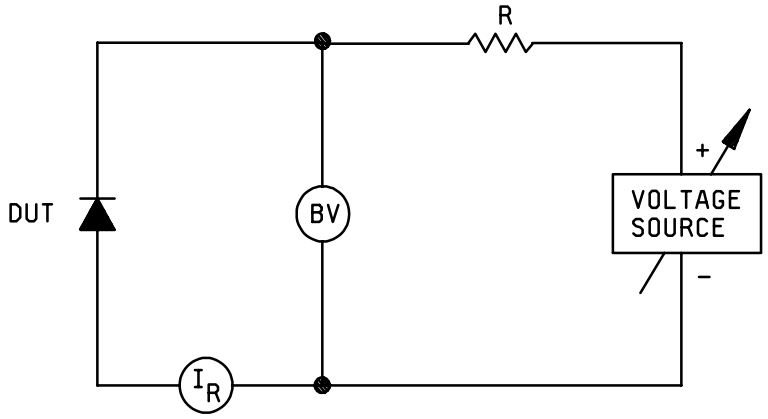
METHOD 4021.2

BREAKDOWN VOLTAGE (DIODES)

1. Purpose. The purpose of this test is to determine if the breakdown voltage of the device is greater than the specified minimum limit.

2. Test circuit. The resistance R is a current-limiting resistance and is chosen to avoid excessive current flowing through the device. (See figure 4021-1.)



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 4021-1. Test circuit for breakdown voltage (diodes).

3. Procedure. The reverse current shall be adjusted from zero until either the minimum limit for breakdown voltage or the specified test current is reached. The device is acceptable if the specified minimum limit for BV is reached before the test current reaches the specified value. If the specified test current is reached first, the device is rejected.

4. Summary. The test current (see 3.) shall be specified in the applicable specification sheet.

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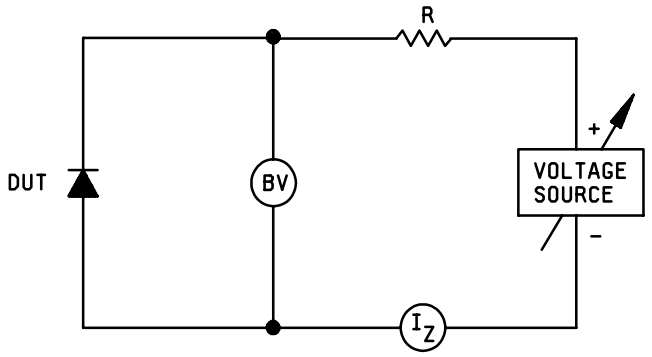
METHOD 4022

BREAKDOWN VOLTAGE
(VOLTAGE REGULATORS AND VOLTAGE-REFERENCE DIODES)

1. Purpose. This test is designed to measure the breakdown voltage of voltage regulator and voltage-reference devices under the specified conditions.

2. Test circuit. See figure 4022-1.



NOTE: The voltmeter being used to measure the terminal voltage should present an open circuit to the terminals across which the voltage is being measured.

FIGURE 4022-1. Test circuit for breakdown voltage (voltage regulators and voltage-reference diodes).

3. Procedure. The reverse current shall be adjusted from zero until the specified test current is reached. The specified test current shall remain applied for the specified time to approach thermal equilibrium with the device mounted as specified in the individual specification sheet. The breakdown voltage shall then be read from the voltmeter.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. Test current (see 3.).

b. Time after application of test current when breakdown voltage shall be read.

c. Method of mounting.

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METHOD 4023.2

SCOPE DISPLAY

1. Purpose. The purpose of this test is to define criteria for inspection of the dynamic reverse characteristics of rectifiers, switching, and zener diodes when viewed on a curve tracer. This inspection criteria may not be applicable to specific rectifier designs where the device is not intended to be driven into avalanche breakdown, or where the applicable specification sheet has not provided for this inspection.

2. Scope.

   a. This test applies to all devices requiring stable or sharp and stable breakdown characteristics. NOTE: Since low voltage zeners do not inherently have, and some other devices may not have a sharp breakdown, specific exceptions in requirements are also provided herein. For ideal reverse see figure 4023-1. For soft knee see 4023-2. For drift see 4023-3.

   b. For condition A, stable (only) types, figures 4023-3, 4023-7, 4023-9, and 4023-10 shall apply.

   c. For condition B, sharp and stable types, figures 4023-2 through 4023-11 shall apply. The ideal sharp and stable trace is one which exhibits a single horizontal line up to the point of breakdown, then transitions vertically to form a 90 degree angle while maintaining the single line (see figure 4023-1). Deviations from this ideal, which are not specifically allowed in this method or applicable specification sheet shall be cause for rejection of the DUT. The following depictions (figures 4023-2 through 4023-11) have been compiled to describe commonly observed faults. Tolerances from acceptable devices have been assigned when applicable.

3. Procedures

   a. The curve tracer presentation shall be configured so that the horizontal axis shall be calibrated in volts per division and the vertical axis shall be calibrated in amperes per division (or fractions thereof). The vertical and horizontal axis of the curve tracer presentation will be graduated into eight or ten divisions, each representing a precalibrated increment of current or voltage.

   b. A series load resistor shall be used to limit the device reverse current and prevent device damage. This typical resistance should be approximately one quarter or more of the device resistance at the breakdown specification, when the curve trace set-up permits. Example: A device to be observed at I_{BR} of 100 μA which is specified to be 400 volts minimum, would have a series resistance chosen according to the following:

      $R \geq 0.25\ (400 / 0.0001)$, therefore:
      $R \geq 1\ M\Omega$

      The curve tracer peak voltage (V_{CT}) may also require limitation, particularly if the series load resistance described cannot be achieved. See figure 4023-1 and 3.e. for typical load line relationships to assure safe reverse current monitoring.

      *Unless otherwise specified, the breakdown current shall be the current used for the breakdown voltage test.

   c. The trace should occur in the first and third quadrant of the display and be slowly adjusted from zero volts to attain the specified current with the maximum amount of resolution for determination of trace characteristics. 8-9

* d. The DUT shall be held under breakdown conditions for at least two second to ensure freedom from intermittent instability for breakdown drift. NOTE: All figures herein are shown in the first quadrant.

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e. The vertical and horizontal sensitivity shall be adjusted on the curve tracer to provide a rendition of the complete trace to the specified current. Horizontal and vertical sensitivity shall be adjusted to provide a trace occupying no less than 50 percent of the available screen.

f. The curve trace voltage shall not be simply set at a predetermined value and snapped on instantaneously. This may be done only if the product to be tested is known to have a sufficiently narrow breakdown voltage (V_{BR}) range with a predetermined series (load line) resistor setting (see b.) and described below, to assure that the device will not be overpowered. This is typically the case for zener diodes prescreened on V_Z (or V_{BR}). The peak open circuit supply voltage of the curve tracer (V_{CT}) may then be adjusted such that the V_{CT} setting can provide no more current (I_{BR} or I_Z) than that required for avalanche breakdown, taking into account the series load resistance R in figure 4023-1. Unless otherwise specified, these relationships may be calculated by:

$$I_{BR} = \frac{V_{CT} - V_{BR}}{R}, \text{ and } V_{CT} = I_{BR}R + V_{BR}$$

The resistance R may be determined by:

$$R = \frac{V_{CT} - V_{BR}}{I_{BR}}$$

The V_{BR} (or V_Z) utilized in this equation should be the minimum expected so as to always maximize the R value selected.

g. Allowance for deviation from the desired characteristics described in this method or applicable specification sheet shall be granted by the qualifying activity. If a particular rejectable trace described is expected in a manufacturer's normal process, it shall be identified and explained during device conformance/ qualification. Devices exhibiting the exceptional trace characteristic shall be present in the conformance/qualification lot to establish reliability.

h. Any device that is stable and passes the applicable illustrated scope conditions shall be passed. Any device that exceeds the conditions in the applicable illustrate scope conditions will be failed. Any device that passes but is continuing to move, drift or otherwise change shall be observed for another 2 seconds. This cycle of 2 second intervals will continue until the part stabilizes and passes by still meeting the pass criteria or fails by exceeding the pass criteria. Any device that is still drifting after a total of 10 seconds shall be failed as being chronically unstable.

4. Summary. The following shall be specified in the applicable specification sheet. Test condition to be used.

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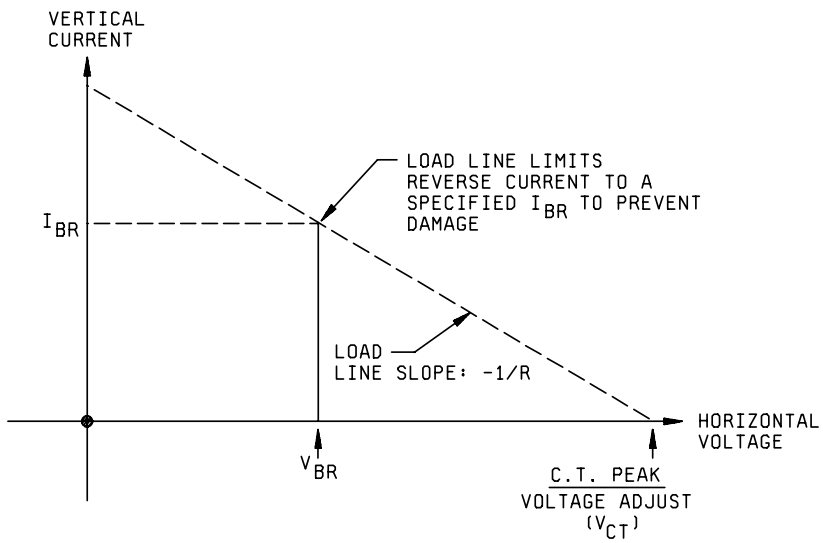
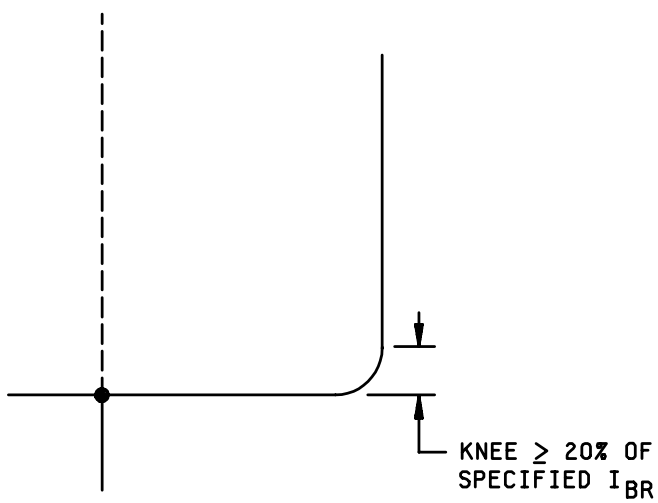


This ideal trace exhibits none of the characteristics described on the figures below. Also, illustrated are the basic curve tracer adjustments and relation for a safe maximum operating current (I_{BR}) with the series load resistor (R) versus peak open circuit voltage (V_{CT}) and device breakdown voltage (V_{BR}).

FIGURE 4023-1. Ideal reverse.



The knee area is the area in which the trace transitions from the horizontal to the vertical. Unless otherwise specified, this area should not require more than 10 percent of the total horizontal voltage component being viewed, or more than 20 percent of the specified I_{BR}. Not applicable to signal diodes, low voltage zeners, fast, ultrafast, and Schottky rectifiers or low voltage zeners ≤ 10 volts.

FIGURE 4023-2. Soft knee.

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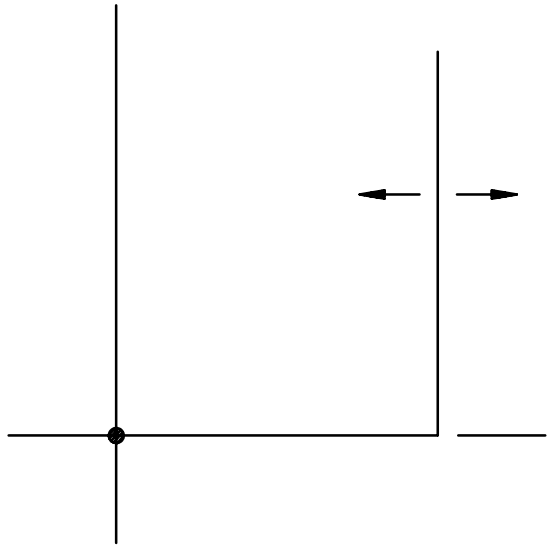
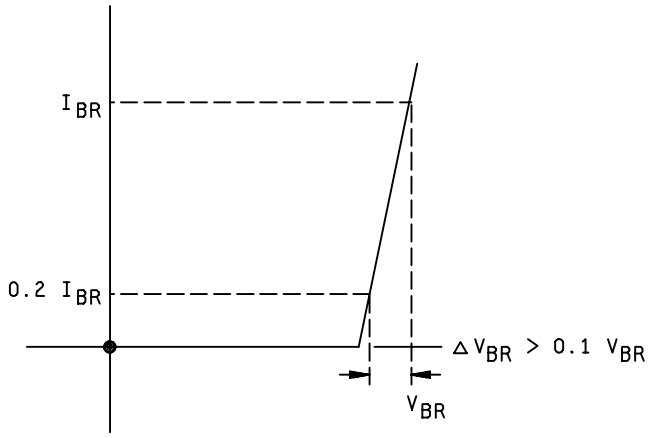


The vertical component of the trace should remain stable in the horizontal axis. An undesirable drift is defined as greater than a 10 percent increase or 2 percent decrease in actual breakdown voltage up to 1,500 volts. If over 1,500 volts, the allowable drift should be separately specified.

FIGURE 4023-3. Drift.



The slope shall be less than 10 percent of V_{BR} when viewed between 20 percent to 100 percent of the specified I_{BR} or I_Z. Low voltage zeners below 5.5 volts are in exception to this requirement also, or other devices, as may be specified.

FIGURE 4023-4. Slope.

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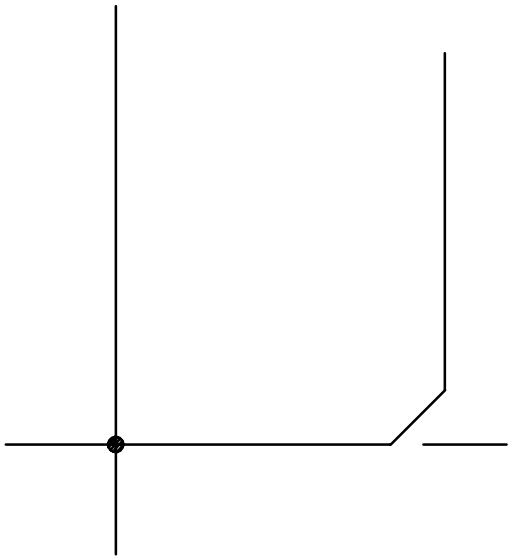
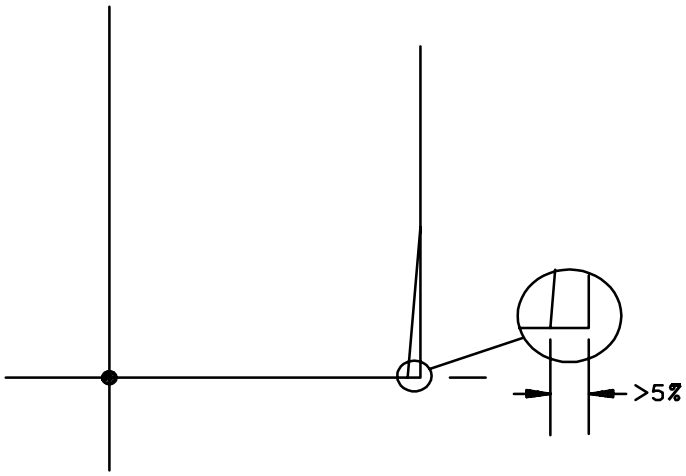


The double break is the area in which the trace transitions from the horizontal to the vertical. Unless otherwise specified, this area should not occupy more than 10 percent of the total horizontal voltage component being viewed, or more than 20 percent of the specified I_{BR} or I_{ZT}. This requirement is not applicable to ultrafast or Schottky rectifiers, and low voltage zeners ≤ 10 volts.

FIGURE 4023-5. Double break (reject criteria for sharp knee devices).



For standard rectifiers and zeners, the region at the knee may display a secondary trace no more than 5 percent of the total voltage of the DUT (see detail).

FIGURE 4023-6. Double trace.

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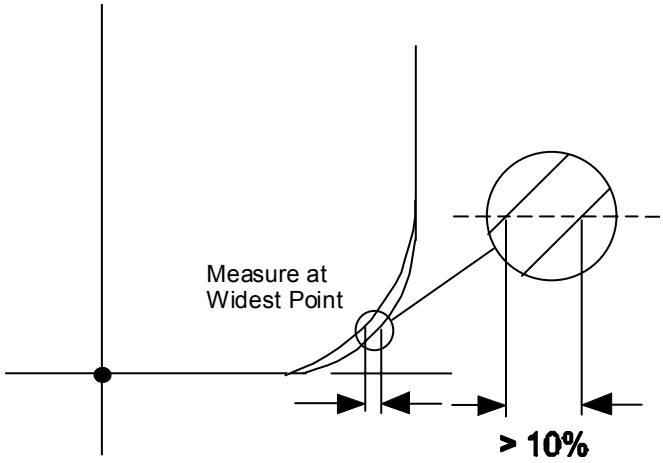
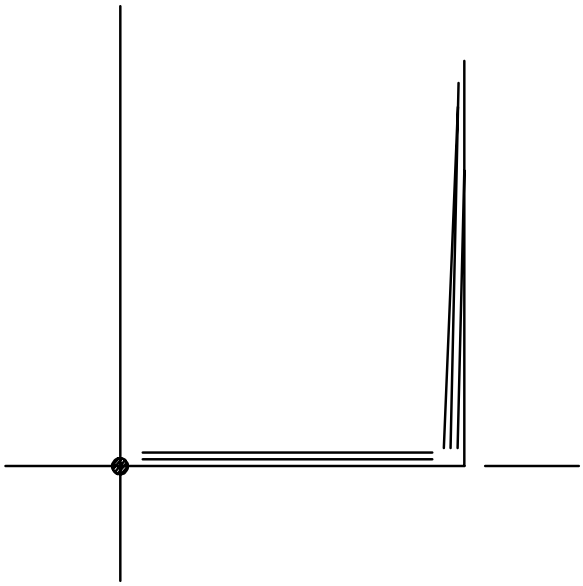


For soft knee diodes including signal diodes, low voltage zeners, and altered junction fast, superfast and ultrafast rectifiers, the region at the knee may display a secondary trace no more than 10 percent of the total voltage of the DUT (see detail).

FIGURE 4023-6b. Double trace, Soft knee.



Any jittery movement of the trace in any direction, not caused by power line voltage fluctuations, shall not occur.

FIGURE 4023-7. Unstable (jitter).

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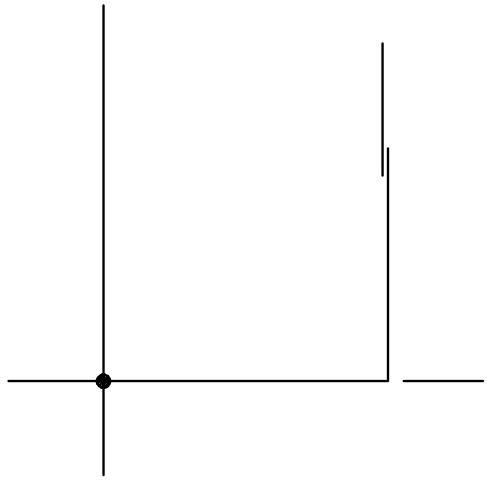
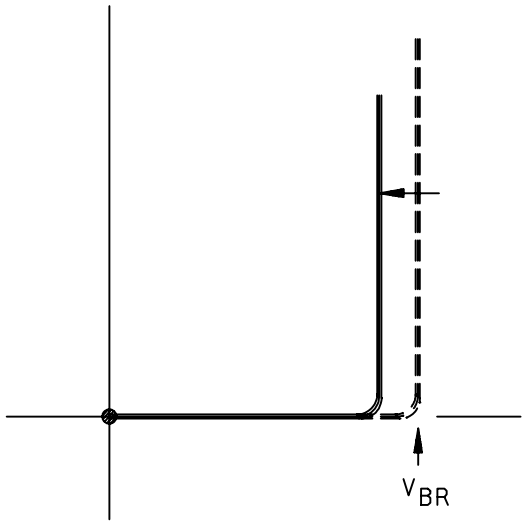


The vertical component shall not depart from a single vertical line, except as allowed on figures 4023-5 and 4023-6.

FIGURE 4023-8. Discontinuity.



The vertical component shall not decrease its value abruptly by 2 percent or more of V_{BR}.

FIGURE 4023-9. Snap back - collapsing V_{BR}.

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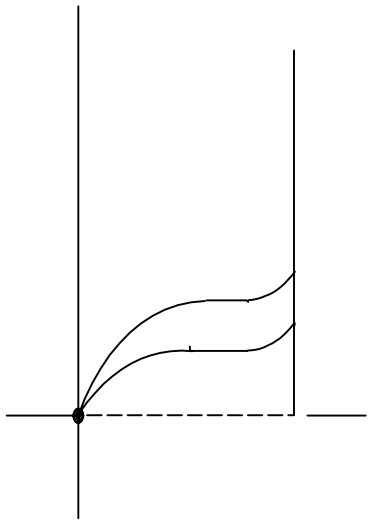
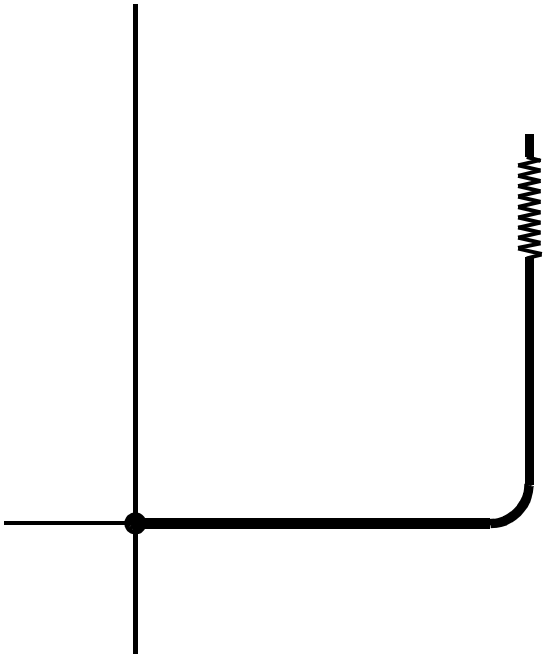


Leakage current (vertical) shall not degrade from an initial value.

FIGURE 4023-10. Floater.



Instability (arcing) appearing at or near the specified I_{BR} region on the vertical trace (such as may be coincident with visible sparking activity within the device die region) shall not be present. Noise at or near the knee is permissible, such as typically observed on avalanche-zener devices.

FIGURE 4023-11. Arcing.

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METHOD 4026.3

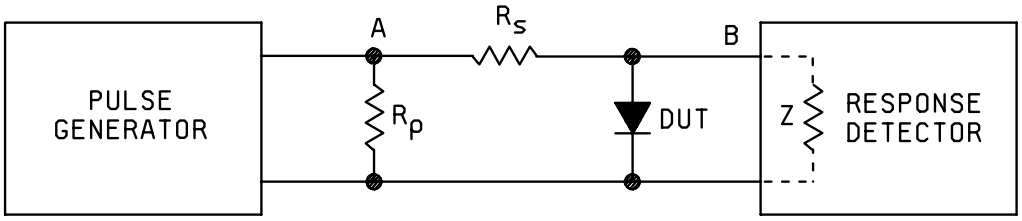
FORWARD RECOVERY VOLTAGE AND TIME

1. Purpose. The purpose of this test is intended to measure the forward voltage and recovery time of the device. A device reveals an excessive transient forward voltage when it is switched rapidly into the forward conductance region. The amplitude and time duration of this voltage peak can be measured by observing the voltage waveform across the device when a flat-top pulse of the specified amplitude, rise time, pulse width, and frequency are applied to the device.

2. Test circuit. See figure 4026-1.

a. The forward transient test circuit shown on figure 4026-1 is used in conjunction with a pulse generator and an output sensing device. Care should be taken to minimize lead length where lead inductance might cause ringing in the test circuit.

b. The value of resistor R_p shall be chosen to optimize the impedance match between pulse generator and test circuit, thereby minimizing the ringing in the test circuit.



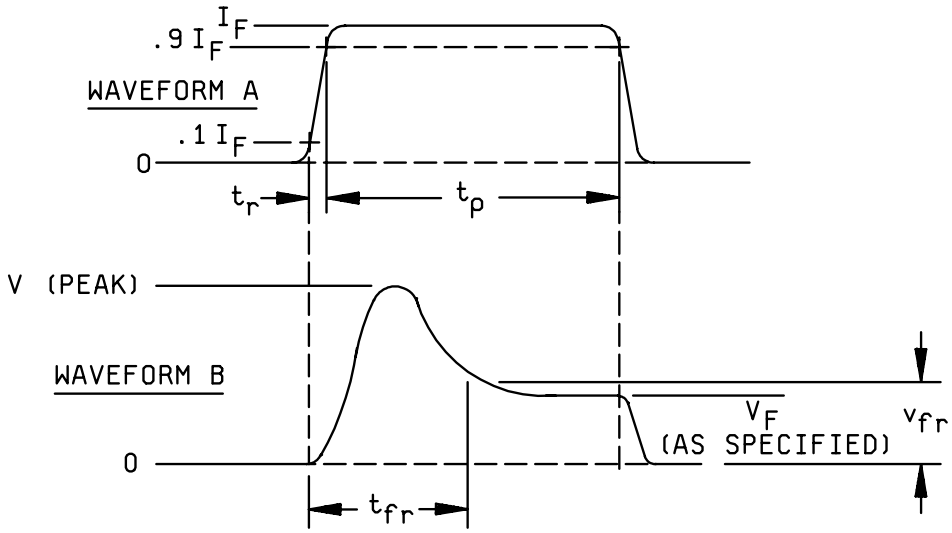


FIGURE 4026-1. Test circuit for forward recovery voltage and time.

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3. Procedure. The test shall be performed using the following:

3.1 Conditions:

a. Pulse input A:

(1) I_F amplitude: As specified.

(2) Rise time = 10 ns or as specified.

(3) Pulse width $t_1 \geq 10X$ specified response time.

(4) Generator resistance $R_S \geq 20$ RF ($R_F = V_F/I_F$ at specified IF).

(5) Pulse frequency shall be such that a reduction in frequency shall result in no change in forward recovery characteristics.

b. Response detector input impedance, $Z \geq 100\ R_F$.

4. Summary. The following conditions shall be specified in the applicable specification sheet.

a. I_F of input waveform A (see 3.1).

b. Rise time if other than 10 nanoseconds (see 3.1).

c. Forward recovery voltage $V_{(peak)}$ chosen to terminate the forward recovery time measurement (see figure 4026-1).

d. The following measurements should be made: Forward recovery time (t_{fr}) (measured from the time forward voltage becomes positive to the time that forward voltage recovers to a specified v_{fr}) (see figure 4026-1).

e. The peak forward voltage $V_{(peak)}$ (see figure 4026-1). This symbol is interchangeable with V_{FM}.

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METHOD 4031.4

REVERSE RECOVERY CHARACTERISTICS

1. Purpose. The purpose of this test is to measure the reverse recovery time and other specified recovery characteristics related to signal, switching, and rectifier diodes by observing the reverse transient current versus time when switching from a specified forward current to a reverse biased state in a specified manner.

2. General guide for selecting appropriate condition. Four conditions are given to include recommended practice for the range of diodes considered. A general guide for selecting the appropriate condition letter is:

a. Signal diodes with reverse recovery time less than 6 ns.

b. Low to medium current rectifiers with maximum specified recovery times of 50 to 3,000 ns.

c. High current rectifiers with maximum specified recovery times of 350 ns or greater.

d. Ultra-fast rectifiers, particularly on new specification sheets.

Further, detailed guidance is given under each condition below.

3. Test condition A. This condition is particularly relevant to low current, signal diodes faster than 6 ns and tested at 10 mA. However, it is practicable for measurements up to 20 ns and 100 mA.

3.1 Circuit notes for condition A.

a. Rise time of the reverse voltage pulse across a noninductive calibration resistor in place of the DUT shall be less than 20 percent of the recovery time of the DUT, for greatest accuracy.

b. Oscilloscope rise time shall be less than 20 percent of device recovery time, for greatest accuracy.

c. Proper coaxial networks and terminations shall be employed to ensure against error-producing pulse reflections.

d. $R > 10\ R_L$.

e. Unless otherwise specified, $R_L = Z_{PG} + Z_{SCOPE} = 100\ \Omega$.

f. $C > 10\ PW \div R_L$.

g. PW > 2 x maximum specified t_{rr} (see figure 4031-1.)

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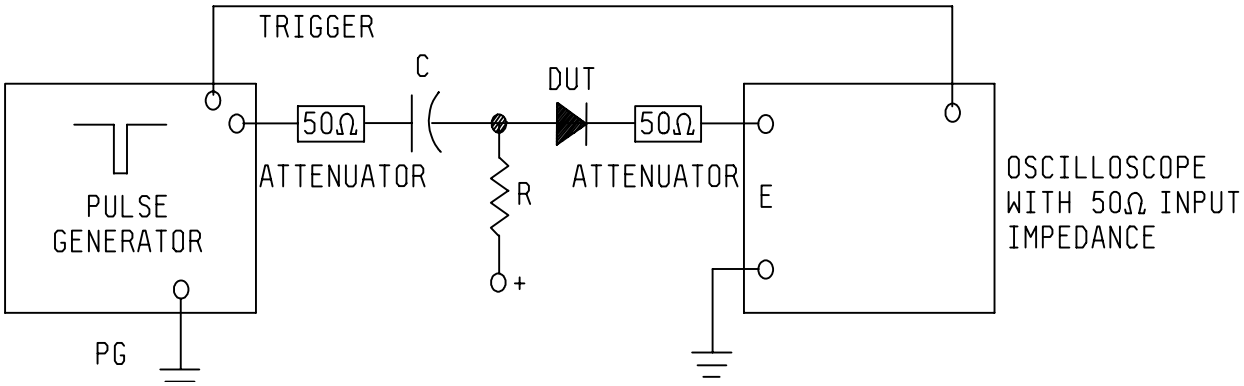

NOTE: The test circuit shall comply with the test conditions as stated in 2.1.
PW = Pulse width of reverse voltage pulse (see figure 4031-2).
R_L = Load resistance.
C = Coupling capacitance.

FIGURE 4031-1. Test circuit for condition A.

3.2 Procedure for condition A. The specified forward current shall be adjusted by resistor R and the + supply. Voltage E, developed across the 50 ohm oscilloscope input impedance shall be measured. Specified forward current shall be calculated by the expression $I_F = E/50$. The time duration of I_F shall be at least 10 times the device recovery time. The oscilloscope trace deflection above zero reference shall be adjusted by the oscilloscope vertical sensitivity to produce an amplitude of 2 cm minimum vertical deflection. Adjustment of the reverse transient current (I_{RM}) shall be made by varying the pulse generator output, observing the voltage E across the 50 ohm oscilloscope input impedance, and calculating I_{RM} by the expression I = E/50. When reverse bias voltage V_R is specified, and I_{RM} is not, the DUT shall be replaced with a shorting bar and I_{RM} shall be calculated by the expression $V_R/50$ (see figure 4031-2.)

3.3 Summary for condition A. The following conditions shall be specified in the applicable specification sheet.

a. Forward current, I_F.

b. Reverse current I_{RM} (preferred), or reverse voltage (optional alternative).

c. Load resistance, if other than 100 Ω (this is the sum of Z_{PG} and Z_{SCOPE}).

d. Ambient temperature in °C.

e. Generator impedance, if other than 50 Ω.

f. Recovery current measuring point, $i_{R(REC)}$, if different from 10 percent of I_{RM}.

The following measurement shall be made: t_{rr} (see figure 4031-2).

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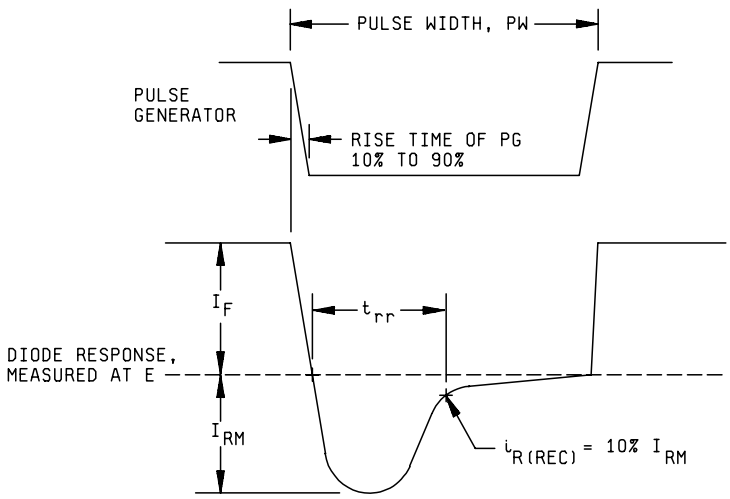

FIGURE 4031-2. Response pulse waveforms for condition A.

4. Test condition B. (See suggested conditions in table 4031-I (e.g., B1, B2) and figure 4031-3A and 4031-3B for test circuit and board layout.) This condition is particularly relevant to medium current (axial and similar) types of standard and fast rectifiers with maximum specified recovery times between 50 and 3,000 ns that measured at peak forward currents greater than 100 mA and less than or equal to 1.0 ampere. It is readily adapted to lower test currents. This test is also appropriate for devices with recovery times less than 50 ns that are measured at peak forward currents of 1A or less; below 25 ns, or at higher current, particular care shall be used to achieve low loop inductance and low circuit rise times to achieve acceptable repeatability.

This condition differs from condition D in that the reverse current (I_{RM}) is limited by the test circuit, not by the DUT.

TABLE 4031-I. Test condition B.

Designation (condition)		B1	B2	B3	B4	B5
Test current, (amperes) (see figure 4031-4)	I_F	0.5	0.5	1.0	1.0	0.01
	I_{RM}	1.0	0.5	1.0	1.0	0.01
	$i_{R(REC)}$	0.25	0.1	0.5	0.1	0.005
Circuit resistor 1/ (ohms)	R_F	33	33	50	50	1,200
	R_R	9	9	15	15	200
	R_4	1.00	1.00	1.00	1.00	10.0

1/ Preferred nominal resistance values are shown; modification of R_F and R_R may be needed to achieve the rise time of 4.1.a and the I_{RM} specified.

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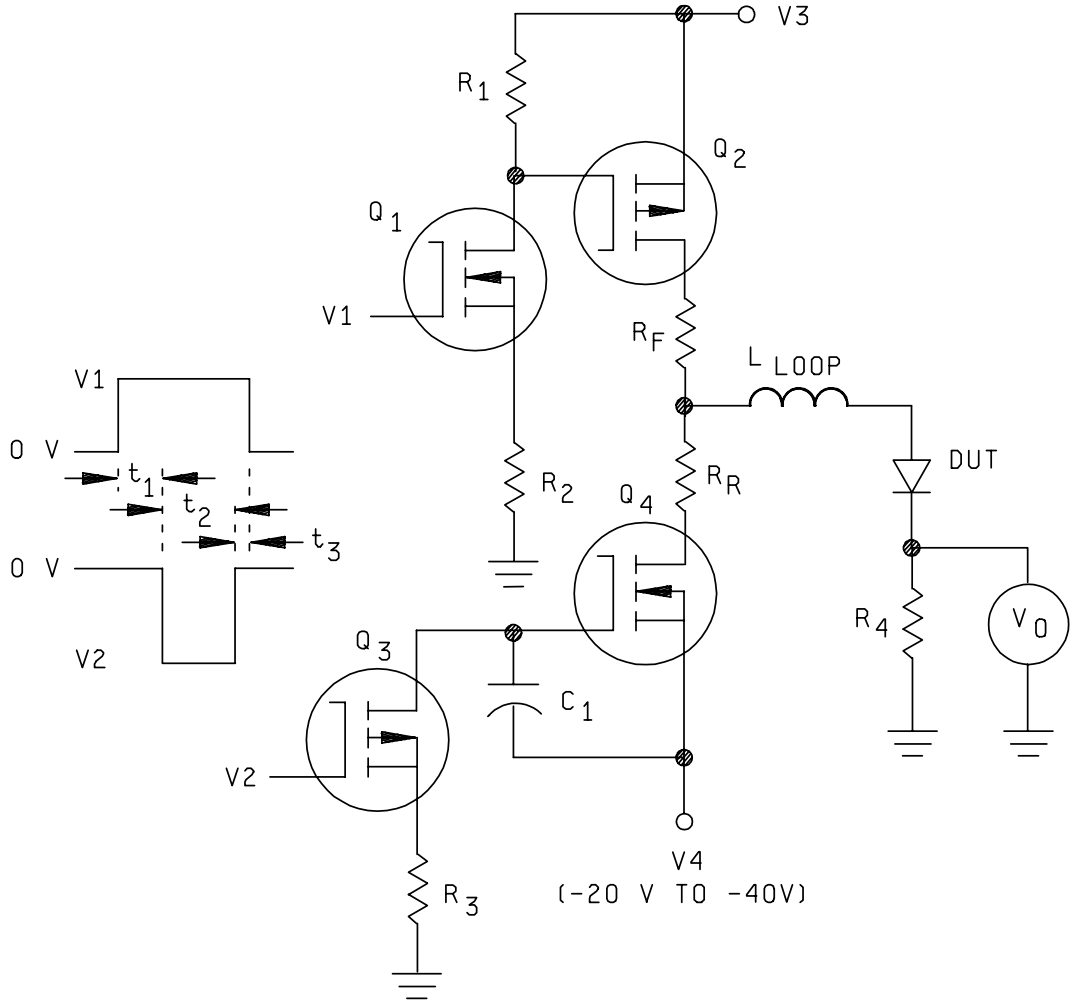
4.1 Circuit notes for condition B. The timing and test circuit of figure 4031-3A is a guide to what is needed. An equivalent circuit may be used. Figure 4031-3B shows a suggested configuration for R_4. Duty factor shall be 5 percent maximum.

a. The rise time of the reverse voltage pulse across a noninductive calibration resistor in place of DUT shall be less than 20 percent of the recovery time of the DUT.

b. The oscilloscope rise time shall be less than 50 percent of the pulse generator rise time.



V_3 and R_F control forward current I_F.
V_4 and R_R control reverse current I_{RM}.
$t_{rr(max)}$ is the longest to be measured.
$t_{rr(min)}$ is the shortest expected.

$t_1 > 5\ t_{rr(max)}$.
$t_2 > t_{rr}$.
$t_3 > 0$.
$L_1/R_4 < t_{rr(min)}/10$.
(L_1 is the self inductance of R_4)

FIGURE 4031-3A. Test circuit for condition B.

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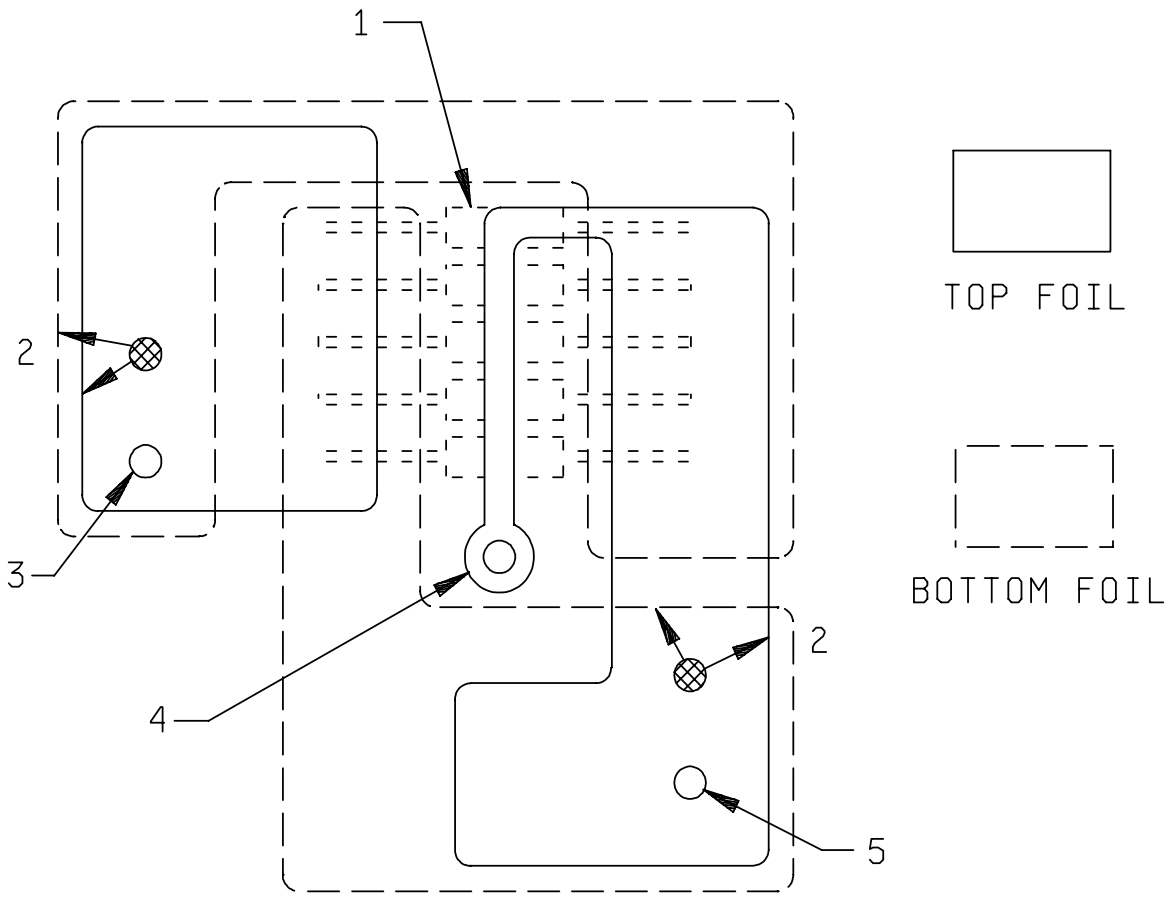

NOTES:

1. Resistor assembly R_4 consists of 10 resistors (1 Ω, .25 W metal film), 5 on top and 5 on the bottom foils. The center of resistor bodies are not shown, and leads are shown dotted so that conducting foils may be more clearly shown. Bottom resistor current flow L to R (⟶) is opposite to top current flow R to L (⟵), providing magnetic field cancellation. Sense lead to the center conductor of the probe jack exits at right angle to resistor axes and is located between the top and bottom resistor layers.
2. Cross hatched circular areas show the connections between those top and bottom foil regions indicated by arrows.
3. To ground of circuit and probe.
4. To center conductor of miniature probe jack.
5. To cathode of DUT.

FIGURE 4031-3B. Suggested board layout for low L_1/R_4 for condition B.

4.2 Procedure for condition B. Specified forward current (I_F) shall be adjusted by varying positive voltage, V_3. Reverse current (I_{RM}) shall be controlled by varying the negative voltage, V_4 (see figure 4031-4). With the DUT in place the circuit shall be capable of higher than specified I_{RM}; the circuit, and not the diode, must limit I_{RM}.

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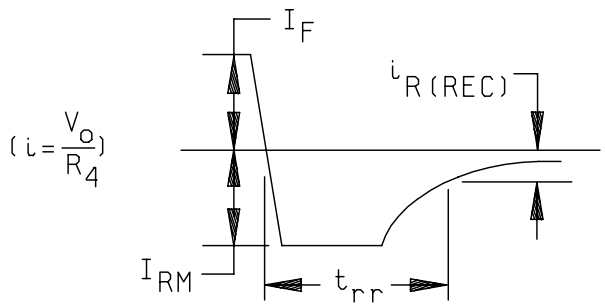


FIGURE 4031-4. Current through DUT (condition B).

4.3 Summary for condition B. The following conditions shall be specified in the applicable specification sheet.

a. Test condition (e.g., B1, B2) (see 3.) If not in table 4031-I, specify c, d, and e.

b. Ambient temperature, if other than +25°C.

c. Forward current, I_F.

d. Reverse current, I_{RM}.

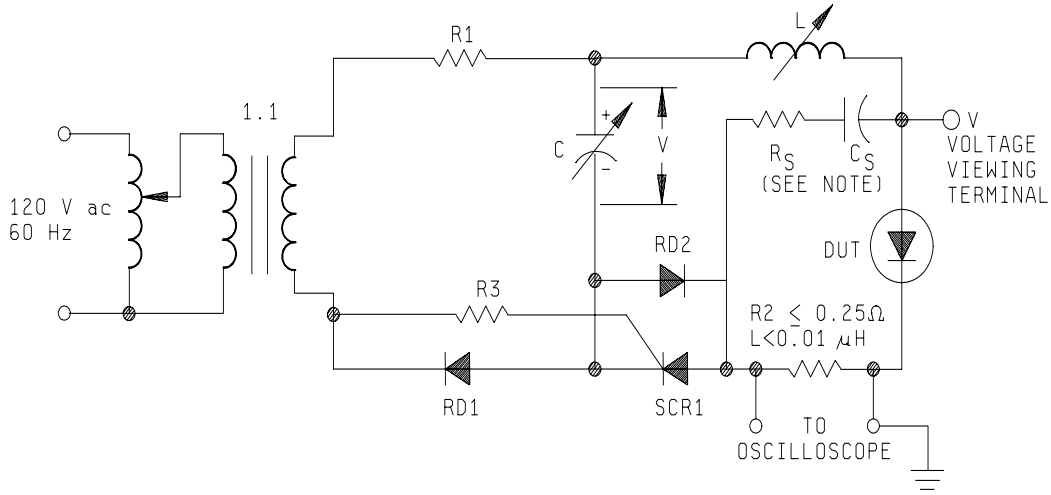
e. Load resistances R_F and R_R.

f. Recovery measuring point, $i_{R(REC)}$.

NOTE: Specify c through f, only if not a condition designation in table 4031-1.

The following measurement shall be made: t_{rr} (see figure 4031-4).

5. Test condition C. This test is intended for high current rectifiers with reverse recovery times equal to or greater than 350 ns and tested with peak forward currents equal to or greater than 10 amperes. See figure 4031-5.



NOTE: R_S and C_S are snubber components, when their use is specified

FIGURE 4031-5. Circuit for measuring reverse recovery characteristics (condition C).

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5.1 Circuit notes for condition C

a. The circuit is designed to simulate the commutation duty encountered in power rectifier diode circuits while also keeping average power dissipation low to minimize the need for thermal management.

b. The resistance of the C.L. and DUT loop (R_2 and parasitics) is small, e.g., $2\pi\sqrt{L/C}$ much greater than R so the test current will essentially be sinusoidal, possessing a width of $\sqrt{LC}$, a di/dt of V/L and a peak value of $\pi\sqrt{L/C}$. The peak voltage across the capacitor shall be as small as practicable to achieve the desired test conditions. The effects of reverse voltage magnitude on the test device recovery characteristics are neglected.

c. The minimum forward current pulse time (t_p) shall be at least five times the recovery time (t_{rr}) of the DUT so that the di/dt will be linear and of the same value before and after current reversal.

d. The oscilloscope rise time shall be less than 20 percent of t_a or t_b (see figure 4031-6), whichever is less.

e. The inductance of the current viewing resistor shall be extremely low, e.g., 0.01 micro Henry. Abrupt recovery rectifiers (figure 4031-6) can cause current oscillations which may be reduced by using a lower inductance current viewing resistor and by properly terminating the oscilloscope cable. A current transformer 1/ with suitable rise time may be substituted for the current viewing resistor 1/. Rectifier diode RD2 provides a very low inductance path around SCR1 if the reverse recovery time of SCR1 is shorter than that of the DUT. An external SCR triggering source may be required to achieve stable triggering.

f. A slight oscillation may appear on the waveform following device recovery. This may be reduced by lowering the current viewing resistor's inductance, or properly terminating the viewing cable. The oscillation, however, does not affect the test results.

g. D_2 and its circuit branch should provide a very low inductance path around the SCR if the reverse recovery time of the SCR is shorter than that of the DUT.

h. R_3 shall be sufficiently large such that the SCR triggers only after the capacitor, C, has had ample time to charge to its desired value. If stable triggering or ample charging is a problem, a momentary pushbutton switch may be inserted in line with R_3 to provide triggering. A pulse transformer technique is also acceptable in the triggering circuit.

5.2 Procedure for condition C. C, L, and V are adjusted to obtain the specified test current di/dt and magnitude, I_{FM}. The recovery time for rectifier diodes is defined as $t_{rr} = t_a + t_b$ (see figure 4031-6), t_a is measured from the instant of current reversal to the instant that current reaches its peak reverse value $I_{RM(REC)}$ and t_b is measured from $I_{RM(REC)}$ to the instant the straight line connecting $I_{RM(REC)}$ and 0.25 $I_{RM(REC)}$ intercepts the zero current axis. The recovery time for devices with abrupt recovery characteristics is defined in the same manner except t_b is measured from $I_{RM(REC)}$ to the instant the test current waveform intercepts the zero current axis, if applicable.

1/ Pearson Electronics, Inc. or equivalent types.

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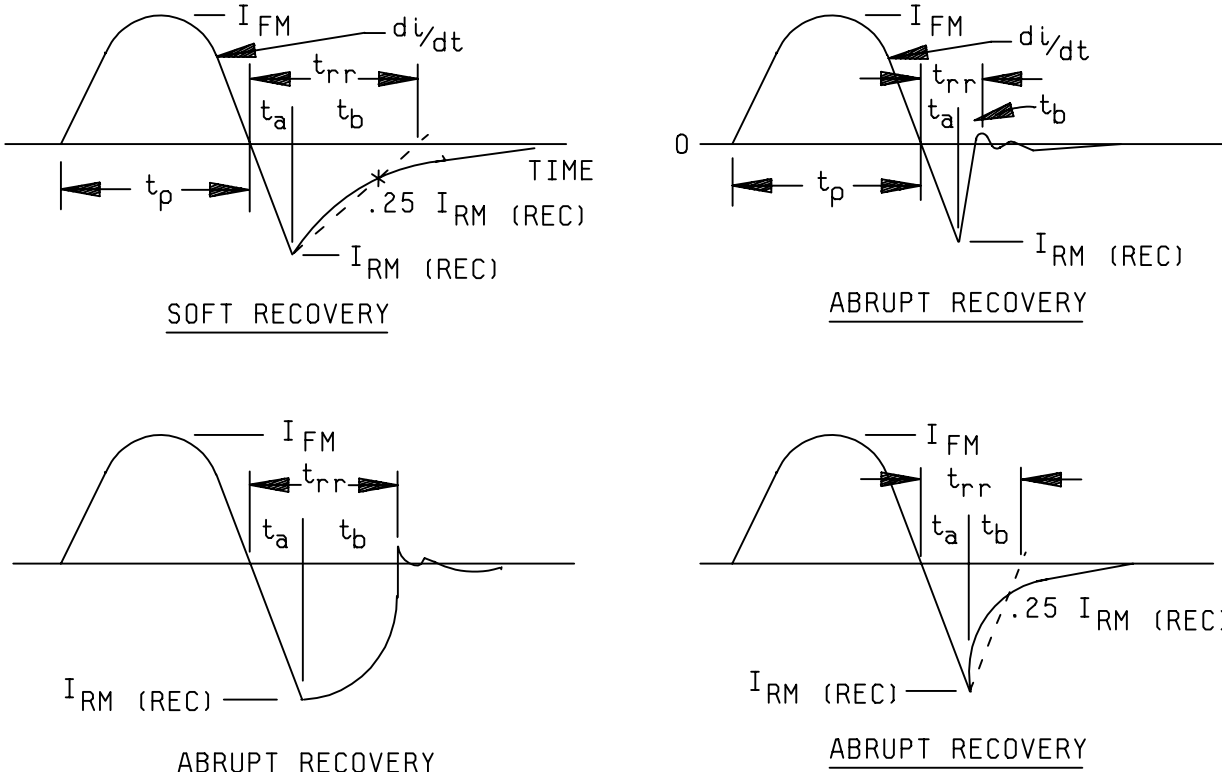

FIGURE 4031-6. Test current waveforms for various types of rectifier diodes under test in the circuit for measuring reverse recovery characteristics.

5.3 Summary for condition C.

a. The following conditions shall be specified in the applicable specification sheet:

(1) Case temperature in °C.

(2) Test repetition rate, in Hz.

(3) Peak forward current, I_{FM}, in amperes.

(4) Rate of decrease of forward current, di/dt, in A/μs.

(5) Minimum test current pulse width, tp, in microseconds. (Duty cycle shall be ≤ one percent).

b. The following characteristics shall be specified for measurement in the applicable specification sheet as required:

(1) Reverse recovery time (defined as $t_{rr} = t_a + t_b$), t_a, t_b.

(2) Reverse recovery current, $I_{RM(REC)}$, in amperes.

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6. Test condition D. (See suggested conditions in table 4031-II. (e.g., D1, D2, D3)) This condition is intended for ultra-fast medium current rectifiers (axial and case mount, or equivalent styles) measured at $I_F \geq 1A$ and with reverse recovery time ≤ 100 ns. With good engineering practice, condition D can adequately measure t_{rr} down to about 10 ns; it can also utilize I_f up to at least 10 A.

TABLE 4031-II. Test condition D.

Device ratings		Designation (condition)	Values for testing	
I_O or I_F (AV) (A)	t_{rr} (ns)		I_F (A)	di/dt (μ/s)
1 to 4	> 65 to 100	D1	2	100
to 20	> 65 to 100	D2	6	100
over 20	> 65 to 100	D3	10	100
1 to 4	≤ 65	D4	2	200
to 20	≤ 65	D5	6	200
over 20 1/	≤ 65	D6	10	200

1/ For devices with substantially higher rated current, it is desirable to use test conditions for I_F close to rated current, and higher values of di/dt.

6.1 Test circuit. Refer to figures 4031-7 and 4031-8 for timing and circuit details. Equivalent circuits may be used. The forward current generator consisting of Q_1, Q_2, R_1, and R_2 may be replaced with any functionally equivalent circuit. Likewise, the current-ramp generator consisting of Q_3, Q_4, R_3, and C_1. The duty factor shall be ≤5 percent.

a. This method presumes that good engineering practice will be employed in the construction of the test circuit, e.g., short leads, good ground plane, minimum inductance of the measuring loop, and minimum self-inductance (L_1) of the current sampling resistor (R_4). Also, appropriate high speed generators and instruments shall be used.

b. The measuring-loop inductance (L_{LOOP}, see figure 4031-7) represents the net effect of all inductive elements, whether lumped or distributed, e.g., bonding wires, test fixture, circuit board foil, or inductance of energy storage capacitors. The value of L_{LOOP} should be 100 nH or less. The reason for controlling this circuit parameter is that it, combined with diode characteristics including C_T, determines the value of t_b.

c. The turn-off reverse-voltage overshoot shall not be allowed to exceed the device rated breakdown voltage. Ringing and overshoot may become a problem with $R_{LOOP} < 2\sqrt{(L/C)}$; where $L = L_{LOOP}$. That is another reason for minimizing L_{LOOP}.

d. Regarding breakdown voltage, $-V_4$ should be kept as low as practicable, especially when test low voltage devices. A value of approximately 30 volts is recommended.

e. The time constant of the self-inductance of the current-sample resistor R_4 (see figure 4031-8) shall be kept low relative to t_a because the observed values of t_a and I_{RM} increase with increasing self-inductance. Since the value of R_4 is not specified, the recommended maximum inductance is expressed as a time constant (L_1/R_4) with a maximum value of t_a (minimum)/10, where t_a (minimum) is the lowest t_a value expected. This ratio was chosen as a practical compromise and would yield an observed t_a, which is 10 percent high ($\Delta t_a = L_1/R_4$). The I_{RM} error is a function of the L_1/R_4 time constant and di/dt. For a di/dt of 100 A/μs the observed I_{RM} would also be 10 percent high. $\Delta I_{RM} = L_1/R_4$ di/dt.

f. The di/dt of 100 A/μs was chosen so as to provide reasonably high signal levels and still not introduce the large I_{RM} errors caused by higher di/dt. Higher values of di/dt, without large errors, can be achieved with lower L_1/R_4.

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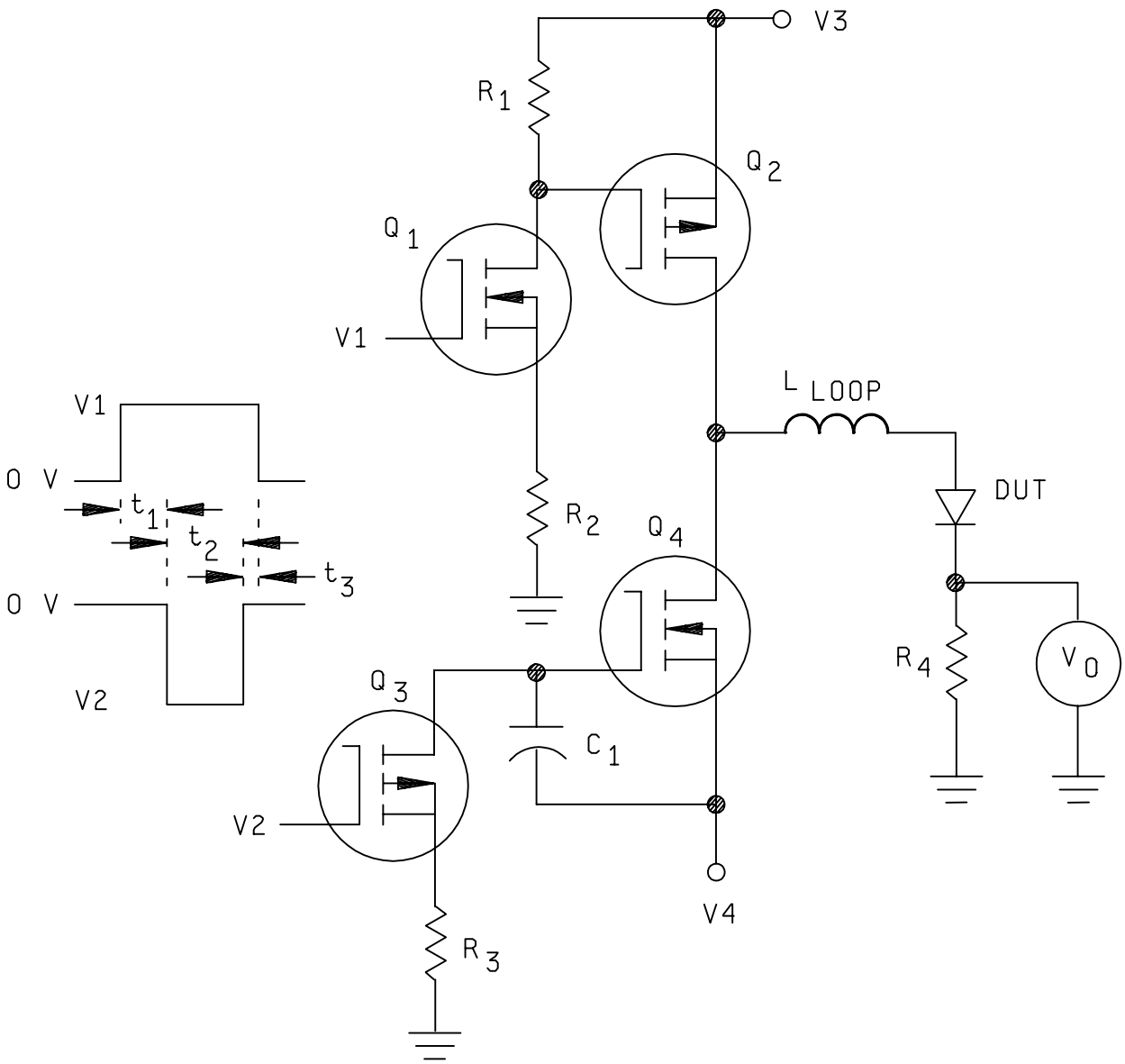

V_1 amplitude controls forward current (I_F).
V_2 amplitude controls di/dt.
$t_{a(max)}$ is the longest t_a to be measured.
$t_{a(min)}$ is the shortest t_a to be measured.

$t_1 > 5\ t_{a(max)}$.
$t_2 > t_{rr}$.
$t_3 > 0$.
$L_1/R_4 < t_{a(min)}/10$.
L_1 is the self inductance of R_4.

FIGURE 4031-7. t_{rr} test circuit for condition D.

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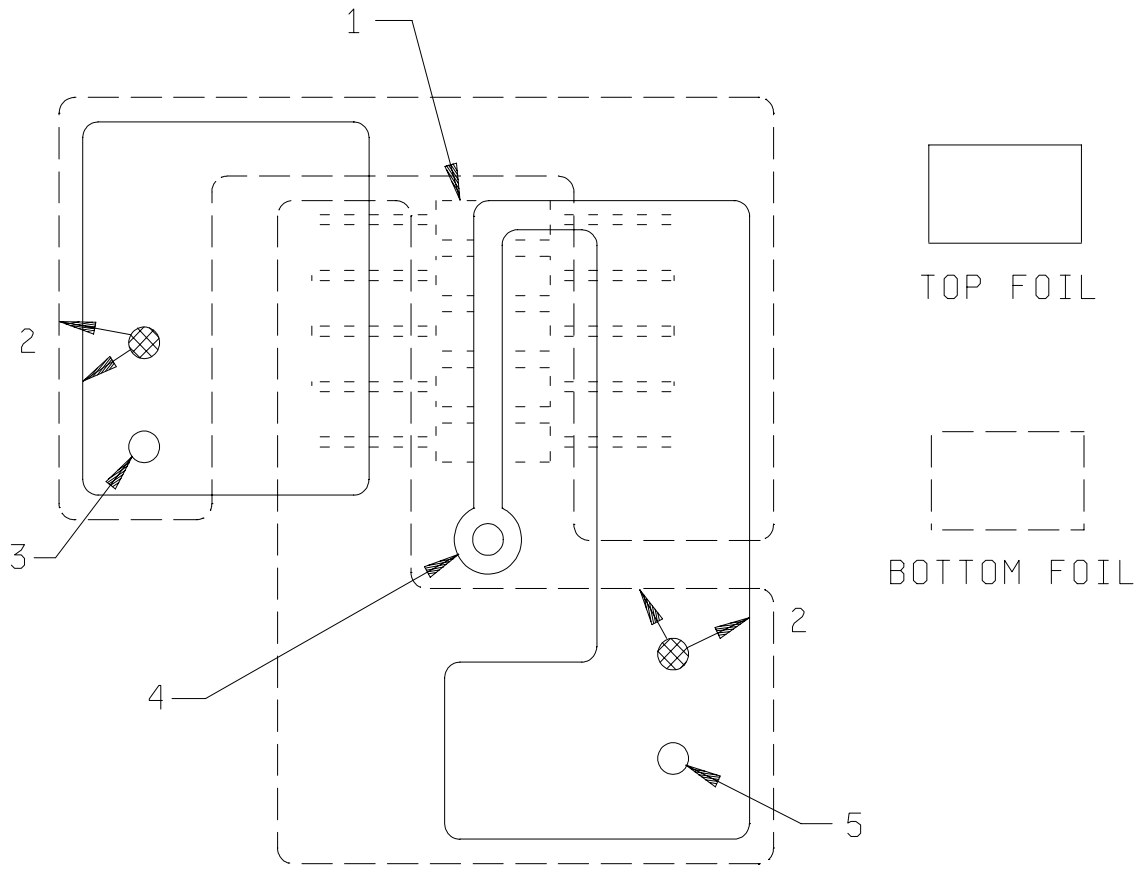

NOTES:

1. Resistor assembly R_r is made from 10 resistors (1 Ω, .25 W metal film), 5 on top and 5 on the bottom foils. The center of resistor bodies are not shown, and leads are shown dotted so that conducting foils may be more clearly shown. Bottom resistor current flow L or R (⟶) is opposite to top resistor current flow R to L (⟵), providing magnetic field cancellation. Sense lead to the center conductor of the probe jack exits at right angle to resistor axes and is located between the top and bottom resistor layers.
2. Crosses hatched circular areas show the connections between those top and bottom foil regions indicated by arrows.
3. To ground of circuit and probe.
4. To center conductor of miniature probe jack.
5. To cathode of DUT.

FIGURE 4031-8. Suggest board layout for low L_1/R_4 for condition D.

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6.2 Procedure for condition D. Adjust V_1 for the specified forward current, I_F. Adjust $-V_2$ for the specified di/dt (see figures 4031-7 and 4031-9).

6.3 Summary for condition D.

a. The following conditions shall be specified in the applicable specification sheet:

(1) Designation (condition, see table 4031-II). If another is desired, 4 and 5 herein shall be specified. If another is desired, d and e shall be specified.

(2) $-V_4$, reverse ramp power supply voltage.

(3) T_C, case temperature, if other than +25°C.

(4) I_F, .25 (minimum) of the continuous rated current is the suggested alternative (see table 4031-II).

(5) di/dt, 100 A/µs is the suggested alternative (see table 4031-II).

b. The following characteristics shall be specified for measurement:

(1) Reverse recovery time, t_{rr} (see figure 4031-9).

(2) $I_{RM(REC)}$ (see figure 4031-9)

NOTE: An additional measurement, t_a may be made if desired to compute $t_b = t_{rr} - t_a$, and the recovery softness factor, RSF = t_b/t_a.

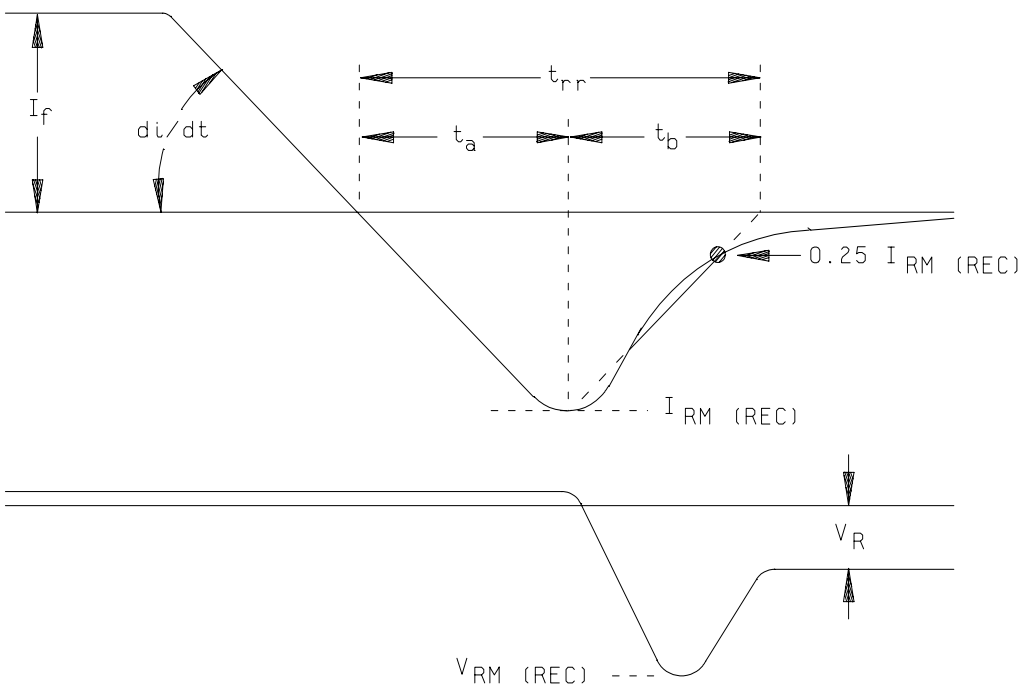

FIGURE 4031-9. Generalized reverse recovery waveforms for condition D.

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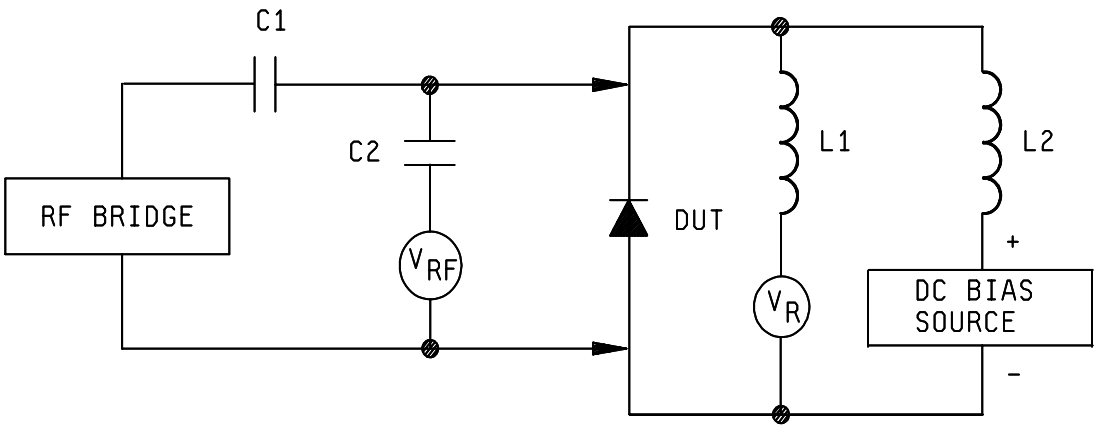
METHOD 4036.1

Quality Factor (Q) FOR VOLTAGE VARIABLE CAPACITANCE DIODES

1. Purpose. The purpose of this test is to measure the quality factor (Q) of the device. By definition, Q expresses the ratio of reactance to effective resistance of the device, under rf signal conditions and specified dc bias conditions.

2. Test circuit. See figure 4036-1.



NOTE: The impedance of C1, C2, and L1, L2 shall be small and large, respectively, compared to the DUT at the frequency of measurement.

FIGURE 4036-1. Test circuit for measuring Q.

3. Procedure. The test equipment shall be connected as shown in figure 4036-1. The dc bias supply shall be adjusted for the specified voltage where Q is to be measured. Unless otherwise specified, the rf level shall be adjusted to 50 mV (rms). The parallel resistance Rp and capacitance Cp of the test device shall be measured using rf bridge methods. Unless otherwise specified, the point of measurement shall be .062 inch (1.57 mm) from the device body. Q shall be calculated using the following formula: $Q = 2\pi fRpCp$.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test frequency.

b. Reverse dc bias (V_R).

c. RF level if other than 50 mV (rms).

d. Required Q.

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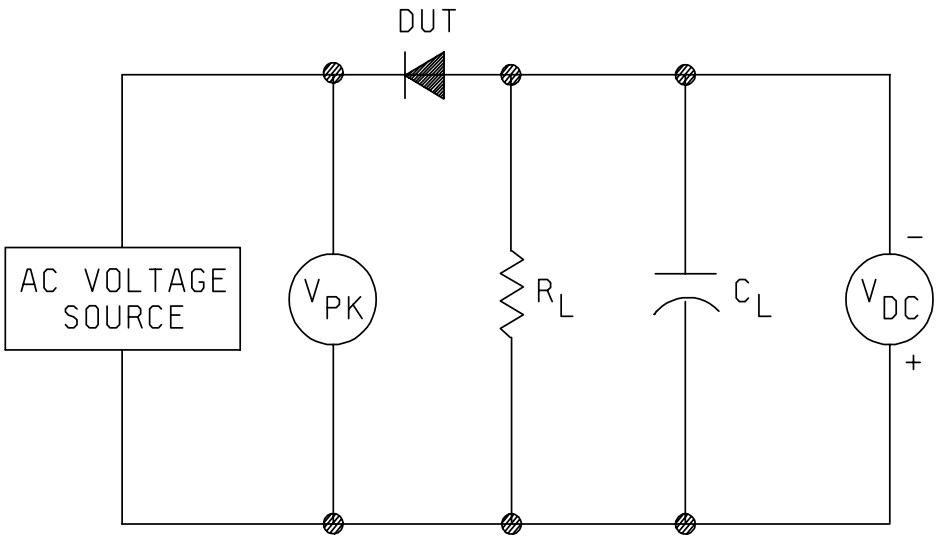
METHOD 4041.2

RECTIFICATION EFFICIENCY

1. Purpose. The purpose of this test is to measure rectification efficiency which is the ratio of dc output voltage to peak ac input voltage.

2. Test circuit. See figure 4041-1.



NOTE: The voltmeter shall have a high impedance as compared with the load circuit of R_L and C_L.

FIGURE 4041-1. Test circuit for rectification efficiency.

3. Procedure. The ac signal shall be adjusted to the specified frequency and signal level measured by means of peak reading voltmeter (V_{pk}). The rectified output voltage shall be measured by means of voltmeter (V_{DC}).

$$\textit{Rectification efficiency (\%)} = \frac{V_{DC}}{V_{pk}} X\ 100$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Load capacitor (C_L) and load resistor (R_L).

b. Frequency and amplitude of ac source.

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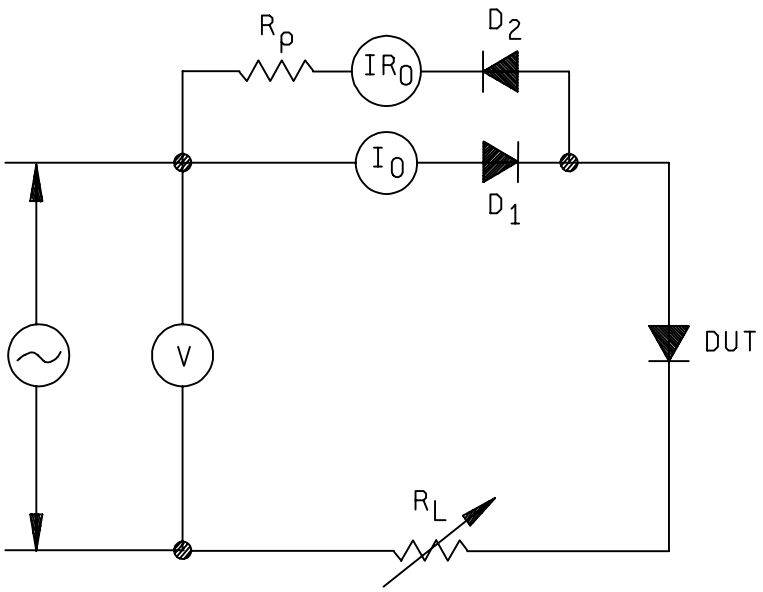
METHOD 4046.1

REVERSE CURRENT, AVERAGE

1. Purpose. This test is designed to measure the average reverse current through the device under the specified conditions.

2. Test circuit. See figure 4046-1.



NOTE: The reverse leakage current at each device D_1 and D_2 shall be less than .05 percent of the maximum allowable specified leakage current of the DUT. In other respects, the devices D_1 and D_2 should be of the same type as the DUT.

FIGURE 4046-1. Test circuit for reverse current, average.

3. Procedure. After thermal equilibrium, at the temperature specified, the specified voltage shall be applied.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test temperature, when required (see 3.).

   b. Test voltage (see 3.).

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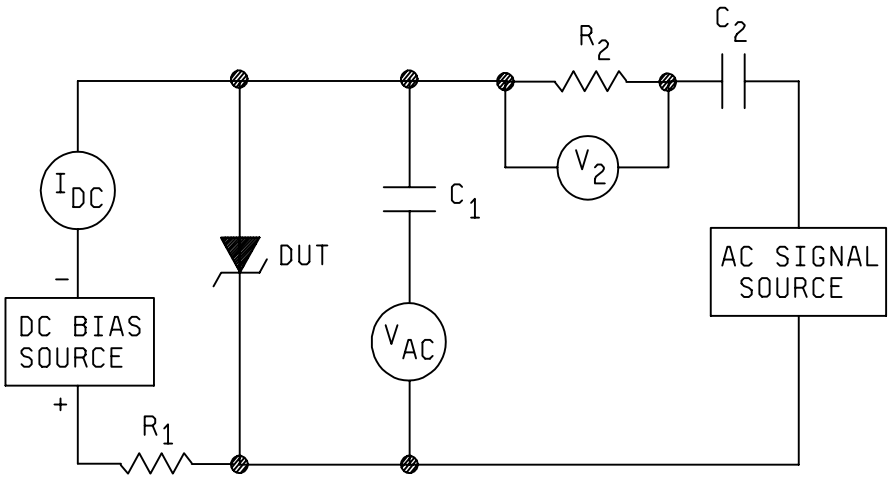
METHOD 4051.3

SMALL-SIGNAL REVERSE BREAKDOWN IMPEDANCE

1. Purpose. The purpose of this test is to measure the reverse breakdown impedance of the device under small-signal conditions.

2. Test circuit. See figure 4051-1.



NOTES:
1. The impedances of C_1 and C_2 shall be small compared to the DUT at the test frequency.
2. Voltmeters V_{AC} and V_2 shall be high input impedance rms types.
3. The resistance of R_1 shall be large compared with the breakdown impedance being measured.
4. A low pass filter may be installed in series with the ac signal source.

FIGURE 4051-1. Test circuit for small-signal reverse breakdown impedance.

3. Procedure. The specified reverse direct current shall be applied to the DUT. An ac signal in the frequency range of 45 through 1,000 Hz shall be applied to the DUT through coupling capacitor C_2. Associated specification limits for Z_{ZT} shall apply at 45 through 60 Hz. Tests at frequencies greater than 60 Hz shall be corrected to those readings taken at 45 through 60 Hz. This current shall be 10 percent of the value of the dc breakdown current through the DUT. The small-signal impedance shall be determined as follows:

$$Z_{ZT} = \frac{V_{(RMS)}}{I_{(RMS)}} = \frac{V_{AC}\,R_2}{V_2}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. DC and ac test currents.

b. Test frequency, if other than 45 to 1,000 Hz.

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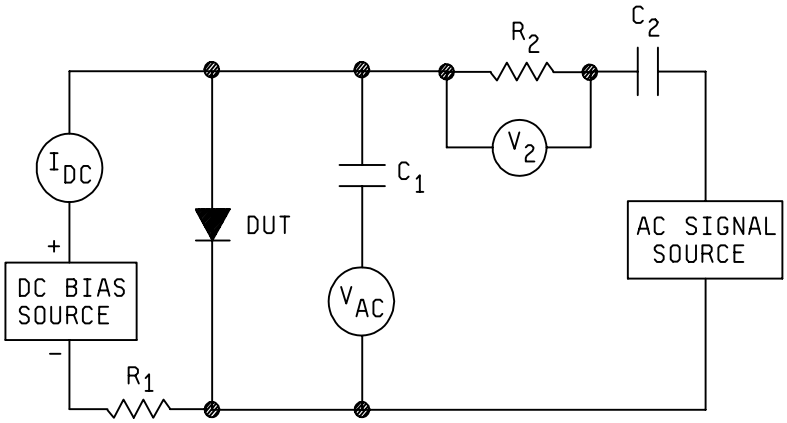
METHOD 4056.2

SMALL-SIGNAL FORWARD IMPEDANCE

1. Purpose. The purpose of this test is to measure the forward impedance of the device under small-signal conditions.

2. Test circuit. See figure 4056-1.



NOTES:
1. The impedances of C_1 and C_2 shall be small compared to the DUT at the test frequency.
2. Voltmeters V_{AC} and V_2 shall be high input impedance types.
3. The resistance of R_1 shall be large compared with the forward impedance being measured.
4. A low pass filter may be installed in series with the ac signal source.

FIGURE 4056-1. Test circuit for small-signal forward impedance.

3. Procedure. The specified forward direct current shall be applied to the DUT. An ac signal in the frequency range of 45 through 1,000 Hz shall be applied to the DUT through coupling capacitor C2. associated specification sheet limits for Z_f shall apply at 45 through 60 Hz. Tests at frequencies greater than 60 Hz shall be corrected to those readings at 45 through 60 Hz. This current shall not be greater than 10 percent of the value of the dc forward current I_f. The small-signal impedance shall be determined as follows:

$$Z_f = \frac{V_{(RMS)}}{I_{(RMS)}} = \frac{V_{AC}\,R_2}{V_2}$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. DC and ac test currents.

b. Test frequency, if other than 45 to 1,000 Hz.

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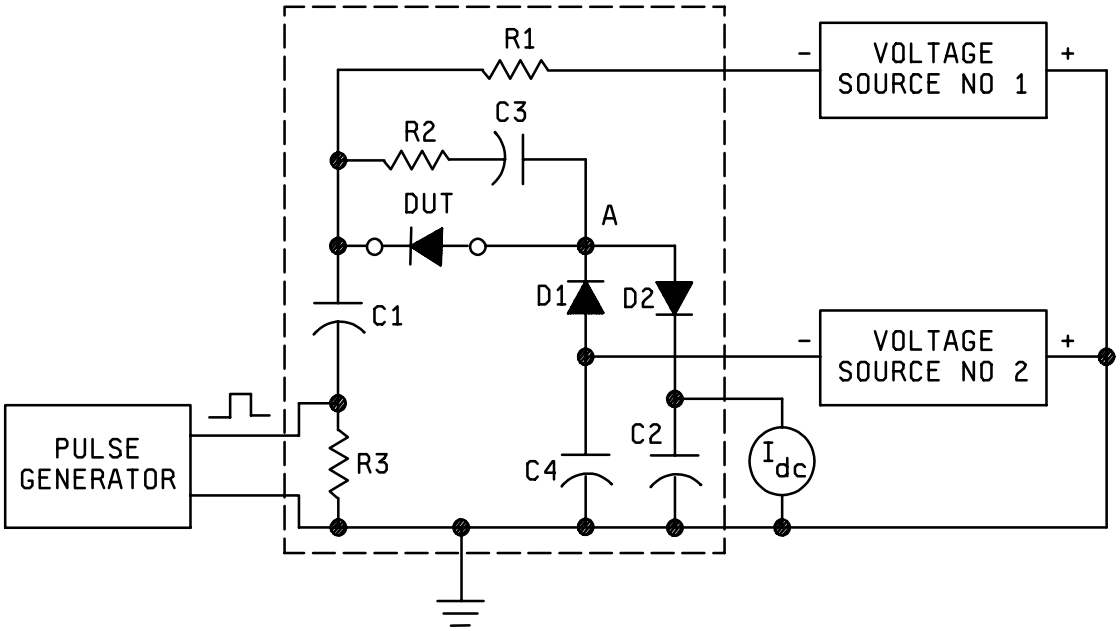
METHOD 4061.1

STORED CHARGE

1. Purpose. The purpose of this test is to measure directly the charge recovered from a semi-conductor diode when it is rapidly switched from a forward biased condition to a reverse biased condition.



2. Test circuit. See figure 4061-1.

FIGURE 4061-1. Test circuit for stored charge.

3. Test precautions.

a. The diode under test is forward biased by the current flowing from voltage source number 2 through diode D1 and through resistor R1 to voltage source number 1. The diode under test is periodically reverse biased by the pulse from the generator and the charge stored in the diode is caused to flow through diode D2 and is measured on the current meter. A similar measurement is made at zero bias current to determine the component of charge resulting from the diode capacitance and the stray circuit capacitance. The stored charge can then be computed from the current readings and the pulse frequency.

b. Resistor R1 should be large enough to ensure a constant current through the diode under test. Capacitor C1 should be large enough to maintain a nearly constant voltage across the diode under test during the pulse. The output impedance of the pulse generator including R3 should have a low value, preferably 10 to 25 Ω. The rise time of the pulse should be short enough and the pulse length should be long enough so that further change will not alter the measurement results.

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c. Diode D1 should have a much smaller stored charge than the diode under test. Diode D2 should have a fast turn on time, a low dynamic resistance at high currents, and a low reverse leakage current. Capacitors C2 and C4 should have low inductance and should be of sufficient capacitance so that a further increase in their values would not alter the measurement results. The current meter should be of sufficiently low impedance that the average voltage drop across it during any test does not exceed 10 millivolts. Capacitor C3 should be of sufficient size that a small current will flow through the current meter with the diode under test removed. Resistor R2 should have approximately the same value as the output impedance of the pulse generator.

d. The portion of the circuit within the dotted lines should be constructed in accordance with good practices for high speed pulse circuits. Particular attention should be paid to minimizing the circuit inductance including the connections to the diode under test. The capacitance between point A and ground should be made as small as possible.

4. Test procedure.

a. Adjust the pulse generator for the desired amplitude, pulse width, and frequency (f). Set voltage source one to zero. Insert the diode under test and adjust voltage source two for the specified voltage from point A to ground as measured on a high impedance voltmeter. A common value used for this voltage is -0.6 volts. Read the current, I_1, flowing through the current meter.

b. Set voltage source one for the specified forward current through the diode under test. Adjust voltage source two for the specified voltage from point A to ground. This voltage must be the same as used in 3.a. Read the current, I_2, flowing through the current meter.

c. The stored charge is given by:

$$Q_S = \frac{I_2 - I_1}{f}$$

5. Summary. The following conditions shall be included in the applicable specification sheet:

a. The bias current I_f at which the stored charge measurement is made (see 4.).

b. Pulse generator rise time (1 percent to 50 percent), amplitude, width, impedance, and frequency (see 4.).

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METHOD 4064

AVALANCHE ENERGY TEST FOR SCHOTTKY DIODES

1. Purpose. This purpose of this test method is to determine the avalanche capability of schottky diodes. The intent of the test is to stress the termination of the device.

2. Scope. This method is intended as a test for diode devices designed and specified with avalanche capability.

3. Circuitry. The circuit shall be designed so that all stray reactances are held to a minimum. The inductor L shall be of a fast response type.

4. Symbols and definitions. The following symbols and terminology apply to this test method:

a. E_{AS}: Non-Repetitive avalanche energy, minimum.

b. I_{AS}: Non-Repetitive avalanche current, maximum.

c. L: Load inductance in accordance with DUT.

d. P_D: Power dissipation of device.

e. R_S: Stray circuit resistance.

f. I_{LPK}: Peak inductor current.

g. $V_{(BR)DUT}$: Breakdown or avalanche voltage of device under test.

h. V_{DD}: Power supply voltage.

i. $V_{(BR)DUT}$: Breakdown or avalanche voltage of device.

k. t_{AV}: Time in avalanche.

5. Procedure.

5.1 Screening. The DUT must be screened prior to avalanche and meet all specified parameters.

5.2 Calculations. The energy delivered to the DUT can be calculated as follows:

a.

$$E_{AS} \approx \frac{1}{2} * L * I_{LPK}^2 * \left(\frac{V_{(BR)DUT}}{V_{(BR)DUT} - V_{DD}} \right)$$

NOTE: $R_S \neq 0$

b.

$$E_{AS} \approx \frac{1}{2} * L * I_{LPK}^2$$

NOTE: It is assumed that $R_S = 0$ for these calculations.

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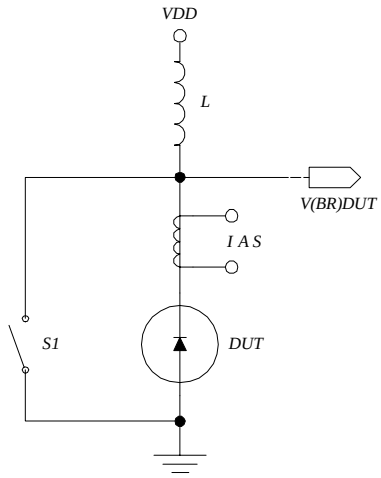
5.3 Test Circuit 1.

5.3.1 The circuit shown below is typical for unclamped inductive switching. In this circuit design the V_{DD} power supply may contribute to the total energy transferred to the diode if its value is not small compared to the $V_{(BR)}$ of the device under test. The calculation of the energy should include the transfer from the V_{DD} supply when the ratio of $V_{(BR)DUT}$ over V_{DD} is less than 10, which is calculation **(a)** in section 5.2.



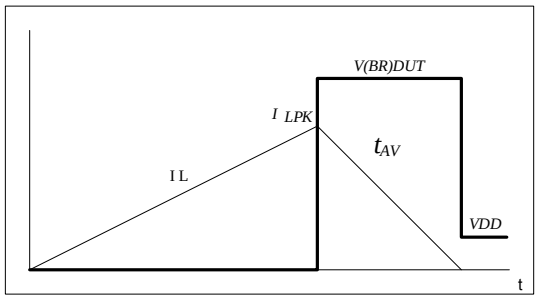
5.3.2 Switch S1 is normally a power semiconductor, such as a mosfet but the breakdown voltage of this device must be greater than that of the device under test.

5.3.3 A current transformer or probe should be used to monitor the avalanche current of the device. This probe must be mounted in either the cathode or anode leg of the device under test.

5.3.4 The value of inductance (L) for the load should be selected to keep the time in avalanche below 200uS. Air core inductors are recommended for this test to avoid the possibility of core problems. If iron core inductors are used, care must be taken such that core saturation is not changing the effective value to the inductance (L), which will lead to non-repeatable test results.

$$t_{AV} \approx \frac{L * I_{LPK}}{V_{(BR)DUT}}$$

5.3.5 The current and voltage waveform below shows typical response of a device in this test circuit.



5.4 Test Circuit 2.

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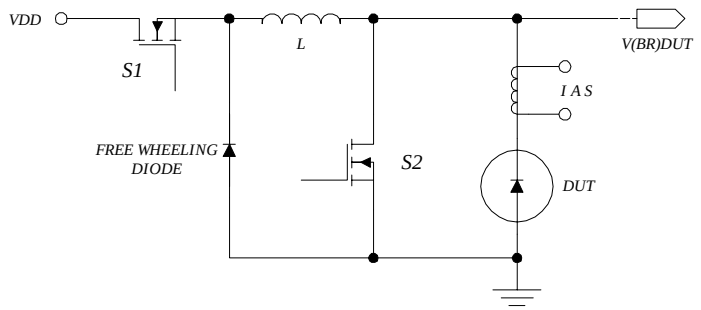
5.4.1 The circuit shown below is also applicable for unclamped inductive switching. In this circuit design the V_{DD} power supply is removed from the test circuit via S1 after the inductive load is fully charged. The calculation of the energy does not need to include the transfer from the V_{DD} supply when using this test circuit, which is calculation (b) in section 5.2.



5.4.2 Switches S1 and S2 are a power semiconductors, such as mosfets but the breakdown voltages of the devices must be greater than that of the device under test. These devices are switched off simultaneously in order to achieve the proper response on the device under test.

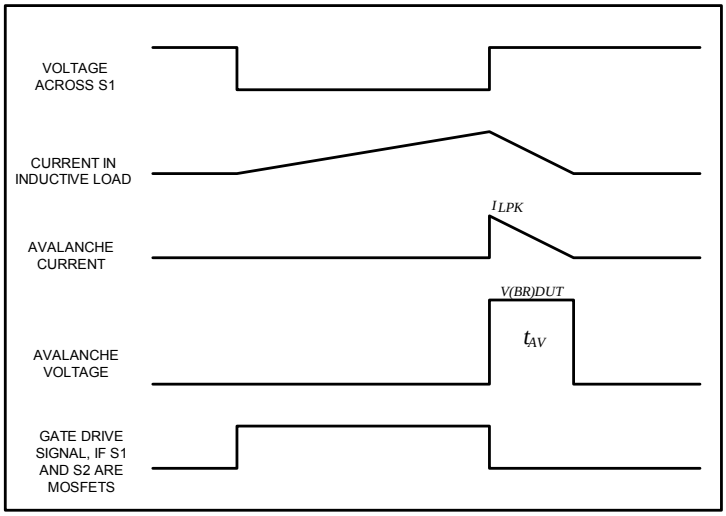
5.4.3 The free wheeling diode is required to close the current loop for the inductive load after S1 opens the connection to the V_{DD} power supply.

5.4.4 A current transformer or probe should be used to monitor the avalanche current of the device. This probe must be mounted in either the cathode or anode leg of the device under test.

5.4.5 The value of inductance (L) for the load should be selected to keep the time in avalanche below 200uS. Air core inductors are recommended for this test to avoid the possibility of core problems. If iron core inductors are used, care must be taken such that core saturation is not changing the effective value to the inductance (L), which will lead to non-repeatable test results.

$$t_{AV} \approx \frac{L * I_{LPK}}{V_{(BR)DUT}}$$

5.4.6 The current and voltage waveform below shows typical response of a device in this test circuit.



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6. Summary. The following conditions shall be specified in the applicable specification sheet:

a. E_{AS}: Non-Repetitive avalanche energy, minimum (joules).

b. I_{AS}: Non-Repetitive avalanche current, maximum (amperes).

c. V_{DD}: Power supply voltage.

d. L: Load inductance in accordance with DUT.

7. Failure criteria. The DUT shall tested and be within all specified static parametric limits at the completion of the test.

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METHOD 4065

PEAK REVERSE POWER TEST

1. Purpose. This describes a test method for subjecting the device under test (DUT) to a high power stress condition in the reverse direction of rectifiers to determine the ability of the device to withstand a specified peak reverse power. This is intended to verify reverse power stress capabilities by various test conditions. Each condition is considered nonrepetitive where there is sufficient time between their applications to permit the device temperature to return to its original value before it may be repeated.

2. Applicability. A current impulse is applied for 20 µs that will provide a constant level of power in the reverse direction of the rectifier. This test method also utilizes a monitoring circuit to sense voltage for determination of power and possible voltage collapse during the current impulse.

3. Definitions. The following symbols and terms shall apply for the purpose of this test method.

a. I_{RSM}: Nonrepetitive reverse surge current (in Amps)

b. $v_{(BR)}$: Breakdown voltage (instantaneous value (in Volts)

c. $V_{(BR)}$: Minimum rated breakdown voltage (in Volts)

d. P_{RSM}: Reverse power nonrepetitive peak (in Watts)

e. d.f.: Duty factor = 100 t_p/ t_{rep} (percentage)

f. t_P: Duration of current surge pulse (in ms or µs).

4. Reverse power test of rectifiers.

4.1 Apparatus. A simplified circuit is shown in figure one where the current source (I) and switch (SW1) combination shall apply the peak value of current pulse I_{RSM} for the pulse duration of 20 µs as required (see Figure 2A). The rise and fall times of the pulse shall be less than 10 percent of the pulse duration and the I_{RSM} will not vary during the impulse by more than 10%. The DUT shall also be monitored during the pulse using an oscilloscope to verify the instantaneous $v_{(BR)}$ voltage. The monitored $v_{(BR)}$ will typically increase during the 20 µs impulse from heating effects as shown in Figure 2B. The $v_{(BR)}$ may also simply be monitored at the end of the pulse duration by a gated switch (SW2) or other automated methods to determine its highest value and also ensure the $v_{(BR)}$ has not collapsed below the rated minimum breakdown voltage V_{BR} of the rectifier from excessive heat. Although a simplified circuit is depicted, there are other more automated test equipment (ATE) methods that can also accomplish this such as the Frothingham RE20A, B, or C as well as a FEC200 tester with a separate dual monitor oscilloscope for both current and voltage.

4.2 Procedure. No current is applied to the DUT prior to the starting time (t_o) of the test. At t_o, SW1 applies I_{RSM} for 20 µs after which SW1 causes the current to cease flowing in the DUT.

a. Apply a specified rectangular impulse level of current I_{RSM} as shown in Figure 2A. The rectangular impulse may decline slightly to optimize a constant peak reverse power level (P_{RSM}) since the $v_{(BR)}$ will increase due to heating effects and positive temperature coefficient during the 20 µs impulse. This impulse shall control the effective power to within 10% during the impulse duration. The DUT is also monitored for the response in reverse voltage $v_{(BR)}$.

b. If testing to a specific peak reverse power (P_{RSM}) requirement, the current (I_{RSM}) will be increased to the level where the calculated P_{RSM} level meets or exceeds the requirement. The P_{RSM} value is determined with the average I_{RSM} and $v_{(BR)}$ values where $P_{RSM} = I_{RSM} \times v_{(BR)}$. These average values typically occur at 10 µs or half way into the 20 µs impulse.

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NOTE: The test may need to be repeated to achieve the desired power level after the initial $v_{(BR)}$ is determined. If repeated, the time between pulses shall be sufficient to permit the DUT temperature to return to its original value.

c. If it is noted that the $v_{(BR)}$ collapses below the minimum rated breakdown voltage $V_{(BR)}$ during the testing in 4.2.1 and 4.2.2, this is considered a failure to the applied P_{RSM} level.

d. Electrical measurements shall also be performed after each reverse power test to ensure the DUT has not permanently degraded. As a minimum, this shall include verification the reverse current (I_R) does not exceed its maximum specified value at the rated voltage V_R for the DUT. Although a device can collapse in 4.2.3 without permanently degrading, such a collapse will still be considered a failure to this Peak Reverse Power test method.

e. If characterizing the DUT for peak reverse power, steps 4.2.1 through 4.2.4 shall be repeated at higher levels until failure occurs. For this purpose, 10% progressive increases in I_{RSM} are recommended. The time between pulses shall be sufficient to permit the DUT temperature to return to its original value before it is repeated.

4.3 Test parameters to be specified and recorded. The following conditions shall be specified:

a. The peak reverse power (P_{RSM}) for rectifiers.

b. Duration of pulses (t_p), shall be 20 μs unless otherwise specified.

c. The $v_{(BR)}$ monitored during the 20 μs impulse. A collapse below minimum rated $V_{(BR)}$ is a failure.

d. Measurements after test.

e. Case, lead, or ambient temperature (T_C, T_L, or T_A), as applicable.

f. Duty factor (d.f.) if more than one impulse is specified.

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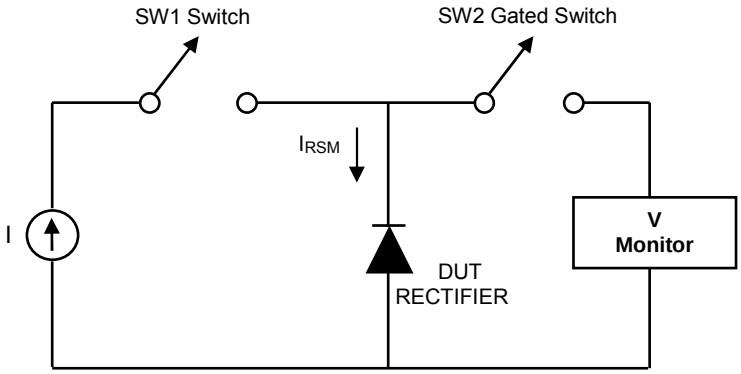

FIGURE 1. Rectangular current pulse test setup.

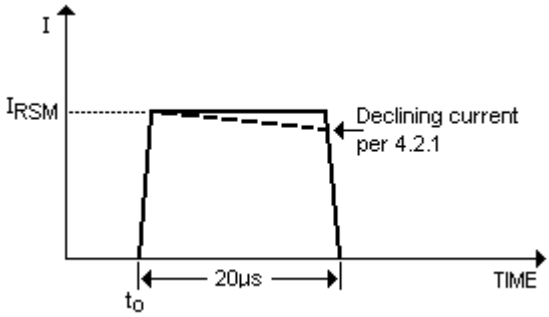

FIGURE 2A. Rectangular 20µs Current Pulse Waveform.

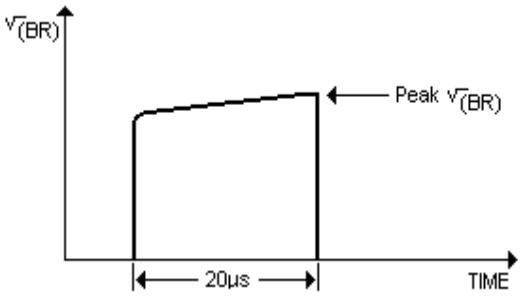

FIGURE 2B. Voltage response.

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METHOD 4066.4

SURGE CURRENT

1. Purpose. The purpose of this test is to subject the device under test (DUT) to high current stress conditions to determine the ability of the device chip and contacts to withstand current surges. This is intended to verify a nonrepetitive surge rating where there is sufficient time between surges to permit the device temperature to return to its original value.

2. Applicability. This test describes three different conditions: A, B, and C. Surge current is applied in the forward direction to signal diodes and rectifier diodes, and in the reverse direction to voltage regulator (zener) diodes. Condition A uses half sinusoidal forward current surges, at low duty factor, applied to either a baseline ac or dc current. Condition B uses rectangular current pulse(s) and is intended primarily for zener diodes or where otherwise applicable. When used with zener diodes, this method utilizes a monitoring circuit to sense possible voltage collapse during the current pulse. Condition C is intended for high current devices that can be applied to either condition A or condition B.

3. Symbols and Definitions. The following symbols and terminology shall apply for the purpose of this test method.

a. d.f: Duty factor = 100 t_p / t_{rep}

b. Duty factor: Applied current surge pulses (in percent).

c. I_F: DC forward current (in A).

d. I_{FRM} AC forward current repetitive peak.

e. I_{FSM}: Nonrepetitive peak value of forward surge current (in A).

f. I_O: Average ac forward current (in A).

g. I_Z : DC reverse zener current (in mA).

h. I_{ZSM}: Nonrepetitive peak value of zener surge current (in mA).

i. n: Number of pulses.

j. t_p: Duration of current surge pulses (in ms).

k. V_{FSM}: Peak forward surge voltage (in V).

l. V_{RSM}: Nonrepetitive peak reverse voltage (in V).

m. V_{RWM} Working peak reverse voltage (in V).

n. V_Z(min): Specified minimum zener voltage.

o. V_{ZSM}: Peak zener surge voltage (in V).

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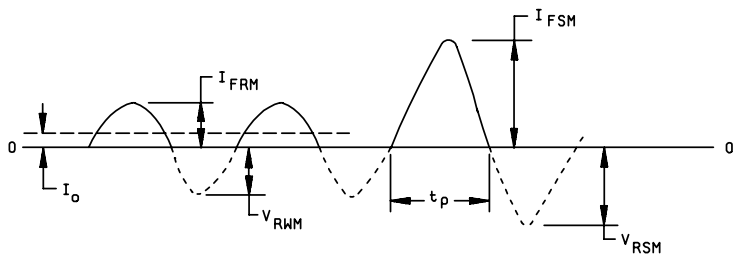
4. Condition A, sinusoidal current surge.

4.1 Apparatus. (As required).

4.2 Procedure. The continuously applied electrical conditions shall be specified and applied to the device under the specified conditions. Unless otherwise specified, the specified number of current pulses (n) shall be superimposed on the continuously applied electrical conditions at the specified duty factor in accordance with figure 4066-1 (condition A1) for rectifiers, or figure 4066-2, (condition A2) for signal and switching diodes, zeners or bridges, as applicable. The surge pulses shall be half-sine waveform and of specified duration (t_p). The duty factor shall be chosen so that the junction temperature is not changed significantly. The "continuously-applied electrical conditions," shall be satisfied if the time of applied current permits the junction temperature rise to be within 10 percent of its final equilibrium value above ambient before each surge or if an additional temperature or surge current is applied beyond that specified to provide equivalent junction temperature heating during surge without the continuous applied electrical conditions. Also reference condition C for the external heating method.



NOTE: Surge current pulse (tp) does not require synchronization with applied baseline ac.

FIGURE 4066-1. Surge pulse applied to continuous halfwave conditions (condition A1).

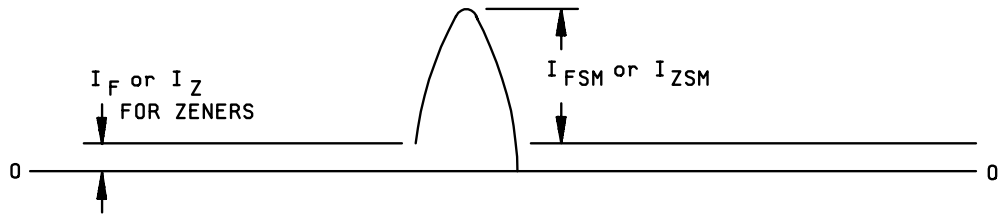


FIGURE 4066-2. Surge pulse applied to continuous dc conditions (condition A2).

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4.3 Test conditions to be specified and recorded. The following conditions shall be specified in the applicable specification sheet:

a. Average forward current (I_O); or dc forward current (I_F) for rectifiers; or zener current (I_Z) for zener diodes; as applicable.

b. Number of current pulses (n).

c. Duration of pulses (t_p), normally 8.3 milliseconds.

d. Duty factor of pulses, normally less than .1 percent, or the period normally between 8 and 60 seconds.

e. Peak value of forward surge current pulse, IFSM for rectifiers, or IZSM for zeners.

f. Nonrepetitive maximum reverse voltage (V_{RSM}), when applicable.

g. Measurements after test.

h. Case, lead, or ambient temperature (T_C, T_L, or T_A), as applicable.

5. Condition B, rectangular current pulse.

5.1 Apparatus. The current source (I) and switch (SW1) combination shown on figure 4066-3 shall be able to apply the peak value of current pulse I_{FSM}or I_Z for the pulse duration (t_p) as required, and shall be able to handle any number of pulses (n) and duty cycle as required in the applicable specification sheet. The rise and fall times of the pulse shall be less than 10 percent of the pulse duration. For zeners, the dashed lines replace the solid connecting lines (vertical) to the DUT. The monitor shall sense V_{ZSM} voltage at the end of the pulse duration before the pulse is removed via gated switch (SW2) to ensure zener voltage has not collapsed below rated $V_{Z(min)}$

5.2 Procedure. As shown on figure 4066-4, no current is applied to the DUT prior to the starting time (t_o) of the test. For zeners, a maximum of 5 percent of rated I_Z may be used for baseline current flow. At t_o, SW1 causes the application of I_{FSM} or I_{ZSM} for time period t_p, after which SW1 causes the current to cease flowing in the DUT. For multiple pulse requirements, SW1 again causes current flow in the DUT after being off for a time necessary to meet the duty factor requirements; this process is repeated for n times as specified. The duty factor and pulse width (t_p) shall be chosen to ensure that the DUT average junction temperature is not changed significantly. For zeners, V_Z monitoring is mandatory. NOTE: If an excessive duty factor is applied where average junction temperature rises with each successive surge, the surge is considered repetitive and must be derated.

5.3 Test conditions to be specified and recorded. The following conditions shall be specified in the applicable specification sheet:

a. The peak surge current (I_{FSM}) for rectifiers or I_{ZSM} for zeners. For rectifiers, this is normally the equivalent rms current as the rated half sine condition. Zeners normally are specified with square wave value of surge current.

b. Number of current pulses (n), shall be five unless otherwise specified.

c. Duration of pulses (t_p), shall be 8.3 ms unless otherwise specified.

d. Duty factor of pulses, normally less than 0.1 percent.

e. V_{ZSM} to be monitored during I_{ZSM} for zeners. A collapse below V_Z (min) is a failure.

f. Measurements after test (see 6.1).

g. Case, lead, or ambient temperature (T_C, T_L, or T_A), as applicable.

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5.4 Alternative to measurements after test. For rectifiers, there is a minor modification to the test that offers the advantage of immediately determining if the DUT survived the test. This consists of monitoring the forward voltage (V_{FSM}) during t_p to determine if device degradation, open-circuit or short-circuit conditions occur. A recorded value of V_{FSM} can be compared to minimum and maximum values in the applicable specification sheet to determine if the device survived the test. NOTE: Zener monitoring is mandatory; it is not an alternative. Collapse below $V_{Z(min)}$ is a failure.

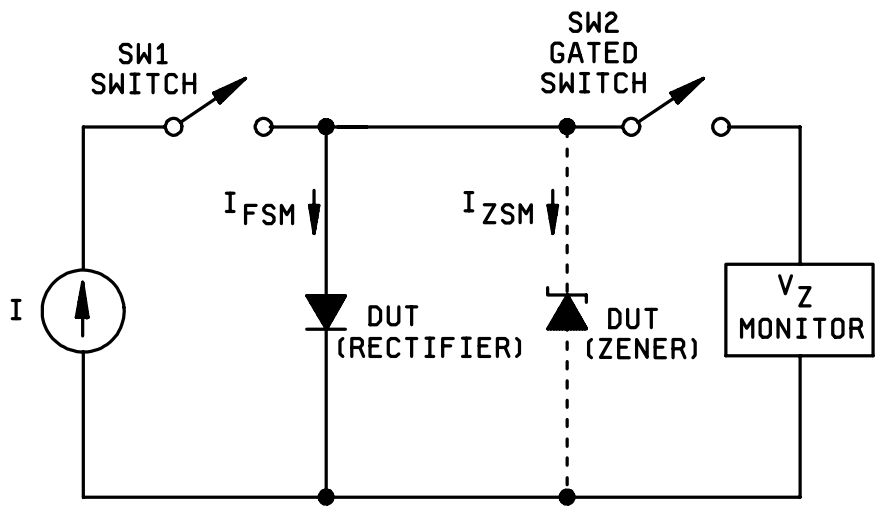

FIGURE 4066-3. Rectangular current pulse test setup.

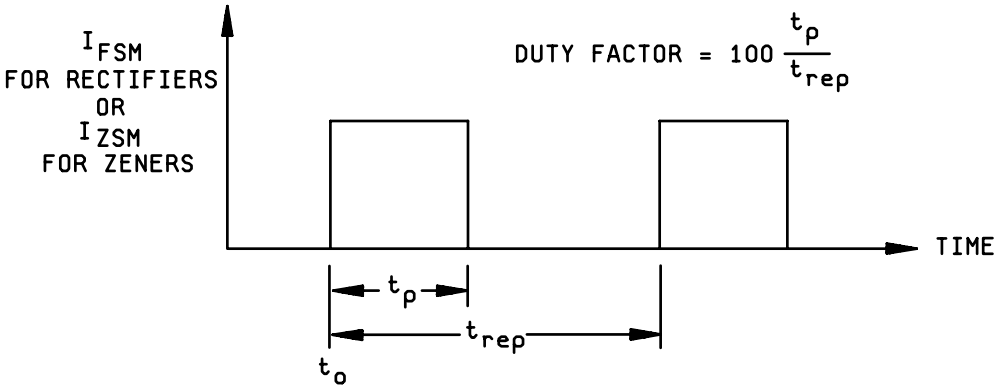

FIGURE 4066-4. Rectangular current pulse waveforms.

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6. Condition C (external heating). The worst case test condition for surge current is for device junction temperature at the rated maximum allowable junction temperature. Test condition A approximates this condition by applying forward current to dissipate power in the DUT. The product of this power dissipation and the device thermal resistance produces a temperature rise of the junction over the case temperature at which the surge test is performed. This represents what actually happens to a device in use. However, the actual junction temperature during the surge current test is only at the rated allowable maximum for those individual devices which have both the worst case maximum forward voltage drop and the worst case maximum thermal resistance. Only a very small percentage of actual devices will truly be worst case. The vast majority of devices will be tested at junction temperatures below rated maximum.

Test condition C avoids this short fall in junction temperature and truly represents worst case operation by externally heating the DUT to the specified rated maximum operating junction temperature of the DUT. Consequently, there is no applied heating current prior to, or concurrent with, the surge current. Once the DUT has stabilized at thermal equilibrium at the specified maximum operating junction temperature, the desired surge current pulses are applied at the specified duty factor. The time between current surges shall be long enough to permit the device junction temperature to return to its original thermal equilibrium.

6.1 Test conditions to be specified and recorded. The following conditions shall be specified in the applicable specification sheet:

a. All conditions defined by the specified test condition in 4.3 or 5.3

b. External heating temperature, T_A.

7. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test condition letter.

b. Case temperature, T_C.

c. Average forward current, I_O, or dc forward current, I_F for rectifiers, or dc zener current I_Z; as applicable for baseline current.

d. Number of current pulses (see 4.3).

e. Duration of pulses (see 4.3).

f. Duty factor of pulses (or time required between pulses).

g. Peak value of forward surge current for rectifiers or I_{ZSM} for zeners.

h. Maximum reverse voltage (non-repetitive), V_{RSM}. (V_{RSM} = 0 for conditions A2 and C.)

i. Measurements after test.

j. Case, lead, or ambient temperature (T_C, T_L, or T_A), as applicable.

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METHOD 4071.1

TEMPERATURE COEFFICIENT OF BREAKDOWN VOLTAGE

1. Purpose. The purpose of this test is to measure the temperature coefficient of breakdown voltage under specified conditions.

2. Apparatus. The apparatus used to measure the temperature coefficient of breakdown voltage shall be capable of demonstrating device conformance to the minimum requirements of the applicable specification sheet.

3. Procedure. The temperature coefficient of breakdown voltage is the percent of the voltage change from the breakdown voltage obtained at the specified reference temperature to the breakdown voltage obtained at the specified test temperatures.

αVZ shall be calculated using the following formula:

$$\alpha VZ = \frac{V_{(BR)(Test\,temperature)} - V_{(BR)(Reference\,temperature)}}{V_{(BR)(Reference\,temperature)}} X \frac{100}{T_{Test} - T_{Ref}} in\,\%/°C$$

Where the reference temperature is the actual ambient (+25°C ±3°C) and the test temperature is the extreme temperature employed in the measurement.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Temperatures.

   b. Test current.

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METHOD 4076.1

SATURATION CURRENT

1. Purpose. The purpose of this test is to measure the saturation current under the specified conditions.

2. Test circuit. See figure 4076-1.

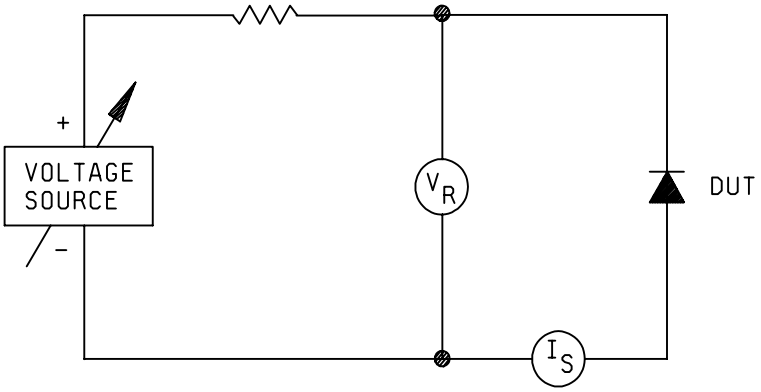

FIGURE 4076-1. Test circuit for saturation current.

3. Procedure. The supply voltage is adjusted until the specified reverse voltage across the diode is achieved. The saturation current is then read from the current meter. Unless otherwise specified, the reverse voltage for measurement of saturation current shall be approximately 80 percent of the nominal breakdown voltage for voltage regulator diodes and approximately 80 percent of the minimum breakdown voltage for rectifiers.

4. Summary. The test voltage (see 3.) shall be specified in the applicable specification sheet:

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METHOD 4081.3

THERMAL RESISTANCE OF DIODES
(FORWARD VOLTAGE, SWITCHING METHOD)

1. Purpose. The purpose of this test is to determine the thermal resistance of lead, case, or surface mounted diodes under the specified conditions.

1.1 Definitions. The following symbols shall apply for the purpose of this test method:

a. D: Heating power duty factor.

b. I_H: Heating current in Amps applied to diode during P_H.

c. I_M: Measuring current in milliamperes.

d. P_C: Magnitude of power in watts applied to diode during measuring and calibration.

e. P_H: Magnitude of heating power in watts applied to diode causing temperature difference T_J - T_R.

f. $R_{\theta JR}$: Thermal resistance, junction-to-reference point, in degrees Celsius/watt.
NOTE: For different package designs, the reference point "R" will be the Lead "L" for axial-leaded packages or leaded-surface-mount packages, the Case "C" for case-mounted packages or surface mounted products mounted by integral electrical contacts in the case (e.g. SMD-.5, SMD-1, SMD-2) , and End Cap "EC" for surface mount MELF style packages.. These package configurations have thermal resistance acronyms of $R_{\theta JL}$, $R_{\theta JC}$, $R_{\theta JEC}$ respectively. Other reference points may also be made such a "Solder Pad" on small surface mount products for $R_{\theta JSP}$.

g. T_{CC}: Case temperature in degrees Celsius, measured at the reference point prior to application of heating power P_H.

h. T_{CH}: Case temperature in degrees Celsius, measured at the reference point after the junction has been heated by P_H.

i. T_J: Junction temperature in degrees Celsius.

j. T_{LC}: Lead temperature in degrees Celsius, measured at the reference point prior to application of heating power P_H.

k. T_{LH}: Lead temperature in degrees Celsius, measured at the reference point after the junction has been heated by P_H.

l. T_{MC}: Calibration temperature in degrees Celsius, measured at reference point.

m. t_{MD}: Measurement delay time in microseconds. This is the delay between when P_H is removed and when the temperature sensitive parameter (TSP) is recorded to determine junction temperature rise (see 3.a).

n. TR: Reference point temperature in degrees Celsius.

o. T_{SP}: Temperature Sensitive Parameter

p. V_{MC}: Value of temperature-sensitive parameter in millivolts, measured at I_M and specific value of T_{MC}.

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q. V_{MH}: Value of temperature-sensitive parameter in millivolts, measured at I_M, and corresponding to the temperature of the junction heated by P_H.

2. Apparatus. The apparatus required for this test shall include the following as applicable to the specified test procedure.

a. Thermocouple material may be copper-constantan (type T), chromal-alumel (type K) or equivalent, for the temperature range -180°C to +370°C. The wire size shall be no larger than AWG size 30. The junction of the thermocouple shall be welded to form a bead rather than soldered or twisted (exception is the type K open junction method where the junction is formed upon each wire's contact with the measured metallic surface). The accuracy of the thermocouple and associated measuring system shall be ±1.0°C.

b. Controlled temperature chamber or heat sink capable of maintaining the specified reference point temperature to within ±1.0°C of the preset (measured) value. For various package mounting configuration examples, see Figure 4081-2 for axial-leaded, Figure 4081-3 and Figure 4081-4 for case mounted, Figure 4081-5 for power SMD mounting, and Figure 4081-6 for small signal LCC surface mounted.

c. Suitable electrical equipment as required to provide controlled levels of conditioning power and to make the specified measurements. The instrument used to electrically measure the temperature-sensitive parameter shall be capable of resolving a voltage change of 1.0 mV. An appropriate sample-and-hold unit or a cathode ray oscilloscope shall be used for this purpose.

3. Procedure. In measuring thermal resistance, the forward voltage is used as the temperature-sensitive parameter (TSP) to indicate the junction temperature (see figure 4081-2 for mounting arrangement).

a. Power application test. The power application test shall be performed in two parts. For both portions of the test, the reference point temperature shall be held constant at the specified value. The value of the temperature-sensitive parameter V_{MC} shall be measured with a measuring current (I_M) that will produce negligible internal heating. The diode under test shall then be operated with heating power (P_H) intermittently applied at a greater than or equal to 0.98 duty factor. The temperature-sensitive parameter V_{MH} shall be measured during the interval between heating pulses with constant measuring current (I_M) applied. The delay time between the heating power turning off and the V_{MH} being read is the measurement delay time t_{MD}.

If it is not possible to maintain the reference point temperature constant during the power application test [such as lead (T_{LH}) or case (T_{CH}) temperature], the difference in the reference temperature at which V_{MH} and V_{MC} are measured shall be recorded. For an axial-leaded device example, the lead temperature difference (T_{LH} - T_{LC}) divided by the average heating power (DP_H) shall be subtracted from the calculated thermal resistance to correct for this error. It is not possible, due to the presence of electrical transients in the voltage waveform, to measure the TSP at the instant that the heating current is removed.

For a particular device type or when the appropriate performance specification does not specify t_{MD}, the shortest t_{MD} time after removal of heating current before the TSP is measured shall be found by performing the test at various power levels and noting the shortest time where the measured value of thermal resistance is essentially independent of power dissipated. Power levels of 25 percent above and below the power corresponding to the specified heating current are recommended for determining this delay time. The junction-to-lead thermal resistance shall therefore be calculated from the value of the temperature-sensitive parameter V_{MH} as measured at the previously determined delay time. This will vary depending on package design and materials, particularly for metal package encapsulations for high power devices involving magnetic materials requiring longer delay time due to switching transients. The heating power (P_H) shall be chosen such that the calculated junction-to-reference point temperature difference as measured at V_{MH} is greater than or equal to +50°C.

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b. Measurement of the temperature coefficient of the temperature-sensitive parameter (calibration). The temperature coefficient of the temperature-sensitive parameter (TSP) shall be measured utilizing the chosen measuring current (I_M) used during the Power Application Test. The DUT shall be externally heated in an oven or on a temperature controlled heat sink. The measuring current shall be chosen such that the TSP varies linearly with temperature over the range of interest and that negligible internal heating ($P_C \approx 0$) occurs during the calibration procedure, i.e., $T_R \approx T_J$. The reference point temperature range used during calibration shall encompass the temperature range encountered in the Power Application Test. The value of the TSP temperature coefficient ($\Delta V_{MC}/\Delta T_{MC}$) shall be calculated from the calibration curve (V_{MC} versus T_{MC}). It can generally be assumed that, for devices of a given design and construction, the temperature coefficient of the TSP is constant. The temperature coefficient shall be measured on 10 devices to validate this assumption. If the relative sample standard deviation of these measurements is less than or equal to ±3 percent, the average of the measured temperature coefficients can be used in the calculation of thermal resistance for all other devices of the design and construction.

c. Calculation of thermal resistance. Examples shown are for thermal resistance junction to lead ($R_{\theta JL}$) for both axial-lead designs and surface mount configurations with very short terminations. Also thermal resistance junction to case ($R_{\theta JC}$) and thermal resistance junction to end cap ($R_{\theta JEC}$) for surface mount MELF packages DO-213AA and DO-213AB JEDEC outlines are described.

3.1 Package considerations and method of calculation.

3.1.1 Axial lead diodes. For axial-lead diodes, the reference point for calculations of the junction-to-lead thermal resistance ($R_{\theta JL}$) shall be at a point on the lead 0.375 inch (9.52 mm) from the body of the diode under test. For thermally unsymmetrical devices, the specified lead temperature shall be the average of the two lead temperatures measured with both leads terminated thermally in the same manner. For surface mount diode packages with short-lead terminations such as J-bends or gull wings, the reference point for calculation of thermal resistance shall be at or near the mounting plain of the terminal configuration of the diode under test. The following equation is used to calculate the junction-to-lead thermal resistance:

$$R_{\theta JR} = \frac{T_J - T_R}{DP_H} = \frac{V_{MH} - V_{MC}}{DP_H} \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]^{-1} Calibration - \left[\frac{T_{LH} - T_{LC}}{DP_H}\right] Optional$$

where V_{MC} is the value of the temperature-sensitive parameter for T_{MC} equal to T_{LC} and $T_{LH} - T_{LC}$ corrects for variations in the lead temperature during the Power Application Test.

3.1.2 Case mounted power diodes. For case-mounted power diodes such as TO-3, stud mounts (DO-4 thru DO-9), and high power surface mount devices (SMD) with a metal bottom for heat transfer, the reference point for calculation of the junction-to-case thermal resistance ($R_{\theta JC}$) shall be at or near the mounting plain and in the heat-flow path to the heat sink for a diode under test. This requires drilling a hole in the component case to insert a thermocouple for accurate measurement as shown in Figure 4081-3, or providing an access-hole in the heat sink to locate the T_R reference point on the case in the heat-flow path as shown in Figures 4081-4 and 4081-5B. The T_{LH} and T_{LC} in 3.1.1 then become T_{CH} and T_{CC} respectively to calculate junction-to-case thermal resistance. The T_{CH} - T_{CC} corrects for possible variations in the case temperature during the Power Application Test. For some of the surface mount designs, an accurate thermal resistance measurement may require soldering the device under test to a heat sink. In these examples, soldering methods should not exceed rated soldering temperatures for the package.

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3.1.3 Low power surface mount. For lower power surface mount packages such as MELFs or LCC devices, this reference point may instead be identified as the end cap temperature (T_{EC}) or the solder pad (T_{SP}) as shown in Figure 4081-6. The T_{LH} and T_{LC} in the above equation would then become T_{ECH} and T_{ECC} or T_{TPH} and T_{TPC} respectively to calculate the junction-to-endcap thermal resistance.

Measurements of T_R and T_{MC} for all examples are made by means of a thermocouple attached to the referenced point. The power dissipation in the DUT is calculated from the equation $P_H = I_H V_F$. If the power dissipation during measuring and calibration is not negligible, then P_C should be subtracted from P_H when calculating the thermal resistance. The P_C is calculated from the equation $P_C = I_M V_M$. The specimen junction-temperature shall be considered stabilized when doubling the time between the initial application of power and the taking of the reading causes no error in the indicated results beyond the required accuracy of measurement. The time for stabilization will typically be 20 to 60 seconds depending on package configuration and size.

3.2 Test circuit. See figure 4081-1.

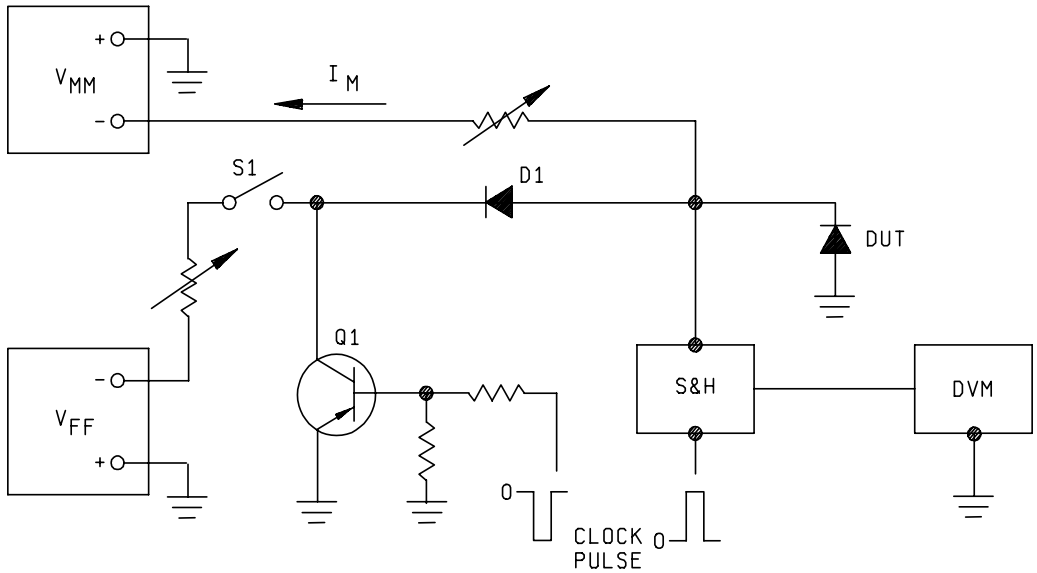

FIGURE 4081-1. Test circuit.

The circuit is controlled by a clock pulse with a pulse width less than or equal to 300 μs and repetition rate less than or equal to 66.7 Hz. When the voltage level of the clock pulse is zero, the transistor Q1 is off and the forward current through the DUT is the sum of the constant heating current and the constant measuring current. Biasing transistor Q1 on, shunts the heating current to ground and effectively reverse biases the diode D1. The sample-and-hold unit (S and H) (or cathode ray oscilloscope) is triggered when the heating current is removed and is used to monitor the forward voltage of the diode under test. During calibration, switch S1 is open.

4. Summary. The following conditions shall be specified in the detail specification:

a. Reference point temperature for heating power measurements.

b. Accept or reject criteria.

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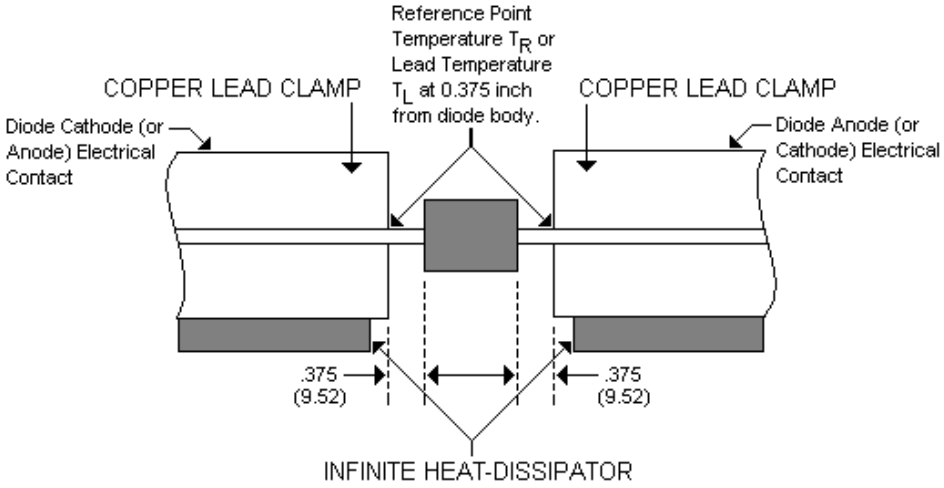

FIGURE 4081-2. Axial-leaded mounting arrangement.

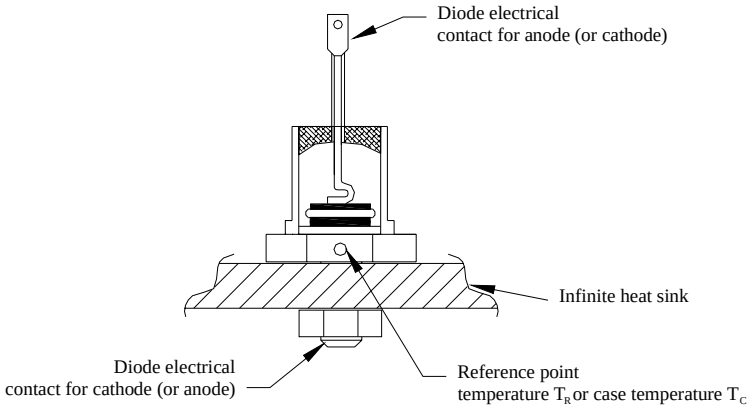

FIGURE 4081-3. Case mounting arrangement. (stud packages).

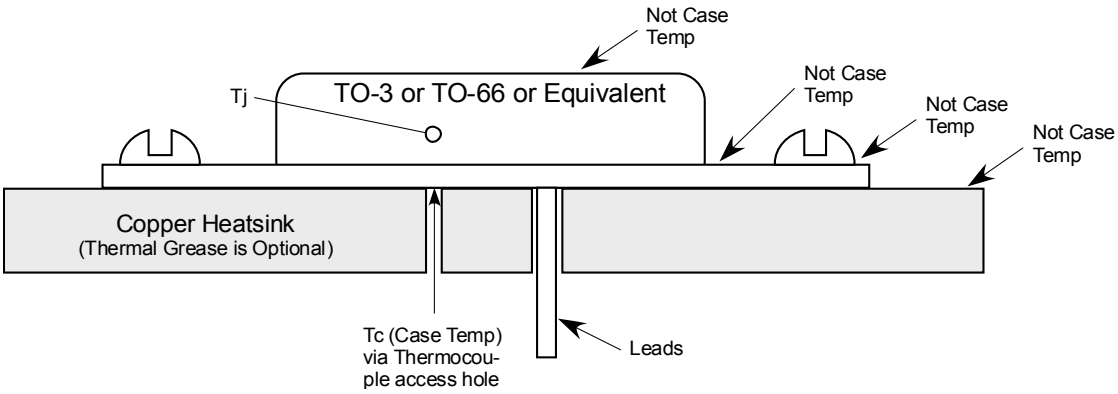

FIGURE 4081-4. Case mounting arrangement. (TO-3 or TO-66).

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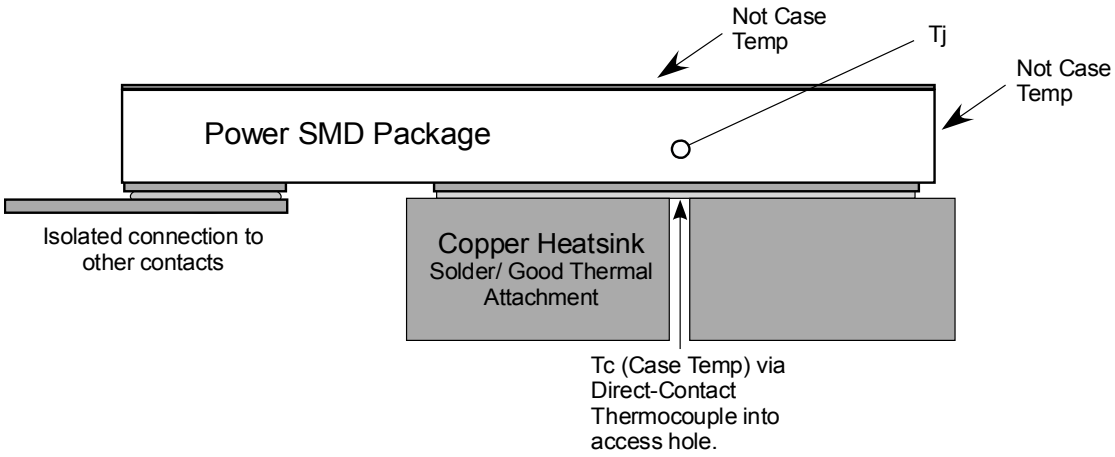

FIGURE 4081-5. Surface-Mount arrangement and Temperature Sensing Location (SMD)

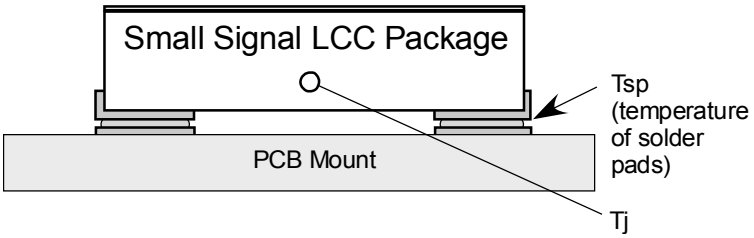

FIGURE 4081-6. Surface-Mount arrangement and Temperature Sensing Location (LCC)

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4100 Series

Electrical characteristics tests for microwave diodes

1. Measurement of conversion loss, output-noise ratio, and other microwave parameters shall be conducted with the device fitted in the holder. All fixed adjustments of the holder shall be made at a laboratory designated by the Government. In the test equipment, the impedance presented to the mixer by the local oscillator (and the signal generator, if used) shall be the characteristic impedance of the transmission line between the local oscillator and mixer (the maximum VSWR, looking toward the local oscillator, shall be 1.05 at the signal and image frequencies).

2. For qualification inspection of reversible UHF and microwave devices, the radio-frequency measurements, excluding the post-environmental-test end points and high-temperature-life (nonoperating) end points, shall be made, first, with the adapter on one end of the device, and then repeated with the adapter at the opposite end of the device; for the environmental and life tests, fifty percent of each sample shall be tested with the adapter on one end of the device and the remaining half of the sample shall be tested with the adapter on the opposite end of the device. End-point measurements shall be made without moving the adapter. This procedure shall be repeated on at least one lot every 6 months.

3. For quality conformance inspection of reversible UHF and microwave devices, the electrical measurements, including the post-environmental-test end points, may be made with the adapter on either end of the device.

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METHOD 4101.3

CONVERSION LOSS

1. Purpose. The purpose of this test is to determine the ratio of the available RF input power to the available IF output power under specified conditions.

2. Test circuits. The following test circuits shall apply. (See figures 4101-1 through 4101-4.)

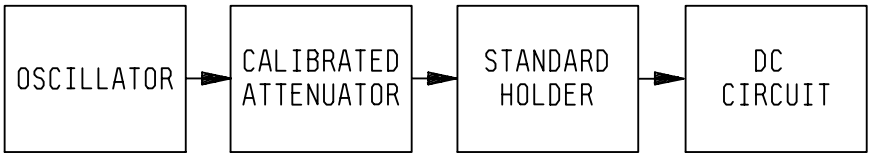

FIGURE 4101-1. Test setup for incremental measurement.

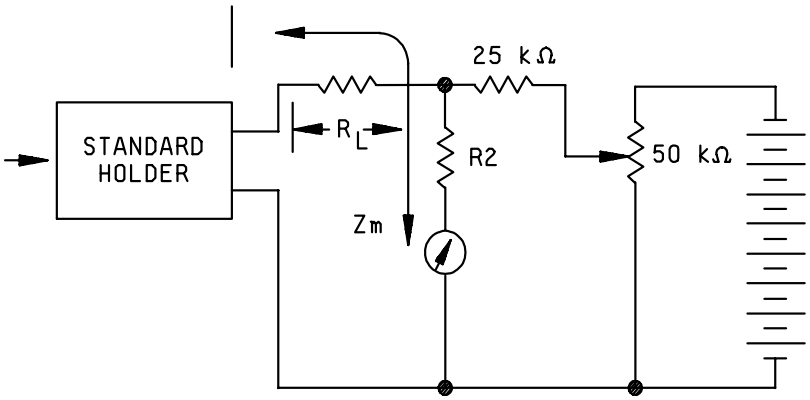

FIGURE 4101-2. Output circuit for the incremental measurement.

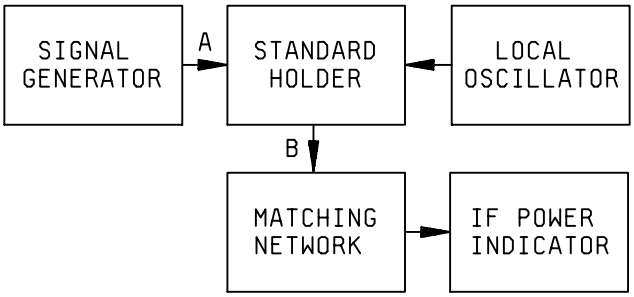

FIGURE 4101-3. Test setup for heterodyne measurement.

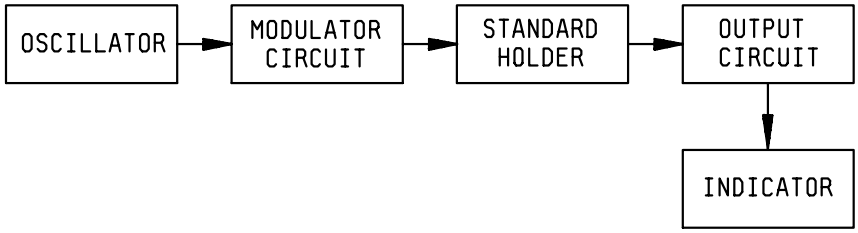

FIGURE 4101-4. Test setup for modulation measurement.

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2.1 Overall noise figure method. See method 4121 for output noise ratio and method 4126 for overall noise figure.

3. Procedure.

3.1 Test condition A (incremental). The equipment for this test is shown in figures 4101-1 and 4101-2. An expression for conversion loss is shown in the equation:

$$L = \frac{G_b}{2P_o\left(\frac{\Delta I}{\Delta P}\right)^2}\left[\frac{4G_b\frac{\Delta I}{\Delta V}}{\left(\frac{G_b+\Delta I}{\Delta V}\right)^2}\right]$$

L = Conversion loss.
ΔI = Incremental change in current.
ΔP = Incremental change in power.

P_o = Average power ($P + 0.5\Delta P$).

$$G_b = \frac{1}{Z_m}$$

$\frac{\Delta I}{\Delta V}$ = IF conductance of diode under test.

IF conductance $= \frac{1}{Z_{if}}$

The diode is loaded by the resistance $R_L + r_2$ that is adjusted to the specified load impedance (Z_m). $Z_m R_L$ is the dc load resistance; load resistance shall be specified. The current supplied by the battery balances out the diode current at some standard power level P, and makes the current in the microammeter zero. With a change in power ΔP, ΔI can be measured directly. With the injection of a small voltage (few millivolts) ΔV at P_o power level, ΔI can be directly measured. (This impedance can be measured by other means. See IF impedance, method 4116, Z_{if}.) These values can be inserted in the equation and the conversion loss can be calculated for the conditions of test.

3.2 Test condition B (heterodyne). A signal generator feeds signal power to the mixer that converts the power to the IF by beating with the local oscillator. The converted power is measured with an IF power meter. Both the available signal power from the generator at A, shown on figure 4101-3, and the increase in the available IF power at B shall be measured when the noise is applied, their ratio being the conversion loss.

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3.3 Test condition C (modulation). The equipment for this test is shown in figure 4101-4. Conversion loss is given by the equation:

$$L = \frac{4n}{(1+n)^2} \bullet \left[\frac{m^2 p}{G_b \ x \ E_B^2}\right]$$

m = modulation coefficient.

P = available power.

E_B = rms modulation voltage across load.

n = ratio of load conductance to IF conductance.

$G_b = \frac{1}{Zm}$

To avoid measuring G_b for each unit, the factor $\frac{4n}{(1+n)^2}$ is assumed to be unity.

The error caused by this approximation is less than 0.5 dB and is in such a direction to make a unit with an extreme conductance seem worse.

$$L = \frac{m^2 p}{G_b E_B^2}$$

Since the modulation coefficient is difficult to measure, this equipment is calibrated with standard diodes measured by any absolute method.

$$L(dB) = 10 \log \frac{(m^2 p)}{(G_b)} = 20 \log E_B$$

A high impedance voltmeter can be used to measure 20 log E_B directly. The voltmeter is set on the 0.01 volt full scale, and the modulation voltage set so that the term 10 log(m^2p/G_p) is equal to 20.0 on the dB scale. To obtain this setting, the modulation is adjusted, so the voltmeter reading on the decibel scale is 20.0 minus the value of conversion loss for the standard diodes. This corresponds to a value of m of 1.58 percent for P = 1.0 mW and G_p = .0025 Ω. The conversion loss for unknown diodes is then 20.0 minus the reading of the output meter in decibels.

3.4 Test condition D (overall-noise-figure). The overall-noise-figure method derives the conversion loss by known properties of the apparatus and is expressed by the equation:

$$\overline{F}_o = L(N + \overline{F}_i - 1)$$

Where:

L = conversion loss of the mixer.

N = output noise ratio of the diode.

F_i = noise figure of the IF amplifier.

L is measured as described in method 4101 and N is measured as described in method 4121.

All terms are ratios.

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4. Detail drawings. The following drawings, as applicable, are used in the performance of this test: JAN 103, 107, 124, 174, 233, 234, and 266; DESC D64100, C64169, D65019, C65042, D65084, C65101, C65017, and C66053.

5. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test condition (see 3.).

   b. Load impedance (Z_m) (see 3.1).

   c. Local oscillator power (see 3.2).

   d. Load resistance (R_L) (see 3.1).

   e. Local oscillator frequency (see 3.2).

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METHOD 4102

MICROWAVE DIODE CAPACITANCE

1. Purpose. The purpose of this test is to measure the low frequency capacitance of a semiconductor diode. The capacitance is the small signal capacitance of the diode as measured in a defined test holder under specified bias conditions.

2. Test circuit. A bridge or meter should be used for the measurement. The specified signal level at the diode terminals, as measured with a suitable voltmeter, should be low enough so that a doubling of the level produces no measurable change in either the capacitance or shunt conductance of the diode. The test holder should be constructed so that the fringing capacitance is not altered by inserting the diode.

3. Procedure. The measurement shall be made at a specified frequency and bias voltage. A low frequency capacitance bridge or meter is used to measure the capacitance of the diode at a specified bias point. The effective case capacitance is measured in the same test holder as the diode. Junction capacitance may be determined by subtracting the effective case capacitance from the total measured capacitance.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Frequency (see 3.).

   b. Bias voltage (see 3.).

   c. Signal level at diode terminals (see 2.).

   d. Bias point (see 3.).

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METHOD 4106

DETECTOR POWER EFFICIENCY

1. Purpose. The purpose of this test is to measure the detector power efficiency.

2. Test circuit. See figure 4106-1.

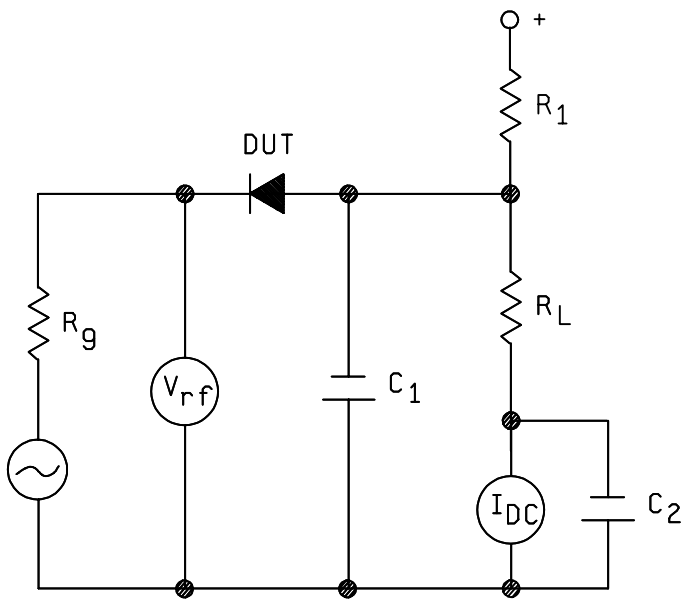

FIGURE 4106-1. Test circuit for detector power efficiency.

3. Procedure. Resistor R_L and capacitor C_1 comprise the load circuit and shall be as specified. Resistor R_1, in conjunction with R_L, provides the specified bias current for the DUT. Capacitor C_2 provides RF bypass for the output current meter I_{DC}. The frequency and amplitude of the ac signal and the output impedance of the generator shall be as specified. The change in output current I_{dc} is measured when the ac signal is applied.

$$Then:\ Detector\ power\ efficiency = \frac{4(\Delta I_{DC})^2 R_L R_G}{V^2 rms} x\ 100\ percent.$$

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Values for circuit components R_L and C_1 (see 3.).

   b. Bias current (see 2.).

   c. Frequency and amplitude of ac signal (see 3.).

   d. Impedance of signal generator (see 3.).

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METHOD 4111.1

FIGURE OF MERIT (CURRENT SENSITIVITY)

1. Purpose. The purpose of this test is to measure the figure of merit of a semiconductor detector diode. The figure of merit is as follows:

$$M = \frac{\beta R_V}{\sqrt{R_V + R_a}}$$

2. Test circuit. The following test circuit shall apply. (See figure 4111-1.)

NOTE: For power calibration.

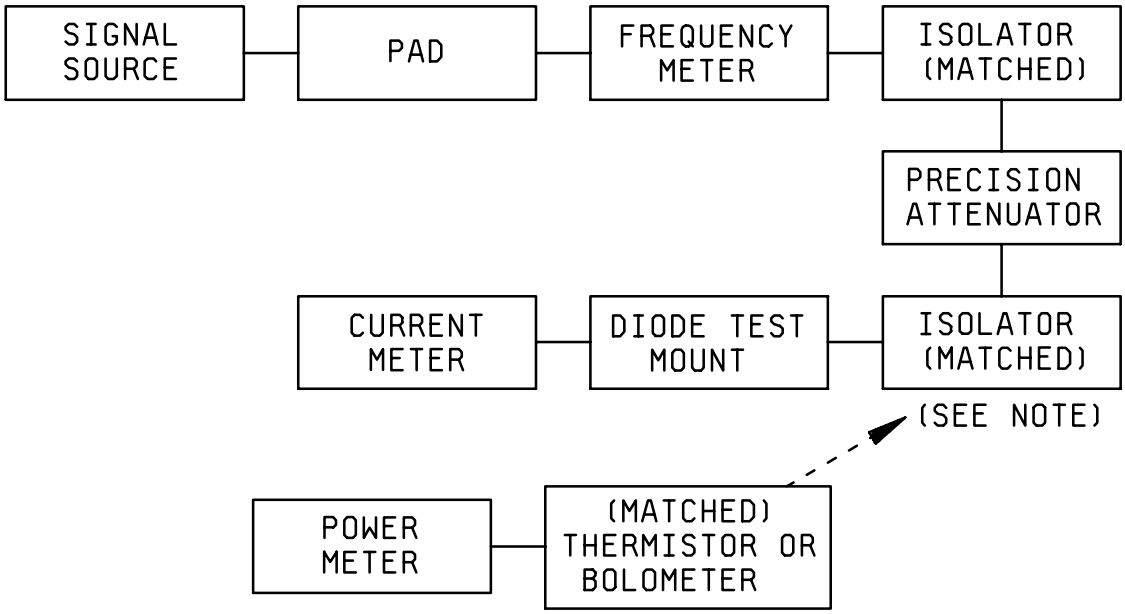

FIGURE 4111-1. Test setup for figure of merit measurement.

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3. Procedure. The equipment for this test is shown on figure 4111-1. A continuous wave (cw) radio frequency (rf) signal is applied to the detector whose output short circuit current is measured and the short circuit current sensitivity (ß) is computed. The figure of merit (M) is then determined from:

$$M = \frac{\beta R_V}{\sqrt{R_V + R_a}}$$

Approximate method:

$$M = \beta\, 2\sqrt{R_X}\ \frac{1 + 1/2\zeta}{\sqrt{1+\zeta}}$$

Where:

ß = i/P

and

i = short circuit diode current

P = power incident at the diode holder

Where:

$$R_X = \frac{1}{\sqrt{(R_1 + R_a)(R_2 + R_a)}}$$

and

R_1 = lower limit of video resistance

R_2 = upper limit of video resistance

R_a = equivalent amplifier noise generating resistance.

and where:

$$\frac{1 + 1/2\zeta}{\sqrt{1+\zeta}}\ \textit{is the correction factor}$$

and:

$$\zeta = \frac{R_V + R_a}{R_X} - 1$$

When the extreme values of the video resistance for a given diode type are known, it is possible to relate figure of merit to rectified current if other conditions are satisfied.

For all normal ranges of video resistance, the correction factor is very close to unity and an approximation:

$$M = 2\beta\sqrt{R_X}$$

therefore, the figure of merit (M) may be determined by measuring the rectified current under proper conditions.

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4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test oscillator frequency (see 2.).

   b. Maximum permissible test oscillator power (see 2.).

   c. DC bias if supplied by an external source.

   d. Ra, if other than 1,200Ω.

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METHOD 4116.1

INTERMEDIATE FREQUENCY (IF) IMPEDANCE

1. Purpose. The purpose of this test is to measure the real part of the impedance at the IF output terminals of the mixer diode under test.

2. Test circuit. The following test circuits shall apply. (See figures 4116-1 and 4116-2)

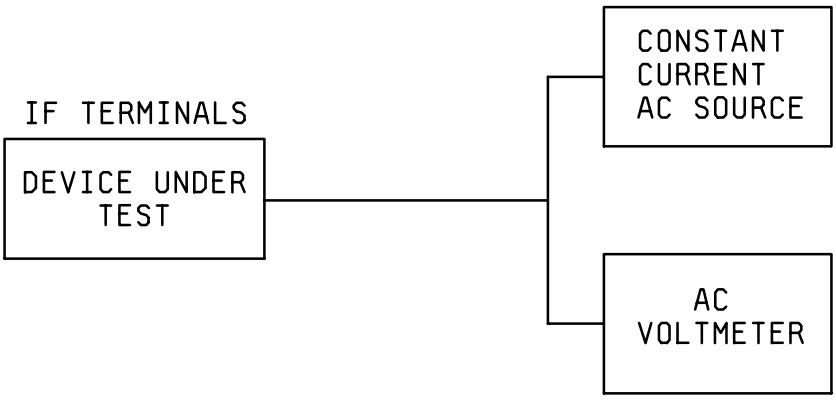

FIGURE 4116-1. AC method.

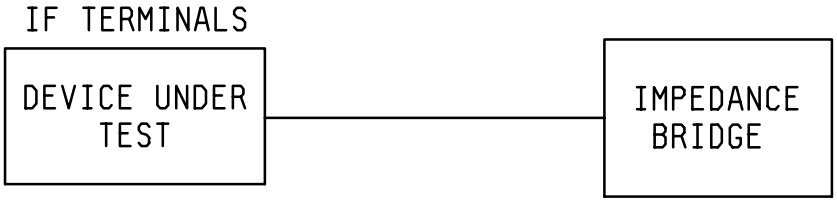

FIGURE 4116-2. Impedance bridge method.

3. Procedure. Since the IF resistance is the slope of the mixer diode's I-V characteristic under the specified test conditions, the requirement of any measuring technique is to measure the slope without affecting the operating characteristics of the DUT. At all times, the device holder RF input port should see a broadband match (minimum of two times IF frequency). The IF test frequency, local oscillator frequency, and power shall be specified.

3.1 Test condition A (ac). With equipment arranged as shown on figure 4116-1, a constant current ac generator is coupled to the diode under test. The dc and ac diode loads are arranged as specified and the ac current is set at a level low enough so that halving the level produces a change in the measured IF impedance of the diode of less than 5 percent. The IF impedance is calculated as follows:

$$Z_{if} = \frac{V}{I}$$

Where:

Z_{if} = diode IF impedance.
V = measured ac voltage.
I = ac current.

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3.2 Test condition B (impedance bridge). The equipment is arranged as shown on figure 4116-2. The impedance bridge signal level is adjusted to a low level using the same criterion in 3.1. The diode IF impedance is determined from the impedance bridge.

4. Detail drawings. The following drawings, as applicable, are used in the performance of this test: JAN 107, 124, 174, 233, 234, and 266; DESC D64100, C64169, D65019, C65042, D65084, C65101, C65017, and C66053.

5. Summary. The following conditions shall be specified in the applicable specification sheet.

a. Test condition (see 3.).

b. Local oscillator frequency (see 3.).

c. Local oscillator power or diode rectified current (see 3.).

d. DC load resistance (see 3.1 and 3.2).

e. AC load impedance (see 3.1 and 3.2).

f. IF test frequency (see 3.).

g. DC bias, if applicable.

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METHOD 4121.2

OUTPUT NOISE RATIO

1. Purpose. The purpose of this test is to measure the output noise ratio of a mixer diode. Since the output noise ratio is a measure of the excess noise generated by a mixer diode in its normal operating condition, the measurement should be in the appropriate standard holder.

2. Test circuit. The following test circuits shall apply. (See figures 4121-1 and 4121-2.)

FIGURE 4121-1. Direct measurement method.

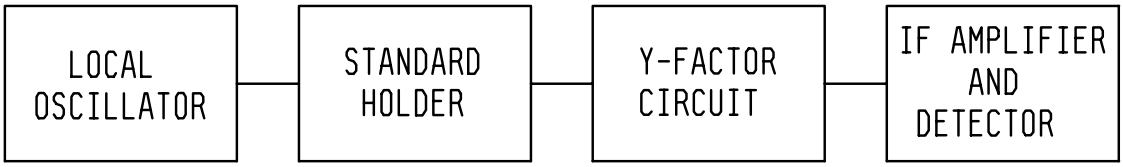

FIGURE 4121-2. Y-factor method.

3. Procedure.

3.1 Test condition A (direct measurement). In this method, the output noise ratio is determined by establishing a reference output reading on the output meter shown on figure 4121-1, with the diode operating under specified test conditions, then a resistor equal to the specified IF impedance of the diode is substituted for the diode. The resistor becomes noisy when the current passes from a noise diode (temperature limited diode). Value for noise resistor shall be specified. The current is adjusted to provide the reference output reading and the noise ratio is computed from the relationship:

$$N = \frac{e\,IR}{2\,kT_o} + 1 = 20\,IR + 1$$

Where:

T_O = +293°K ±5°K and I is the current of the noise diode in amperes.

R = the resistance of the noise resistor.

k = Boltzmann's constant (1.38 x 10^{-23} joules per °K).

e = the electronic charge (1.6 x 10^{-19} coulombs).

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3.2 Test condition B (computational). In this method, the output noise ratio is determined from the equation:

$$N = \frac{\bar{F}_o}{L} - \bar{F}_i + 1$$

Where:

$\bar{F}_o$ = overall receiver noise figure.

L = diode conversion loss.

$\bar{F}_i$ = noise figure of the IF amplifier.

All terms are ratios.

$\bar{F}_o$ and $\bar{F}_i$ are determined as described in method 4126; L is determined as described in method 4101.

3.3 Test condition C (Y-factor). In this method, the output noise ratio is determined by establishing a reference output reading on the output meter shown on figure 4121-2, with the diode operating under specified test conditions, then a resistor equal to the specified IF impedance of the diode is substituted for the diode by a switch in the Y-factor circuit. The output noise ratio is then determined from:

$$N = \bar{F}_i (Y - 1) + 1$$

where:

$$Y = N_{oc}/N_{or}$$

N_{oc} is the reference output reading on the output meter with the diode connected to the circuit.

N_{or} is the output reading with the resistor connected to the circuit.

$\bar{F}_i$ is determined as described in method 4126.

All terms are ratios.

4. Detail drawings. The following drawings, as applicable, are used in the performance of this test: JAN 103, 107, 124, 174, 233, 234, and 266; DESC D64100, C64169, D65019, C65042, D65084, C65101, C65017 and C66053.

5. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test condition (see 3.).

b. Local oscillator frequency (see 2.).

c. Local oscillator power (see 2.).

d. IF frequency (see 2.).

e. Value for noise resistor (see 3.1).

f. DC bias, if applicable.

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METHOD 4126.2

OVERALL NOISE FIGURE AND NOISE FIGURE OF THE IF AMPLIFIER

1. Purpose. The purpose of this test is to measure the overall noise figure of a mixer diode and the noise figure of the associated IF amplifier. Since the noise figure of a network is defined as follows:

$$\overline{F}_O = \frac{(available\,input\,signal\;power)/(available\,input\,noise\,power)}{(available\,output\,signal\;power)/(available\,output\,noisepower)}$$

it is necessary to measure the noise power that is actually delivered to the output termination. This measurement is divided by a similar measure of the output noise that would have been obtained if the network were noiseless and only transmitted the thermal noise of the input termination. In making noise figure measurements, the standard practice is to provide matched impedance at the signal and image frequencies and make suitable corrections (by calculations or appropriate filtering) to obtain an equivalent single-side-band noise figure. The noise figure obtained without a signal band-pass filter to eliminate the image-frequency band is commonly referred to as the double-side-band noise figure and is approximately 3 dB smaller than the single-side-band noise figure, depending on the exact transmission characteristics of the particular mixer. If a single-side-band noise figure is being measured directly, it is necessary to terminate the image resistively in a matched load (isolator) to avoid errors due to second-order effects. These second-order effects may arise from reflection of the image back into the mixer to give a larger or smaller than true value of noise figure, depending on the phase of the reflected image.

2. Apparatus. The apparatus shall be arranged as follows. (See figure 4126-1.)

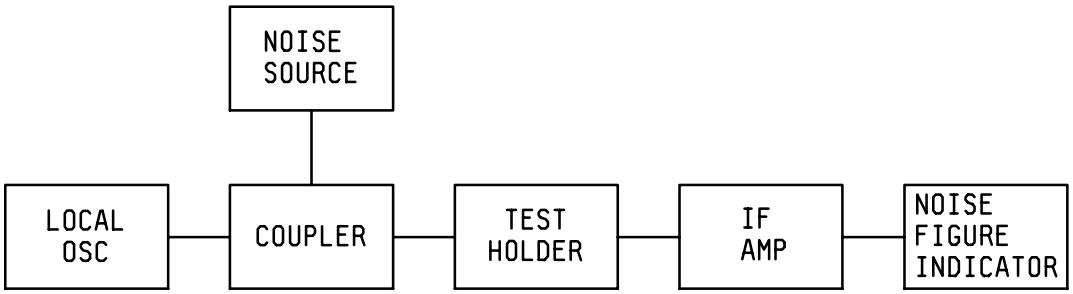

FIGURE 4126-1. Test setup for overall noise figure.

3. Procedure. When using test conditions A and C, the local oscillator frequency and power, IF, and excess noise ratio of noise source shall be specified.

3.1 Test condition A (dispersed-signal-source). A signal source with available power dispersed uniformly over the pass band of the network, and calibrated in terms of available power per unit bandwidth, is used to determine that portion of the output noise power that results from the input termination noise. Suitable dispersed-signal generators are thermionic-noise diodes, gas discharge tubes, resistors of known temperature, or an oscillator whose frequency is swept through the band at a uniform rate. Single-side-band noise figure is obtained by adding 3 dB to the measured (double-side-band) noise figure. At all times, the device holder rf input should see a broadband match (minimum of two times IF frequency).

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3.2 Test condition B (computation). Assuming the IF amplifier noise figure is known, the overall noise figure can be computed as follows:

$$\overline{F}_O = L\left(N + \overline{F}_i - 1\right)$$

Where:

L = diode conversion loss.

N = output noise ratio of the diode.

$\overline{F}_i$ = noise figure of the IF amplifier.

L is measured as described in method 4101 and N is measured as described in method 4121.

All terms are ratios.

3.3 Test condition C (IF amplifier noise figure). Resistors in the particular diode type cases are required, constructed so that when they are inserted in the standard holder (mixer), the output susceptance of the holder is approximately the same as when the diodes are inserted. A sufficient number of resistors should be used so that the output conductance of the standard holder may be finely varied over the specified maximum range for the diode type. A common junction (defining the mixer IF port) joins the holder to the IF amplifier and the noise (temperature-limited diode). The entire circuit, including the noise diode power supply and the current meters, shall be well shielded or filtered to avoid IF feedback. With the resistor in the holder, the IF amplifier gain is adjusted to give an output meter reference reading near full scale. Precise IF attenuation is then inserted, and the noise diode turned on and adjusted in emission to restore the output meter reference reading. The average (dc) noise anode current is then noted and used to compute the IF average noise figure from:

$$F_i = 1 + \frac{eIR}{2kT_o(A-1)} - \frac{T_a}{T_o}$$

$$F_i = 1 + \frac{20IR}{A-1} - \frac{T_a}{T_o}$$

Where:

F_i = noise figure of the IF amplifier (power ratio).

e = electronic charge (1.6×10^{-19} coulombs).

k = Boltzmann's constant (1.38×10^{-23} joules per °K).

T_o = standard noise temperature (+293°K).

T_a = temperature of resistor (°K).

A = inserted IF attenuation (power ratio).

I = average (dc) noise diode current (amperes).

R = reciprocal of IF conductance (ohms).

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4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test condition (see 3.).

   b. Local oscillator frequency (see 3.).

   c. Local oscillator power (see 3.).

   d. IF (see 3.).

   e. DC bias, if bias is supplied by an external source.

   f. Excess noise ratio of noise source (see 3.).

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METHOD 4131.1

VIDEO RESISTANCE

1. Purpose. The purpose of this test is to measure the video resistance of the device. Video resistance shall be defined as the reciprocal of the slope of the current versus voltage characteristic curve at the operating point.

2. Test circuits. The test circuits shall be as follows. (See figures 4131-1 through 4131-4.)

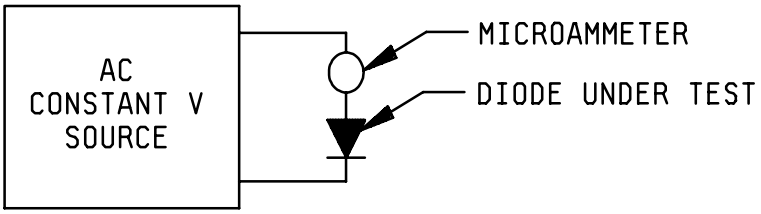

FIGURE 4131-1. Constant voltage method.

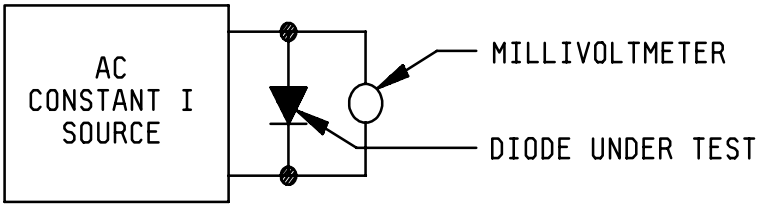

FIGURE 4131-2. Constant current method.

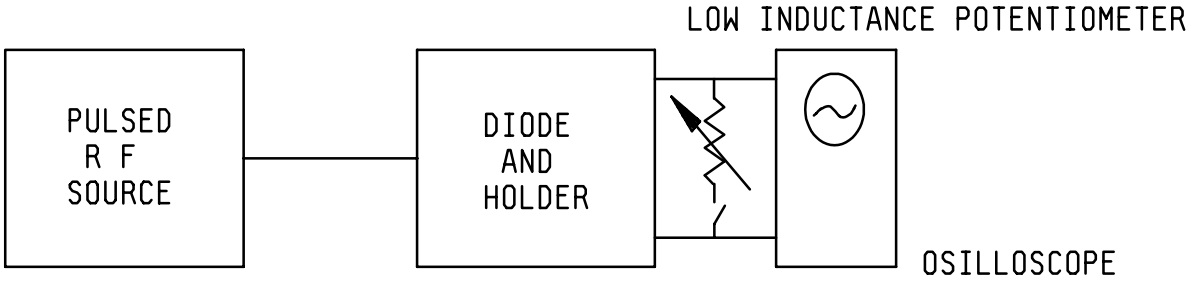

FIGURE 4131-3. Pulsed RF method.

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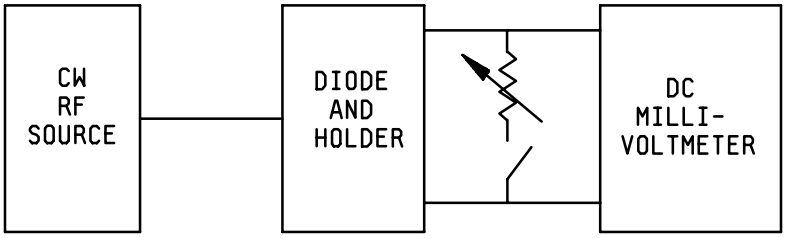

FIGURE 4131-4. Continuous wave RF method.

3. Procedure. The measurement shall be made with the diode operating under the specified test conditions. The applied signal used and the instrument impedance shall be such that doubling or halving their value does not change the video impedance by more than ±5 percent.

3.1 Test condition A (constant voltage). Test equipment used is shown on figure 4131-1. A small specified ac signal is applied to the diode from a constant voltage source. Current is measured with a low resistance microammeter. R_V equals e/i.

3.2 Test condition B (constant current). Test equipment used is shown on figure 4131-2. A small specified ac current is passed through the diode from a constant current source. The voltage is measured across the device with a high impedance millivoltmeter. R_V equals e/i.

3.3 Test condition C (pulsed rf). Test equipment used is shown on figure 4131-3. A pulsed rf signal, as specified, is fed to the diode whose output is fed into the vertical amplifier of an oscilloscope. A resistor is placed in parallel with the device and varied to lower the rectified pulse to half its value. R_V equals the resistance required to halve the pulse. Bandwidth of vertical amplifier should be a minimum of two times the reciprocal of the pulse width.

3.4 Test condition D (continuous wave (cw) radio frequency (rf)). Test equipment used is shown on figure 4131-4. A specified cw rf signal is applied to the detector whose output open circuit rectified voltage is measured on a high impedance dc millivoltmeter. A resistor is placed in parallel with the device and varied to lower this voltage to half its initial value. R_V equals the resistance required to halve the voltage.

4. Summary. The following conditions shall be included in the applicable specification sheet:

a. Test condition (see 3.).

b. Maximum signal voltage (see 3.1).

c. Maximum current (see 3.2).

d. Maximum power (see 3.3 and 3.4).

e. DC bias, if applicable.

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METHOD 4136.1

STANDING WAVE RATIO (SWR)

1. Purpose. The purpose of this test is to measure the SWR of the device at the local oscillator terminals. SWR shall be defined as the ratio of the maximum voltage (or current) to the minimum voltage (or current) along the transmission line between the device and the local oscillator terminals. The measurement shall be made with the diode operating under normal operating conditions.

2. Test circuits. The test circuits shall be as follows: (See figures 4136-1, and 4136-2)

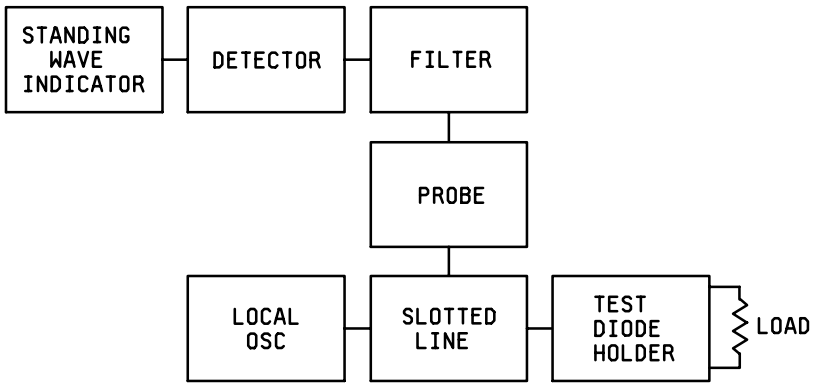

FIGURE 4136-1. Slotted line method.

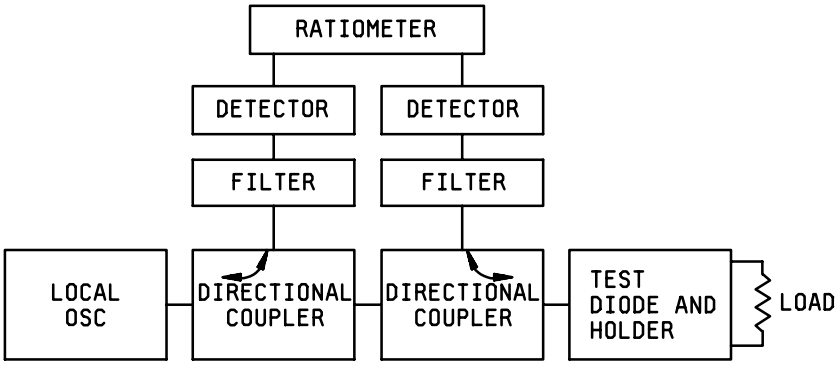

FIGURE 4136-2. Reflectometer method.

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3. Procedure.

3.1 Test condition A (slotted line). A slotted line is inserted between the device in its holder and the local oscillator, and the probe is moved to determine the maximum and minimum voltage or current points. To limit probe errors and keep the power in the slotted line section at a level high enough to operate the standing wave indicator and low enough to maintain small signal conditions, the normal signal generator and indicator connections to the slotted line as shown on figure 4136-1 should be interchanged. That is, the signal generator should be connected to the moving probe and the detector indicator should be connected to the slotted line section opposite the test diode holder.

a. The power source may be used without modulation if a sensitive galvanometer is substituted for the standing wave indicator (tuned voltmeter).

b. The dc load resistance is set to that specified.

c. Insert diode into test holder.

d. Adjust frequency and power level to those specified.

e. Move the probe in the slotted line until the standing wave indicator shows at voltage maximum (or current). Adjust the range switch and gain until an SWR of 1 is indicated.

f. Move the probe until a minimum is indicated.

g. Read the SWR directly at the minimum point.

3.2 Test condition B (reflectometer). A calibrated reflectometer is inserted between the device in its holder and the local oscillator; then the SWR is read, see figure 4136-2.

a. Adjust frequency and power level to those specified.

b. The dc load resistance is set to that specified.

c. Insert diode into the test holder.

d. The reflection coefficient and the SWR can be read directly.

NOTE: When this technique is used, the filter detector combination shall have an SWR <1.2.

4. Summary. The following conditions shall be as specified in the-applicable specification sheet:

a. Test condition (see 3.).

b. DC load resistance (see 3.1 and 3.2).

c. Test frequency (see 3.1 and 3.2).

d. Power level (see 3.1 and 3.2).

e. Maximum voltage (or current), if applicable.

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METHOD 4141.1

BURNOUT BY REPETITIVE PULSING

1. Purpose. The purpose of this test is to determine the capabilities of the device to withstand repetitive pulses.

2. Test circuit. See figure 4141-1.

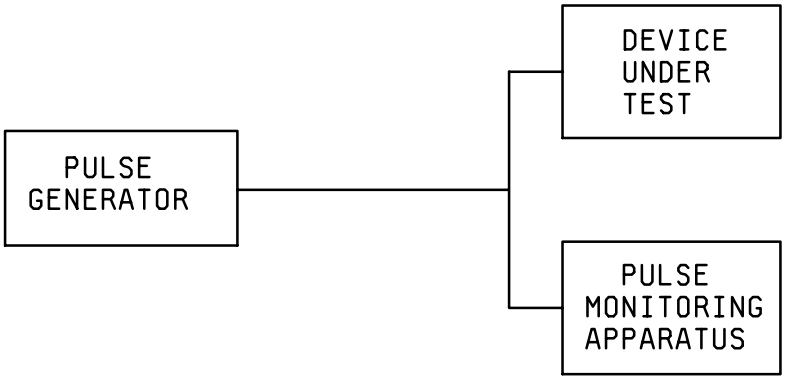

FIGURE 4141-1. Test setup for repetitive pulsing.

3. Procedure. This method shall be acceptable to determine the device capability to withstand repetitive pulses. The general method of measuring device capability to withstand burnout by repetitive pulsing is to apply the specified number of pulses to the DUT and then measure the specified electrical parameters. The pulse polarity shall be such as to cause the current to flow in the forward direction. When the maximum change in the specified electrical parameter is exceeded, the device shall have failed to meet this burnout test. The pulse generator source impedance shall be specified. While the device to be tested is not in the circuit, adjust the pulse generator output for the specified open-circuit pulse voltage, pulse width, and pulse repetition rate. Then insert the device in the circuit. The device shall be left in the circuit for a minimum specified time.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Pulse generator source impedance (see 3.).

   b. Pulse width (see 3.).

   c. Pulse voltage (see 3.).

   d. Pulse repetition rate (see 3.).

   e. Minimum time that the device is under test (see 3.).

   f. Polarity of applied pulse (see 3.).

   g. Minimum pulse energy per pulse absorbed by diode, if applicable.

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METHOD 4146.1

BURNOUT BY SINGLE PULSE

1. Purpose. The purpose of this test is to determine the capability of the device to withstand a single pulse.

2. Test circuit. The test circuit shall be as follows: (See figure 4146-1)

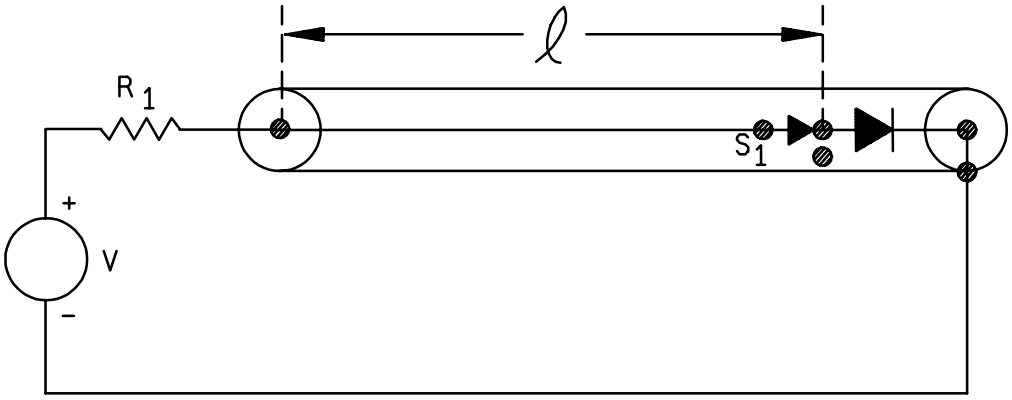

FIGURE 4146-1. Burnout by single pulse.

3. Procedure. The device shall be subjected to a pulse from the coaxial line shown on figure 4146-1. The line shall be charged with the specified voltage, and the contact shall be made by dropping the center conductor vertically from a height of 2 ±.05 inches (50.8 ±1.27 mm) above the contact position. The electrical and mechanical connection shall be such as to have a minimum effect on the free fall of the conductor. The polarity of the inner conductor with respect to the outer conductor shall be such as to cause the device current to flow in the forward direction or as specified.

4. Detail drawings. DSCC drawings B66054 and C66058 as applicable, are used to perform this test.

5. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test voltage (see 3.).

   b. Polarity, if required.

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METHOD 4151

RECTIFIED MICROWAVE DIODE CURRENT

1. Purpose. The purpose of this test is to measure the rectified microwave diode current under conditions for conversion loss.

2. Apparatus. The apparatus used for this test should be capable of demonstrating device conformance to the minimum requirements of the applicable specification sheet.

3. Procedure. The rectified microwave diode current shall be measured under the conditions for conversion loss. The test shall be conducted in the mixer shown on the specified drawing under the conditions specified for the conversion loss test.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test apparatus (see 2.).

   b. Conversion loss test conditions (see 3.).

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4200 Series

Electrical characteristics tests for thyristors (controlled rectifiers)

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METHOD 4201.2

HOLDING CURRENT

1. Purpose. The purpose of this test is to measure the holding current of the device under the specified conditions.

2. Test circuit. See figure 4201-1.

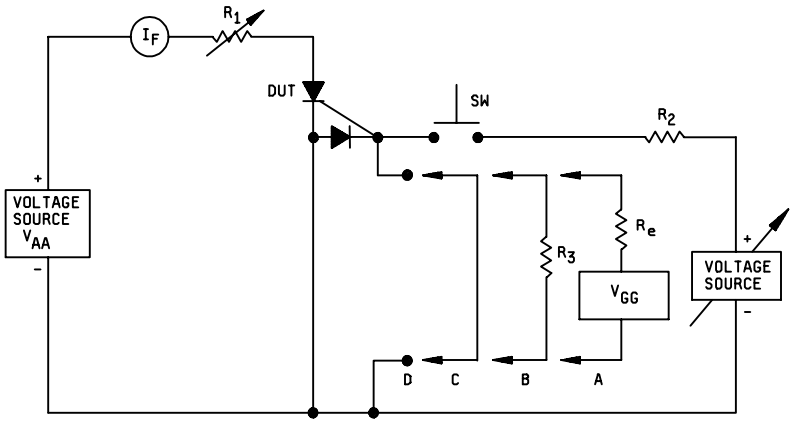

FIGURE 4201-1. Test circuit for holding current.

3. Procedure. The anode supply voltage is set at its specified value with resistance R_1 adjusted so that the initial forward current, I_{F1}, which flows when the device is triggered, equals the value specified. Switch SW is then momentarily closed to trigger the device and reopened. The initial current is quickly reduced to the specified test current I_{F2}. Then the specified gate bias condition is applied. The resistance R_1 is then gradually increased, until the device turns off. The value of forward current immediately prior to turn-off is the holding current.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Anode supply voltage, V_{AA}.

b. Initial forward current, I_{F1}.

c. Forward test current, I_{F2}.

d. Bias condition, gate to cathode, as applicable:

A: Bias (specify V_{GG}, gate-to-cathode polarity, equivalent bias circuit resistance, R_e).

B: Resistance return (specify value of R_3).

C: Short-circuit.

D: Open-circuit.

e. Gate trigger source voltage, open circuit magnitude and pulse width.

f. Total gate trigger circuit resistance, R_2.

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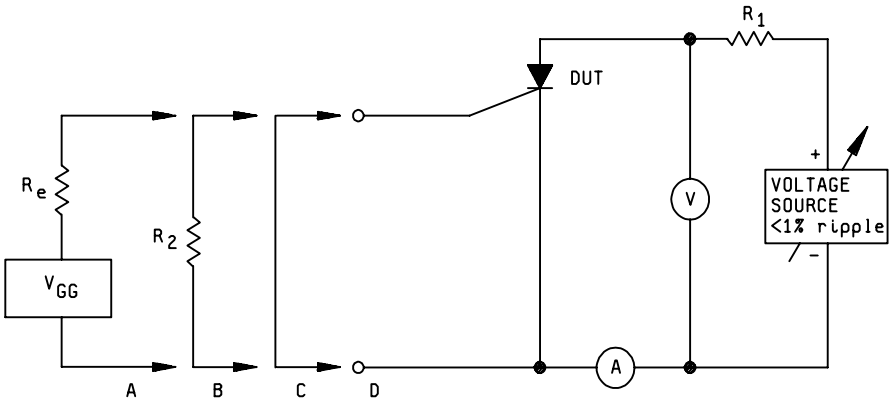
METHOD 4206.1

FORWARD BLOCKING CURRENT

1. Purpose. The purpose of this test is to measure the forward blocking current under the specified conditions, using the dc method or the ac method, as applicable.

2. DC method.

2.1 Test circuit. R_1 shall be chosen to limit the current flow in the event the device switches to the on state. (See figure 4206-1)



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 4206-1. Test circuit for forward blocking current (dc method).

2.2 Procedure. The supply voltage is adjusted to obtain the specified value of forward voltage across the device with the specified gate bias condition applied (see figure 4206-1). The forward blocking current is then read from the current meter.

2.3 Summary. The following conditions shall be specified in the applicable specification sheet:

a. DC method.

b. Test voltage.

c. Bias condition, gate-to-cathode, as applicable:

A: Bias (specify V_{GG}, gate-to-cathode polarity, equivalent bias circuit resistance, R_e).

B: Resistance return (specify value of R_2).

C: Short-circuit.

D: Open-circuit.

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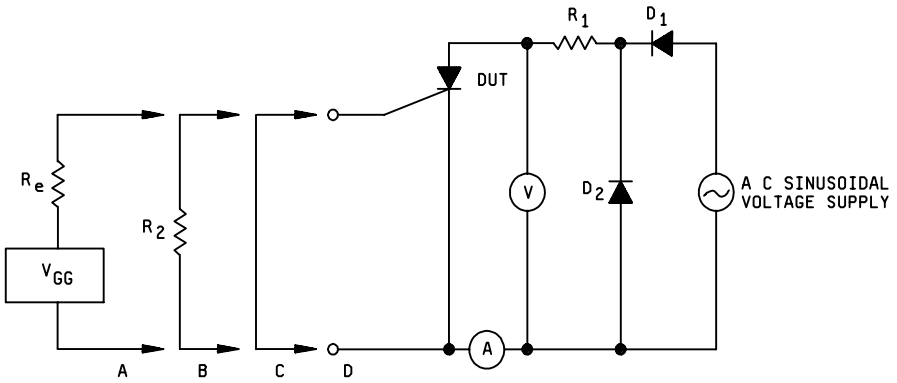
3. AC method.

3.1 Test circuit. R_1 shall be chosen to limit the current flow in the event the device switches to the on state. D_1 and D_2 are diodes capable of blocking the peak value of the ac voltage supply. Peak reading techniques shall be used to measure the necessary parameters. (See figure 4206-2)



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 4206-2. Test circuit for forward blocking current (ac method).

3.2 Procedure. The peak supply voltage is adjusted to obtain the specified peak forward voltage across the device with the specified gate bias condition applied (see figure 4206-2). The peak forward blocking current is then read from the current indicator. Voltage should be gradually applied to prevent turn-on of the device due to excessive dv/dt.

3.3 Summary. The following conditions shall be specified in the applicable specification sheet:

a. AC method.

b. Peak forward test voltage.

c. Frequency.

d. Bias condition, gate-to-cathode, as applicable:

A: Bias (specify V_{GG}, gate-to-cathode polarity, equivalent bias circuit resistance, R_e).

B: Resistance return (specify value of R_2).

C: Short-circuit.

D: Open-circuit.

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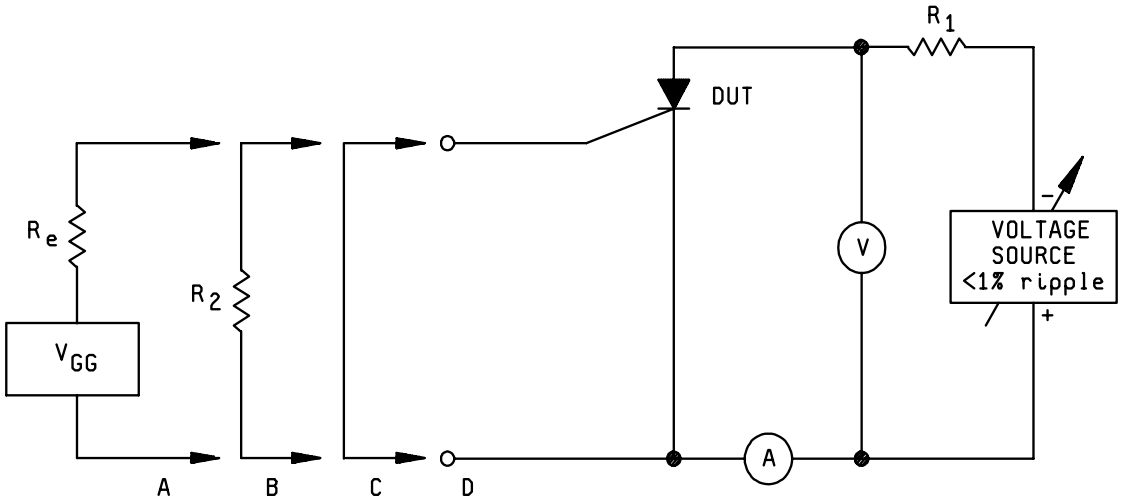
METHOD 4211.1

REVERSE BLOCKING CURRENT

1. Purpose. The purpose of this test is to measure the reverse blocking current under the specified conditions, using the dc method or the ac method, as applicable.

2. DC method.

2.1 Test circuit. R_1 shall be chosen to limit the current flow in the event of the device goes into reverse breakdown.



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the readings shall be corrected for the drop across the ammeter.

FIGURE 4211-1. Test circuit for reverse blocking current (dc method).

2.2 Procedure. The supply voltage is adjusted to obtain the specified value of reverse voltage across the device with the specified gate bias condition applied (see figure 4211-1). The reverse blocking current is then read from the current meter.

2.3 Summary. The following conditions shall be specified in the applicable specification sheet:

a. DC method.

b. Test voltage.

c. Bias condition, gate-to-cathode, as applicable:

A: Bias (specify V_{GG}, gate-to-cathode polarity, equivalent bias circuit resistance, R_e).

B: Resistance return (specify value of R_2).

C: Short-circuit.

D: Open-circuit.

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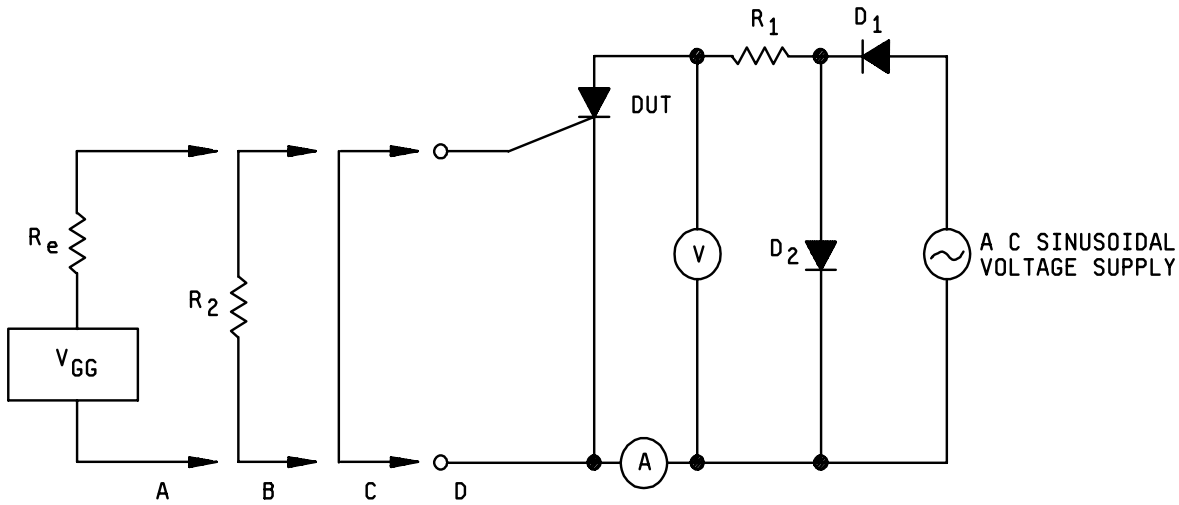
3. AC method.

3.1 Test circuit. R_1 shall be chosen to limit the current flow in the event the device goes into reverse breakdown. D_1 and D_2 are diodes capable of blocking the peak value of the ac voltage supply. Peak reading techniques shall be used to measure the necessary parameters. (See figure 4211-2)



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 4211-2. Test circuit for reverse blocking current (ac method).

3.2 Procedure. The peak supply voltage is adjusted to obtain the specified peak reverse voltage across the device with the specified gate bias condition applied (see figure 4211-2). The peak reverse blocking current is then read from the current indicator.

3.3 Summary. The following conditions shall be specified in the applicable specification sheet:

a. AC method.

b. Peak reverse test voltage.

c. Frequency.

d. Bias condition, gate-to-cathode, as applicable:

A: Bias (specify V_{GG}, gate-to-cathode polarity, equivalent bias circuit resistance, R_e).

B: Resistance return (specify value of R_2).

C: Short-circuit.

D: Open-circuit.

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METHOD 4216

PULSE RESPONSE

1. Purpose. The purpose of this test is to measure the pulse response of the device under the specified conditions.

2. Test circuit. See figure 4216-1.

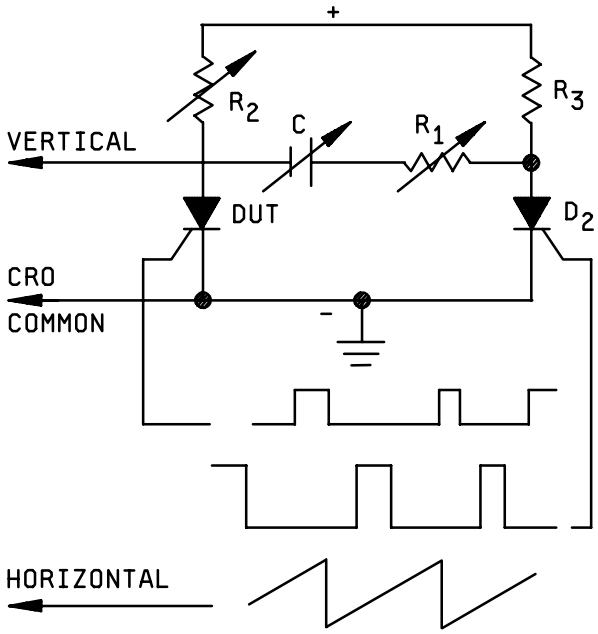

FIGURE 4216-1. Test circuit for pulse response.

3. Procedure. The pulse response of the device shall be measured in the circuit on figure 4216-1. R_2 is adjusted to permit the specified value of forward current to flow in the device being measured when it is the on-state. C, R_1, and the secured controlled rectifier, D_2, are used to switch off the device being measured. C shall be large enough to ensure that the device will turn off. R_1 limits the recurrent peak reverse current to below the rated value. The pulse repetition rate should be low enough to ensure that the anode-cathode voltage of the device being measured reaches the value of forward working voltage specified for the measurement.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Anode voltage (see 3.).

b. Resistor R_2 (see 3.).

c. Test current.

d. Repetition rate.

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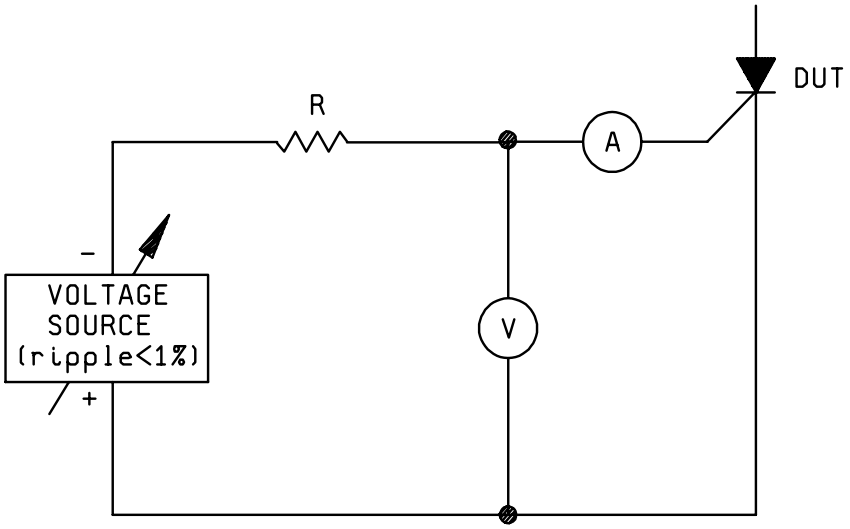
METHOD 4219

REVERSE GATE CURRENT

1. Purpose. The purpose of this test is to measure the dc reverse gate current of the device at a specified reverse gate voltage.

2. Test circuit. R is chosen to limit the current in the event the reverse gate breakdown voltage is exceeded. (See figure 4219-1)



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 4219-1. Test circuit for reverse gate current.

3. Procedure. Set the specified reverse gate voltage and read the reverse gate current.

4. Summary. The dc reverse gate voltage shall be specified in the applicable specification sheet:

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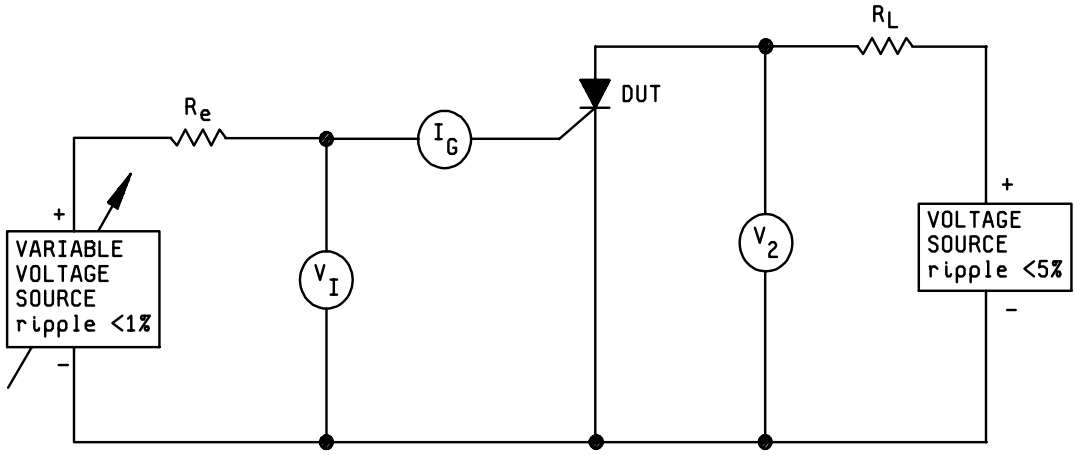
METHOD 4221.1

GATE-TRIGGER VOLTAGE
OR
GATE-TRIGGER CURRENT

1. Purpose. The purpose of this test is to measure the dc gate-trigger voltage or dc gate-trigger current.

2. Test circuit. Care should be taken to minimize noise or spurious signals in the trigger circuit. (See figure 4221-1)



NOTE: The ammeter shall present essentially a short-circuit to the terminals between which the current is being measured or the voltmeter readings shall be corrected for the drop across the ammeter.

FIGURE 4221-1. Test circuit for gate-trigger voltage or gate-trigger current.

3. Procedure. The anode voltage, V_2, is set to the specified value. The gate voltage, V_1, is slowly increased from zero. The gate-trigger current or gate-trigger voltage is read as the highest value achieved prior to a sharp decrease in anode voltage.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Anode voltage, V_2 (see 3.).

b. Load resistance, R_L.

c. Equivalent gate circuit resistance, R_e (the resistance looking into the gate circuit from the DUT gate-to-cathode terminals).

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METHOD 4223

GATE-CONTROLLED TURN-ON TIME

1. Purpose. The purpose of this test is to measure the time between initiation (10 percentage point) of gate pulse and the time at which the output pulse is at 90 percent of its final value.

2. Test circuit. The anode circuit loop L/R shall be >0.01 and <0.1 of the forward current rise time, t_r. The open-circuit, gate-voltage rise time shall be <0.1 of the delay time, t_d of the DUT. V_{AA} must have stabilized at its peak value prior to triggering the gate pulse generator. (See figures 423-1, and 4223-2)

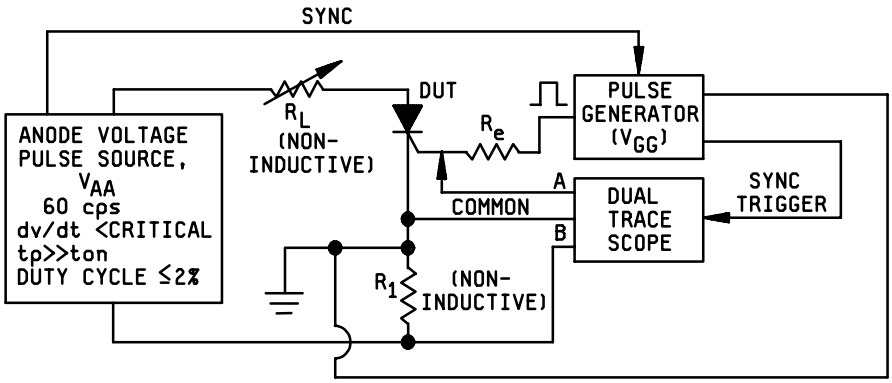

FIGURE 4223-1. Test circuit for gate-controlled turn-on time.

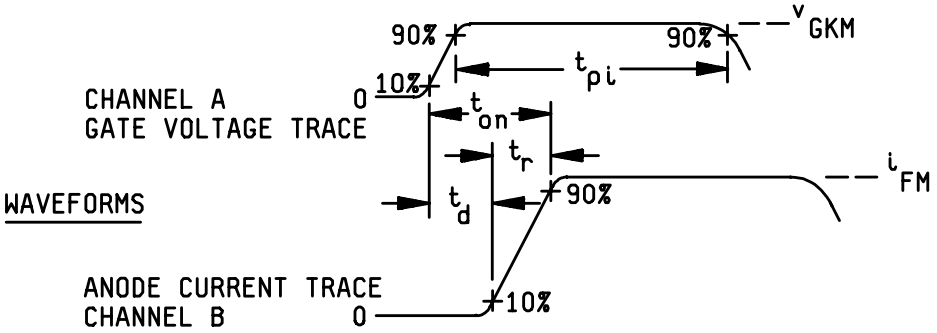

FIGURE 4223-2. Waveforms, gate-controlled turn-on time.

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3. Procedure. Set the anode voltage pulse source and the gate conditions as specified. Adjust R_L to achieve the specified i_{FM}. The turn-on time is then read from the dual trace scope as shown on figure 4223-2.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Peak anode supply voltage, V_{AA}.

   b. Peak forward current, i_{FM}.

   c. Peak open-circuit, gate supply voltage, V_{GG}.

   d. Gate pulse width, t_{p1}.

   e. Equivalent gate-source resistance, R_e.

   f. Minimum and maximum allowable di/dt of the forward current pulse.

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METHOD 4224

CIRCUIT-COMMUTATED TURN-OFF TIME

1. Purpose. The purpose of this test is to measure the turn-off time of the device under the specified conditions.

2. Test circuit. (See figures 4224-1, and 4224-2)

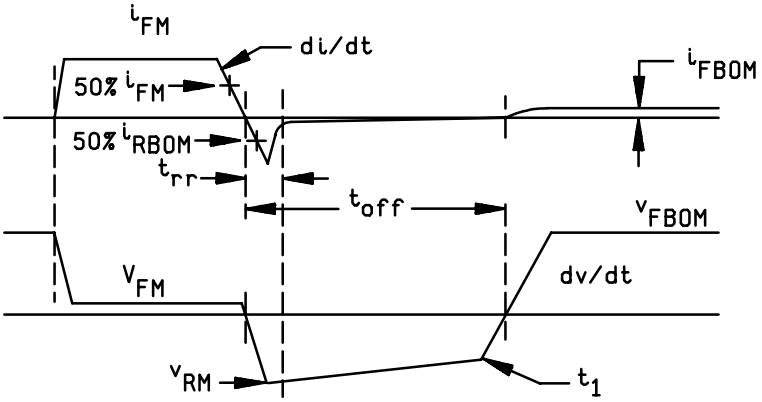

FIGURE 4224-1. Circuit-commutated turn-off time waveforms.

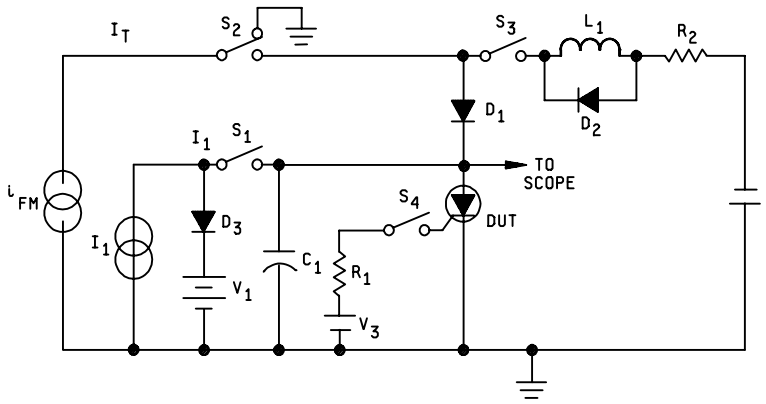

FIGURE 4224-2. Test circuit for circuit-commutated turn-off time.

NOTE: The simplified circuit diagram on figure 4224-2 illustrates the operating principles of a circuit used to generate the waveforms illustrated on figure 4224-1. For purposes of clarity, the circuit diagram utilizes current generators, ideal switches, and no provision for repetitive test cycles.

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3. Test description. The test is performed by first causing the thyristor under test to conduct the specified on-state current at the specified thermal condition. This current is conducted for the specified time (a period long enough to establish carrier equilibrium). Next, the current is reversed through the thyristor at the specified rate (di/dt) by means of an externally applied reverse blocking voltage. The reverse current recovers stored charge from the anode and cathode junctions of the thyristor, allowing the thyristor to support the specified reverse blocking voltage. A further waiting time is required for the collector junction charges to recombine before the thyristor is capable of blocking forward voltage. Since this recombination cannot be observed directly, the test is performed by applying an off-state voltage at the specified rate of rise (dv/dt) after successively shorter waiting times until it is observed that the thyristor is unable to support the off-state voltage (without switching to the on-state). The thyristor current and voltage waveforms are illustrated on figure 4224-1.

4. Procedure.

a. S_2 and S_4 are closed simultaneously causing the thyristor under test to switch to the on-state and conduct the specified current i_{FM}; S_4 is then opened to disconnect the gate trigger supply R_1 and V_3.

b. After the specified on-state current duration, S_3 is closed to cause current reversal. The rate of current change (di/dt) is determined by L_1 and R_2. Diode D_2 prevents a commutation voltage transient when the thyristor under test begins to recover its reverse blocking capability. Diode D_1 shall have a longer reverse recovery time than the thyristor under test so that the reverse voltage appears across the thyristor under test.

c. The application of off-state voltage is initiated by closing S_1. The current I_1 completes the reverse recovery of D_1 and is then diverted to C_1. C_1 charges linearly with time at a rate equal to I_1/C_1 producing the required dv/dt illustrated on figure 4224-1. This voltage rises to a value equal to V_1 which is adjusted to the specified off-state voltage.

5. Summary. The following conditions shall be specified in the applicable specification sheet:

a. On-state current amplitude.

b. On-state current duration, t_{on}.

c. Commutation rate (di/dt) (the slope of the line from 50 percent of + peak to 50 percent of - peak).

d. Peak reverse voltage (maximum).

e. Reverse voltage at t_1 (minimum).

f. Operating temperature.

g. Test repetition rate.

h. Rate of rise of reapplied off-state voltage (dv/dt).

i. Off-state voltage.

j. Gate bias conditions (between gate trigger pulses):

(1) Gate-source voltage.

(2) Gate-source resistance.

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METHOD 4225

GATE-CONTROLLED TURN-OFF TIME

1. Purpose. The purpose of this test is to measure the gate-controlled turn-off time of the device under the specified conditions.

2. Test circuit. The circuit used for the test is shown on figure 4225-1. The thyristor is turned on by the gate pulse delivered by the on pulse generator. On-state current is determined by the off-state supply voltage and the load resistor R_L.

After a predetermined time, a specified gate turn-off current is supplied to the gate terminal by the off pulse generator.

The storage time and fall time may be observed by means of an oscilloscope connected across the current sensing resistor.

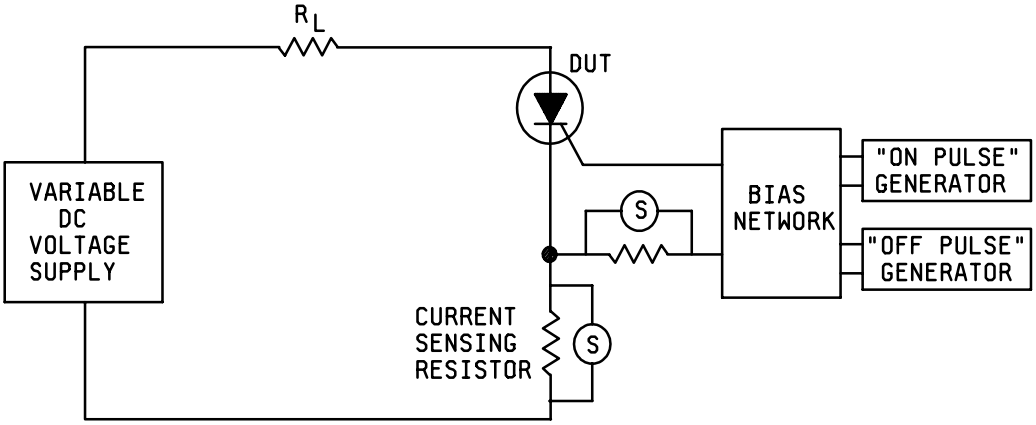

FIGURE 4225-1. Gate turn-off test circuit.

Storage time is the time interval between the 10 percent point on the leading edge of the gate current off-pulse and the 90 percent point on the trailing edge on-state current waveform. Fall time is the time interval between the 90 percent and 10 percent points on the trailing edge of the on-state current waveform. Turn-off time is the sum of storage time and fall time. Typical waveforms are shown on figure 4225-2.

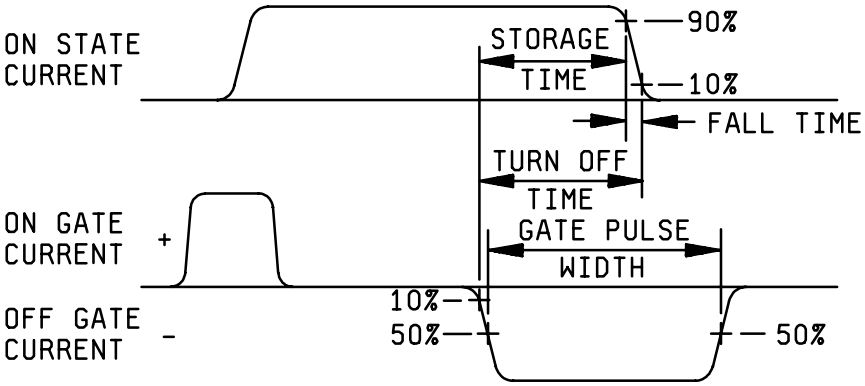

FIGURE 4225-2. Typical gate turn-off circuit waveforms.

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3. Test description. A turn-off thyristor can be switched from the on-state to the off-state with a control signal of appropriate polarity to the gate terminal. The delay and fall times of anode current during the turn-off of the thyristor are affected by gate trigger pulse variations and anode circuit conditions. This method establishes a test circuit and provision for measuring of critical test conditions.

4. Procedure.

   a. Gate current or gate source voltage rise time shall not exceed 10 percent of the storage time interval.

   b. Duty cycle should be chosen considering heating effects of switching power losses. Sufficient anode current off time of at least 10 times the off pulse width shall be allowed to ensure that the DUT remains turned off after the turn-off pulse ends.

   c. The inductance of the anode circuit should be minimized to prevent anode voltage overshoot on turn-off.

5. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Off-state voltage.

   b. On-state current.

   c. Switching repetition rate.

   d. Duty cycle (percent on-time).

   e. Operating temperature (case or ambient).

   f. Bias network (show circuit).

   g. Gate turn-off current (peak); or gate source voltage and gate source resistance.

   h. R_L.

   i. Gate on pulse width and amplitude.

   j. Gate off pulse width, amplitude, and delay time from gate on pulse.

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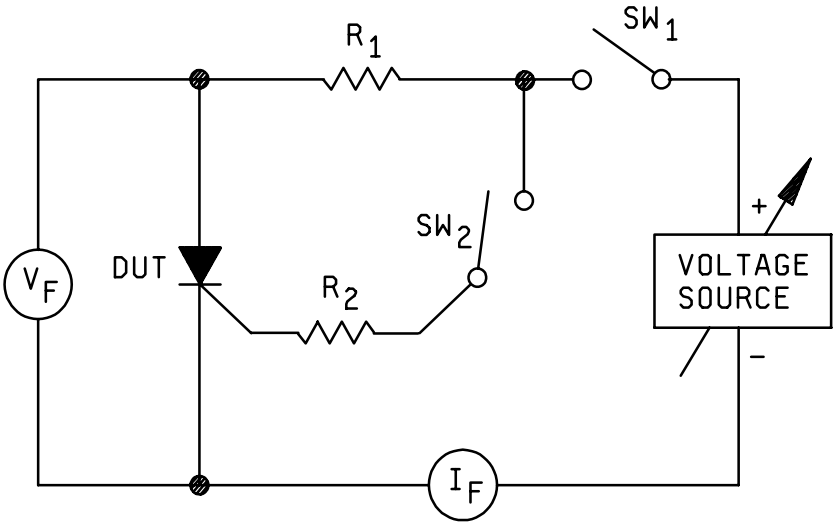
METHOD 4226.1

FORWARD ON VOLTAGE

1. Purpose. The purpose of this test is to measure the voltage in the forward direction across the device under the specified conditions.

2. Test circuit. See figure 4226-1.



NOTE: When specified, switch SW_1 shall be used to provide pulses of short-duty cycle to minimize device heating. When pulsing techniques are used, other suitable peak-reading techniques shall be used to measure the necessary parameters, and the duty cycle and pulse width shall be specified.

FIGURE 4226-1. Test circuit for forward on voltage.

3. Procedure. The supply voltage is adjusted to obtain the specified value of forward current through the device with SW_1 and SW_2 closed. SW_2 shall be opened, and then the forward voltage is read when the forward current equals the specified value. When the specified test current is greater than 0.20 ampere, the voltage measuring probes shall be connected to the device inside of the current carrying connections. For axial lead devices, the voltage measuring probe(s) shall contact the lead(s) at a point .375 ±.062 inch (9.52 ±1.57 mm) from the case. For all other devices, the voltage shall be measured across the normal electrical connection points.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Test current (see 3.).

b. Duty cycle and pulse width when pulse techniques are to be used (see above note).

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METHOD 4231.2

EXPONENTIAL RATE OF VOLTAGE RISE

1. Purpose. The purpose of this test is to determine if the device is capable of blocking a forward voltage which is increasing at an exponential rate starting from zero without switching on in the forward direction.

2. Test circuit. R_2 is chosen to discharge C between cycles when SW is opened and R_L is a protective resistor chosen to limit the maximum device current if the device turns on during the voltage rise. Switch SW should have a closure time (including bounce) of not more than 0.1 T and be closed a minimum of 5 T. (See figure 4231-1, and 4231-2)

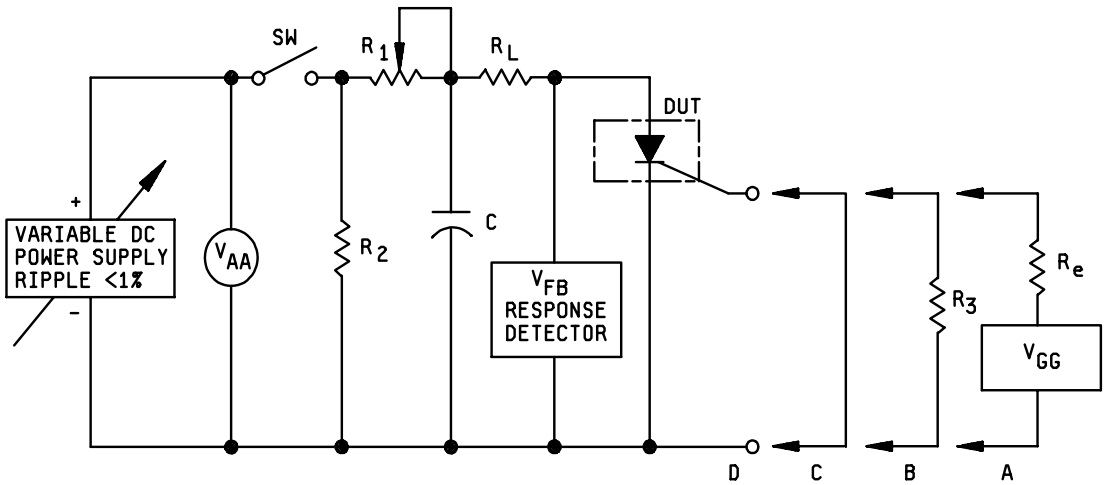

FIGURE 4231-1. Test circuit for exponential rate of voltage rise.

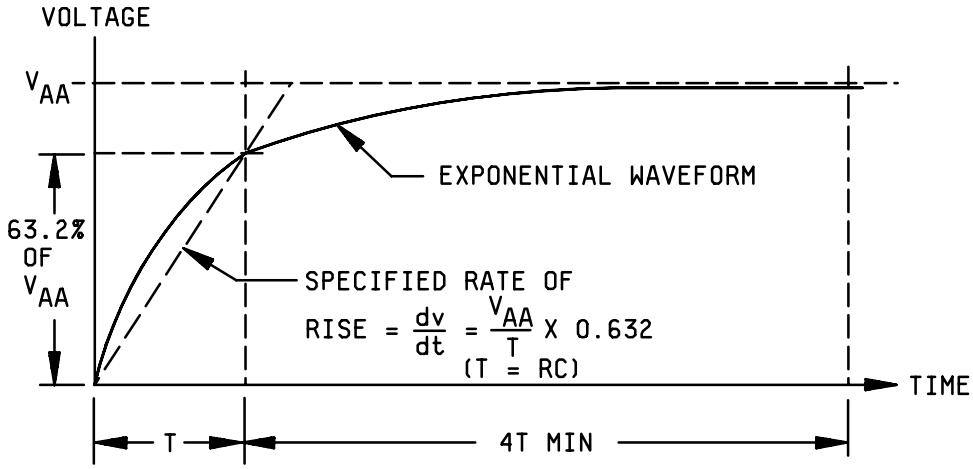

FIGURE 4231-2. Waveforms across the DUT.

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3. Procedure. The voltage V_{AA} shall be adjusted to the specified value with switch SW open (see figure 4231-1). The resistor, R_1, shall be adjusted to achieve the specified rate of voltage rise, dv/dt, across the DUT with the specified gate bias condition applied. The rate of voltage rise is defined as shown on figure 4231-2. Close SW and monitor V_{FB} on the response detector. A device shall be considered a failure if V_{FB} does not rise to, and maintain, a value greater than the minimum specified forward-blocking voltage during the first 5 T of each voltage pulse after switch SW is closed.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Test voltage, V_{AA}.

   b. Rate of voltage rise, dv/dt (see figure 4231-2).

   c. Value of C and R_L.

   d. Repetition rate.

   e. Duration of test.

   f. Minimum forward-blocking voltage, V_{FB}.

   g. Test temperature.

   h. Bias condition, gate-to-cathode, as applicable:

      A: Bias (specify V_{GG}, gate-to-cathode polarity, equivalent bias circuit resistance, R_e).

      B: Resistance return (specify value of R3).

      C: Short-circuit.

      D: Open-circuit.

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4300 Series

Electrical characteristics tests for tunnel diodes

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METHOD 4301

JUNCTION CAPACITANCE

1. Purpose. The purpose of this test is to determine the small signal junction capacitance of the tunnel diode under the specified conditions.

2. Test circuit. See figure 4301-1.

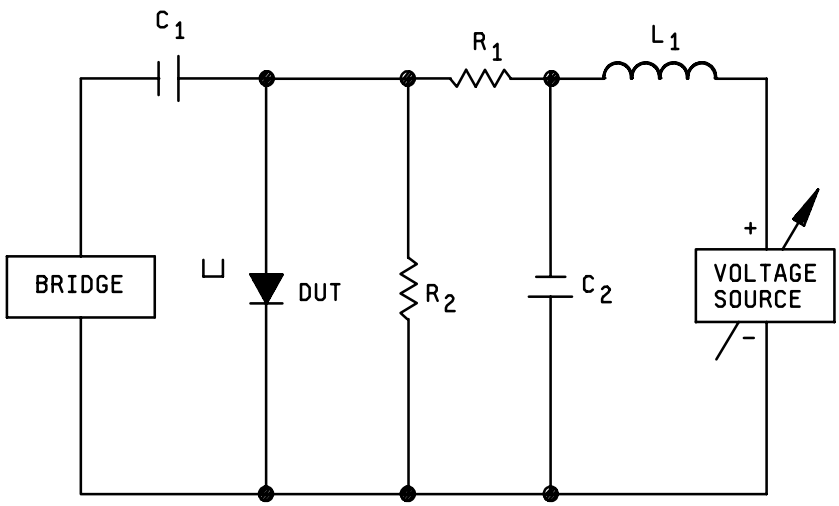

FIGURE 4301-1. Test circuit for junction capacitance.

3. Procedure. Since junction capacitance is a function of bias, it is necessary to specify the forward bias at which C_1 is to be determined. The true value of junction capacitance (at a given bias) is obtained by subtracting the capacitance of the diode package from the observed capacitance. Isolation of the dc power supply from the complex impedance bridge (see figure 4301-1) is affected by the R_1, L_1, C_2 branch of the circuit.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Values for the circuit elements R_1, C_1, C_2, L_1, and R_2.

b. Signal frequency.

c. Bias level.

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METHOD 4306.1

STATIC CHARACTERISTICS OF TUNNEL DIODES

1. Purpose. The purpose of this test is to measure the static characteristics (V_p, V_v, I_p, I_v, V_{FP}, and R_d) of the tunnel diode under the specified conditions:

2. Test circuit. See figures 4306-1, 4306-2, and 4306-3.

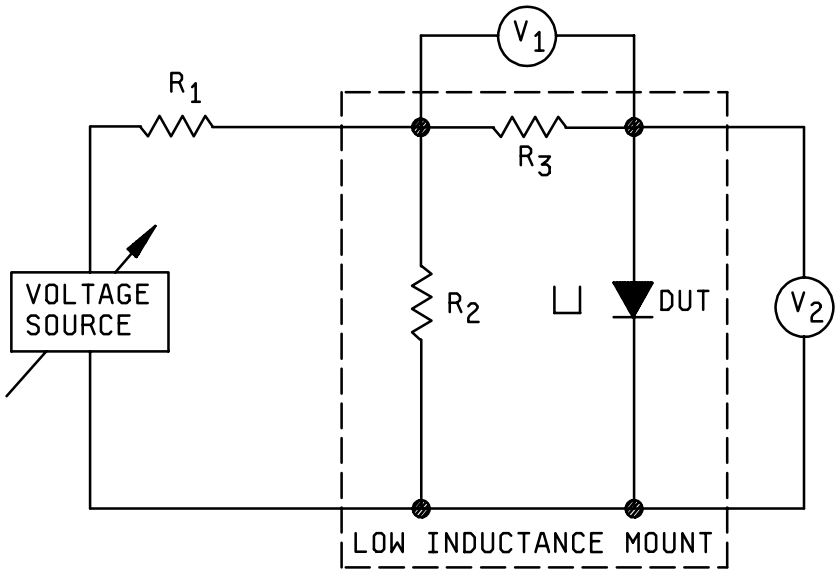

FIGURE 4306-1. Test circuit for static characteristics of tunnel diodes (dc method).

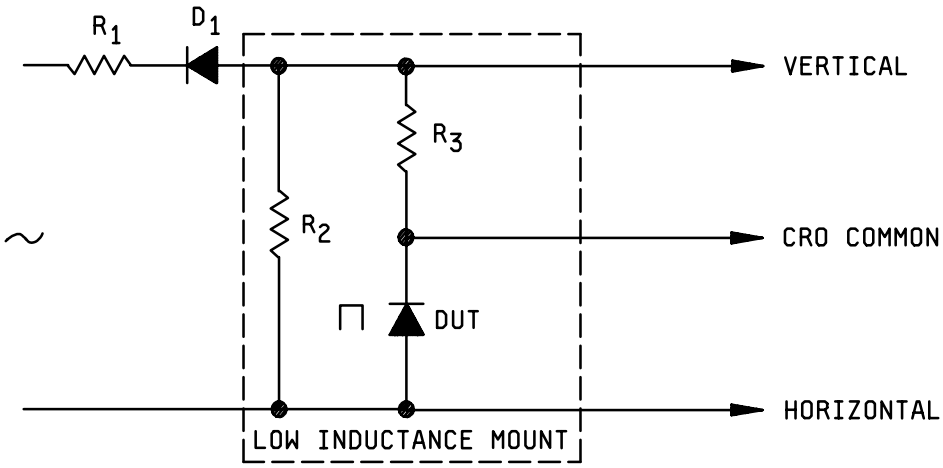

FIGURE 4306-2. Test circuit for static characteristics of tunnel diodes (ac method).

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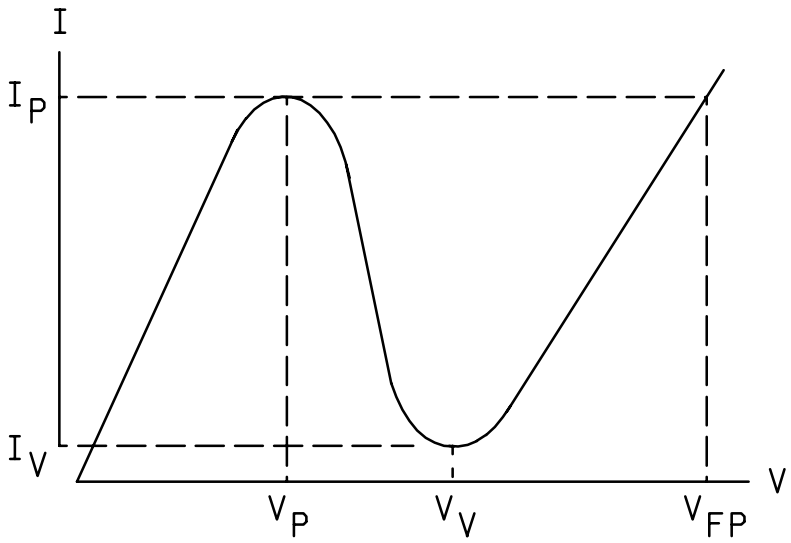

FIGURE 4306-3. Typical tunnel diode forward characteristic.

3. Procedure.

   a. For the measurement of the static characteristics by point-by-point method, the circuit of figure 4306-1 shall be used. Resistor, R_2, is small to obtain low voltage and low impedance. Resistor R_3 is a current measuring resistor. Resistor R_1 is much larger than R_2. To obtain a plot in the negative resistance region R_1 shall be less than the magnitude of the incremental negative resistance of the tunnel diode.

   b. For the measurement of the static forward characteristics of the device by oscillographic means, the circuit shown on figure 4306-2 shall be used. The magnitude of R_1 shall be less than the magnitude of the incremental negative resistance of the tunnel diode. Resistance R_3 is a current measuring resistor and should be chosen to give a suitable CRO deflection. Since the negative resistance is represented by the inverse slope of the I_V curve between the peak and valley voltage points, its approximate value can be estimated from the curve. For a more accurate method for the measurement of the negative resistance see method 4321.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

   a. Resistors R_1, R_2, and R_3 (see 3.a. and 3.b.).

   b. Signal frequency (see 3.b.).

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METHOD 4316

SERIES INDUCTANCE

1. Purpose. The purpose of this test is to measure the value of the small signal series inductance under the specified conditions.

2. Test circuit. See figure 4316-1.

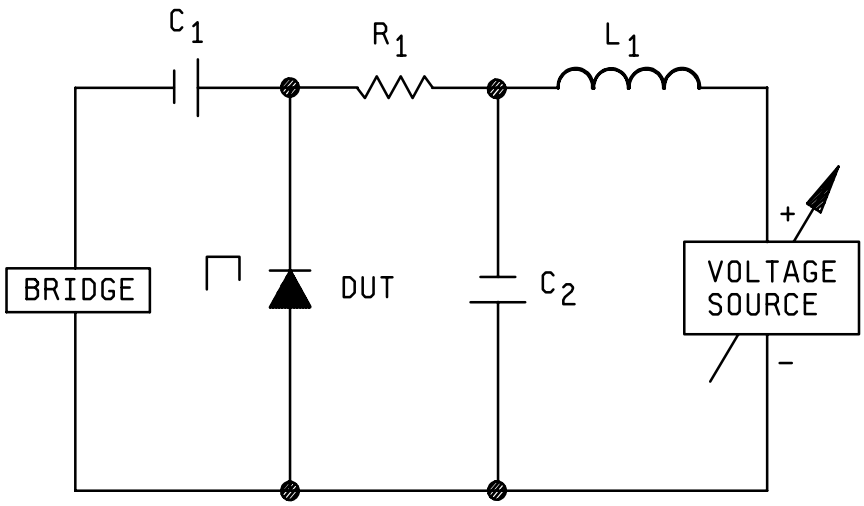

FIGURE 4316-1. Test circuit for series inductance.

3. Procedure. The device shall be reverse biased for the series inductance measurement. A sufficiently high frequency signal shall be employed to emphasize the inductive reactance, but not high enough to allow any capacitive parasitics to short-circuit the device, thus precluding the determination of L_S. A recommended frequency device is one approximately 25 percent of the self-resonant frequency of the DUT. Isolation of the dc power supply from the complex impedance is accomplished by the choke, L_1, in conjunction with C_1, R_1, C_2, branch (see figure 4316-1).

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Values for circuit elements, R_1, L_1, C_1, and C_2.

b. Signal frequency.

c. Reverse bias at which L_S is measured.

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METHOD 4321

NEGATIVE RESISTANCE

1. Purpose. The purpose of this test is to determine the magnitude of the negative resistance under the specified conditions.

2. Test circuit. See figures 4321-1 and 4321-2.

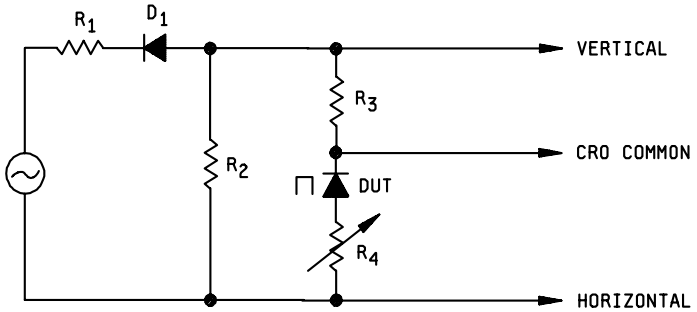

FIGURE 4321-1. Test circuit for negative resistance, short-circuit stable method.

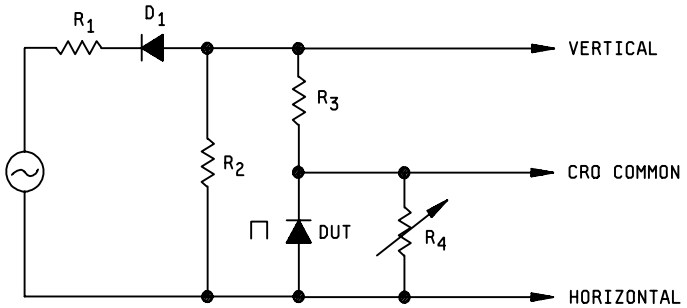

FIGURE 4321-2. Test circuit for negative resistance, open-circuit stable method.

3. Procedure. The magnitude of R_1 shall be less than the incremental negative resistance of the tunnel diode. Resistor R_3 is a current limiting resistor and should be chosen to give a suitable CRO deflection. Diode D_1 is a half wave rectifier.

3.1 Short-circuit stable method. Shunt the tunnel diode, with a variable resistor R_4 (see figure 4321-1). Vary R_4 until the slope of the negative resistance appears horizontal (zero slope) on the curve trace. The shunting resistance is now equal to the magnitude of the negative resistance, R_d. ($R_4 = R_d$.)

3.1.1 Open-circuit stable method. In series with the tunnel diode connect a variable resistor R_4 (see figure 4321-2). Vary R_4 until the slope in the negative resistance appears vertical (infinite slope) on the curve trace. The series resistance R_4 is now equal to the magnitude of the negative resistance ($R_4 = R_d$).

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Source impedance R_1.

b. Current sensing resistor, R_3.

c. Variable resistor, R_4.

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METHOD 4326

SERIES RESISTANCE

1. Purpose. The purpose of this test is to determine the series resistance of the device under the specified conditions.

2. Test circuit. See figure 4326-1.

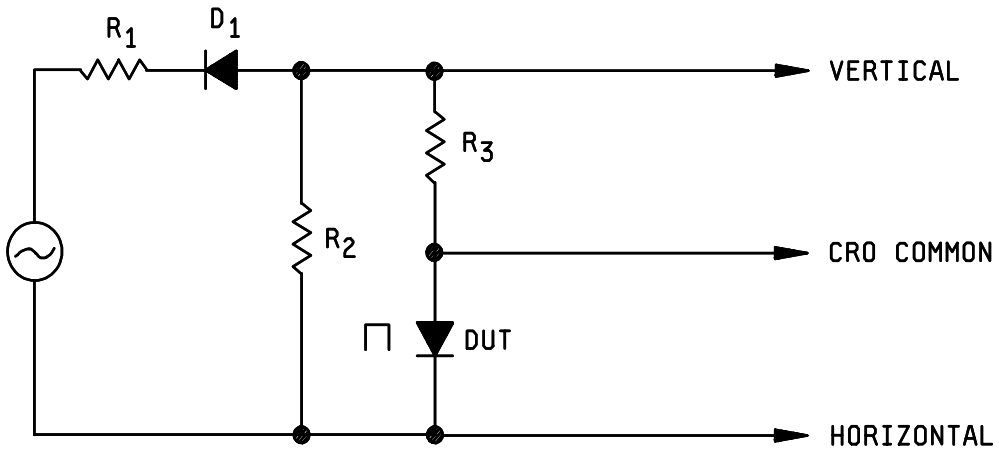

FIGURE 4326-1. Test circuit for series resistance.

3. Procedure. The measurement of the series resistance shall be accomplished for the device when biased in the reverse direction (see figure 4326-1). The linearity of the ohmic region shall be assured and the value of the power dissipation shall be such that no error is introduced as a result of excessive diode heating. The slope of the linear portion of the reverse biased tunnel diode shall be sealed within a specified accuracy in the direct determination of the series resistance of the device.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Current sensing resistor R_3.

b. Reverse bias at which R_3 is to be measured.

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METHOD 4331

SWITCHING TIME

1. Purpose. The purpose of this test is to measure the switching time of the tunnel diode under the specified conditions.

2. Test circuit. See figure 4331-1.

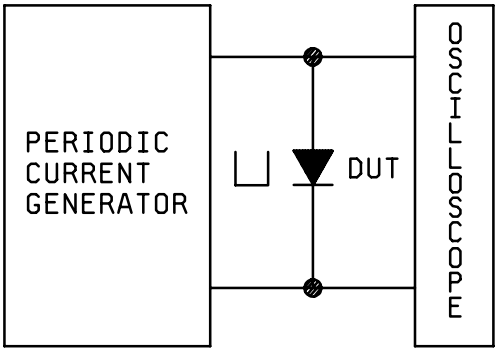

FIGURE 4331-1. Test circuit for switching time.

3. Procedure. A block diagram of the measuring circuit is shown in figure 4331-1. To perform the switching time measurement, it is necessary that the maximum generator current be greater than the diode peak current and that changes in generator current during measurement time be negligible compared to I_P. The oscilloscope input probe impedance shall be such that the current absorbed by the probe is at all times less than the peak current of the diode.

4. Summary. The following conditions shall be specified in the applicable specification sheet:

a. Generator current.

b. Repetition rate.

c. Rise time of oscilloscope.

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5000 Class

High reliability space application tests

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METHOD 5001.2

WAFER LOT ACCEPTANCE TESTING

The content of this test method has been transferred to MIL-PRF-19500, Appendix D.

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METHOD 5002

CAPACITANCE VOLTAGE MEASUREMENTS TO DETERMINE OXIDE QUALITY

1. Purpose. The purpose of this test is to determine the quality of an oxide layer as indicated by capacitance voltage measurements of a metal-oxide semiconductor capacitor. The overall shape and position of the initial C/V curve can be interpreted in terms of the charge density, and to a certain extent charge type, at the oxide-semiconductor interface. By applying an appropriate bias while heating the sample to a moderate temperature (e.g., +200°C), the mobile ion contamination level of the sample oxide may be determined.

2. Apparatus/materials. Capacitance-voltage plotting system complete with heated/cooled stage and probe (Princeton Applied Research Model 410, MSI Electronics Model 868 or equivalent). A C/V plotter may be constructed from the following components (see figure 5002-1 for equipment setup).

2.1 Manual setup.

a. L-C meter (Boonton 72B or equivalent).

b. X-Y recorder (hp 7035B or equivalent).

c. DC voltmeter (Systron Donner 7050 or equivalent).

d. DC power supply, 0 to 100 volts.

e. Heated/cooled stage (Thermochuck TP-36 or equivalent).

f. Probe in micromanipulator.

2.2 Automatic C/V plotter. (CSM-16 or equivalent).

3. Suggested procedure.

3.1 Sample preparation.

a. The sample is typically a silicon wafer on which has been grown the oxide to be measured, or wafers with known clean oxide which is exposed to a furnace at temperature to measure the furnace cleanliness. An array of metal dots on the surface of the oxide provides the top electrodes of the metal-oxide semiconductor capacitors. The metal may either have been deposited through a shadow mask to form the dots, or it may have been deposited uniformly over the oxide surface and then etched into the dot pattern by photolithographic techniques. Cleanliness of the metal deposition is paramount. Contamination introduced during metal deposition is as catastrophic to the oxide quality as is contamination introduced during oxide growth. The metal shall have been annealed, except in cases where the method is being used to investigate the effectiveness of annealing.

NOTE: This test also may be used to determine metal deposition system cleanliness when used with oxide samples known to be contamination free.

b. The minimum dot size should be such that the capacitance of the MOS capacitor is > 20 pF.

c. The oxide thickness is typically 1,100 Å. Reduced sensitivity results from oxide thickness greater than 2,000 Å.

d. The backside of the sample shall have the oxide removed to expose the silicon. The backside may have metal, such as aluminum or gold deposited on it.

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3.2 C/V plot (at room temperature).

a. Place the wafer on the heated/cooled stage. Use vacuum to hold the wafer firmly in place.

b. Zero the capacitance meter as necessary, place the paper in X-Y plotter and set up the voltage source for the desired range.

c. Select the capacitor dot to be measured and carefully lower the probe to contact it.

d. Lower the pen on the X-Y plotter and sweep the voltage over the desired range so a C/V trace for an N-type substrate or P-type substrate, similar to that shown on figure 5002-2, is obtained.

NOTE: If an anomalous trace is obtained, it may be because the capacitor is leaking or shorted. In this case, another dot should be selected.

3.3 Mobile ion drift.

a. Use the capacitor dot measured in 3.2.d.

b. With the probe making good contact, apply a positive bias of 10_{10} v/cm to the capacitor dot. (For a 1,000 Å thick oxide, this is a 10-volt bias.) A different voltage is acceptable, if the manufacturer can demonstrate effectiveness.

c. Heat the sample to +300°C ±5°C with the bias applied. Hold at this temperature for 3 minutes (different times may be acceptable if the manufacturer can demonstrate effectiveness).

d. With the bias still applied, cool the sample to room temperature (the heating and cooling cycle can be automatically programmed if the Thermochuck system is used).

NOTE: Be certain that the probe does not lose contact with the capacitor dot during the heat/cool cycle. If it should, the test is invalid and should be repeated.

e. Lower the pen on the X-Y plotter and sweep the voltage over the range necessary to obtain a C/V trace similar to that obtained in 3.2.d. The trace may be displaced on the voltage scale from the original trace, but should be parallel to the original trace. Label this trace as the (+) trace.

f. Apply a negative bias of the same magnitude selected in 3.3.b to the capacitor dot and repeat steps 3.3.c and 3.3.d.

g. Lower the pen on the X-Y plotter and sweep the voltage over the range again. This trace may be displaced from the two previous traces and should be labeled as the (-) trace.

h. An automatic system that performs equivalent functions may be substituted for steps 3.3.b and 3.3.g.

3.4 Interpretation.

a. Determine the V_{FB} (voltage difference between original trace and bias trace, taken at 90 percent capacitance level (see figure 5002-2)).

b. Determine the mobile ion contamination concentration (For mobile ion density versus voltage shift (VFB) see figure 5002-3), N_O, as follows:

$$N_o = \frac{\varepsilon 0 \; K_{ox} \; \Delta \; V_{FB}}{q \; t_{ox}}$$

Where: $\in 0$ = permittivity of free space (8.85×10^{-12} coulomb volt^{-1} m^{-1}).

K_{ox} = dielectric constant of the oxide (3.8 for silicon dioxide).

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q = the charge on an electron (1.6×10^{-19} coulomb).

t_{ox} = oxide thickness (in meters).

Example:

ΔV_{FB} (measured from C/V curves similar to those shown on figure 5002-2) = 1.4 V.

t_{ox} (measured on wafer prior to metal deposition) = 950 Å.

$$N_o = \frac{(8.85 \times 10^{-12})(3.8)(3.14)}{(1.6 \times 10^{-19}(950 \times 10^{-10})} = 3.1 \times 10^{15}/\text{meter}^2 = 3.1 \times 10^{11}/\text{cm}^2$$

So, the mobile ion contamination level is 3.1×10^{11} mobile ions per square centimeter in this example.

c. Considerably more information concerning the oxide and the semiconductor substrate can be obtained from interpretation of the C/V trace.

4. Summary.

4.1 Calibration. The voltage scale calibration of the X-Y plotter should be checked against the DVM during set up. Other instruments should be calibrated at regular intervals.

4.2 Accuracy. The voltage accuracy obtainable is ±0.1 volt and the ΔV_{FB} accuracy obtainable is ±0.2 volt. The practical lower limit of detectability of mobile ion contamination is on the order of $2 \times 10^{11}/\text{cm}^2$.

4.3 Documentation. Record results in appropriate control document.

Reference:

Whelon, N.V., "Graphical Relation Between Surface Parameters of Silicon, to be Used in Connections with MOS Capacitance Measurements", Phillips Res. Apt., 620-630 (1965).

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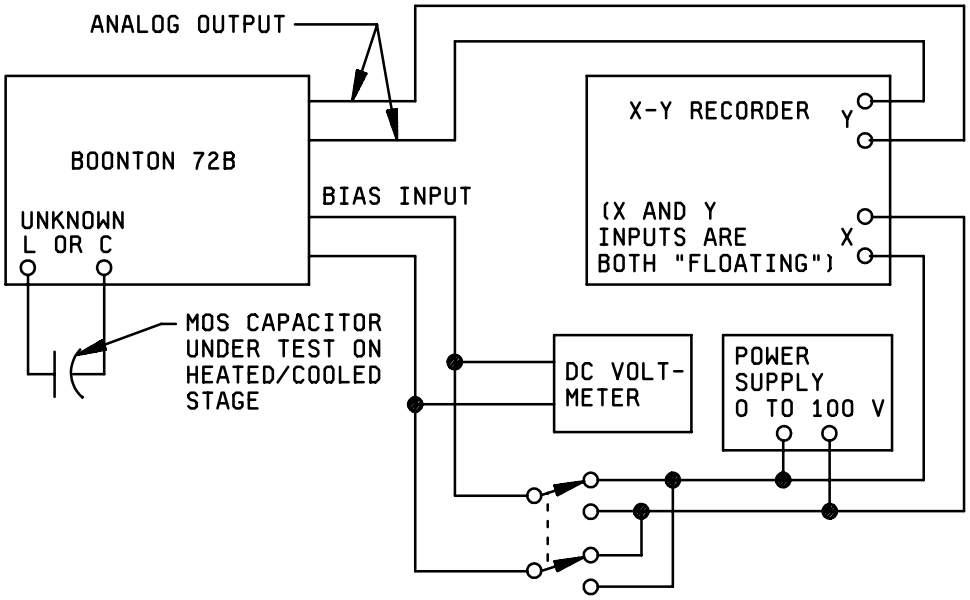

FIGURE 5002-1. Diagram of equipment set-up for measuring relationship of metal-insulator-semiconductor structures.

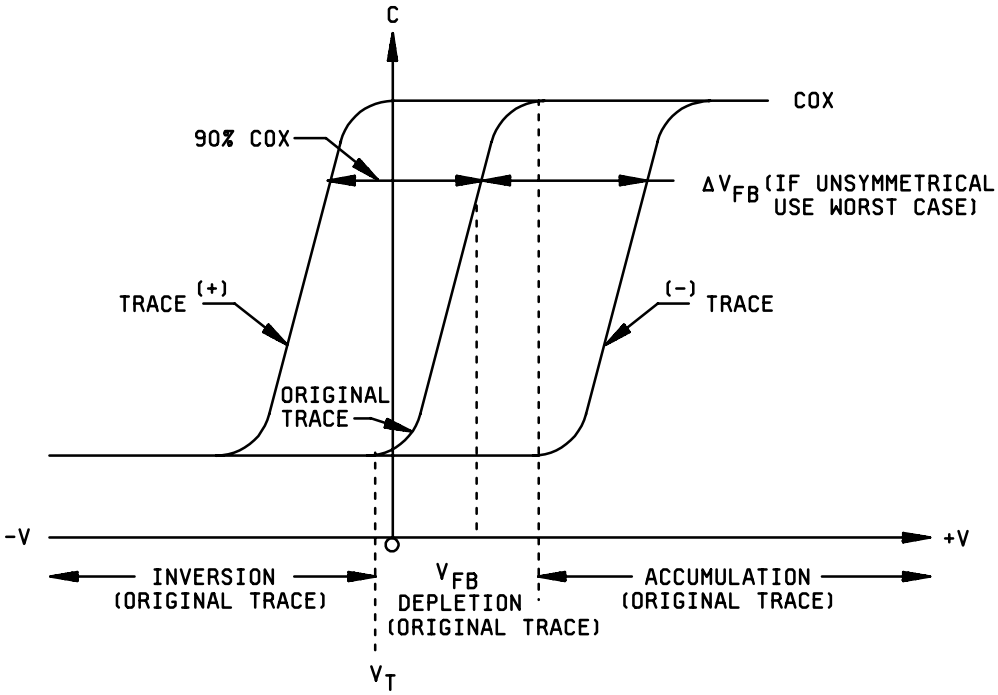

FIGURE 5002-2. C/V traces.

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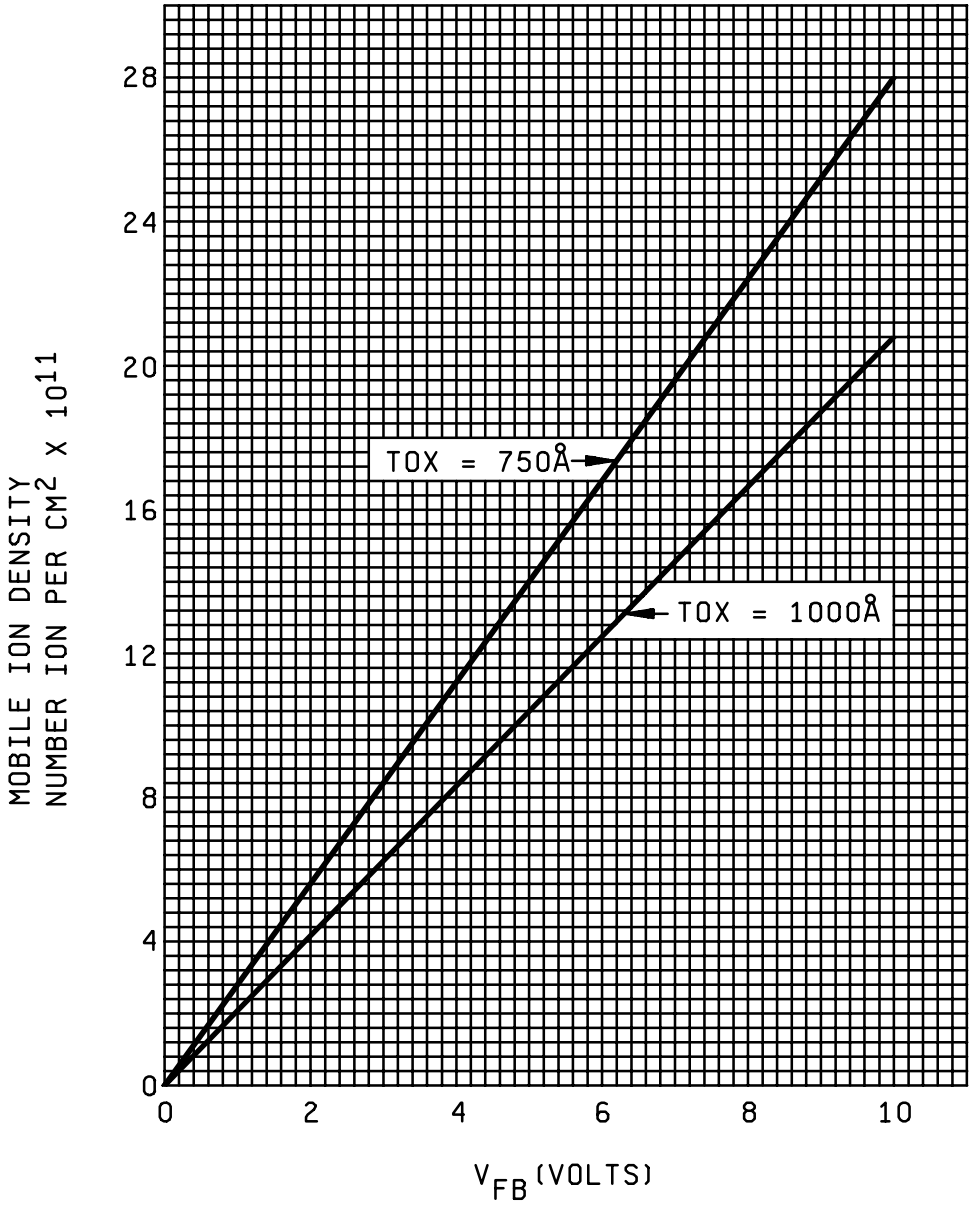

FIGURE 5002-3. Mobile ion density versus voltage shift (V_{FB}).

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METHOD 5010

CLEAN ROOM AND WORKSTATION AIRBORNE PARTICLE CLASSIFICATION AND MEASUREMENT

1. Purpose. This test method provides a classification system for, and means of measuring, air cleanliness. It is intended to be used in conjunction with the environmental controls specified in MIL-PRF-19500.

2. Air cleanliness classes. There are three classes defined by this method. Classifications are based upon particle count with a maximum allowable number of particles per unit volume 0.5 micron or larger, or 5.0 microns and larger. Particle counts are to be taken during normal work activity periods and at a location which will yield the particle count of the air as it approaches the work location.

2.1 Class 100 (3.5). Particle counts must not exceed a total of 100 particles per cubic foot (3.5 particles per liter) of a size of 0.5 micron or larger.

2.2 Class 1,000 (35). Particle counts must not exceed a total of 1,000 particles per cubic foot (35 particles per liter) of a size of 0.5 micron or larger of 7 particles per cubic foot (0.25 particles per liter) of a size 5.0 microns and larger.

2.3 Class 10,000 (350). Particle counts must not exceed a total of 10,000 particles per cubic foot (350 particles per liter) of a size of 0.5 micron or larger or 65 particles per cubic foot (2.3 particles per liter) of a size of 5.0 microns and larger.

2.4 Class 100,000 (3,500). Particle counts must not exceed a total of 100,000 particles per cubic foot (3,500 particles per liter) of a size of 0.5 micron or larger or 700 particles per cubic foot (25 particles per liter) of a size of 5.0 microns and larger.

3. Particle counting methods. For proof of meeting the requirements of the class of clean room or clean work station, one or more of the following particle counting methods shall be employed on the site of use.

3.1 Particle sizes 0.5 micron and larger. The equipment to be used must employ the light scattering measurement principle as specified in ASTM F50.

3.2 Particle sizes 5.0 micron and larger. A microscopic counting of particles collected on a membrane filter, through which a sample of the air to be measured has been drawn, may be used in lieu of the light scattering measurement principle as specified in ASTM F25 and SAE-ARP-743.

4. Monitoring techniques. Appropriate equipment shall be selected and monitoring routines established to measure the air cleanliness levels under normal use conditions.

5. Items to be specified. The general specification shall specify the following information:

a. The class of the workstation or clean room.

b. The frequency of test. Unless otherwise specified, this frequency shall be, at a minimum, once per month per working shift.

c. The locations within the clean environment to be monitored.

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(Project 5961-2912)

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