The documentation and process conversion measures necessary to comply with this revision shall be completed by 3 June 2016.

INCH-POUND

MIL-PRF-19500/535F
3 March 2016
SUPERSEDING
MIL-PRF-19500/535E
30 May 2014

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, PNP, SILICON, POWER,
THROUGH HOLE, TYPES 2N5003 AND 2N5005,
QUALITY LEVELS JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for PNP, silicon, through hole power transistors for use in high-speed power-switching applications. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS). Two levels of product assurance (JANHC and JANKC) are provided for unencapsulated devices.

* 1.2 Package outlines. The device package outlines are as follows: T6-C, similar to TO-59 in accordance with figure 1 for all encapsulated device types. See figure 2 for unencapsulated devices.

1.3 Maximum ratings unless otherwise specified T_A = +25°C.

P_T (1) T_A = +25°C	P_T (2) T_C = +25°C	$R_{\theta JA}$	$R_{\theta JC}$ (3)	V_{CBO}	V_{CEO}	V_{EBO}	I_C	I_C (4)	Reverse pulse energy (5)	T_{stg} and T_J
W	W	°C/W	°C/W	V dc	V dc	V dc	A dc	A dc	mJ	°C
2	58	88	3	-100	-80	-5.5	-5	-10	15	-65 to +200

(1) Derate linearly 11.4 mW/°C for T_A > +25°C.
(2) For derating see figure 3.
(3) For thermal impedance see figure 4.
(4) This value applies for $P_W \leq 8.3$ ms, duty cycle ≤ 1 percent.
(5) This rating is based on the capability of the transistors to operate safely in the unclamped inductive load energy test circuit figure 5 herein.

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

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1.4 Primary electrical characteristics.

Limits	h_{FE2} (1) V_{CE} = -5 V I_C= -2.5A		$\|h_{fe}\|$ V_{CE} = -5 V I_C = -500 mA dc f = 10 MHz		$V_{BE(sat)2}$ (1) I_C = -5 A dc I_B = -500 mA dc	$V_{CE(Sat)2}$ (1) I_C = -5 A dc I_B = -500 mA dc	C_{obo} V_{CB} = -10 V dc I_E = 0 f = 1 MHz
	2N5003	2N5005	2N5003	2N5005			
					V dc	V dc	pF
Min	30	70	6	7			
Max	90	200			-2.2	-1.5	250

(1) Pulsed (see 4.5.1).

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: “JAN”, “JANTX”, “JANTXV” and “JANS”.

* 1.5.2 JAN certification mark and quality level for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet is: "JANHC" and “JANKC”.

* 1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

* 1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "5003" and "5005".

* 1.5.4 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet is "A" (see figure 2 and 6.6.2).

* 1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

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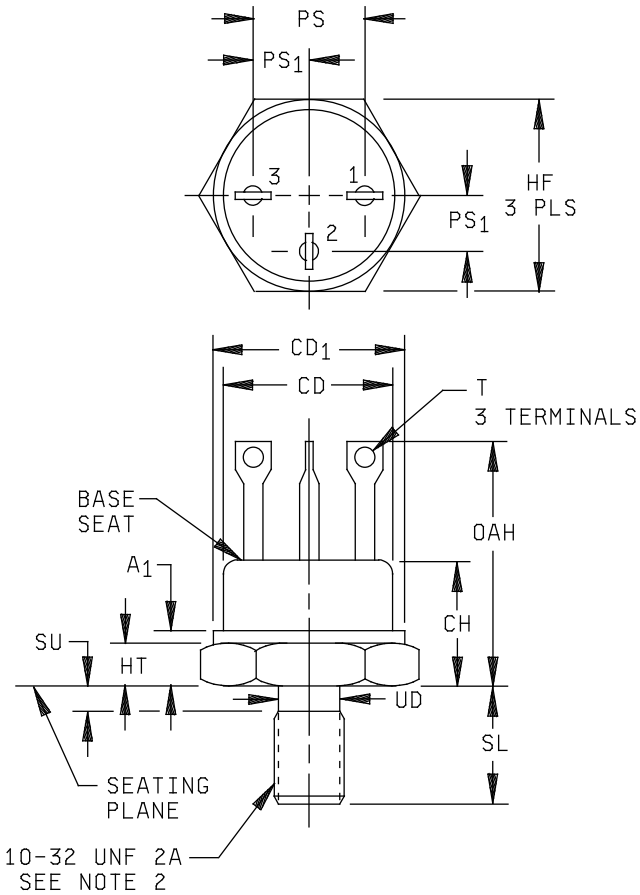

Ltr	Dimension				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A_1		.250		6.35	
CD	.330	.360	8.38	9.14	
CD_1	.370	.437	9.40	11.10	
CH	.320	.468	8.13	11.89	
HF	.424	.437	10.77	11.10	
HT	.090	.150	2.29	3.81	
OAH	.575	.763	14.61	19.38	5
PS	.185	.215	4.70	5.46	4, 8
PS_1	.090	.110	2.29	2.79	4, 8
SL	.400	.455	10.16	11.56	
SU		.078		1.98	7
T	.040	.065	1.02	1.65	
UD	.155	.189	3.94	4.80	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. See NSB Handbook H28, “Screw-Thread Standards for Federal Services”.
4. The orientation of the terminals in relation to the hex flats is not controlled.
5. All three terminals.
6. The case temperature may be measured anywhere on the seating plane within .125 inch (3.18 mm) of the stud.
7. Terminal spacing measured at the base seat only.
8. This dimension applies to the location of the center line of the terminals.
9. Terminal - 1, emitter; terminal - 2, base; terminal - 3, collector. Collector lead is isolated from the case.
10. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions of transistor types 2N5003 and 2N5005 (T6-C, similar to TO-59).

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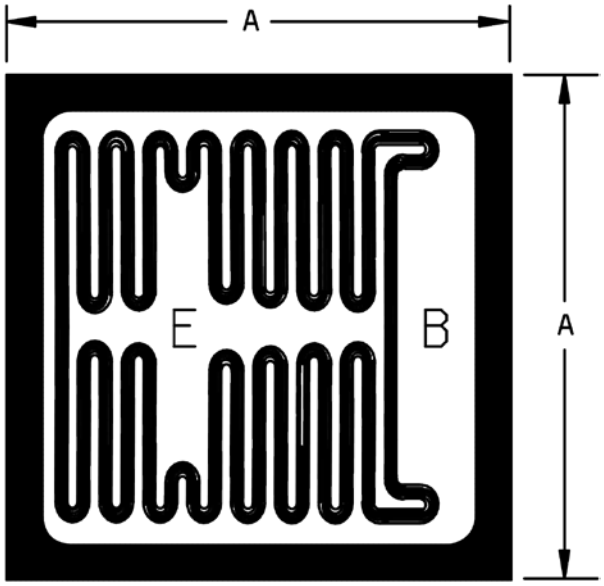

Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.117	.127	2.97	3.23

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm).
4. The physical characteristics of the die are:
   Thickness: .008 (0.20 mm) to .012 (0.30 mm), tolerance is ±.005 (0.13 mm).
   Top metal: Aluminum, 40,000 Å minimum, 50,000 Å nominal.
   Back metal: Gold 2,500 Å minimum, 3,000 Å nominal.
   Back side: Collector.
   Bonding pad: B = .015 (0.38 mm) x .0072 (.183 mm).
   E = .015 (0.38 mm) x .0060 (.152 mm).

Inches	mm
.005	0.13
.006	0.15
.0072	0.183
.008	0.20
.012	0.30
.015	0.38
.117	2.97
.127	3.23

FIGURE 2. Physical dimensions JANHCA and JANKCA die dimensions.

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2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 or 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 or 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at http://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

$R_{\theta JA}$ Thermal resistance junction to ambient.
$R_{\theta JC}$ Thermal resistance junction to case.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1 and 2.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

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3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (list applicable JAN levels). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see appendix E, table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance (see 4.3.3)	Thermal impedance (see 4.3.3)
9	I_{CES1} and h_{FE2}	Not applicable
11	I_{CES1} and h_{FE2} ΔI_{CES1} = 100 percent or -100 nA, whichever is greater; $\Delta h_{FE2} = \pm$ 20 percent.	I_{CES1} and h_{FE2}
12	See 4.3.2	See 4.3.2
13	Subgroups 2 and 3 of table I herein: ΔI_{CES1} = +100 percent of initial value or -100 nA, whichever is greater $\Delta h_{FE2} = \pm$ 20 percent.	Subgroup 2 of table I herein: ΔI_{CES1} = +100 percent of initial value or -100 nA, whichever is greater $\Delta h_{FE2} = \pm$ 20 percent.

(1) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

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4.3.1 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500 "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.2 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = -10 - -30 V dc. Power shall be applied to achieve T_J = +135°C minimum using a minimum P_D = 75 percent of P_T maximum, T_A ambient rated as defined in 1.3. NOTE: No heat sink or forced air cooling on the device shall be permitted. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

* 4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW} (V_C and V_H where appropriate). See table II, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with, table E-V of MIL-PRF-19500 and table I herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions in table E-VIA (JANS) and table E-VIC (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and as follows. Delta requirements shall be in accordance with 4.5.3 herein:

* 4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

Subgroup	Method	Condition
B4	1037	V_{CB} = -10 V dc, adjust device current, or power, to achieve a minimum ΔT_J of +100°C.
B5	1026	V_{CB} = -10 V dc; $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table E-VIA, adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjust T_A or P_D to achieve a T_J = +225°C minimum.
B6	3131	See 1.3.

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4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action.

Step	Method	Condition
1	1026	Steady-state life: Test condition B, 1,000 hours minimum, V_{CB} = -10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, T_A = +150°C, V_{CB} = 80 percent of rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Delta requirements shall be in accordance with the applicable steps of 4.5.3 herein; delta requirements only apply to subgroup C6.

4.4.3.1 Quality level JANS (see table E-VII of MIL-PRF-19500).

Subgroup	Method	Condition
C2	2036	Test condition A, weight = 7 pounds (3.2 kg), ±5 ounces (0.16 kg), application time = 15 seconds; Test condition D1, torque = 6 inch-ounce, application time = 15 seconds; Test condition D2, torque = 15 in-lbs, application time = 15 seconds.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and in accordance with thermal impedance curves.
C6	1026	1,000 hours at V_{CB} = -10 V dc; power shall be applied to achieve T_J = +150°C minimum and a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3 n = 45, c = 0. The sample size may be increased and the test time decreased so long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

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* 4.4.3.2 Quality levels JAN, JANTX and JANTXV (see table E-VII of MIL-PRF-19500).

Subgroup	Method	Condition
C2	2036	Test condition A, weight = 7 pounds, ±5 ounces, application time = 15 seconds; Test condition D1, torque = 6 inch-ounce, application time = 15 seconds; Test condition D2, torque = 15 in-lbs, application time = 15 seconds.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3), and in accordance with thermal impedance curves.
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein. Delta measurements shall be in accordance with the applicable steps of 4.5.3.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Inspection conditions. Unless otherwise specified herein all inspections shall be conducted at a case temperature (T_C) of +25°C.

* 4.5.3 Delta requirements. Delta requirements shall be as specified below: (1) (2) (3) (4) (5)

Steps	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
* 1.	Collector to emitter cutoff current	3041	Condition C, V_{CE} = -60 V dc	ΔI_{CES1}	100 percent of initial value or -100 nA, whichever is greater.		
2.	Forward-current transfer ratio	3076	I_C = -2.5 V dc, V_{CE} = -5 V dc pulsed (see 4.5.1)	Δh_{FE2}	± 20 percent change from initial reading.		

(1) See MIL-PRF-19500 for sampling plan.
(2) Devices which exceed the group A limits for this test shall not be accepted.
(3) The delta measurements for table E-VIA (JANS) of MIL-PRF-19500 are as follows:
  a. Subgroup 4, see 4.5.3 herein, steps 1 and 2.
  b. Subgroup 5, see 4.5.3 herein, steps 1 and 2.
(4) The delta measurements for table E-VIB (JAN, JANTX and JANTXV) of MIL-PRF-19500 are as follows:
  a. Step 1, see 4.5.3 herein, steps 1 and 2.
  b. Step 3, see 4.5.3 herein, steps 1 and 2.
(5) The delta measurements for table E-VII of MIL-PRF-19500 are as follows: Subgroup 6, see 4.5.3 herein, steps 1 and 2.
* (6) The delta measurements for table E-IX of MIL-PRF-19500 are as follows: Subgroups 1 and 2, see 4.5.3 herein, steps 1 and 2.

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* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical examination 3/	2071					
* Solderability 3/ 4/	2026					
Resistance to solvents 3/ 4/ 5/	1022					
* Salt atmosphere (corrosion)	1041	n = 6 devices, c = 0, (For laser marked devices only)				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles.				
Hermetic seal 4/ Fine leak Gross leak	1071					
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hours or T_A = +300°C at t = 2 hours n = 11 wires, c = 0				
Decap internal visual (design verification) 4/	2075	n = 4 devices, c = 0				
Subgroup 2						
Thermal impedance 6/	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
Breakdown voltage, collector to emitter	3011	Bias condition D, I_C = -100mA, I_B = 0, pulsed (see 4.5.1).	$V_{BR(CEO)}$	-80		V dc
Collector to emitter cutoff current	3041	Bias condition C, V_{CE} = -60 V dc, V_{BE} = 0.	I_{CES1}		-1.0	µA dc
Collector to emitter cutoff current	3041	Bias condition C, V_{CE} = -100 V dc, V_{BE} = 0.	I_{CES2}		-1.0	mA dc
Collector to emitter cutoff current	3041	Bias condition D, V_{CE} = -40 V dc, I_B = 0.	I_{CEO}		-50	µA dc
Emitter to base cutoff current	3061	Bias condition C, V_{EB} = -4 V dc, I_C = 0.	I_{EBO1}		-1.0	µA dc
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = -5.5 V dc, I_C = 0.	I_{EBO2}		-1.0	mA dc

See footnotes at end of table.

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* TABLE I. Group A inspection. - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward - current transfer ratio	3076	V_{CE} = -5 V dc, I_C = -50 mA dc				
2N5003 2N5005			h_{FE1}	20 50		
Forward - current transfer ratio	3076	V_{CE} = -5 V dc, I_C = -2.5 A dc, pulsed (see 4.5.1).				
2N5003 2N5005			h_{FE2}	30 70	90 200	
Forward - current transfer ratio	3076	V_{CE} = -5 V dc, I_C = -5 A dc, pulsed (see 4.5.1).	h_{FE3}			
2N5003 2N5005				20 40		
Base-emitter voltage (nonsaturated)	3066	Test condition B, V_{CE} = -5 V dc, I_C = -2.5 A dc, pulsed (see 4.5.1)	V_{BE}		-1.45	V dc
Base-emitter saturation voltage	3066	Test condition B, I_C = -2.5 A dc, I_B = -250 mA dc, pulsed (see 4.5.1)	$V_{BE(sat1)}$		-1.45	V dc
Base-emitter saturation voltage	3066	Test condition B, I_C = -5 A dc, I_B = -500 mA dc, pulsed (see 4.5.1)	$V_{BE(sat2)}$		-2.2	V dc
Collector-emitter saturation voltage	3071	I_C = -2.5 A dc, I_B = -250 mA dc, pulsed (see 4.5.1)	$V_{CE(sat1)}$		-0.75	V dc
Collector-emitter saturation voltage	3071	I_C = -5 A dc, I_B = -500 mA dc pulsed (see 4.5.1)	$V_{CE(sat2)}$		-1.5	V dc
Subgroup 3						
High-temperature operation:		T_C = +150°C				
Collector to emitter cutoff current	3041	Bias condition C; V_{CE} = -60 V dc, V_{BE} = 0.	I_{CES}		-500	µA dc
Low-temperature operation:		T_C = -55°C				
Forward-current transfer ratio	3076	V_{CE} = -5 V dc, I_C = -2.5 A dc, pulsed (see 4.5.1)	h_{FE4}			
2N5003 2N5005				15 25		

See footnotes at end of table.

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* TABLE I. Group A inspection. - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Common-emitter, small-signal, short-circuit, forward-current transfer ratio	3206	V_{CE} = -5 V dc, I_C = -100 mA dc, f = 1 kHz	h_{fe}			
2N5003				20		
2N5005				50		
Magnitude of common-emitter, small-signal short-circuit, forward-current transfer ratio	3306	V_{CE} = -5 V dc, I_C = -500 mA dc f = 10 MHz	$\|h_{fe}\|$			
2N5003				6		
2N5005				7		
Open-circuit output capacitance	3236	V_{CB} = -10 V dc, I_E = 0, f = 1 MHz	C_{obo}		250	pF
Switching time		I_C = -5 A dc, I_{B1} = -500 mA dc	t_{on}		0.5	µs
		I_{B2} = -500 mA dc	t_s		1.4	µs
		$V_{BE(off)}$ = -3.7 V	t_f		0.5	µs
		R_L = 6Ω, (see figure 6)	t_{off}		1.5	µs
Subgroup 5						
Safe operating area (dc)	3051	Pre-pulse condition for each test: V_{CE} = 0, I_C = 0, T_C = +25°C Pulse condition for each test t_p = 1 sec. 1 cycle T_C = +25°C, (see figure 7)				
Test #1		V_{CE} = -12 V dc, I_C = -5 A dc				
Test #2		V_{CE} = -32 V dc, I_C = -1.7 A dc				
Test #3		V_{CE} = -80 V dc, I_C = -100 mA dc				

See footnotes at end of table.

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* TABLE I. Group A inspection. - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 5 - Continued.						
* Safe operating area (unclamped inductive)	3053	Condition C, T_C = +25°C, R_{BB1} = 10Ω, R_{BB2} = 100Ω, L = 0.3 mH, RL = 0.1Ω, V_{CC} = -10 V dc V_{BB1} = -10 V dc, V_{BB2} = -4 V dc I_{CM} = -10 A dc (See figure 5)				
End-point electrical measurements		See 4.5.3 and subgroup 2 of table I.				
Subgroups 6 and 7						
Not applicable						

1/ For sampling plan, see MIL-PRF-19500.
2/ For resubmission of failed in subgroup 1 of table I, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.
6/ This test required for the following end-point measurements only:
Group B, step 1 of 4.4.2.2 herein (JAN, JANTX, and JANTXV).
Group B, subgroups 3, 4, and 5 (JANS).
Group C, subgroup 2 and 6.
Group E, subgroup 1 and 2.

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TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and 4.5.3 herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	Intermittent operation life: V_{CB} = -10 V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C.	
Electrical measurements		See table I, subgroup 2 and 4.5.3 herein.	
Subgroup 4			
Thermal impedance curves		See MIL-PRF-19500.	Sample size N/A
Subgroup 5			
Not applicable			
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B.	

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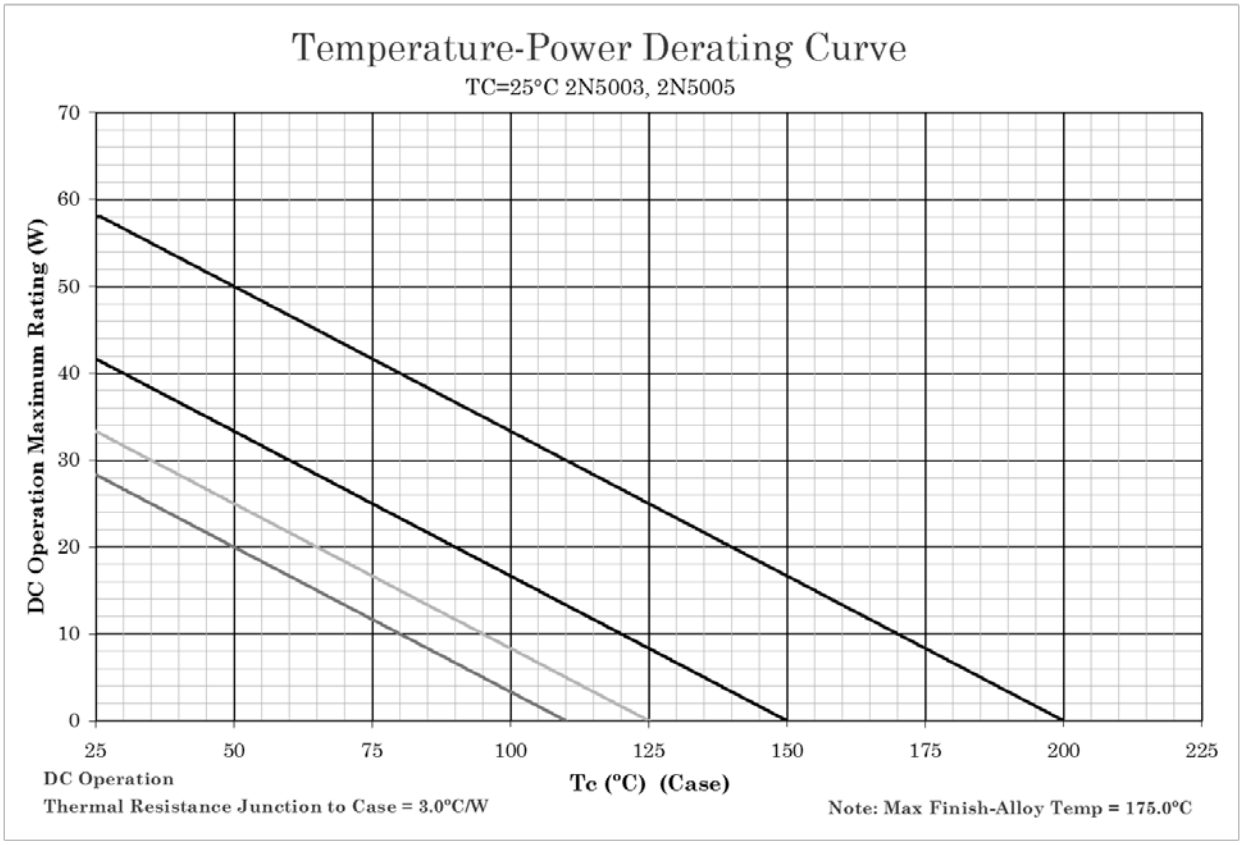

NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ +125°C, and +110°C to show power rating where most users want to limit T_J in their application.

FIGURE 3. Temperature-power derating for ($R_{\theta JC}$) 2N5003 and 2N5005 (similar to TO-59).

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Maximum Thermal Impedance

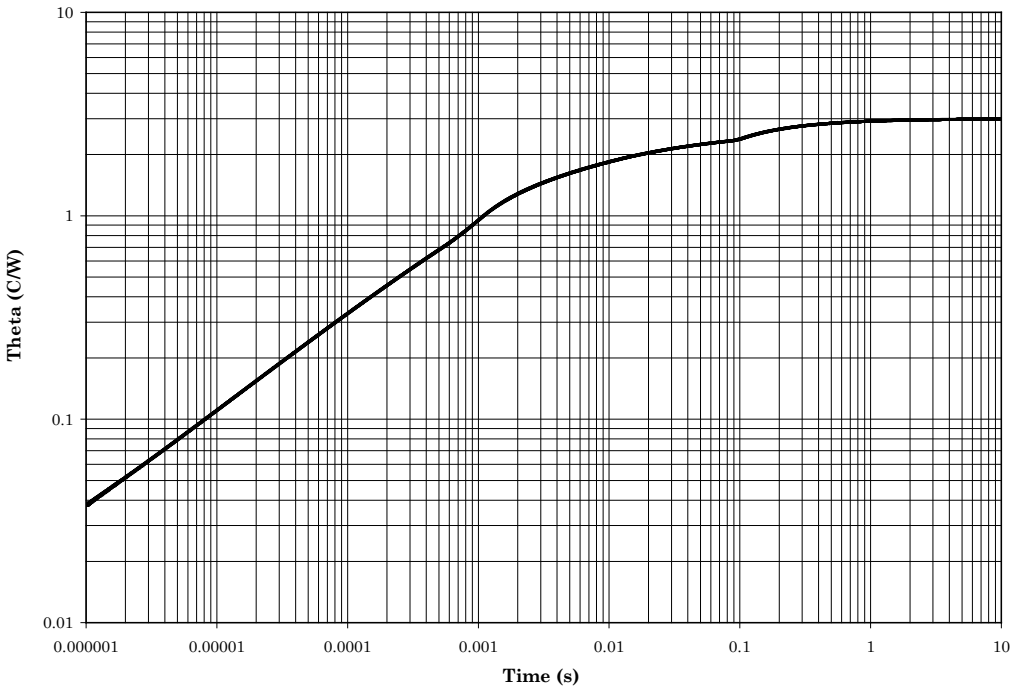
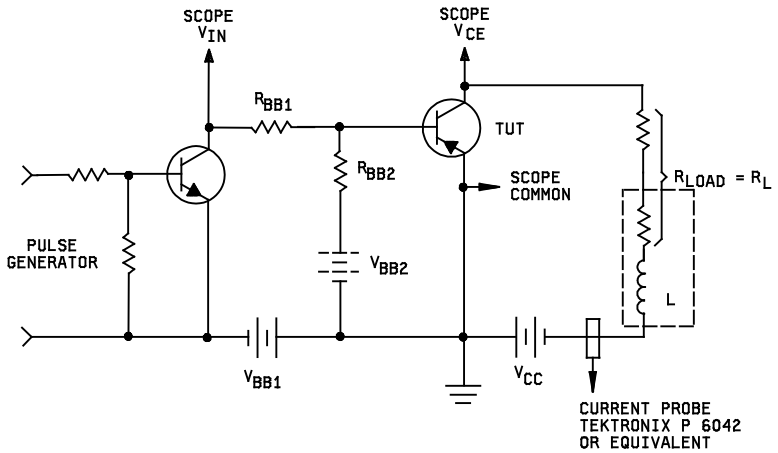


FIGURE 4. Thermal impedance graph ($R_{\theta JC}$) for 2N5003 and 2N5005 (similar to TO-59).



R_{BB1} = 10Ω	V_{CC} = -10 V dc
R_{BB2} = 100Ω	I_C = -10 A
L = 0.3 mH	V_{BB1} = -10 V dc
R_L = 0.1Ω	V_{BB2} = -4 V dc

FIGURE 5. Unclamped inductive load energy test circuit.

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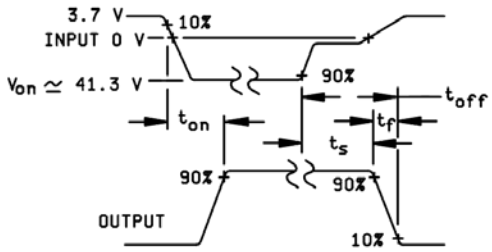

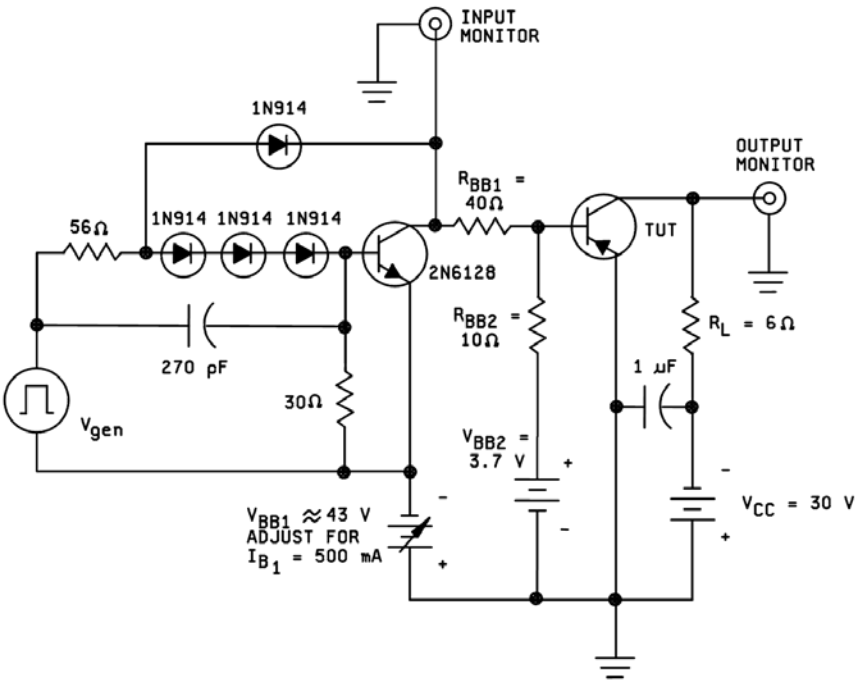

NOTES:

1. V_{gen} is -30 pulse (from 0 V) into a 50 ohm termination.
2. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f = 15$ ns, $Z_{out} = 50$ ohm, duty cycle ≤ 2 percent.
3. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 1$ ns, $R_{IN} \geq 10$ MΩ, $C_{IN} \leq 11.5$ pF.
4. Resistors shall be noninductive types.
5. The dc power supplies may require additional bypassing in order to minimize ringing.
6. An equivalent drive circuit may be used.

FIGURE 6. Switching time test circuit.

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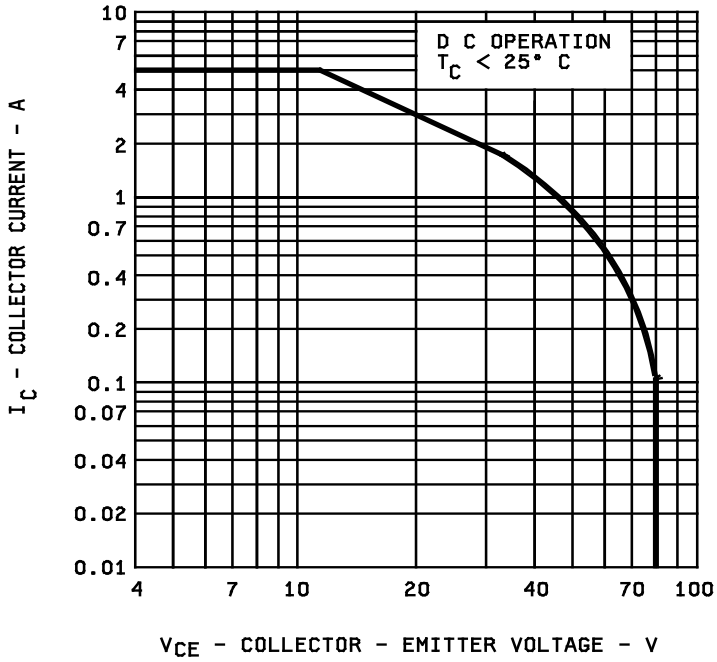

FIGURE 7. Maximum safe operating area.

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5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

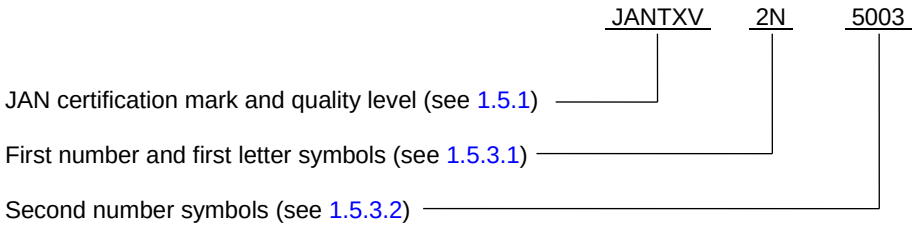
* d. The complete PIN, see 1.5 and 6.6.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 Interchangeability information. The 2N5003 and 2N5005 (MIL-PRF-19500/535) are inactive for new design. For new design use 2N7372 (MIL-PRF-19500/612). MIL-PRF-19500/612 is a T0-254 package version of MIL-PRF-19500/535, which is a T0-210 (T0-59) package version. The military 2N7372 contains the same die as the military 2N5003 and 2N5005.

* 6.5 PIN construction example.

* 6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



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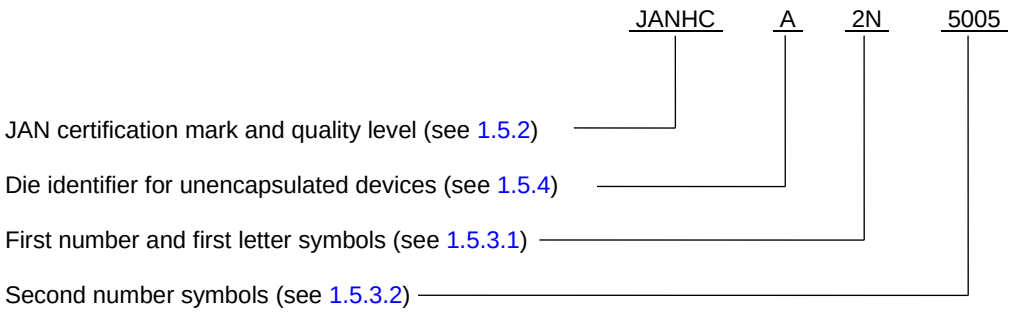
* 6.5.2 Unencapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



* 6.6 List of PINs.

* 6.6.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN2N5003	JANTX2N5003	JANTXV2N5003	JANS2N5003
JAN2N5005	JANTX2N5005	JANTXV2N5005	JANS2N5005

* 6.6.2 List of PINs for unencapsulated devices. The following is a list of possible PINs available on this specification sheet. The qualified die suppliers with the applicable letter version (e.g., JANHCA2N5003) will be identified on the QML.

JANHC ordering information	
PIN	Manufacturer CAGE
	33178
2N5003 2N5005	JANHCA2N5003 JANHCA2N5005
2N5003 2N5005	JANKCA2N5003 JANKCA2N5005

* 6.7 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@.dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

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6.8 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Air Force - 19, 99

Preparing activity:
DLA - CC

(Project 5961-2016-015)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.

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