

NOTICE OF CHANGE

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The documentation and process measures necessary to comply with this notice shall be completed by 1 May 1998.

MIL-STD-883E
NOTICE 1
1 December 1997

DEPARTMENT OF DEFENSE
TEST METHODS STANDARD
MICROCIRCUITS

TO ALL HOLDERS OF MIL-STD-883E:

1. THE FOLLOWING TEST METHODS OF MIL-STD-883E HAVE BEEN REVISED AND SUPERSEDE THE TEST METHODS LISTED:

NEW METHOD	DATE	SUPERSEDED METHOD	DATE
1019.5	1 December 1997	1019.4	15 November 1991

2. THE FOLLOWING PAGES OF MIL-STD-883E HAVE BEEN REVISED AND SUPERSEDE THE PAGES LISTED:

METHOD	NEW PAGE	DATE	SUPERSEDED PAGE	DATE
—	iii	31 December 1996	iii	REPRINTED WITHOUT CHANGE
—	iv	1 December 1997	iv	31 December 1996
—	v	31 December 1996	v	REPRINTED WITHOUT CHANGE
—	vi	31 December 1996	vi	REPRINTED WITHOUT CHANGE
2032.1	5	1 June 1993	5	REPRINTED WITHOUT CHANGE
	6	1 December 1997	6	1 June 1993
	7	1 June 1993	7	1 June 1993
	8	1 December 1997	8	1 June 1993
	13	1 June 1993	13	REPRINTED WITHOUT CHANGE
	13a	1 December 1997	NEW	—
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	14	1 December 1997	14	19 August 1994
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	8	1 December 1997	8	31 October 1995

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3. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

4. Holders of MIL-STD-883E will verify that page changes, additions, and corrections indicated above have been entered. This notice page will be retained as a check sheet. This issuance, together with appended pages, is a separate publication. Each notice is to be retained by stocking points until the military standard is completely revised or canceled.

NOTE: The margins of this notice are marked with asterisks to indicate where changes (additions, modifications, corrections, deletions) from the previous notice were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous notice.

CONCLUDING MATERIAL

Custodians:

Army - CR
Navy - EC
Air Force - 17
NASA-NA

Preparing activity:
DLA - CC

Review activities

Army - AR, MI, SM
Navy - OS, SH, TD, AS, CG, MC
Air Force - 19, 85, 99

(Project 5962-1801)

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METHOD 1019.5

IONIZING RADIATION (TOTAL DOSE) TEST PROCEDURE

- 1. **PURPOSE.** This test procedure defines the requirements for testing packaged semiconductor integrated circuits for ionizing radiation (total dose) effects from a cobalt-60 (⁶⁰Co) gamma ray source. In addition this procedure provides an accelerated annealing test for estimating low dose rate ionizing radiation effects on devices. This annealing test is important for low dose-rate or certain other applications in which devices may exhibit significant time-dependent effects. This procedure addresses only steady state irradiations, and is not applicable to pulse type irradiations. This test may produce severe degradation of the electrical properties of irradiated devices and thus should be considered a destructive test.

1.1 **Definitions.** Definitions of terms used in this procedure are given below:

- a. **Ionizing radiation effects.** The changes in the electrical parameters of a device or integrated circuit resulting from radiation-induced charge. These are also referred to as total dose effects.
- b. **In-flux test.** Electrical measurements made on devices during irradiation exposure.
- c. **Not in-flux test.** Electrical measurements made on devices at any time other than during irradiation.
- d. **Remote tests.** Electrical measurements made on devices which are physically removed from the radiation location.
- e. **Time dependent effects.** Significant degradation in electrical parameters caused by the growth or annealing or both of radiation-induced trapped charge after irradiation. Similar effects also take place during irradiation.
- f. **Accelerated annealing test.** A procedure utilizing elevated temperature to accelerate time-dependent effects.

2. **APPARATUS.** The apparatus shall consist of the radiation source, electrical test instrumentation, test circuit board(s), cabling, interconnect board or switching system, an appropriate dosimetry measurement system, and an environmental chamber (if required for time-dependent effects measurements). Adequate precautions shall be observed to obtain an electrical measurement system with sufficient insulation, ample shielding, satisfactory grounding, and suitable low noise characteristics.

2.1 **Radiation source.** The radiation source used in the test shall be the uniform field of a ⁶⁰Co gamma ray source. Uniformity of the radiation field in the volume where devices are irradiated shall be within ±10 percent as measured by the dosimetry system, unless otherwise specified. The intensity of the gamma ray field of the ⁶⁰Co source shall be known with an uncertainty of no more than ±5 percent. Field uniformity and intensity can be affected by changes in the location of the device with respect to the radiation source and the presence of radiation absorption and scattering materials.

2.2 **Dosimetry system.** An appropriate dosimetry system shall be provided which is capable of carrying out the measurements called for in 3.2. The following American Society for Testing and Materials (ASTM) standards or other appropriate standards shall be used:

- ASTM E 666 - Standard Method for Calculation of Absorbed Dose from Gamma or X Radiation.
- ASTM E 668 - Standard Practice for the Application of Thermoluminescence Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices.
- ASTM E 1249 - Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices.

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ASTM E 1250 - Standard Method for Application of Ionization Chambers to Assess the Low Energy Gamma Component of Cobalt 60 Irradiators Used in Radiation Hardness Testing of Silicon Electronic Devices.

ASTM E 1275 - Standard Practice for Use of a Radiochromic Film Dosimetry System.

These industry standards address the conversion of absorbed dose from one material to another, and the proper use of various dosimetry systems. ^{1/}

2.3 Electrical test instruments. All instrumentation used for electrical measurements shall have the stability, accuracy, and resolution required for accurate measurement of the electrical parameters. Any instrumentation required to operate in a radiation environment shall be appropriately shielded.

2.4 Test circuit board(s). Devices to be irradiated shall either be mounted on or connected to circuit boards together with any associated circuitry necessary for device biasing during irradiation or for in-situ measurements. Unless otherwise specified, all device input terminals and any others which may affect the radiation response shall be electrically connected during irradiation, i.e., not left floating. The geometry and materials of the completed board shall allow uniform irradiation of the devices under test. Good design and construction practices shall be used to prevent oscillations, minimize leakage currents, prevent electrical damage, and obtain accurate measurements. Only sockets which are radiation resistant and do not exhibit significant leakages (relative to the devices under test) shall be used to mount devices and associated circuitry to the test board(s). All apparatus used repeatedly in radiation fields shall be checked periodically for physical or electrical degradation. Components which are placed on the test circuit board, other than devices under test, shall be insensitive to the accumulated radiation or they shall be shielded from the radiation. Test fixtures shall be made such that materials will not perturb the uniformity of the radiation field intensity at the devices under test. Leakage current shall be measured out of the radiation field. With no devices installed in the sockets, the test circuit board shall be connected to the test system such that all expected sources of noise and interference are operative. With the maximum specified bias for the test device applied, the leakage current between any two terminals shall not exceed ten percent of the lowest current limit value in the pre-irradiation device specification. Test circuit boards used to bias devices during accelerated annealing must be capable of withstanding the temperature requirements of the accelerated annealing test and shall be checked before and after testing for physical and electrical degradation.

2.5 Cabling. Cables connecting the test circuit boards in the radiation field to the test instrumentation shall be as short as possible. If long cables are necessary, line drivers may be required. The cables shall have low capacitance and low leakage to ground, and low leakage between wires.

2.6 Interconnect or switching system. This system shall be located external to the radiation environment location, and provides the interface between the test instrumentation and the devices under test. It is part of the entire test system and subject to the limitation specified in 2.4 for leakage between terminals.

2.7 The environmental chamber. The environmental chamber for time-dependent effects testing, if required, shall be capable of maintaining the selected accelerated annealing temperature within $\pm 5^{\circ}\text{C}$.

^{1/} Copies may be obtained from the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.

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3. **PROCEDURE.** The test devices shall be irradiated and subjected to accelerated annealing (if required for time-dependent effects testing) as specified by a test plan. This plan shall specify the device description, irradiation conditions, device bias conditions, dosimetry system, operating conditions, measurement parameters and conditions, and accelerated annealing test conditions (if required).

3.1 **Sample selection and handling.** Only devices which have passed the electrical specifications as defined in the test plan shall be submitted to radiation testing. Unless otherwise specified, the test samples shall be randomly selected from the parent population and identically packaged. Each part shall be individually identifiable to enable pre- and post-irradiation comparison. For device types which are ESD-sensitive, proper handling techniques shall be used to prevent damage to the devices.

3.2 **Burn-in.** For some devices, there are differences in the total dose radiation response before and after burn-in. Unless it has been shown by prior characterization or by design that burn-in has negligible effect (parameters remain within postirradiation specified electrical limits) on the total dose radiation response, then one of the following must be done:

3.2.1 The manufacturer shall subject the radiation samples to the specified burn-in conditions prior to conducting total dose radiation testing or

3.2.2 The manufacturer shall develop a correction factor (which is acceptable to the parties to the test), taking into account the changes in total dose response resulting from subjecting product to burn-in. The correction factor shall then be used to accept product for total dose response without subjecting the test samples to burn-in.

3.3 **Dosimetry measurements.** The radiation field intensity at the location of the device under test shall be determined prior to testing by dosimetry or by source decay correction calculations, as appropriate, to assure conformance to test level and uniformity requirements. The dose to the device under test shall be determined one of two ways: (1) by measurement during the irradiation with an appropriate dosimeter, or (2) by correcting a previous dosimetry value for the decay of the ^{60}Co source intensity in the intervening time. Appropriate correction shall be made to convert from the measured or calculated dose in the dosimeter material to the dose in the device under test.

3.4 **Lead/Aluminum (Pb/Al) container.** Test specimens shall be enclosed in a Pb/Al container to minimize dose enhancement effects caused by low-energy, scattered radiation. A minimum of 1.5 mm Pb, surrounding an inner shield of at least 0.7 mm Al, is required. This Pb/Al container produces an approximate charged particle equilibrium for Si and for TLDs such as CaF_2 . The radiation field intensity shall be measured inside the Pb/Al container (1) initially, (2) when the source is changed, or (3) when the orientation or configuration of the source, container, or test-fixture is changed. This measurement shall be performed by placing a dosimeter (e.g., a TLD) in the device-irradiation container at the approximate test-device position. If it can be demonstrated that low energy scattered radiation is small enough that it will not cause dosimetry errors due to dose enhancement, the Pb/Al container may be omitted.

3.5 **Radiation level(s).** The test devices shall be irradiated to the dose level(s) specified in the test plan within ± 10 percent. If multiple irradiations are required for a set of test devices, then the post-irradiation electrical parameter measurements shall be performed after each irradiation.

3.6 **Radiation dose rate.**

CAUTION: For the application of some bipolar and biCMOS devices to space-level dose rates, testing at condition A dose rates may not provide worst case results. These are devices that fail due to reduced transistor gain.

NOTE: For those bipolar and biCMOS devices where the application involves space level dose rates and the excess base current has been observed to increase at decreasing dose rates, testing may be accomplished at the lowest dose rate of interest in accordance with condition C in order to obtain a conservative estimate of device performance.

3.6.1 **Condition A.** For condition A (standard condition) the dose rate shall be between 50 and 300 rad(Si)/s [0.5 and 3 Gy(Si)/s] ^{60}Co 2/ The dose rates may be different for each radiation dose level in a series; however, the dose rate shall not vary by more than ± 10 percent during each irradiation.

2/ The SI unit for the quantity absorbed dose is the gray, symbol Gy. 100 rad = 1 Gy.

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3.6.2 Condition B. For condition B, for MOS devices only, if the maximum dose rate is < 50 rad(Si)/s in the intended application, the parties to the test may agree to perform the test at a dose rate \geq the maximum dose rate of the intended application. Unless the exclusions in 3.12.1b are met, the accelerated annealing test of 3.12.2 shall be performed.

3.6.3 Condition C. For condition C, (as an alternative) the test may be performed at the dose rate of the intended application if this is agreed to by the parties to the test.

3.7 Temperature requirements. Since radiation effects are temperature dependent, devices under test shall be irradiated in an ambient temperature of $24^{\circ}\text{C} \pm 6^{\circ}\text{C}$ as measured at a point in the test chamber in close proximity to the test fixture. The electrical measurements shall be performed in an ambient temperature of $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. If devices are transported to and from a remote electrical measurement site, the temperature of the test devices shall not be allowed to increase by more than 10°C from the irradiation environment. If any other temperature range is required, it shall be specified.

3.8 Electrical performance measurements. The electrical parameters to be measured and functional tests to be performed shall be specified in the test plan. As a check on the validity of the measurement system and pre- and post-irradiation data, at least one control sample shall be measured using the operating conditions provided in the governing device specifications. For automatic test equipment, there is no restriction on the test sequence provided that the rise in the device junction temperature is minimized. For manual measurements, the sequence of parameter measurements shall be chosen to allow the shortest possible measurement period. When a series of measurements is made, the tests shall be arranged so that the lowest power dissipation in the device occurs in the earliest measurements and the power dissipation increases with subsequent measurements in the sequence.

The pre- and post-irradiation electrical measurements shall be done on the same measurement system and the same sequence of measurements shall be maintained for each series of electrical measurements of devices in a test sample. Pulse-type measurements of electrical parameters should be used as appropriate to minimize heating and subsequent annealing effects. Devices which will be subjected to the accelerated annealing testing (see 3.12) may be given a preirradiation burn-in to eliminate burn-in related failures.

3.9 Test conditions. The use of in-flux or not in-flux testing shall be specified in the test plan. (This may depend on the intended application for which the data are being obtained.) The use of in-flux testing may help to avoid variations introduced by post-irradiation time dependent effects. However, errors may be incurred for the situation where a device is irradiated in-flux with static bias, but where the electrical testing conditions require the use of dynamic bias for a significant fraction of the total irradiation period. Not-in-flux testing generally allows for more comprehensive electrical testing, but can be misleading if significant post-irradiation time dependent effects occur.

3.9.1 In-flux testing. Each test device shall be checked for operation within specifications prior to being irradiated. After the entire system is in place for the in-flux radiation test, it shall be checked for proper interconnections, leakage (see 2.4), and noise level. To assure the proper operation and stability of the test setup, a control device with known parameter values shall be measured at all operational conditions called for in the test plan. This measurement shall be done either before the insertion of test devices or upon completion of the irradiation after removal of the test devices or both.

3.9.2 Remote testing. Unless otherwise specified, the bias shall be removed and the device leads placed in conductive foam (or similarly shorted) during transfer from the irradiation source to a remote tester and back again for further irradiation. This minimizes post-irradiation time dependent effects.

3.9.3 Bias and loading conditions. Bias conditions for test devices during irradiation or accelerated annealing shall be within ± 10 percent of those specified by the test plan. The bias applied to the test devices shall be selected to produce the greatest radiation induced damage or the worst-case damage for the intended application, if known. The specified bias shall be maintained on each device in accordance with the test plan. Bias shall be checked immediately before and after irradiation. Care shall be taken in selecting the loading such that the rise in the junction temperature is minimized.

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3.10 Post-irradiation procedure. Unless otherwise specified, the following time intervals shall be observed:

- a. The time from the end of an irradiation to the start of electrical measurements shall be a maximum of 1 hour.
- b. The time to perform the electrical measurements and to return the device for a subsequent irradiation, if any, shall be within two hours of the end of the prior irradiation.

To minimize time dependent effects, these intervals shall be as short as possible. The sequence of parameter measurements shall be maintained constant throughout the tests series.

3.11 Extended room temperature anneal test. The tests of 3.1 through 3.10 are known to be overly conservative for some devices in a very low dose rate environment (e.g. dose rates characteristic of space missions). The extended room temperature anneal test provides an estimate of the performance of a device in a very low dose rate environment even though the testing is performed at a relatively high dose rate (e.g. 50-300 rad(Si)/s). The procedure involves irradiating the device per steps 3.1 through 3.10 and post-irradiation subjecting the device under test to a room temperature anneal for an appropriate period of time (see 3.11.2c) to allow leakage-related parameters that may have exceeded their pre-irradiation specification to return to within specification. The procedure is known to lead to a higher rate of device acceptance in cases:

- a. where device failure when subjected to the tests in 3.1 through 3.10 has been caused by the buildup of trapped positive charge in relatively soft oxides, and
- b. where this trapped positive charge anneals at a relatively high rate.

3.11.1 Need to perform an extended room temperature anneal test. The following criteria shall be used to determine whether an extended room temperature anneal test is appropriate:

- a. The procedure is appropriate for either MOS or bipolar technology devices.
- b. The procedure is appropriate where only parametric failures (as opposed to functional failure) occurs. The parties to the test shall take appropriate steps to determine that the device under test is subject to only parametric failure over the total ionizing dose testing range.
- c. The procedure is appropriate where the natural annealing response of the device under test will serve to correct the out-of-specification of any parametric response. Further, the procedure is known to lead to a higher rate of device acceptance in cases where the expected application irradiation dose rate is sufficiently low that ambient temperature annealing of the radiation induced trapped positive charge can lead to a significant improvement of device behavior. Cases where the expected application dose rate is lower than the test dose rate and lower than 0.1 rad(Si)/s should be considered candidates for the application of this procedure. The parties to the test shall take appropriate steps to determine that the technology under test can provide the required annealing response over the total ionizing dose testing range.

3.11.2 Extended room temperature anneal test procedure. If the device fails the irradiation and testing specified in 3.1 through 3.10, an additional room temperature annealing test may be performed as follows:

- a. Following the irradiation and testing of 3.1 through 3.10, subject the device under test to a room temperature anneal under worst-case static bias conditions. For information on worst case bias see 3.9.3.
- b. The test will be carried out in such a fashion that the case of the device under test will have a temperature within the range $24^{\circ}\text{C} \pm 6^{\circ}\text{C}$.

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- c. Where possible, the room temperature anneal should continue for a length of time great enough to allow device parameters that have exceeded their pre-irradiation specification to return to within specification or post-irradiation-parametric limit (PIPL) as established by the manufacturer. However, the time of the room temperature anneal shall not exceed t_{max} where

$$t_{max} = \frac{D_{spec}}{R_{max}}$$

D_{spec} is the total ionizing dose specification for the part and R_{max} is the maximum dose rate for the intended use.

- d. Test the device under test for electrical performance as specified in 3.7 and 3.8. If the device under test passes electrical performance tests following the extended room temperature anneal, this shall be considered acceptable performance for a very low dose rate environment in spite of having previously failed the post-irradiation and electrical tests of 3.1 through 3.10.
- 3.12 MOS accelerated annealing test. The accelerated annealing test provides an estimate of worst-case degradation of MOS microcircuits in low dose rate environments. The procedure involves heating the device following irradiation at specified temperature, time and bias conditions. An accelerated annealing test (see 3.12.2) shall be performed for cases where time dependent effects (TDE) can cause a device to degrade significantly or fail. Only standard testing shall be performed as specified in 3.1 through 3.10 for cases where TDE are known not to cause significant device degradation or failure (see 3.12.1) or where they do not need to be considered, as specified in 3.12.1.
- 3.12.1 Need to perform accelerated annealing test. The parties to the test shall take appropriate steps to determine whether accelerated annealing testing is required. The following criteria shall be used:
 - a. The tests called out in 3.12.2 shall be performed for any device or circuit type that contains MOS circuit elements (i.e., transistors or capacitors).
 - b. TDE tests may be omitted if:
 1. circuits are known not to contain MOS elements by design, or
 2. the ionizing dose in the application, if known, is below 5 krad(Si), or
 3. the lifetime of the device from the onset of the irradiation in the intended application, if known, is short compared with TDE times, or
 4. the test is carried out at the dose rate of the intended application, or
 5. the device type or IC technology has been demonstrated via characterization testing not to exhibit TDE changes in device parameters greater than experimental error (or greater than an otherwise specified upper limit) and the variables that affect TDE response are demonstrated to be under control for the specific vendor processes.

At a minimum, the characterization testing in (5) shall include an assessment of TDE on propagation delay, output drive, and minimum operating voltage parameters. Continuing process control of variables affecting TDE may be demonstrated through lot sample tests of the radiation hardness of MOS test structures.
 - c. This document provides no guidance on the need to perform accelerated annealing tests on technologies that do not include MOS circuit elements.
- 3.12.2 Accelerated annealing test procedure. If the device passes the tests in 3.1 through 3.10 or if it passes 3.11 (if that procedure is used) to the total ionizing dose level specified in the test plan or device specification or drawing and the exclusions of 3.12.1 do not apply, the accelerated annealing test shall be conducted as follows:

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a. Overtest

1. Irradiate each test device to an additional 0.5-times the specified dose using the standard test conditions (3.1 through 3.10). Note that no electrical testing is required at this time.

2. The additional 0.5-times irradiation in 3.12.2.a.1 may be omitted if it has been demonstrated via characterization testing that:

- a. none of the circuit propagation delay, output drive, and minimum operating voltage parameters recover toward their pre-irradiation value greater than experimental accelerated annealing test of 3.12.2.b, and
- b. the irradiation biases chosen for irradiation and accelerated annealing tests are worst-case for the response of these parameters during accelerated annealing.

The characterization testing to establish worst-case irradiation and annealing biases shall be performed at the specified level. The testing shall at a minimum include separate exposures under static and dynamic irradiation bias, each followed by worst-case static bias during accelerated annealing according to 3.12.2.b.

b. Accelerated annealing. Heat each device under worst-case static bias conditions in an environmental chamber according to one of the following conditions:

1. At 100°C ±5°C for 168 ±12 hours, or
2. At an alternate temperature and time that has been demonstrated via characterization testing to cause equal or greater change in the parameter(s) of interest, e.g., propagation delay, output drive, and minimum operating voltage, in each test device as that caused by 3.12.2.b.1, or
3. At an alternate temperature and time which will cause trapped hole annealing of >60% and interface state annealing of <10% as determined via characterization testing of NMOS test transistors from the same process. It shall be demonstrated that the radiation response of test transistors represent that of the device under test.

c. Electrical testing. Following the accelerated annealing the electrical test measurements shall be performed as specified in 3.8 and 3.9.

3.13 Test report. As a minimum, the report shall include the device type number, serial number, the manufacturer, package type, controlling specification, date code, and any other identifying numbers given by the manufacturer. The bias circuit, parameter measurement circuits, the layout of the test apparatus with details of distances and materials used, and electrical noise and current leakage of the electrical measurement system for in-flux testing shall be reported using drawings or diagrams as appropriate. Each data sheet shall include the test date, the radiation source used, the bias conditions during irradiation, the ambient temperature around the devices during irradiation and electrical testing, the duration of each irradiation, the time between irradiation and the start of the electrical measurements, the duration of the electrical measurements and the time to the next irradiation when step irradiations are used, the irradiation dose rate, electrical test conditions, dosimetry system and procedures and the radiation test levels. The pre- and post-irradiation data shall be recorded for each part and retained with the parent population data in accordance with the requirements of MIL-PRF-38535 or MIL-PRF-38534. Any anomalous incidents during the test shall be fully documented and reported. The accelerated annealing procedure, if used, shall be described. Any other radiation test procedures or test data required for the delivery shall be specified in the device specification, drawing or purchase order.

4. SUMMARY. The following details shall be specified in the applicable acquisition document as required:

- a. Device-type number(s), quantity, and governing specifications (see 3.1).
- b. Radiation dosimetry requirements (see 3.3).

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- c. Radiation test levels including dose and dose rate (see 3.5 and 3.6).
- d. Irradiation, electrical test and transport temperatures if other than as specified in 3.7.
- e. Electrical parameters to be measured and device operating conditions during measurement (see 3.8).
- f. Test conditions, i.e., in-flux or not-in-flux type tests (see 3.9).
- g. Bias conditions for devices during irradiation (see 3.9.3).
- h. Time intervals of the post-irradiation measurements (see 3.10).
- i. Requirement for extended room temperature anneal test, if required (see 3.11).
- j. Requirement for accelerated annealing test, if required (see 3.12).
- k. Documentation required to be delivered with devices (see 3.13).

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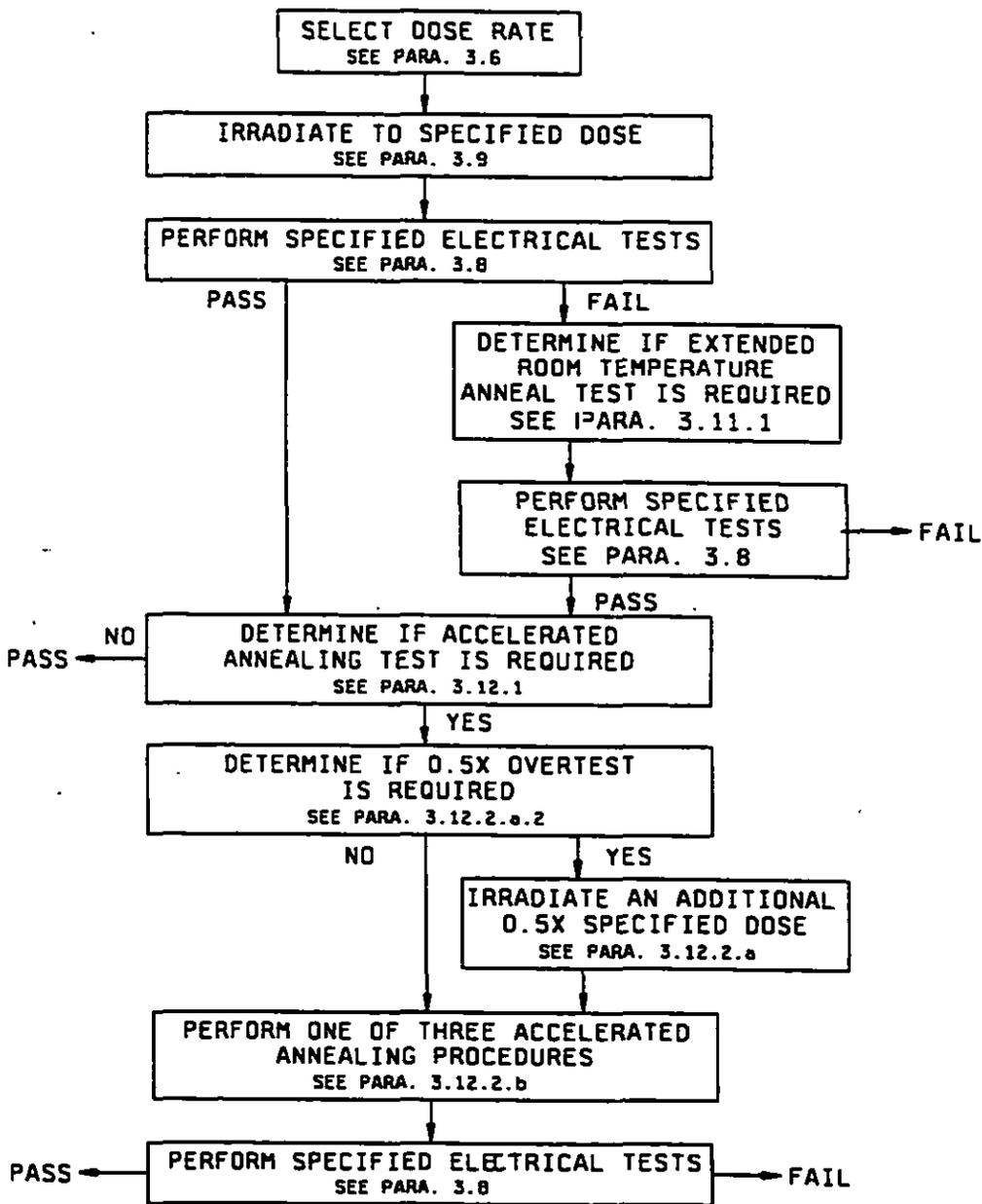


FIGURE 1019-1. Flow diagram for ionizing radiation test procedure.

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- (34) Resistor ladder rung is that portion of a resistor ladder structure intended to be laser trimmed to result in an incremental change in resistance.
- (35) Resistor loop is a resistor structure resembling a loop in appearance that can be trimmed. A coarse loop structure is one in which trimming results in a large resistance change (one that can cause an out-of-tolerance condition to occur). A fine loop structure is one in which trimming results in a small resistance change (one that cannot cause an out-of-tolerance condition to occur).
- (36) Resistor material, self passivating is one on which a conformal insulating layer can be thermally grown (such as tantalum nitride on which tantalum pentoxide is grown).
- (37) Scorching is discoloration of laser trimmed thin film resistor material without alteration of its physical form.
- (38) Scratch, metallization is any tearing defect, including probe marks, in the surface of the metallization. A mar on the metallization surface is not considered to be a scratch.
- (39) Scratch, resistor is any tearing defect in the resistor film. A mar on the resistor surface is not considered to be a scratch.
- (40) Sidebar is that portion of a resistor ladder structure to which rungs are attached. Sidebars are not intended to be laser trimmed.
- (41) Substrate is the supporting structural material into or upon which, or both, functional circuits are formed.
- (42) Surface Acoustic Wave (SAW) element is a planar element fabricated typically using thin film manufacturing techniques on various substrate materials. Size varies as a function of frequency and design features include interdigitated fingers.
- (43) Terminal is a metal area used to provide an electrical access point to functional circuitry.
- (44) Thick film is conductive, resistive or dielectric material screen printed onto a substrate and fired at temperature to fuse into its final form.
- (45) Thin film is conductive, resistive or dielectric material, usually less than 50,000Å in thickness, that is deposited onto a substrate by vacuum evaporation, sputtering, or other means.
- (46) Underlying material is any layer of material below the top-layer metallization. This includes metallization, resistor, passivation or insulating layers, or the substrate itself.
- (47) Via is an opening in the insulating material in which a vertical conductive electrical connection from one metallization layer to another in a multilayer substrate is made.
- (48) Vitrification is conversion into glass or a glassy substance by heat and fusion.
- (49) Void, metallization is any missing metallization where the underlying material is visible (exposed). Voids typically are caused by photolithographic, screen, or mask related defects, not by scratches.
- (50) Void, resistor is any missing resistor material where the underlying material is visible (exposed). Voids typically are caused by photolithographic, screen, or mask related defects, not by scratches.

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- (51) Wraparound conductor is one which extends around the edge of the substrate by design.
- (52) Coupling (air) bridge is a raised layer of metallization used for interconnection that is isolated from the surface of the element by an air gap or other insulating material.
- (53) Pit is a depression produced in a substrate surface typically by nonuniform deposition of metallization or by nonuniform processing such as excessively powered laser trim pulses.
- (54) Substrate, hard is the inorganic, rigid material into or upon which or both, functional circuits are formed. Typical materials are alumina and silicon.
- (55) Blister, metallization is a hollow bump that can be flattened.
- (56) Nodule, metallization is a solid bump that cannot be flattened.
- (57) Substrate via is an opening in the substrate material in which a vertical conductive electrical connection from one metallization layer to another is made.

3.1 Thin film element inspection. Inspection for visual defects described in this section shall be conducted on each planar thin film passive element. The "high magnification" inspection shall be within the range of 100X to 200X for both class H and class K. The "low magnification" inspection shall be within the range of 30X to 60X for both class H and class K. When inspection is performed prior to mounting, then elements utilizing ceramic or glass type substrates, without backside metallization, shall be inspected using backlighting for conditions of hair-line voiding or bridging. Patterned substrates that have geometries of 2.0 mils or greater shall be inspected at 10X to 60X magnification.

Class H

Class K

3.1.1 Operating metallization defects "high magnification". No element shall be acceptable that exhibits:

NOTE: The metallization defect criteria contained in this section apply to operating metallization only.

3.1.1.1 Metallization scratches.

- a. A scratch or probe mark in the metallization, excluding bonding pads, that both exposes under-lying material anywhere along its length and leaves less than 50 percent of the original metallization width undisturbed (see 2032-1h).

NOTE: These criteria do not apply to capacitors (see 3.1.1.1e).

NOTE: Underlying material does not have to be exposed along the full length of the scratch.

- a. Same as Class H.

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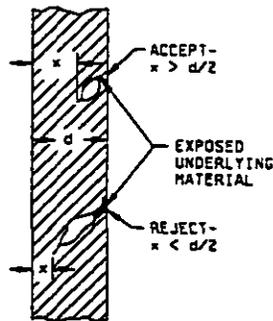


FIGURE 2032-1h. Class H metallization scratch criteria.

Class H

- 3.1.1.1 b. Scratch in the bonding pad area that both exposes underlying material and reduces the metallization path width, where it enters the bonding pad, and leaves less than 50 percent of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately (see figure 2032-2h).

Class K

- 3.1.1.1 b. Less than 75 percent (see figure 2032-2k).

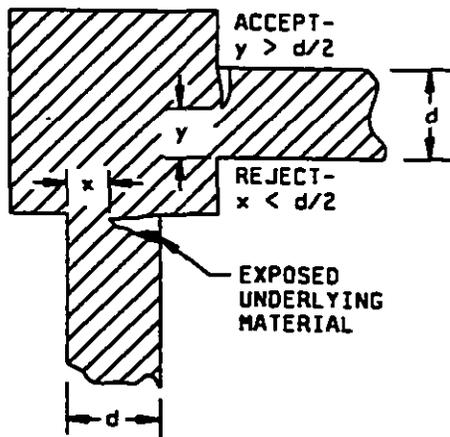


FIGURE-2032-2h. Class H metallization width reduction at bonding pad criteria.

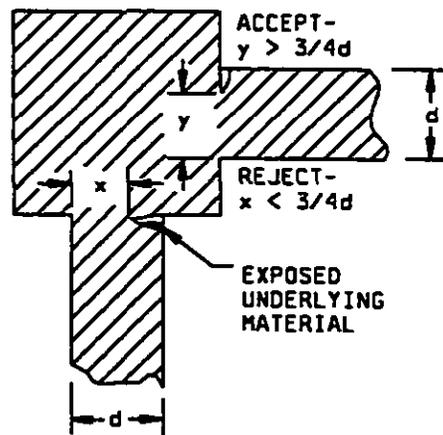


FIGURE 2032-2k. Class K metallization width reduction at bonding pad criteria.

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Class H

Class K

- 3.1.1.1 c. Scratch that completely crosses metallization and damages the metallization on either side.
- d. Scratches or probe marks in the bonding pad area that expose underlying material over greater than 25 percent of the original unglassivated metallization area.
- e. For capacitors only, a scratch in the metallization, other than in the bonding pad area, that exposes the dielectric material.

- 3.1.1.1 c. Same as class H.
- d. Same as class H.
- e. Same as class H.

3.1.1.2 Metallization voids.

- a. Void(s) in the metallization, excluding bonding pads, that leaves less than 50 percent of the original metallization width undisturbed (see figure 2032-3h).

- a. Same as Class H

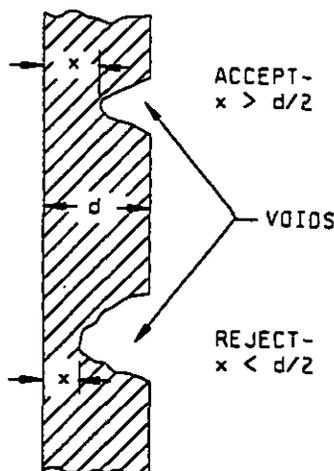


FIGURE 2032-3h. Class H metallization void criteria.

- b. Void(s) in the bonding pad area that reduces the metallization path width, where it enters the bonding pad, to less than 50 percent of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately.

- b. Less than 75 percent

NOTE: Figures 2032-2h and 2032-2k illustrate metallization width reduction at bonding pad criteria for scratches. Void criteria are similar.

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Class H

Class K

3.1.1.8 Metalized through-hole defects.
"high magnification". No element shall be acceptable that exhibits:

- a. Through-hole metallization that is not vertically continuous or that does not cover at least a continuous 50 percent of the inside, circumferential surface area unless by design.

a. Same as class H.

3.1.1.9 Wrap-around connection defects.
"high magnification". No element shall be acceptable that exhibits:

- a. Unmetallized area in the edges of wrap-around connections greater than 50 percent of the largest dimension of the edge metallization (see figure 2032-8h).

a. Same as class H.

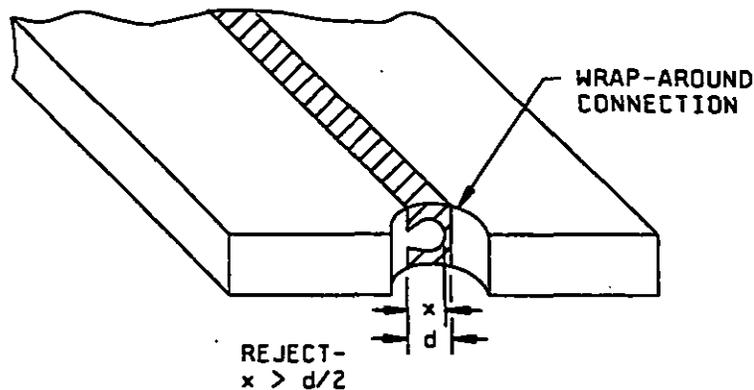


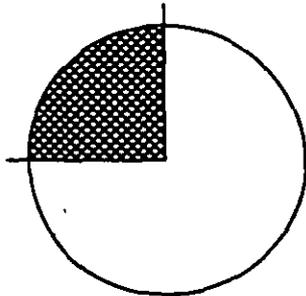
FIGURE 2032-8h. Class H wrap-around connection unmetallized area criterion.

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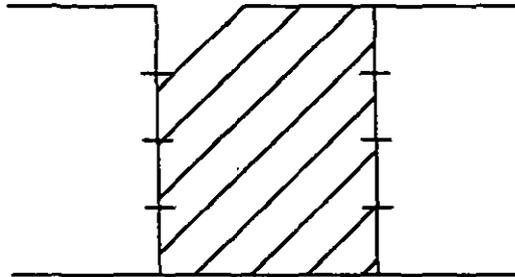
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- 3.1.1.10 Substrate via defects, "low magnification". When inspected from each side of the substrate, no element shall be acceptable that exhibits:
 - a. A complete void through the via.
 - b. Any lifting, peeling, or blistering of the via metallization.
 - c. Via fill less than 75% of the total surface area of the via plug and less than 75% of the substrate thickness.
- NOTE: These are *minimum requirements*. Via flatness and other requirements shall be in accordance with the applicable detail drawings.



VIA FILL < 75%
REJECT



VIA FILL < 75%
REJECT

FIGURE 2032-8Bh. Classes H and K via fill criteria.

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Class H

Class K

3.1.2 Passivation defects "high magnification".

No element shall be acceptable that exhibits:

- a. Either multiple lines (color fringing) or a complete absence of passivation visible at the edge and continuing under the metallization (see figure 2032-8Ah). A passivation defect that exhibits a line of separation from the metallization is acceptable.

NOTE: These criteria apply to conductive substrate elements only.

NOTE: Double or triple lines at the edge of the passivation defect indicate it can have sufficient depth to penetrate down to the bare substrate.

- a. Same as class H.

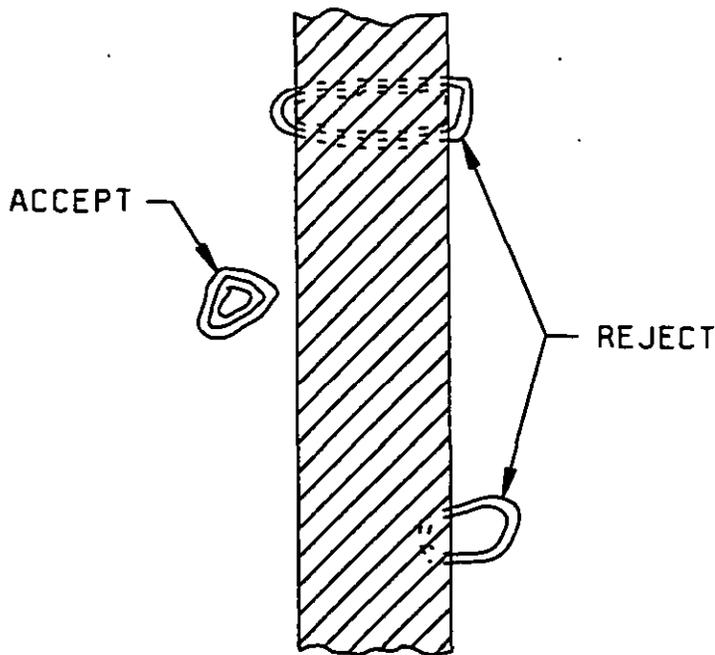


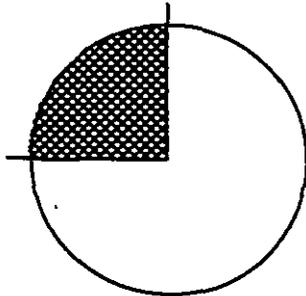
FIGURE 2032-8Ah. Class H passivation defect criteria.

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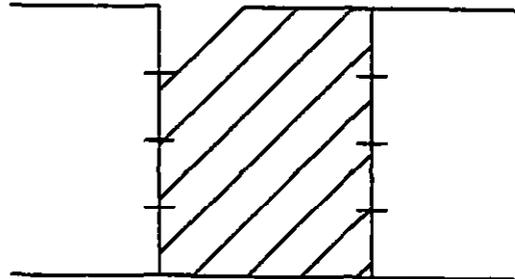
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- 3.2.1.9 Substrate via defects, "low magnification". When inspected from each side of the substrate, no element shall be acceptable that exhibits:
 - a. A complete void through the via.
 - b. Any lifting, peeling, or blistering of the via metallization.
 - c. Via fill less than 75% of the total surface area of the via plug and less than 75% of the substrate thickness.
- NOTE: These are minimum requirements. Via flatness and other requirements shall be in accordance with the applicable detail drawings.



VIA FILL < 75%
REJECT



VIA FILL < 75%
REJECT

FIGURE 2032-43Bh. Classes H and K via fill criteria.

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TABLE I. Group A electrical tests for classes level S and level B devices - Continued. 1/

- 1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.
- 2/ At the manufacturer's option, the applicable tests required for group A testing (see 1/) may be conducted individually or combined into sets of tests, subgroups (as defined in table I), or sets of subgroups. However, the manufacturer shall predesignate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.
- 3/ The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as predesignated in 2/, shall be 116/0.
- 4/ A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.
- 5/ If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For class level S only, if this testing results in a percent defective greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.

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TABLE IIa. Group B tests for class level S devices. 1/

Test	MIL-STD-883		Quantity (accept no.) Sample size no. accept no.
	Method	Condition	
Subgroup 1			
a. Physical dimensions <u>2/</u> b. Internal water-vapor content <u>2/ 3/</u>	2016 1018	5,000 ppm maximum water content at 100°C	2(0) 3(0) or 5(1) <u>4/</u>
Subgroup 2 <u>5/</u>			
a. Resistance to solvents b. Internal visual and mechanical c. Bond strength (1) Thermocompression (2) Ultrasonic (3) Flip-chip (4) Beam lead d. Die shear or substrate attach strength test	2015 2013, 2014 2011	Failure criteria from design and construction requirements of applicable acquisition document 1. Test condition C or D 2. Test condition C or D 3. Test condition F 4. Test condition H In accordance with method 2019 or 2027 for the applicable die size	3(0) 2(0) Sample size <u>6/</u> number = 22, c = 0 3(0)
Subgroup 3			
Solderability <u>7/</u>	2003	Soldering temperature of 245°C ±5°C	Sample size number = 22, c = 0
Subgroup 4 <u>2/</u>			
a. Lead integrity <u>8/</u> b. Seal (a) Fine (b) Gross c. Lid torque <u>9/</u>	2004 1014 2024	Test condition B2, lead fatigue As applicable As applicable	Sample size number = 45, c = 0
Subgroup 5 <u>10/</u>			
a. End-point electrical parameters <u>11/</u> b. Steady state life c. End-point electrical parameter <u>11/</u>	1005	As specified in the applicable device specification Test condition C, D, or E As specified in the applicable device specification	Sample size number = 45, c = 0

See footnotes at end of table.

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TABLE IIa. Group B tests for class level S devices - Continued. 1/

Test	MIL-STD-883		Quantity (accept no.) Sample size no. Accept number
	Method	Condition	
<u>Subgroup 6</u>			Sample size Number = 15, c = 0
a. End-point electrical parameters		As specified in the applicable device specification	
b. Temperature cycling	1010	Condition C, 100 cycles minimum	
c. Constant acceleration	2001	Test condition E: Y ₁ orientation only	
d. Seal (a) Fine (b) Gross	1014	As specified in the applicable device specification	
e. End-point electrical parameters			
<u>Subgroup 7</u> 12/			

- 1/ Electrical reject devices from that same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electrical and provided the rejects are exposed to the full temperature/ time exposure of burn-in.
- 2/ Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot.
- 3/ This test is required only if it is a glass-frit-sealed package. Unless handling precautions for beryllia packages are available and followed method 1018, procedure 3 shall be used. See 6/ of table IV.
- 4/ Test three devices; if one fails, test two additional devices with no failures. At the manufacturers option, if the initial test sample (i.e., 3 or 5 devices) fails, a second complete sample may be tested at an alternate laboratory that has been granted current suitability status by the qualifying activity. If this sample passes, the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with five additional devices from the same lot.
- 5/ Resistance to solvents testing required only on devices using inks or paints as a marking medium.
- 6/ Unless otherwise specified, the sample size number for conditions C and D is the number of bond pulls selected from a minimum number of four devices, and for condition F or H is the number of dice (not bonds).

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- 7/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin-lead fusing after burn-in. The sample size number applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.
- 8/ The sample size number of 45 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test and lid torque test, if applicable, (see 9/) in order to meet the requirements of subgroup 4. For pin grid array leads and rigid leads, use method 2028. For leaded chip carrier packages, use condition B1. For leadless chip carrier packages only, use test condition D and a sample size number of 15 based on the number of pads tested taken from 3 devices minimum. Seal test (subgroup 4b) need be performed only on packages having leads exiting through a glass seal.
- 9/ Lid torque test shall apply only to glass-frit-sealed packages.
- 10/ The alternate removal-of-bias provisions of 3.3.1 of method 1005 shall not apply for test temperature above 125°C.
- 11/ Read and record group A subgroups 1, 2, and 3.
- * 12/ Subgroup 7 has been deleted from table Iia. The requirements for ESD testing are specified in appendix A of MIL-PRF-38535.

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TABLE V. Group E (radiation hardness assurance tests). 1/

Test	MIL-STD-883		Class level S		Class level B	
	Method	Condition	Quantity/ accept number	Notes	Quantity/ accept number	Notes
<u>Subgroup 1</u> <u>2/</u> Neutron irradiation a. Qualification b. QCI Endpoint electrical parameters	1017	25°C	(a) 2(0) devices/wafer 11(0) devices/wafer lot	<u>3/</u>	(a) 2(0) device/wafer 5(0) devices/wafer lot 11(0) devices/ inspection lot	<u>4/</u>
		As specified in accordance with device specification	(b) 2(0) devices/wafer 11(0) devices/wafer lot	<u>3/</u>	(b) 2(0) devices/wafer 5(0) devices/wafer lot 11(0) devices/ inspection lot	<u>4/</u>
<u>Subgroup 2</u> <u>5/</u> Steady-state total dose irradiation a. Qualification b. QCI Endpoint electrical parameters	1019	25°C Maximum supply voltage	(a) 4(0) devices/wafer 2(0) devices/wafer 22(0) devices/wafer lot	(a) <u>6/</u> <u>8/</u>	(a) 2(0) devices/wafer 5(0) devices/wafer lot 22(0) devices/ inspection lot	<u>7/</u>
		As specified in accordance with device specification	(b) 4(0) devices/wafer 2(0) devices/wafer 22(0) devices/wafer lot	(b) <u>6/</u> <u>8/</u>	(b) 2(0) devices/wafer 5(0) devices/wafer lot 22(0) devices/ inspection lot	<u>7/</u>
<u>Subgroup 3</u> <u>2/ 9/</u> Transient ionizing irradiation Endpoint electrical parameters	1021 Digital 1023 Linear	25°C As specified in accordance with device specification	2(0) devices/wafer 11(0) devices/wafer lot	<u>3/</u>	2(0) devices/wafer 11(0) devices/ inspection lot	<u>4/</u>
<u>Subgroup 4</u> <u>2/</u> Radiation latch-up	1020	As specified in the device specification	As specified in the device specification		As specified in the device specification	
<u>Subgroup 5</u> <u>2/</u> Single event effects	ASTM F-1192	As specified in the device specification	4(0) devices/wafer			

1/ Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total exposure shall not be considered cumulative unless testing is performed within the time limits of the test method. Group E tests may be performed prior to device screening (see 3.5.3).

2/ This test is to be conducted only when specified in the purchase order or contract.

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TABLE V. Group E (radiation hardness assurance tests) - Continued. 1/

- 3/ In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
- 4/ In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
- 5/ Class level B devices shall be inspected using either the class level B quantity/accept number criteria as specified, or by using the class level S criteria on each wafer.
- 6/ In accordance with wafer for device types with less than or equal to 4,000 equivalent transistors/chip selected from the wafer. The manufacturer shall define and document sampling procedures.
- 7/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).

- 8/ In accordance with wafer for device types with greater than 4,000 equivalent transistors/chip selected from the wafer. The manufacturer shall define and document sampling procedures.

- 9/ Upset testing during qualification on first QCI shall be conducted when specified in purchase order or contract. When specified, the same microcircuits may be tested in more than one subgroup.

3.5.2 Alternate group B inspection for class level B. At the manufacturer's option, (class level B only), group B inspection shall be performed on any inspection lot of each qualified package type and lead finish from each different week of sealing. Different inspection lots may be used for each subgroup. After this alternate group B inspection is successfully completed, all other device types manufactured on the same assembly line using the same package type and lead finish sealed in the same week may be accepted without further group B testing. A manufacturer shall not accept inspection lots containing devices of a particular package type and lead finish until after the successful completion of group B testing for that package type and lead finish for each week of seal.

3.5.2.1 Nonconformance for the alternate group B inspection. When a failure has occurred in group B using the alternate group B procedure, samples from three additional inspection lots of the same package type, lead finish, and week of seal as the failed package shall be tested to the failed subgroup(s). If all three inspection lots pass, then all devices manufactured on the same assembly line using the same package type and lead finish and sealed in the same week may be accepted for group B inspection. If one or more of the three additional inspection lot fail, then no inspection lot containing devices manufactured on the same assembly line using the same package type and lead finish sealed in the same week shall be accepted for group B inspection until each inspection lot has been subjected to and passed the failed subgroup(s).

3.5.3 Group E samples. At the manufacturer's option (but subject to the criteria defined by 3.5.3.1, 3.5.3.2, and 3.5.3.3), group E samples need not be subjected to all the screening tests of method 5004, but shall be assembled in a group D qualified package and, as a minimum, pass group A, subgroups 1 and 7, electrical tests at 25°C prior to irradiation.

3.5.3.1 Group E tests shall be performed on samples that have been exposed to burn-in or

3.5.3.2 as an alternative, the requirement of 3.5.3.1 can be waived if previous testing has shown that burn-in produces negligible changes in the device total dose response or

3.5.3.3 as an alternative, the Group E tests can be performed on samples which have not received burn-in if the results of the Group E tests are corrected for the changes in total dose response which would have been caused by burn-in. This correction shall be carried out in a manner acceptable to the parties to the test.

3.6 Disposition of samples. Disposition of sample devices used in groups A, B, C, D, and E testing shall be in accordance with the applicable device specification.

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3.7 Substitution of test methods and sequence.

3.7.1 Accelerated qualification or quality conformance testing for class level B. When the accelerated temperature/time test conditions of condition F of method 1005 are used for any operating life or steady state reverse bias subgroups on a given sample for purposes of qualification or quality conformance inspection, the accelerated temperature/time test conditions shall be used for all of those named subgroups. When these accelerated test conditions are used for burn-in screening test (test condition F of method 1015) or stabilization bake (any test temperature above the specified maximum rated junction temperature for devices with aluminum/ gold metallurgical systems) for any inspection lot, it shall be mandatory that they also be used for the operating life, and steady-state reverse bias tests of method 5005, as applicable, or qualification or quality conformance inspection. Qualification and quality conformance inspection may be performed using accelerated conditions on inspection lots that have been screened using normal test conditions.

3.8 Data reporting. When required by the applicable acquisition document, the following data shall be made available for each lot submitted for qualification or quality conformance inspection:

- a. Results of each subgroup test conducted, initial, and any resubmission.
- b. Number of devices rejected.
- c. Failure mode of each rejected device and, for class S, the associated mechanism for catastrophic failures of each rejected device.
- d. Number of additional samples added, when applicable.
- e. Resubmitted lots, identification and history.
- f. Read and record variables data on all specified electrical parameter measurements in group B.

4. SUMMARY. The following details shall be specified in the applicable device specification:

- a. Device class and procedure paragraph if other than 3.
- b. Sequence of test, sample size, test method, and test condition where not specified, or if other than specified.
- c. Test condition, cycles, temperatures, axis, etc., where not specified, or if other than specified (see 3).
- d. Acceptance procedure (see 3.3) and quantity (accept number) or sample size number and acceptance number, if other than specified (see 3).
- e. Electrical parameters for group A.
- f. Electrical parameters for groups B, C, D, and E end point measurements, where applicable.
- g. Requirements for failure analysis (see 3.8).
- h. Requirements for data recording and reporting if other than specified in 3.8.
- i. Restriction on resubmission of failed lots (see 3.4), where applicable.
- j. Steady-state life test circuits, where not specified or if other than specified (see subgroup 1 of table III and subgroup 5 of table IIa).
- k. Parameters on which delta measurements are required.

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3.8.5.1 Thermal stability. The thermal stability of the polymeric material shall be determined by heating the specimens from room temperature to not less than 210°C, at a heating rate between 10°C/minute and 20°C/minute, in a nitrogen atmosphere with 20-30 milliliter/minute nitrogen flow. The weight loss at 200°C shall be determined.

3.8.5.2 Filler content. The filler content of polymeric materials using a filler to promote properties such as electrical or thermal conductivity shall be determined by heating the specimen from room temperature to 600°C, at a heating rate between 10°C/minute and 20°C/minute, in an air atmosphere with 20-30 milliliter/minute air flow. The temperature shall be maintained at 600°C until constant weight is obtained. It is permitted to perform 3.8.5.1, followed by heating from 210°C to 600°C as detailed above. The filler content shall be reported as weight percent of the cured specimen.

3.8.6 Outgassed materials. Ten test specimens shall be prepared using gold- or nickel-plated Kovar or ceramic packages, (dielectric materials may be prepared using aluminum coated silicon as the substrate). (The use of "leadless" packages is permitted to reduce moisture contributions due to package construction). The material shall be cured using the minimum cure schedule and shall receive the minimum pre-seal bake specified in the assembly document(s) (see 3.5.1). After a pre-seal bake, the packages shall be hermetically sealed. Only those packages that meet the fine and gross leak test requirements of test method 1014 shall be submitted for moisture content analysis. If less than 10 test specimens remain after hermetically testing, the failed packages shall be replaced by additional hermetical packages processed and tested in the same manner as the original group.

3.8.6.1 Testing for short term outgassing of moisture and other gaseous species. Five packages containing polymer prepared in accordance with 3.8.6 shall be heated in accordance with MIL-STD-883, method 1008, 24 hours at 150°C. The packages shall then be immediately (less than or equal to 5 minutes) inserted into the ambient gas analysis apparatus. The packages shall be subjected to ambient gas analysis in accordance with MIL-STD-883, method 1018, procedure 1. In addition to moisture, other gaseous species present in quantities greater than or equal to 100 ppmv (0.01 percent V/V) shall be reported in ppmv or percent V/V.

All polymeric materials tested shall have quantities of material equivalent in mass and exposed surface area to that of the intended application. Gold plated Kovar tabs and alumina blanks may be used as facsimile device elements. Several polymeric materials of different application may be tested in combination with each other in this test, however their combined moisture content shall not exceed 5,000 ppmv.

3.8.6.2 Testing for long term outgassing of moisture and other gaseous species. Provided that the moisture requirement of 3.5.3 has been met by packages tested in 3.8.6.1, the remaining five devices containing polymer from the group prepared in accordance with 3.8.6 shall be heated in accordance with MIL-STD-883, method 1008 for 1,000 hours at 150°C. The packages shall then be immediately (less than or equal to 5 minutes) inserted into the ambient gas analysis apparatus. The packages shall be subjected to ambient gas analysis in accordance with MIL-STD-883, method 1018, procedure 1. In addition to moisture, other gaseous species present in quantities greater than or equal to 100 ppmv (0.01 percent V/V) shall be reported in ppmv or percent V/V.

3.8.7 Ionic impurities. A water-extract analysis shall be performed to determine the level of ionic contamination in the cured polymeric material. The total ion content (specific electrical conductance) and the specific ionic content for the hydrogen (pH), chloride, sodium, fluoride and potassium ions shall be measured. Other ions present in quantities > 5 ppm shall also be reported in ppm. The methods of analysis submitted in the following paragraphs are suggested techniques. Alternate methods of analysis may be selected where it can be shown that the techniques are equivalent and the method of analysis is approved by the qualifying activity.

3.8.7.1 Sample preparation. Adequate material shall be cured to obtain 3 gram samples of polymer following grinding, for final preparation. The material shall be cured on teflon or other inert surface in a forced draft oven. When possible the cured specimen shall be removed from the curing substrate and ground to 60-100 mesh particles; polymeric film samples less than or equal to 0.025 cm thick shall be cured and cut into less than or equal to 0.25 cm² samples; gels or low modulus materials may be cast directly into the flat bottom of the sample flask for the extraction. Smaller sample sizes may be selected where it can be shown that the accuracy of the test method has not changed.

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3.8.7.2 Extraction procedure. 3 grams (equivalent resin) of the ground or cut equivalent polymer shall be added to a cleaned; tared, 250-ml flasks made of pyrex, or equivalent. The weight of the cured material in each flask shall be recorded to the nearest milligram. 150.0 grams of deionized water with a measured specific conductance less than or equal to 0.1 millisiemens/meter (specific resistivity greater than or equal to 1.0 megohm-centimeter) shall be added to the flask. A blank shall be prepared by adding 150.0 grams of the deionized water and a boiling chip to a second 250-ml flask. The flasks shall be refluxed for 20 hours.

NOTE: 1.0 mho = 1.0 siemens; 1.0 mho/cm = 100.0 siemens/meter.

3.8.7.3 Measurement of ionic content

3.8.7.3.1 Total ionic content. The total extractable ionic content shall be determined by measuring the specific electrical conductance of the water-extract samples and the blank using a conductivity meter with an immersion conductivity cell having a cell constant of 0.01/centimeter (alternatively 0.1 cm⁻¹ to adjust for proper analysis of the solution). The total ionic content, in millisiemens/meter, shall be obtained by subtracting the specific conductance of the blank from the specific conductance of the samples.

3.8.7.3.2 Hydrogen ion content (pH). The pH of the water extract shall be determined using a pH meter with a standard combination electrode.

3.8.7.3.3 Specific ion analysis. Specific ion analysis of the water extract shall be conducted using ion chromatography or a demonstrated equivalent. The ion concentrations in the extract shall be converted to the sample extractable concentrations by multiplying the ratio of the deionized water weight (W) to polymer sample weight (S); that is, by (W/S). The chloride, sodium, fluoride and potassium ion levels and all other ions detected in quantities > 5 ppm shall be reported in ppm.

3.8.8 Bond strength. The bond strength of the polymeric material shall be determined in accordance with 3.8.8.1, 3.8.8.2 or 3.8.8.3 below. As a minimum, five elements shall be tested to failure at the following conditions:

- a. At 25°C.
- b. At 25°C after 1,000 hours at 150°C in an air or nitrogen ambient.

The average bond strength at each test condition shall be determined in kilograms (force).

3.8.8.1 Bond strength. The bond strength shall be determined in accordance with method 2019 of MIL-STD-883. A gold-metallized substrate or a gold- or nickel-plated package shall be used as the bonding surface for bond strength testing.

3.8.8.1.1 Type I materials. Suppliers shall use 0.08 inch-square (0.2 centimeter-square) gold-plated Kovar tabs.

3.8.8.1.2 Type II materials. Suppliers shall use 0.08 inch-square (0.2 centimeter-square) alumina chips.

3.8.8.2 Bond strength. The bond strength may be determined in accordance with ASTM D1002 as an alternative to test method 2019. If ASTM D1002 is used, the results must be correlated to assure that the bond strength of the adhesive is shown to be equivalent to the Method 2019 failure criteria.

3.8.8.3 Molding compounds or encapsulants. Molding compounds or encapsulants shall be tested in accordance with MIL-STD-883, test method 1034.

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STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

1. The preparing activity must complete blocks 1, 2, 3, and 8. In block 1, both the document number and revision letter should be given.
2. The submitter of this form must complete blocks 4, 5, 6, and 7.
3. The preparing activity must provide a reply within 30 days from receipt of the form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

RECOMMEND A CHANGE	1. DOCUMENT NUMBER MIL-STD-883E Notice 1	2. DOCUMENT DATE (YYMMDD) 97/12/01
3. DOCUMENT TITLE Test Method Standard Microcircuits		
4. NATURE OF CHANGE <i>(Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)</i>		
5. REASON FOR RECOMMENDATION		
6. SUBMITTER		
a. NAME (Last, First, Middle Initial)	b. ORGANIZATION	
c. ADDRESS (include Zip Code)	d. TELEPHONE (include Area Code)	e. DATE SUBMITTED (YYMMDD)
	(1) Commercial	
	(2) AUTOVON	
	<i>(if applicable)</i>	
8. PREPARING ACTIVITY		
a. NAME Mr. Jeff Bowling	b. TELEPHONE (Include Area Code)	
	(1) Commercial (614) 692-0532	(2) AUTOVON 850-0532
c. ADDRESS (include Zip Code) Defense Supply Center Columbus (DSCC-VAS) P.O. Box 3990 Columbus, OH 43216-5000	IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: Defense Quality and Standardization Office 5203 Leesburg Pike, Suite 1403, Falls Church, VA 22041-3466 Telephone (703) 756-2340 AUTOVON 289-2340	