

The documentation and process conversion measures necessary to comply with this document shall be completed by 26 October 2006.

INCH-POUND

MIL-PRF-19500/366L
 26 July 2006
 SUPERSEDING
 MIL-PRF-19500/366K
 24 July 2004

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, AMPLIFIER,
 TYPES 2N3498, 2N3498L, 2N3498U4, 2N3499, 2N3499L, 2N3499U4, 2N3500, 2N3500L, 2N3500U4, 2N3501,
 2N3501L, 2N3501UB, AND 2N3501U4, JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

Device types 2N3498, 2N3499, 2N3500 and their corresponding L suffix versions are inactive for new design after 14 April 1995.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, low-power amplifier and switching transistors. Four levels of product assurance are provided for each device type as specified in MIL-PRF-19500. Two levels of product assurance are provided for die.

1.2 Physical dimensions. See figure 1 (similar to TO-5, TO-39), figure 2 (surface mount, 2N3501UB), figure 3 (U4), and figures 4 and 5 (die).

1.3 Maximum ratings unless otherwise specified $T_A = +25^\circ\text{C}$.

Types	P_T $T_A = +25^\circ\text{C}$ (1)	P_T $T_C = +25^\circ\text{C}$ (1)	P_T $T_{SP} = +25^\circ\text{C}$ (1)	$R_{\theta JA}$	$R_{\theta JC}$	$R_{\theta JSP}$	V_{CBO}	V_{CEO}	V_{EBO}	I_C	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>$^\circ\text{C/W}$</u>	<u>$^\circ\text{C/W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>mA dc</u>	<u>$^\circ\text{C}$</u>
2N3498, L,	1	5	N/A	175	30	N/A	100	100	6	500	-65 to +200
2N3498U4	1	4	N/A	175	15	N/A	100	100	6	500	
2N3499, L,	1	5	N/A	175	30	N/A	100	100	6	500	
2N3499U4	1	4	N/A	175	15	N/A	100	100	6	500	
2N3500, L,	1	5	N/A	175	30	N/A	150	150	6	300	
2N3500U4	1	4	N/A	175	15	N/A	150	150	6	300	
2N3501, L,	1	5	N/A	175	30	N/A	150	150	6	300	
2N3501U4	1	4	N/A	175	15	N/A	150	150	6	300	
2N3501UB	.5	N/A	1.5	325	N/A	90	150	150	6	300	

(1) See derating curve figures 6, 7, 8, 9, and 10.

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dsc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil>.

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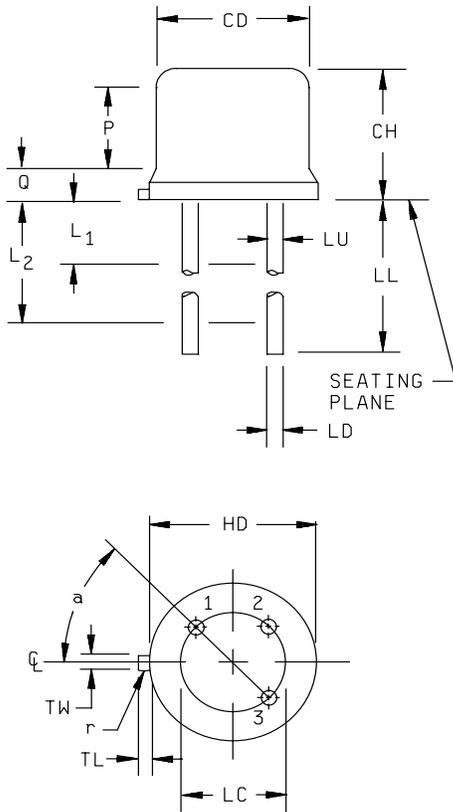
* 1.4 Primary electrical characteristics at $T_A = +25^\circ\text{C}$.

Type	h_{FE} at $V_{CE} = 10\text{ V dc}$				$ h_{fe} $ $V_{CE} = 20\text{ V dc}$ $I_C = 20\text{ mA dc}$ $f = 100\text{ MHz}$	C_{obo} $V_{CB} = 10\text{ V dc}$ $I_E = 0$ $100\text{ kHz} \leq f \leq 1\text{ MHz}$
	h_{FE1} (1) $I_C = 0.1\text{ mA dc}$	h_{FE4} (1) $I_C = 150\text{ mA dc}$	h_{FE5} (1) $I_C = 300\text{ mA dc}$	h_{FE6} (1) $I_C = 500\text{ mA dc}$		
	<u>Min</u> <u>Max</u>	<u>Min</u> <u>Max</u>				
2N3498, L, 2N3498U4	20	40 120	15	15	1.5 8	10
2N3499, L, 2N3499U4	35	100 300	15	20	1.5 8	10
2N3500, L, 2N3500U4	20	40 120	15	15	1.5 8	8
2N3501, L, 2N3501U4	35	100 300	20	15	1.5 8	8

(1) Pulsed (see 4.5.1).

Types (1)	$V_{CE(sat)}$ (1)		$V_{BE(sat)}$ (1)		t_{on}	t_{off}
	$I_C = 10\text{ mA dc}$ $I_B = 1\text{ mA dc}$	$I_C = 300\text{ mA dc}$ $I_B = 30\text{ mA dc}$	$I_C = 10\text{ mA dc}$ $I_B = 1\text{ mA dc}$	$I_C = 300\text{ mA dc}$ $I_B = 30\text{ mA dc}$	$I_C = 150\text{ mA dc}$ $I_{B1} = 15\text{ mA dc}$ $V_{EB} = 5\text{ V dc}$	$I_C = 150\text{ mA dc}$ $I_{B1} = -I_{B2} = 15\text{ mA dc}$
	<u>Min</u> <u>Max</u>	<u>Min</u> <u>Max</u>	<u>Min</u> <u>Max</u>	<u>Min</u> <u>Max</u>	<u>Max</u> Ns	<u>Max</u> ns
2N3498	0.2	0.6		1.4	115	1,150
2N3498U4	0.2	0.6		1.4	115	1,150
2N3499	0.2	0.6		1.4	115	1,150
2N3499U4	0.2	0.6		1.4	115	1,150
2N3500	0.2		.8		115	1,150
2N3500U4	0.2		.8		115	1,150
2N3501	0.2		.8		115	1,150
2N3501U4	0.2		.8		115	1,150

(1) Pulsed (see 4.5.1).



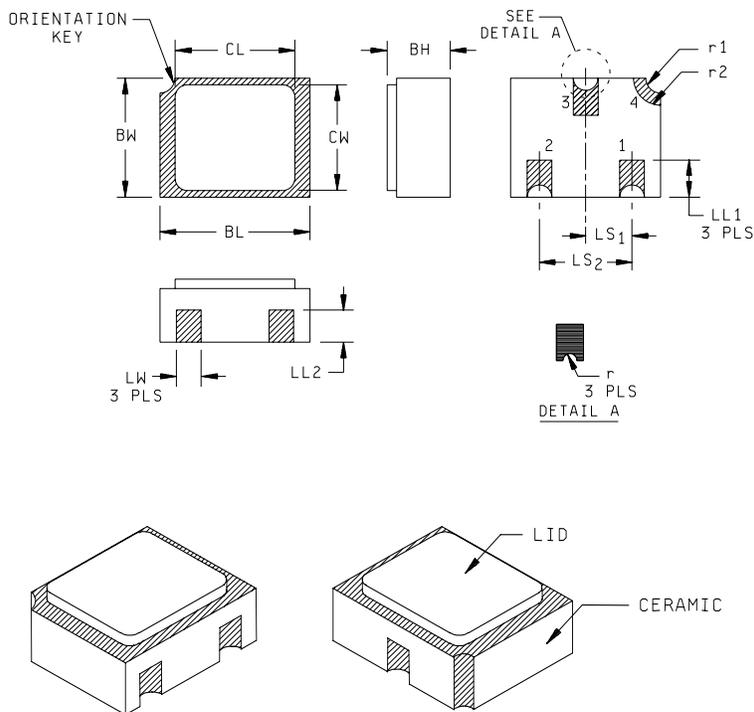
Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	7
LL	See notes 7, 12, and 13				
LU	.016	.019	0.41	0.48	7, 13
L ₁		.050		1.27	13
L ₂	.250		6.35		13
TL	.029	.045	0.74	1.14	3
TW	.028	.034	0.71	0.86	10, 11
P	.100		2.54		5
Q		.050		1.27	4
r		.010		.25	11
α	45° TP		45° TP		6

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Symbol CD shall not vary more than .010 (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) relative to tab. Device may be measured by direct methods or by gauge.
7. Symbol LD applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum. Lead diameter shall not exceed .042 inch (1.07 mm) within L₁ and beyond LL minimum.
8. Lead designation, shall be as follows: 1 - emitter, 2 - base, 3 - collector.
9. Lead number three is electrically connected to case.
10. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
11. Symbol r applied to both inside corners of tab.
12. For transistor types 2N3498, 2N3499, 2N3500, and 2N3501, LL = .50 inch (12.7 mm) minimum and .750 inch (19.1 mm) maximum. For transistor types 2N3498L, 2N3499L, 2N3500L, and 2N3501L, LL = 1.50 inch (38.1 mm) minimum and 1.750 inch (44.5 mm) maximum.
13. All three leads.
14. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

FIGURE 1. Physical dimensions (similar to TO-5, TO-39).

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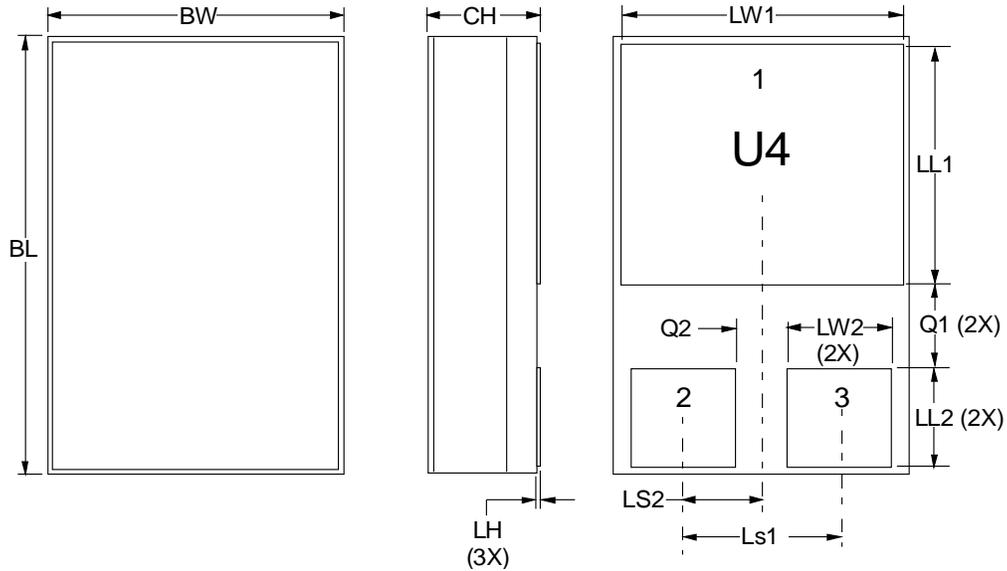


Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.96	
LL2	.017	.035	0.43	0.89	
LS1	.036	.040	0.91	1.02	
LS2	.071	.079	1.81	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r1		.012		.305	
r2		.022		.559	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

FIGURE 2. Physical dimensions, surface mount (2N3501UB version).



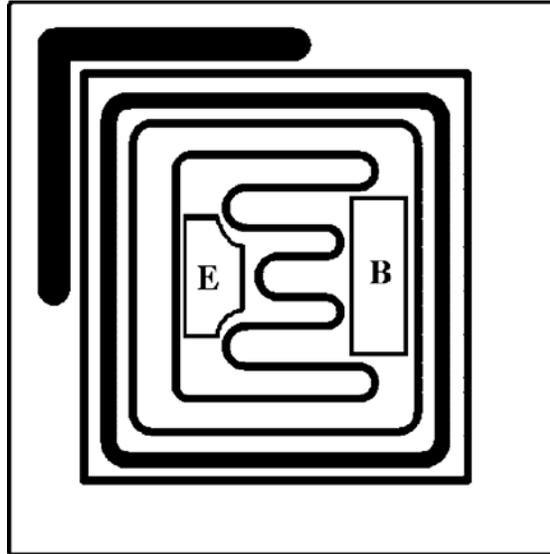
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.215	.225	5.46	5.72
BW	.145	.155	3.68	3.94
CH	.049	.075	1.24	1.91
LH		.005		0.13
LW1	.135	.145	3.43	3.68
LW2	.047	.057	1.19	1.45
LL1	.115	.125	2.91	3.17
LL2	.045	.055	1.14	1.40
LS1	.070	.095	1.78	2.41
LS2	.038	.048	0.97	1.21
Q1	.045	.070	1.14	1.78
Q2	.025	.035	0.64	0.88
1	Collector			
2	Base			
3	Emitter			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Terminal 1 is collector.
4. Terminal 2 is base.
5. Terminal 3 is emitter.
6. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

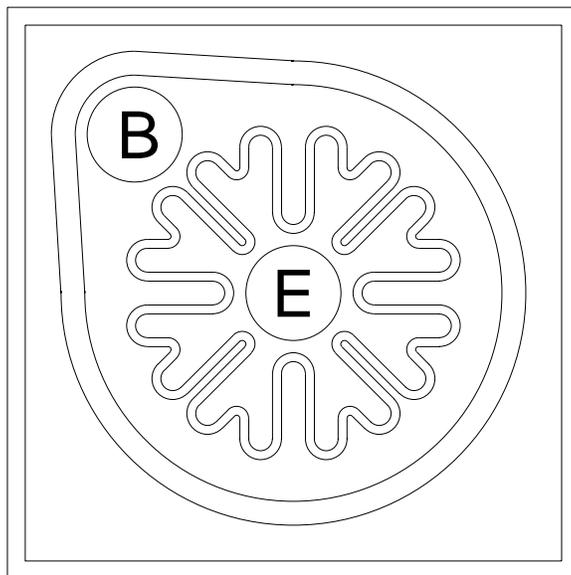
FIGURE 3. Physical dimensions and configuration U4.

A - Version



1. Chip size040 x .040 inch \pm .001 inch (1.02 x 1.02 mm \pm 0.025mm).
2. Chip thickness010 \pm .0015 inch (0.25 \pm 0.038mm).
3. Top metal Aluminum 15,000 \AA minimum, 18,000 \AA nominal.
4. Back metal Al/Ti/Ni/Ag 12k \AA /3k \AA /7k \AA /7k \AA min., 15k \AA /5k \AA /10k \AA /10k \AA nom.
Gold 2,500 \AA minimum, 3,000 \AA nominal.
Eutectic Mount - No Gold.
5. Backside Collector.
6. Bonding pad..... B = .006 x .008 inch (0.15 x 0.20 mm).
E = .006 x .004 inch (0.15 x 0.10 mm).

FIGURE 4. Physical dimensions, JANHCA and JANKCA die.



B - Version

1. Die size	.030 (0.76 mm) x .030 inch (0.76 mm).
2. Die thickness	.008 (.20 mm) ± .0016 inch (0.04 mm).
3. Base pad	.005 inch (0.13 mm) diameter.
4. Emitter pad	.005 inch (0.13 mm) diameter.
5. Back metal	Gold, 6,500 ± 1,950 Å.
6. Top metal	Aluminum, 22,500 ± 2,500 Å.
7. Back side	Collector.
8. Glassivation	SiO ₂ , 7,500 ± 1,500 Å.

FIGURE 5. Physical dimensions, JANHCB and JANKCB die.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

* 3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

PCB	Printed circuit board
$R_{\theta JA}$	Thermal resistance junction to ambient.
$R_{\theta JC}$	Thermal resistance junction to case.
$R_{\theta JSP}$	Thermal resistance junction to solder pads.
TRB	Technical review board.
T_{SP}	Temperature of solder pads.
UB	Surface mount case outlines (see figure 2).

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (similar to TO-5, TO-39), figure 2 (surface mount, 2N3501UB), figure 3 (U4), and figures 4 and 5 (die).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

* 4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANS, JANTXV, and JANTX levels only). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
3c	Thermal impedance method 3131 of MIL-STD-750, see figures 11, 12, 13, and 14, and 4.3.3.	Thermal impedance method 3131 of MIL-STD-750, see figures 11, 12, 13, and 14, and 4.3.3.
7	Optional	Optional
9	I_{CBO2} and h_{FE4}	Not applicable
11	I_{CBO2} and h_{FE4} ; ΔI_{CBO2} 100 percent of initial value or 5 nA dc, whichever is greater; $\Delta h_{FE4} = \pm 15$ percent of initial value.	I_{CBO2} and h_{FE4}
12	See 4.3.2	See 4.3.2
13	Subgroups 2 and 3 of table I herein; $\Delta I_{CBO2} = 100$ percent of initial value or 5 nA dc, whichever is greater; $\Delta h_{FE4} = \pm 15$ percent of initial value.	Subgroups 2 of table I herein; $\Delta I_{CBO2} = 100$ percent of initial value or 5 nA dc, whichever is greater; $\Delta h_{FE4} = \pm 15$ percent of initial value.
14	Required	Required

4.3.1 Screening (JANHNC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500, "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

* 4.3.2 Power burn-in conditions. Power burn-in conditions are as follows: $V_{CB} = 10 - 30$ V dc; power shall be applied to achieve $T_J = +135^\circ\text{C}$ minimum using a minimum power dissipation = 75 percent of maximum rated P_T (see 1.3). NOTE: No heat sink or forced air-cooling on the devices shall be permitted. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J , and mounting conditions) may be used. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval. Use method 3100 of MIL-STD-750 to measure T_J .

* 4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{MD} (and V_C where appropriate). The thermal impedance limit shall comply with the thermal impedance graph in figures 11, 12, 13, and 14 (less than or equal to the curve value at the same t_H time) and shall be less than the process determined statistical maximum limit as outlined in method 3131 of MIL-STD-750. See group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of subgroups 1 and 2 of table I herein, inspection only (table E-VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIa (JANS) of MIL-PRF-19500 and 4.4.2.1. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.2 herein: delta requirements only apply to subgroups B4, and B5. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with table I, subgroup 2 and 4.5.2 herein.

4.4.2.1 Group B inspection (JANS), table E-VIa of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
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B4	1037	$V_{CB} = 10 \text{ V dc}$.
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B5	1027	$V_{CB} = 10 \text{ V dc}$; $P_D \geq 100$ percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.)
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Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table VIa, adjust T_A or P_D to achieve $T_J = +275^\circ\text{C}$ minimum.

Option 2: 216 hours minimum, sample size = 45, $c = 0$; adjust T_A or P_D to achieve a $T_J = +225^\circ\text{C}$ minimum.

4.4.2.2 Group B inspection, (JAN, JANJ, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
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1	1026	Steady-state life: 1,000 hours minimum, $V_{CB} = 10 \text{ V dc}$, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75$ percent of maximum rated P_T as defined in 1.3. $n = 45$ devices, $c = 0$. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
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2	1048	Blocking life, $T_A = +150^\circ\text{C}$, $V_{CB} = 80$ percent of rated voltage, 48 hours minimum. $n = 45$ devices, $c = 0$.
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3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$. $n = 22$, $c = 0$.
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4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- a. For JAN, JANJ, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.
- b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANJ, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2. Delta measurements shall be in accordance with 4.5.2 herein.

* 4.4.3.1 Group C inspection (JANS), table E-VII of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E; (not applicable for UA, UB and U4 devices).
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and applied thermal impedance curves. See 4.3.3.
C6	1026	1,000 hours at $V_{CB} = 10$ V dc; power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum and a minimum of $P_D = 75$ percent of maximum rated P_T as defined in 1.3 $n = 45$, $c = 0$. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

* 4.4.3.2 Group C inspection (JAN, JANJ, JANTX, and JANTXV), table E-VII of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E; not applicable for UA, UB, and U4 devices.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3 herein) $n = 22$, $c = 0$.
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein; delta measurements shall be in accordance with the applicable steps of 4.5.2.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

* 4.5.2 Delta requirements. Delta requirements shall be as specified below: 1/ 2/ 3/

Step	Inspection <u>4/</u>	MIL-STD-750		Symbol	Limit		Unit
		Method	Conditions		Min	Max	
1.	Collector to base cutoff current 2N3498, 2N3499 2N3500, 2N3501	3036	Bias condition D; $V_{CB} = 50$ V dc $V_{CB} = 75$ V dc	ΔI_{CBO2} <u>5/</u>	± 100 percent of initial value or 10 nA dc, whichever is greater.		
2.	Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 10$ mA dc; pulsed (see 4.5.1)	Δh_{FE3} <u>5/</u> <u>6/</u>	± 25 percent change from initial reading		
3.	Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 150$ mA dc; pulsed (see 4.5.1)	Δh_{FE4} <u>5/</u>	± 25 percent change from initial reading		
4.	Collector to emitter voltage (saturated)	3071	$I_C = 10$ mA dc; $I_B = 1.0$ mA dc; pulsed (see 4.5.1)	$\Delta V_{CE(sat)}$ ¹ <u>5/ 6/ 7/</u>	± 50 mV dc change from previous measured value		

1/ The delta measurements for table E-VIa (JANS) of MIL-PRF-19500 are as follows:

- a. Subgroup 4, see 4.5.2 herein, steps 3 and 4.
- b. Subgroup 5, see 4.5.2 herein, steps 1 and 2.

2/ The delta measurements for group B, (see 4.4.2.2 herein, JAN, JANTX, and JANTXV) are as follows: After each step in 4.4.2.2, see 4.5.2 herein, steps 1 and 3.

3/ The delta measurements for table E-VII of MIL-PRF-19500 are as follows: Subgroup 6, see 4.5.2 herein, step 1 (for JANS only).

4/ Electrical characteristics for "L", "U4", and "UB" suffix devices are identical to their corresponding "non-L", "non-U4" and "non-UB" suffix devices unless otherwise noted.

5/ Devices which exceed the table I limits shall not be returned to the lot, but will not be considered failures.

6/ JANS only.

7/ Maximum limit for this test characterized at $\leq .125$ inch (3.18 mm) from the case.

TABLE I. Group A inspection.

Inspection <u>1/ 2/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 3/</u>						
Visual and mechanical examination <u>4/</u>	2071	n = 45 devices, c = 0				
Solderability <u>4/ 5/</u>	2026	n = 15 leads, c = 0				
Resistance to solvents <u>4/ 5/ 6/</u>	1022	n = 15 devices, c = 0				
Temp cycling <u>4/ 5/</u>	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal <u>5/</u> Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements <u>5/</u>		Table I, subgroup 2				
Bond strength <u>4/ 5/</u>	2037	Precondition T _A = +250°C at t = 24 hours or T _A = +300°C at t = 2 hours n = 11 wires, c = 0				
Decap internal visual (design verification) <u>4/</u>	2075	n = 4 devices, c = 0				
<u>Subgroup 2</u>						
Thermal impedance	3131	See 4.3.3	Z _{θJX}			°C/W
Collector to base cutoff current 2N3498, 2N3499 2N3500, 2N3501, 2N3501UB	3036	Condition D, V _{CB} = 100 V dc V _{CB} = 150 V dc	I _{CB01}		10 10	μA dc μA dc
Collector to emitter cutoff current 2N3498, 2N3499 2N3500, 2N3501, 2N3501UB	3041	Condition D; pulsed (see 4.5.1) V _{CE} = 80 V dc V _{CE} = 120 V dc	I _{CE0}		1 1	μA dc μA dc
Breakdown voltage, collector to emitter 2N3498, 2N3499 2N3500, 2N3501, 2N3501UB	3011	Bias condition D; I _C = 10 mA dc; pulsed (see 4.5.1)	V _{(BR)CEO}	100 150		V dc V dc
Emitter to base, cutoff current	3061	Bias condition D; V _{EB} = 6 V dc	I _{E01}		10	μA dc
Collector to base cutoff current 2N3498, 2N3499 2N3500, 2N3501, 2N3501UB	3036	Bias condition D; V _{CB} = 50 V dc V _{CB} = 75 V dc	I _{CB02}		50 50	nA dc nA dc
Emitter to base cutoff current	3061	Bias condition D; V _{EB} = 4 V dc	I _{E02}		25	nA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued						
Collector to emitter saturation voltage	3071	$I_C = 10 \text{ mA dc}; I_B = 1 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.2	V dc
Collector to emitter saturation voltage 2N3500, 2N3501, 2N3501UB only	3071	$I_C = 150 \text{ mA dc}; I_B = 15 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)2}$		0.4	V dc
Collector to emitter saturation voltage 2N3498, 2N3499 only	3071	$I_C = 300 \text{ mA dc}; I_B = 30 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)3}$		0.6	V dc
Base emitter saturation voltage	3066	Test condition A; $I_C = 10 \text{ mA dc};$ $I_B = 1 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)1}$		0.8	V dc
Base emitter saturation voltage (2N3500, 2N3501, 2N3501UB only)	3066	Test condition A; $I_C = 150 \text{ mA dc};$ $I_B = 15 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)2}$		1.2	V dc
Base emitter saturation voltage (2N3498, 2N3499 only)	3066	Test condition A; $I_C = 300 \text{ mA dc};$ $I_B = 30 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)3}$		1.4	V dc
Forward-current transfer ratio 2N3498, 2N3500 2N3499, 2N3501, 2N3501UB	3076	$V_{CE} = 10 \text{ V dc}; I_C = 0.1 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE1}	20 35		
Forward-current transfer ratio 2N3498, 2N3500 2N3499, 2N3501, 2N3501UB	3076	$V_{CE} = 10 \text{ V dc}; I_C = 1.0 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE2}	25 50		
Forward-current transfer ratio 2N3498, 2N3500 2N3499, 2N3501, 2N3501UB	3076	$V_{CE} = 10 \text{ V dc}; I_C = 10 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE3}	35 75		
Forward-current transfer ratio 2N3498, 2N3500 2N3499, 2N3501, 2N3501UB	3076	$V_{CE} = 10 \text{ V dc}; I_C = 150 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE4}	40 100	120 300	
Forward-current transfer ratio 2N3500 2N3501, 2N3501UB	3076	$V_{CE} = 10 \text{ V dc}; I_C = 300 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE5}	15 20		
Forward-current transfer ratio 2N3498 2N3499	3076	$V_{CE} = 10 \text{ V dc}; I_C = 500 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE6}	15 20		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> – Continued.						
Forward-current transfer ratio 2N3500 2N3501, 2N3501UB	3076	$V_{CE} = 10 \text{ V dc}; I_C = 300 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE5}	15 20		
Forward-current transfer ratio 2N3498 2N3499	3076	$V_{CE} = 10 \text{ V dc}; I_C = 500 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE6}	15 20		
<u>Subgroup 3</u>						
High temperature operation		$T_A = +150^\circ\text{C}$				
Collector to base cutoff current 2N3498, 2N3499 2N3500, 2N3501, 2N3501UB	3036	Bias condition D $V_{CB} = 50 \text{ V dc}$ $V_{CB} = 75 \text{ V dc}$	I_{CBO3}		50	$\mu\text{A dc}$
Low temperature operation		$T_A = -55^\circ\text{C}$				
Forward-current transfer ratio 2N3498, 2N3500 2N3499, 2N3501, 2N3501UB	3076	$V_{CE} = 10 \text{ V dc}; I_C = 150 \text{ mA dc}$	h_{FE7}	22 45		
<u>Subgroup 4</u>						
Magnitude of small-signal short-circuit forward current transfer ratio	3306	$V_{CE} = 20 \text{ V dc}; I_C = 20 \text{ mA dc};$ $f = 100 \text{ MHz}$	$ h_{fe} $	1.5	8	
Small-signal short-circuit forward current transfer ratio 2N3498, 2N3500 2N3499, 2N3501, 2N3501UB	3206	$V_{CE} = 10 \text{ V dc}; I_C = 10 \text{ mA dc};$ $f = 1 \text{ kHz}$	h_{fe}	35 75	300 375	
Open circuit output capacitance 2N3498, 2N3499 2N3500, 2N3501, 2N3501UB	3236	$V_{CB} = 10 \text{ V dc}; I_E = 0;$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{obo}		10 8	pF pF
Input capacitance (output open- circuited)	3240	$V_{EB} = 0.5 \text{ V dc}; I_C = 0;$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{ibo}		80	pF
Noise figure (Test 2)	3246	$V_{CE} = 10 \text{ V dc}; I_C = 0.5 \text{ mA dc};$ $R_g = 1 \text{ k}\Omega; f = 10 \text{ kHz}$	NF		6	dB
Turn-on time		$V_{EB} = 5 \text{ V dc}; I_C = 150 \text{ mA dc};$ $I_{B1} = 15 \text{ mA dc};$ (see figure 15)	t_{on}		115	ns
Turn-off time		$I_C = 150 \text{ mA dc}, I_{B1} = I_{B2} = 15$ $\text{mA dc};$ (see figure 15)	t_{off}		1150	ns

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/ 2/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u>						
Safe operating area (continuous dc)	3051	$T_C = 25^\circ\text{C}$; $t_r \geq 10$ ns; 1 cycle; (see figure 16); $t = 1$ s				
<u>Test 1</u>						
2N3498, 3N3499 2N3500, 3N3501 3N3501UB		$V_{CE} = 10$ V dc; $I_C = 500$ mA dc $V_{CE} = 16.67$ V dc; $I_C = 300$ mA dc $V_{CE} = 10$ V dc; $I_C = 113$ mA dc				
<u>Test 2</u>						
2N3498, 2N3499, 2N3500, 2N3501 2N3501UB		$V_{CE} = 50$ V dc; $I_C = 100$ mA dc $V_{CE} = 50$ V dc; $I_C = 23$ mA dc				
<u>Test 3</u>						
2N3498, 2N3499, 2N3500, 2N3501 2N3501UB		$V_{CE} = 80$ V dc; $I_C = 40$ mA dc $V_{CE} = 80$ V dc; $I_C = 14$ mA dc				
Safe operating area (clamped switching)	3053	$T_A = +25^\circ\text{C}$; (see figure 17); device fails if clamp voltage is not reached $I_B = 85$ mA dc; $I_C = 500$ mA dc $I_B = 50$ mA dc; $I_C = 300$ mA dc				
2N3498, 2N3499 2N3500, 2N3501, 2N3501UB						
Electrical measurements		See table I, subgroup 2 herein.				
<u>Subgroup 6</u>						
Not required						

1/ For sampling plan see MIL-PRF-19500, unless otherwise specified.

2/ Electrical characteristics for "L" and "U4" suffix devices are identical to the corresponding "non-L" and "non-U4" suffix devices.

3/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

4/ Separate samples may be used.

5/ Not required for JANS devices.

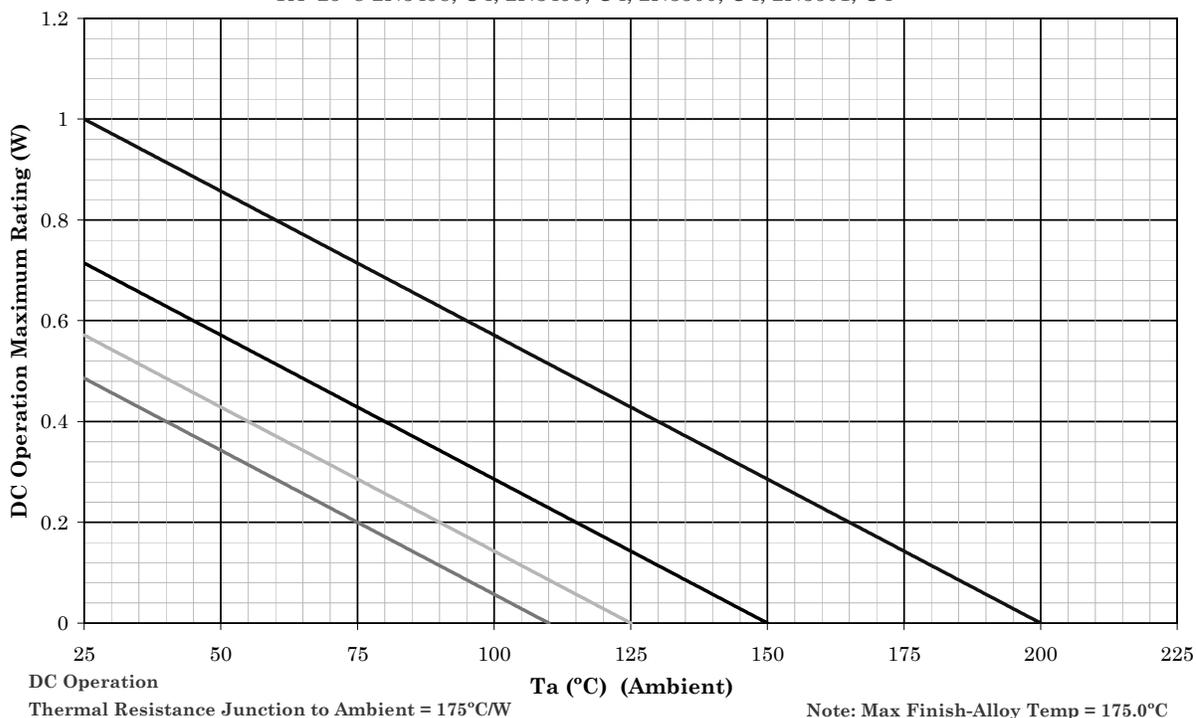
6/ Not required for laser marked devices.

TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and 4.5.2 herein.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	Intermittent operation life: $V_{CB} = 10$ V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of $+100^\circ\text{C}$	
Electrical measurements		See table I, subgroup 2 and 4.5.2 herein.	
<u>Subgroup 4</u>			
Thermal resistance	3131	$R_{\theta JA}$ is required once for qualification. $R_{\theta JC}$ is required once for qualification. $R_{\theta JSP}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (may apply to multiple specification sheets).	15 devices c = 0
Thermal impedance curves		Each supplier shall submit a thermal impedance ($Z_{\theta JX}$) histogram of the entire qualification lot. Thermal impedance curves of the best device in the qualification lot and the qualification lot average. A histogram of thermal resistance ($R_{\theta JX}$) shall be required (116 devices). In addition, the optimal test conditions and thermal impedance limit shall be provided to the qualifying activity in the qualification report for approval. The approved thermal impedance conditions and limit for $Z_{\theta JX}$ shall be used by the supplier in screening and for end-point measurements as applicable. The approved thermal impedance conditions for $R_{\theta JX}$ shall be used by the supplier for conformance inspection.	Sample size N/A
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 6</u>			3 devices
Electrostatic discharge (ESD)	1020		
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition B.	

Temperature-Power Derating Curve

TA=25°C 2N3498, U4, 2N3499, U4, 2N3500, U4, 2N3501, U4



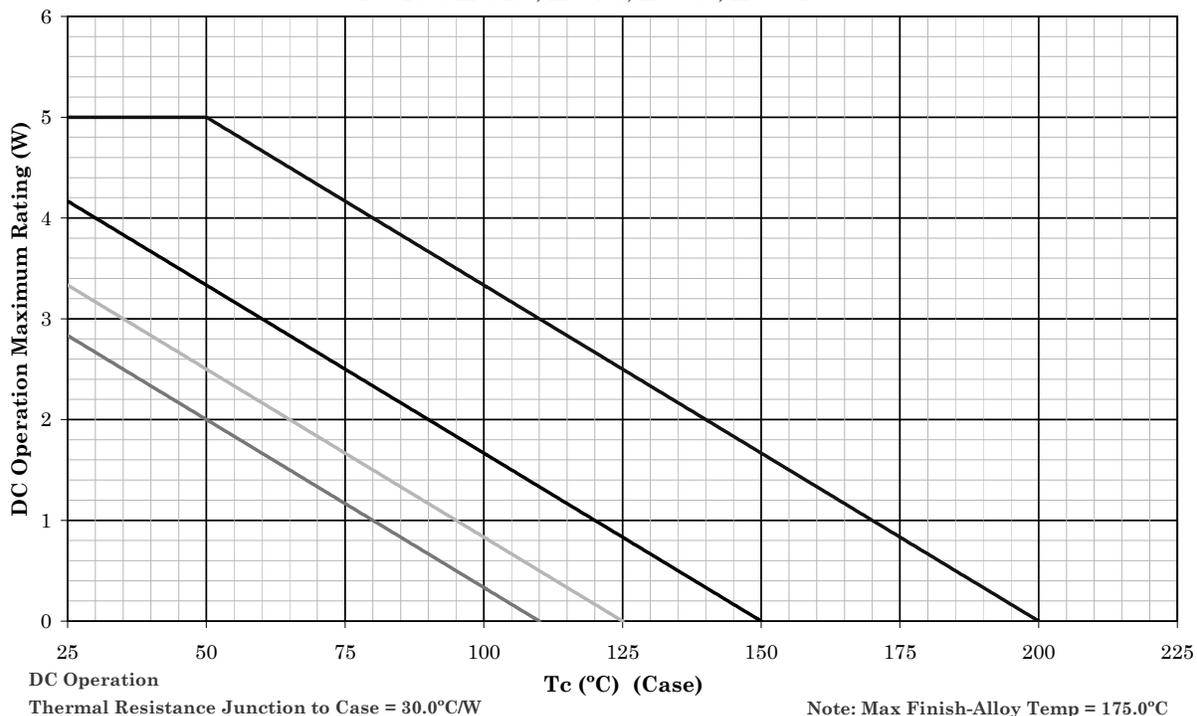
NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 6. Derating for all devices ($R_{\theta JA}$) for 2N3498, 2N3499, 2N3500, and 2N3501 type devices.

Temperature-Power Derating Curve

TC=25°C 2N3498, 2N3499, 2N3500, 2N3501



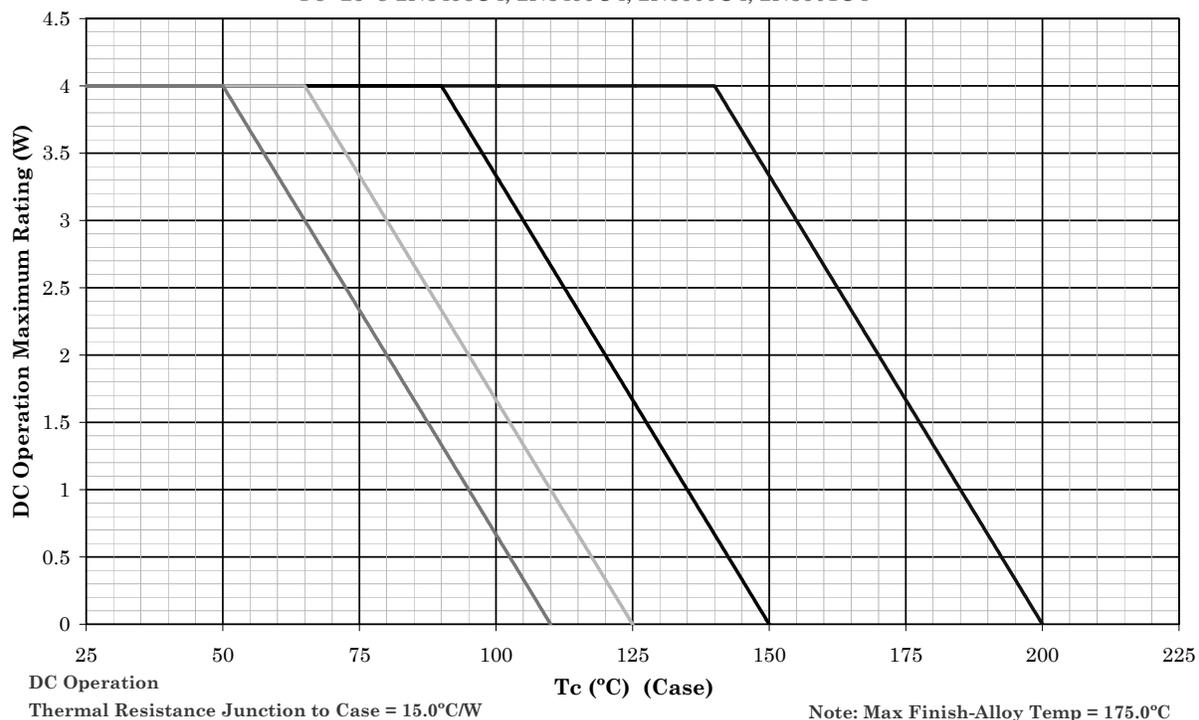
NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 7. Derating for all devices ($R_{\theta JC}$) for 2N3498, 2N3499, 2N3500, and 2N3501 type devices.

Temperature-Power Derating Curve

TC=25°C 2N3498U4, 2N3499U4, 2N3500U4, 2N3501U4



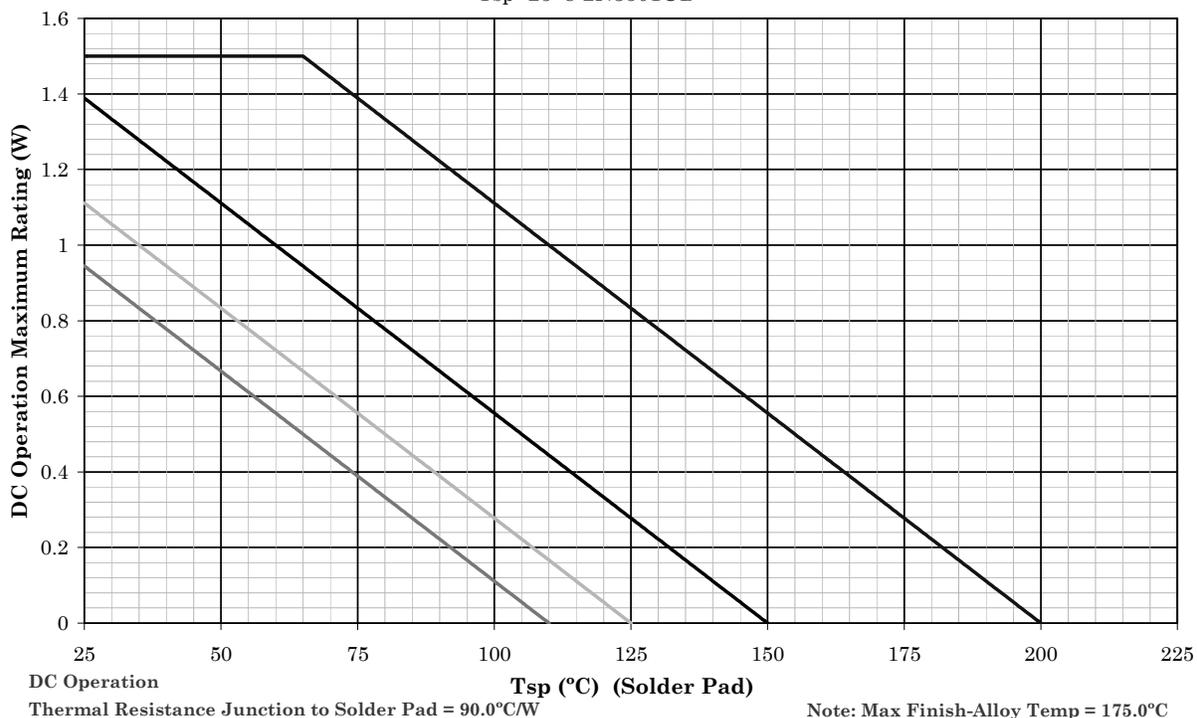
NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 8. Derating for all device ($R_{\theta JC}$) for 2N3498U4, 2N3499U4, 2N3500U4, and 2N3501U4 surface mount device.

Temperature-Power Derating Curve

$T_{sp}=25^{\circ}\text{C}$ 2N3501UB



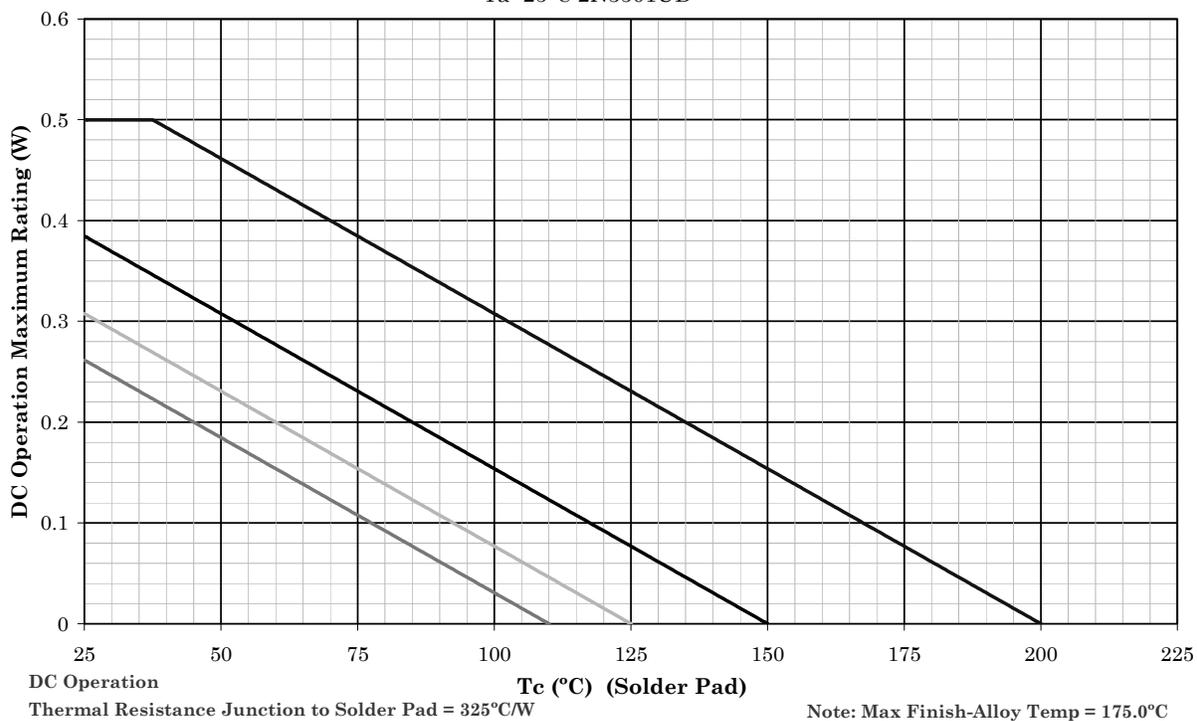
NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^{\circ}\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^{\circ}\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125^{\circ}\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 9. Derating for all devices ($R_{\theta JSP}$) for 2N3501UB type devices.

Temperature-Power Derating Curve

$T_a=25^\circ\text{C}$ 2N3501UB



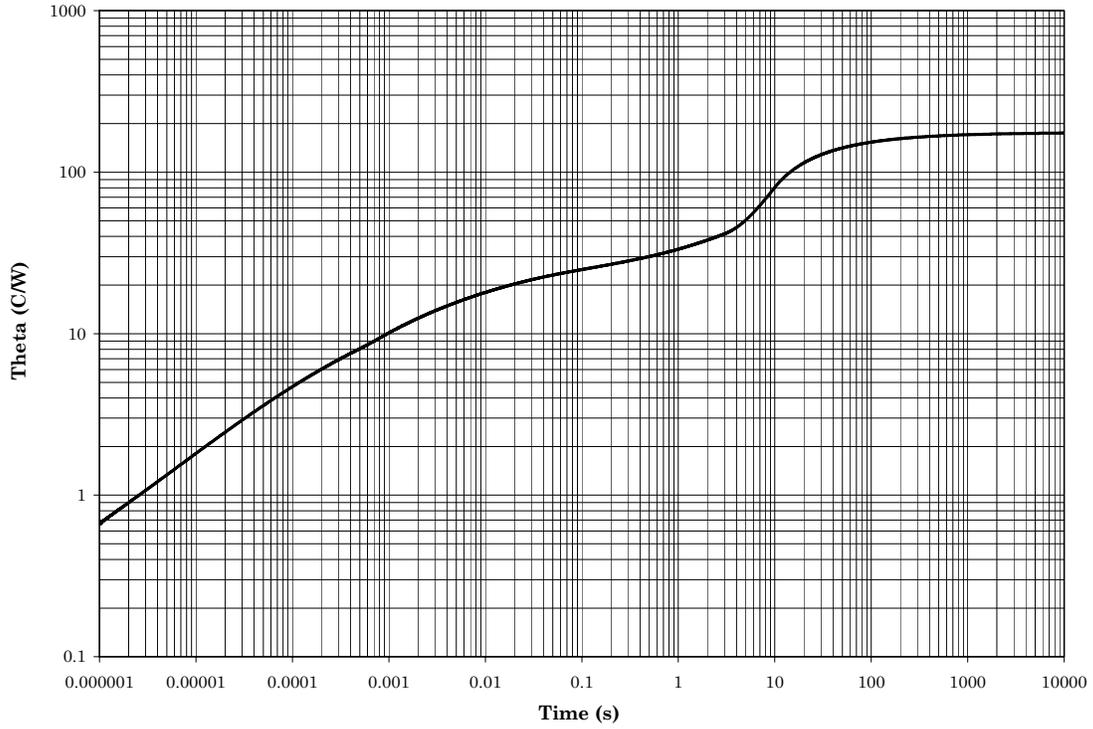
NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 10. Derating for all devices ($R_{\theta JA}$) for 2N3501UB type devices.

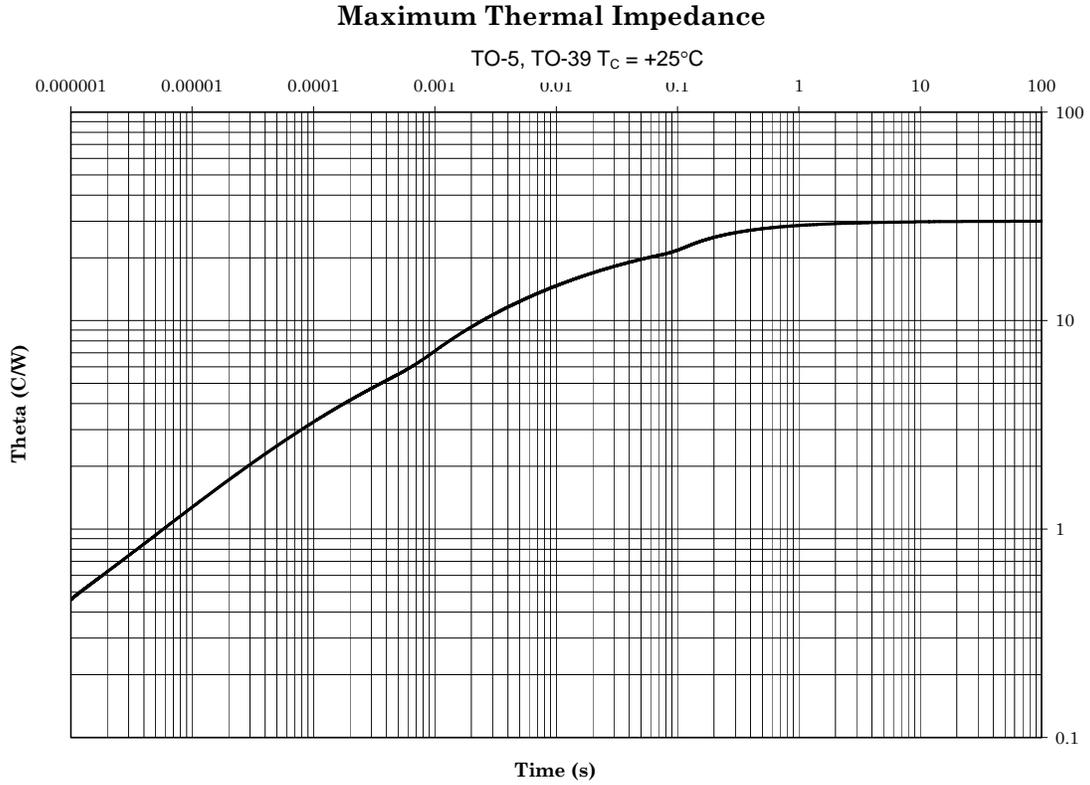
Maximum Thermal Impedance

TO-5 TO-39, Free air, $T_A = +25^\circ\text{C}$.



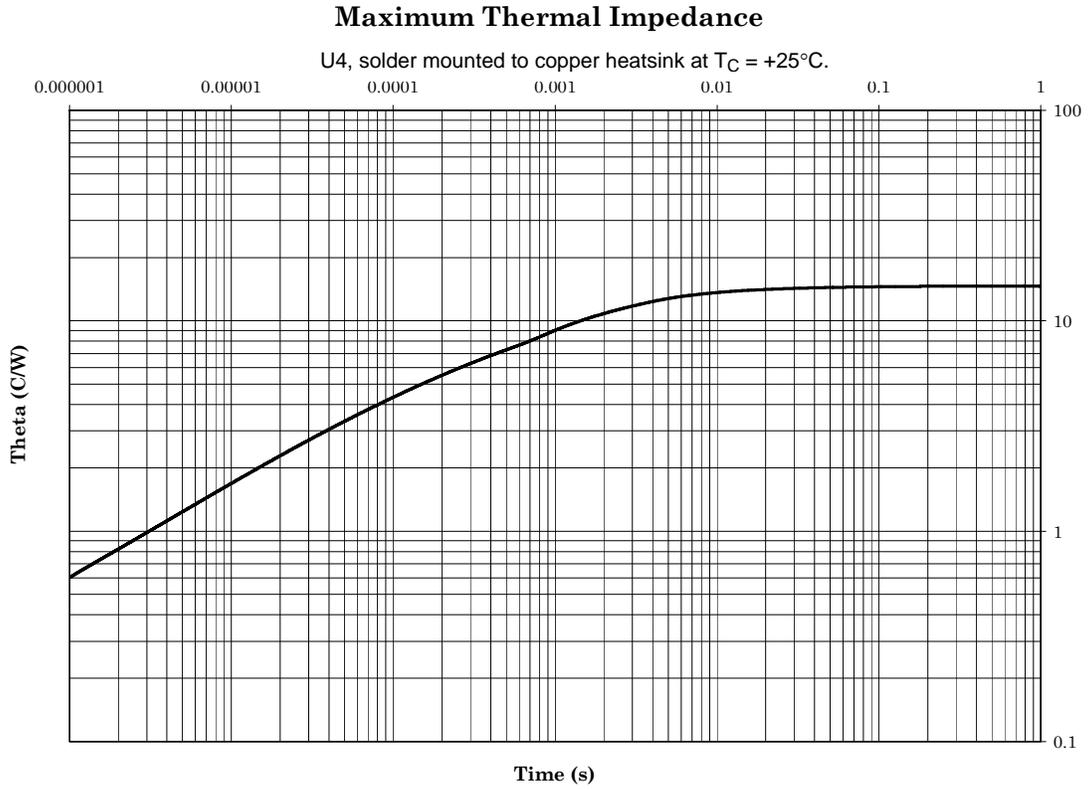
Resistance $R_{\theta JA} = 175^\circ\text{C/W}$.

* FIGURE 11. Thermal impedance graph ($R_{\theta JA}$) for 2N3498, 2N3499, 2N3500, and 2N3501.



Thermal resistance $R_{\theta JC} = 30^\circ\text{C/W}$

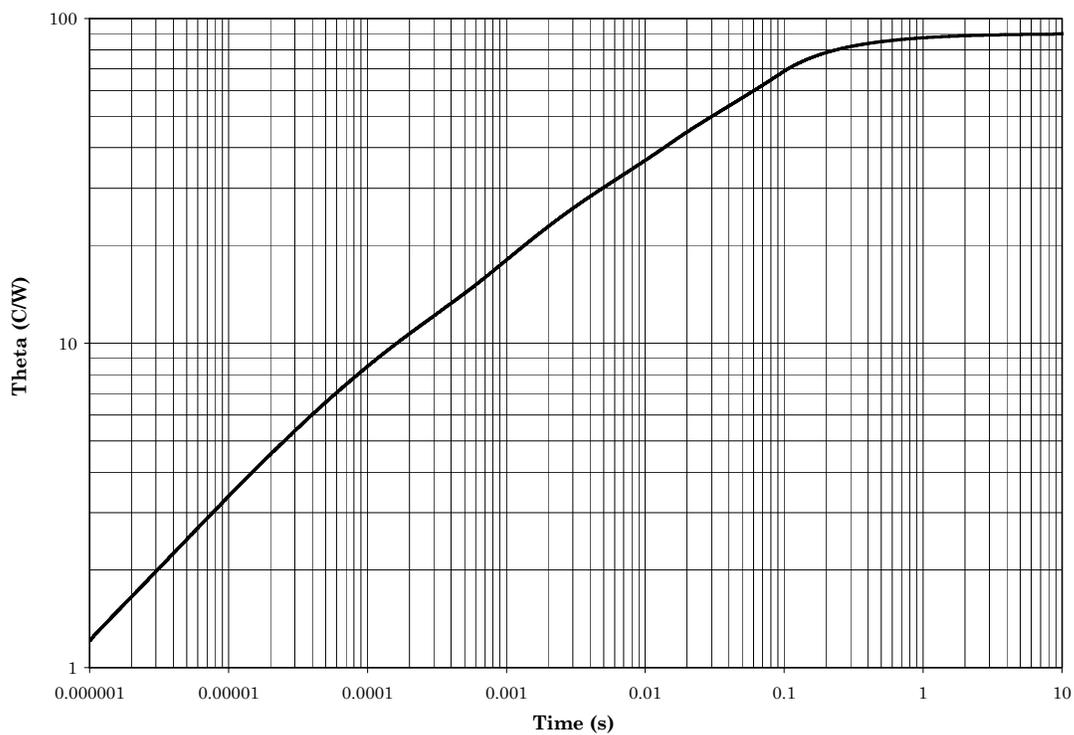
* FIGURE 12. Thermal impedance graph $R_{\theta JC}$ for 2N3498, 2N3499, 2N3500, 2N3501, and all L devices.



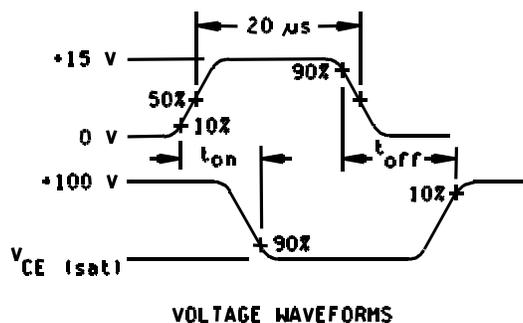
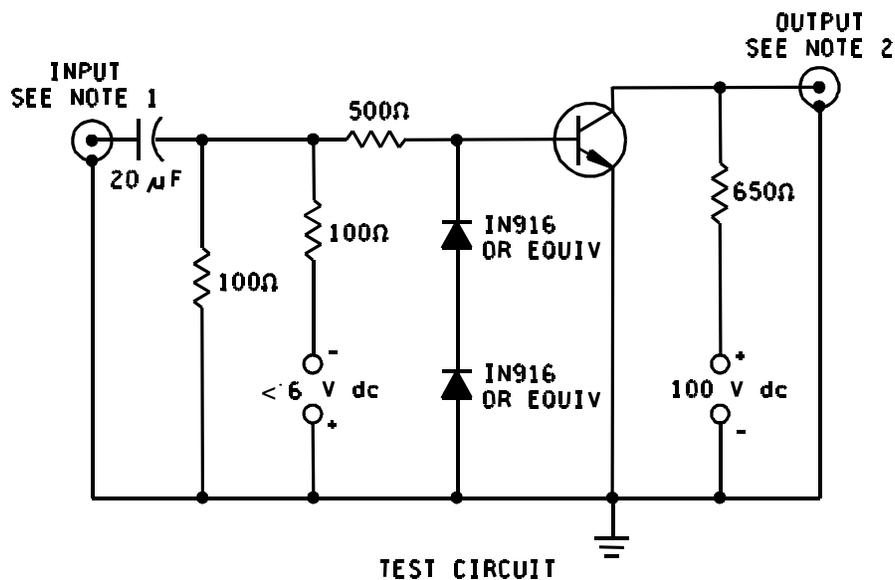
Thermal resistance $R_{\theta JC} = 15^\circ\text{C/W}$

* FIGURE 13. Thermal impedance graph ($R_{\theta JC}$) for 2N3498U4, 2N3499U4, 2N3500U4, and 2N3501U4 (U4).

Maximum Thermal Impedance



* FIGURE 14. Thermal impedance graph ($R_{\theta JSP}$) for 2N3501UB (UB).



NOTES:

1. The input waveform is supplied by a pulse generator with the following characteristics:
Pulse width = $20 \mu\text{s}$, pulse repetition rate = 1 kHz, rise time (t_r) and fall time (t_f) $\leq 10 \text{ ns}$, duty cycle ≤ 2 percent.
2. The output waveform is monitored on a sampling oscilloscope with $Z_{in} \geq 1 \text{ ms}$ and $t_r \leq 1 \text{ ns}$.

FIGURE 15. Turn-on, turn-off switching time test circuit.

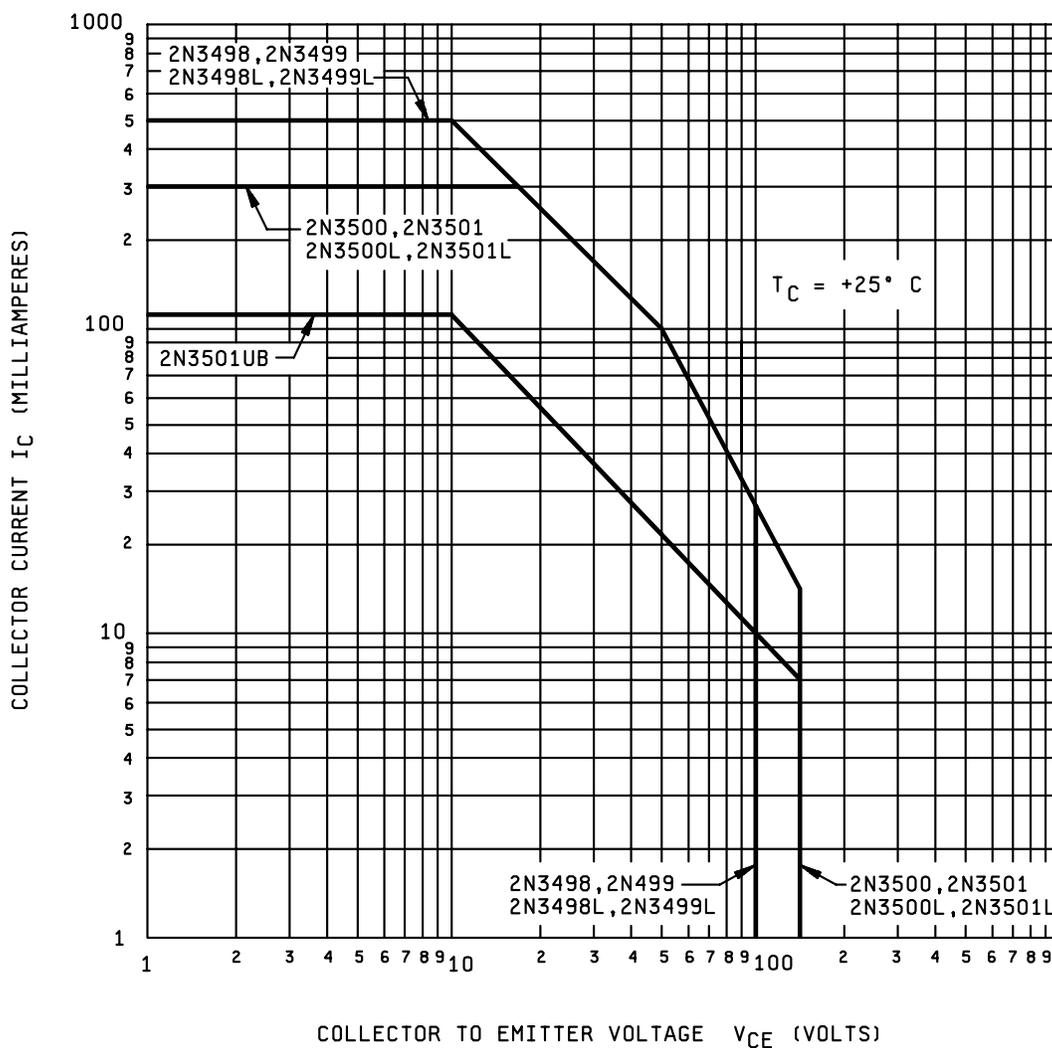
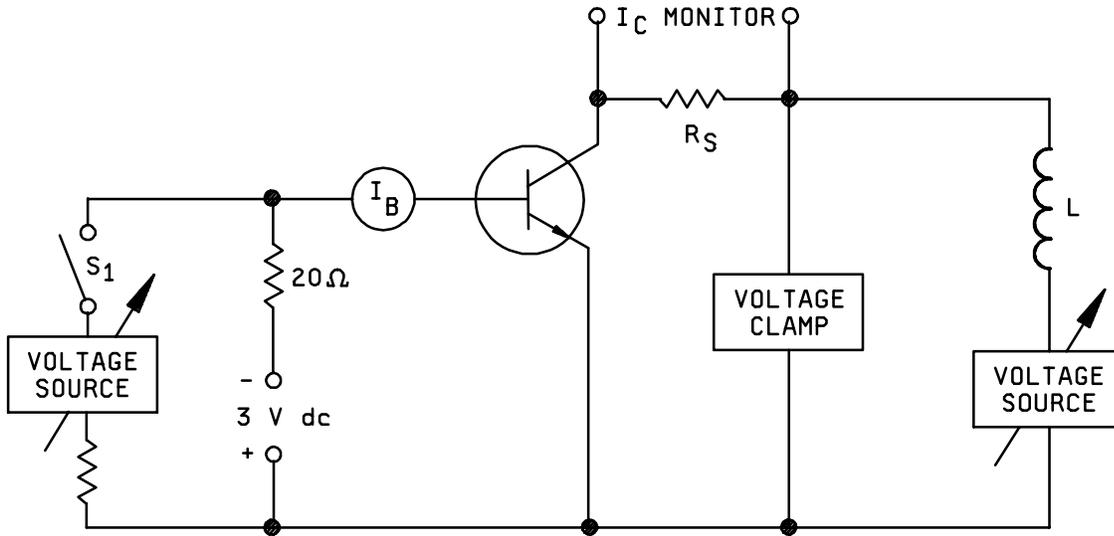


FIGURE 16. Maximum safe operating area.



Voltage clamp:

2N3498, 2N3498L, 2N3499, 2N3499L = 100 V dc

2N3500, 2N3500L, 2N3501, 2N3501L, 2N3501UB = 150 V dc

$R_S \leq 1.0$ ohm (noninductive)

$L =$ (STANCOR C-2688, 0.425 ohm, or equivalent)

Procedure:

1. With switch S_1 closed, set the specified test conditions.
2. Open S_1 .
3. Perform specified end-point tests.

FIGURE 17. Clamped inductive sweep test circuit diagram.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Substitution information. The 2N3498, 2N3499, and 2N3500 devices (including L suffix versions) are now inactive for new design. The 2N3501 is the preferred item and is a direct substitute for the 2N3499, however, due to the higher gain of the 2N3501, it should be evaluated on a case by case basis before it is substituted for the 2N3498 and 2N3500.

* 6.5 Suppliers of JANHC and JANKC die. The qualified JANC suppliers with the applicable letter version (example JANHCA2N3500) will be identified on the QML.

JANHC AND JANKC ordering information		
PIN	Manufacturer	
	43611	34156
2N3498	JANHCA2N3498	JANHCB2N3498
	JANKCA2N3498	JANKCB2N3498
2N3499	JANHCA2N3499	JANHCB2N3499
	JANKCA2N3499	JANKCB2N3499
2N3500	JANHCA2N3500	JANHCB2N3500
	JANKCA2N3500	JANKCB2N3500
2N3501	JANHCA2N3501	JANHCB2N3501
	JANKCA2N3501	JANKCB2N3501

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 11
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5961-3015)

Review activities:
 Army - AR, MI, SM
 Navy - AS, MC
 Air Force - 19, 99

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://assist.daps.dla.mil>.