INCH-POUND

MIL-PRF-19500/733
30 November 2005

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED
(TOTAL DOSE AND SINGLE EVENT EFFECTS)
TRANSISTORS, P-CHANNEL, SILICON, TYPES 2N7523T1, 2N7523U2, 2N7524T1, AND 2N7524U2,
JANTXVR, F AND JANSR, F

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an P-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). See 6.5 for JANHC and JANKC die versions.

1.2 Physical dimensions. See figure 1, TO-254AA (T1) and figure 2, SMD2 TO-276AC (U2).

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Type	P_T (1) T_C = +25°C	P_T T_A = +25°C (free air)	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) T_C = +25°C	I_{D2} (3) (4) T_C = +100°C	I_S	I_{DM} (5)	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A(pk)	°C
2N7523T1	208	1.60	0.60	-30	-30	±20	-45	-45	-45	-180	-55 to +150
2N7523U2	250	2.60	0.50	-30	-30	±20	-56	-56	-56	-224	
2N7524T1	208	1.60	0.60	-60	-60	±20	-45	-45	-45	-180	
2N7524U2	250	2.60	0.50	-60	-60	±20	-56	-56	-56	-224	

(1) Derate linearly by 2.00 W/°C (U2) or 1.67 W/°C (T1) for T_C > +25°C.
(2) See figure 3, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package design and device construction, to 45 A for T1 or to 56 A for U2.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(4) See figure 4, maximum drain current graph.
(5) I_{DM} = 4 X I_{D1}, as defined in note (3).

Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil/.

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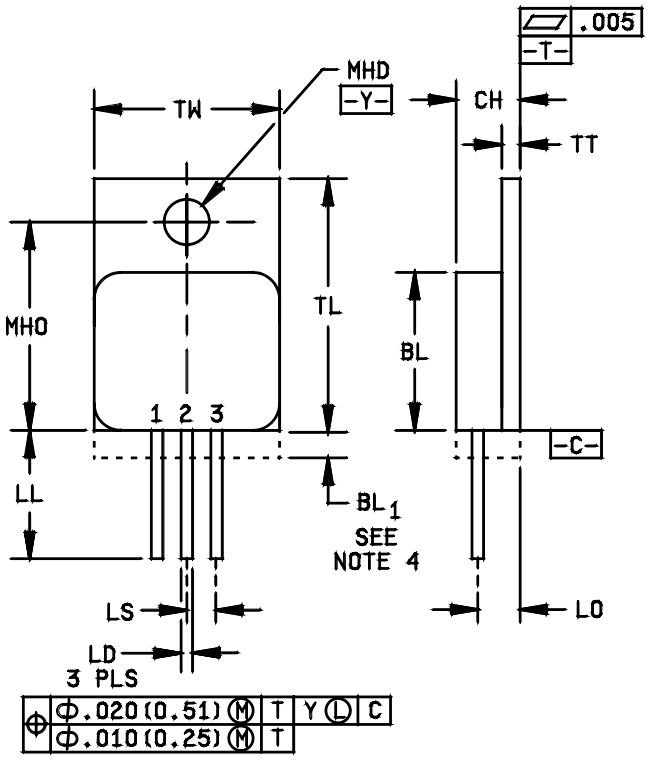
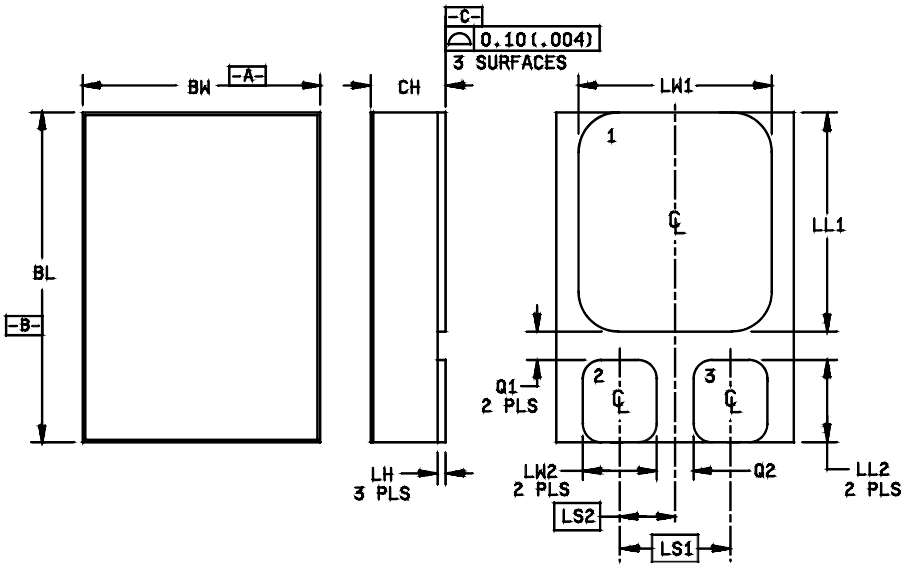


Ltr.	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.535	.545	13.59	13.84
CH	.249	.260	6.32	6.60
LD	.035	.045	0.89	1.14
LL	.510	.570	12.95	14.48
LO	.150 BSC		3.81 BSC	
LS	.150 BSC		3.81 BSC	
MHD	.139	.149	3.53	3.78
MHO	.665	.685	16.89	17.40
TL	.790	.800	20.07	20.32
TT	.040	.050	1.02	1.27
TW	.535	.545	13.59	13.84
Term 1	Drain			
Term 2	Source			
Term 3	Gate			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from the case.
4. This area is for the lead feed-thru eyelets (configuration is optional, but will not extend beyond this zone).
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions for TO-254AA (2N7523T1 and 2N7524T1).



Ltr.	Dimensions			
	Inches		Millimeters	
	Min	Min	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH	.1085	.1205	2.76	3.06
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The lid shall be electrically isolated from the drain, gate and source.
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions for SMD2 TO-276AC (2N7523U2 and 2N7524U2).

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0 mA dc	$V_{GS(TH)}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS}	Max $r_{DS(ON)}$ (1) V_{GS} = 12 V dc		E_{AS} at I_{D1}	I_{AS}
					T_J = +25°C at I_{D2}	T_J = +150°C at I_{D2}		
	V dc	V dc		µA dc	ohm	ohm	mJ	A
		Min	Max					
2N7523T1	-30	-2.0	-4.0	-10	0.014	0.018	1250	-45
2N7523U2	-30	-2.0	-4.0	-10	0.013	0.017	1116	-56
2N7524T1	-60	-2.0	-4.0	-10	0.017	0.034	890	-45
2N7524U2	-60	-2.0	-4.0	-10	0.016	0.032	725	-56

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figures 1 (T3, TO-254AA) and 2 (U2, surface mount TO-276AC) herein.

* 3.4.1 Lead formation and finish. Lead finish shall be solderable in accordance with MIL-STD-750, MIL-PRF-19500 and herein. Where a choice of finish is desired, it shall be specified in the acquisition document (see 6.2). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of MIL-PRF-19500 and 100 percent dc testing in accordance with table I, subgroup 2 herein.

3.4.2 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.5.1 Handling. MOS devices shall be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

a. Devices should be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate shall be terminated to source, $R \leq 100\ k\Omega$, whenever bias voltage is to be applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and table I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 Group E thermal impedance. Each supplier shall submit a thermal impedance ($Z_{\theta JX}$) histogram of the entire qualification lot. The histogram data shall be taken prior to the removal of devices that are atypical for thermal impedance. Thermal impedance curves (from $Z_{\theta JX}$ test pulse time to $R_{\theta JX}$ minimum steady-state time) of the best device in the qual lot and the worst device in the qual lot (that meets the supplier proposed screening limit), or from the thermal grouping, shall be submitted. The optimal test conditions and proposed initial thermal impedance screening limit shall be provided in the qualification report. Data indicating how the optimal test conditions were derived for $Z_{\theta JX}$ shall also be submitted. The proposed specification maximum thermal impedance curve shall be submitted. The qualifying activity may approve a different $Z_{\theta JX}$ limit not to exceed the specification's thermal curve for conformance inspection end-point measurements as applicable. Equivalent data, procedures, or statistical process control plans may be used for part, or all, of the above requirements. The approved thermal impedance conditions and limit for $Z_{\theta JX}$ shall be used by the supplier in screening and table I, subgroup 2. The approved thermal resistance conditions for $R_{\theta JX}$ shall be used by the supplier for conformance inspection. For product families with similar thermal characteristics based on the same physical and thermal die, package, and construction combination (thermal grouping), the supplier may use the same thermal impedance curves.

4.2.2 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. End-point measurements shall be in accordance with table III.

4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV level
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)
7	Optional.	Optional.
9	Subgroup 2 of table I herein; I_{GSSF1}, I_{GSSR1}, I_{DSS1}	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein; I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(TH)1}$ ΔI_{GSSF1} = ± 20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ± 10 μA dc or ± 100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein; I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(TH)1}$
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein; ΔI_{GSSF1} = ± 20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ± 10 μA dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ± 20 percent of initial value. $\Delta V_{GS(TH)1}$= ± 20 percent of initial value.	Subgroups 2 and 3 of table I herein; ΔI_{GSSF1} = ± 20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ± 10 μA dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ± 20 percent of initial value. $\Delta V_{GS(TH)1}$= ± 20 percent of initial value.
14	Required.	Required.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and $V_{GS(th)1}$ shall be invoked.
(3) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 30 V, minimum for t = 250 μs, minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

a. Peak current ..... $I_{AS} = I_{D1}$.

b. Inductance ..... $L = \left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]$ mH minimum.

c. Gate to source resistor R_{GS} ..... $25\ \Omega \le R_{GS} \le 200\ \Omega$.

d. Supply voltage ..... V_{DD} = 25 V dc.

e. Initial case temperature ..... T_C = +25° C, -5° C, +10° C.

f. Gate voltage ..... V_{GS} = 12 V dc.

g. Number of pulses to be applied ..... 1 pulse minimum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIa (JANS) and table VIb (JANTXV) of MIL-PRF-19500, and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1051	Test condition G, 100 cycles.
B3	2077	Scanning electron microscope (SEM) qualification may be performed anytime prior to lot formation.
B4	1042	Condition D, 2,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated; T_A = +175°C, t = 120 hours minimum; or T_A = +150°C, t = 240 hours minimum.
B5	2037	Bond strength, test condition A.
* B6		Not applicable.

4.4.2.2 Group B inspection, table VIb (JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D, 2,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.
B5 and B6		Not applicable.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

	Subgroup	Method	Condition
	C2	2036	Test condition A; weight = 10 pounds; t = 15 s. (Not applicable to U2).
*	C5	3161	Thermal resistance, see 4.3.3, $R_{\theta JC(max)}$ = 0.60 °C/W (T1) or 0.50 ºC/W (U2).
	C6	1042	Intermittent operation life, condition D, 6,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$			
2N7523T1, 2N7524T1					0.45	°C/W
2N7523U2, 2N7524U2					0.40	°C/W
Breakdown voltage, drain to source	3407	V_{GS} = 0 V dc, I_D = -1 mA dc, bias condition C	$V_{(BR)DSS}$			
2N7523T1 and U2				-30		V dc
2N7524T1 and U2				-60		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = -1 mA dc	$V_{GS(TH)1}$	-2.0	-4.0	V dc
Gate reverse current	3411	V_{GS} = +20 V dc, bias condition C, V_{DS} = 0	I_{GSSF1}		+100	nA dc
Gate reverse current	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0	I_{GSSR1}		-100	nA dc
Drain current	3413	V_{GS} = 0 V dc, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS1}		-10	µA dc
Static drain to source on-state resistance	3421	V_{GS} = -12 V dc, condition A, pulsed (see 4.5.1), I_D = I_{D2}	$r_{DS(on)1}$			
2N7523T1					0.014	Ω
2N7523U2					0.013	Ω
2N7524T1					0.017	Ω
2N7524U2					0.016	Ω
Forward voltage	4011	Pulsed (see 4.5.1), I_D = I_{D1}, V_{GS} = 0 V dc	V_{SD}		-5.0	V
Subgroup 3						
High-temperature operation:	3411	T_C = T_J = +125°C				
Gate reverse current	3413	V_{GS} = -20 V dc and +20 V dc, bias condition C, V_{DS} = 0	I_{GSS2}		± 200	nA dc
Drain current	3413	V_{GS} = 0 V dc, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		-25	µA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 3 - continued						
High-temperature operation:		$T_C = T_J = +125°C$				
Static drain to source on-state resistance	3421	V_{GS} = -12 V dc, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)3}$			
2N7524T1					0.017	Ω
2N7524U2					0.016	Ω
2N7523T1					0.027	Ω
2N7523U2					0.026	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = -1 mA dc	$V_{GS(th)2}$	-1.0		V dc
Low-temperature operation:		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = -1 mA dc	$V_{GS(th)3}$		-5.0	V dc
Subgroup 4						
Forward transconductance	3475	I_D = rated I_{D2}, V_{DD} = -15 V (see 4.5.1)	g_{FS}			
2N7523T1 & 2N7524T1				39		S
2N7523U2 & 2N7524U2				40		S
Switching time test	3472	I_D = rated I_{D1}, V_{GS}= -12 V dc, R_G = 2.35 Ω (U2), V_{DD} = 50 percent of rated V_{DS}				
Turn-on delay time			$t_{d(on)}$			
2N7523T1 and U2					35	ns
2N7524T1					35	ns
2N7524U2					30	ns
Rise time			t_r			
2N7523T1					150	ns
2N7523U2					200	ns
2N7524T1					150	ns
2N7524U2					100	ns
Turn-off delay time			$t_{d(off)}$			
2N7523T1					100	ns
2N7523U2					70	ns
2N7524T1 and U2					100	ns
Fall time			tf			
2N7523T1					80	ns
2N7523U2					70	ns
2N7524T1					35	ns
2N7524U2					100	ns

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 5						
Safe operating area test (high voltage)	3474	See figures 5 and 6; t_p = 10 ms, V_{DS} = 80 percent of rated V_{DS}				
Electrical measurements		See table I, subgroup 2 herein.				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B	$Q_{G(on)}$			
2N7523T1					160	nC
2N7523U2					220	nC
2N7524T1					160	nC
2N7524U2					200	nC
On-state gate charge			Q_{GS}			
2N7523T1					60	nC
2N7523U2					70	nC
2N7524T1					60	nC
2N7524U2					65	nC
Gate to drain charge			Q_{GD}			
2N7523T1					65	nC
2N7523U2					50	nC
2N7524T1					65	nC
2N7524U2					60	nC
Reverse recovery time	3473	di/dt ≤ 100A/μs, $I_D = I_{D1}$, V_{DD} ≤ Rated V_{DS}	t_{rr}			
2N7523T1					150	ns
2N7523U2					135	ns
2N7524T1					110	ns
2N7524U2					200	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ This test required for the following end-point measurements only:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JANTXV).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-Irradiation limits		Post-Irradiation limits		Post-Irradiation limits		Unit
				R, F		R		F		
	Method	Conditions		Min	Max	Min	Max	Min	Max	
Subgroup 1										
Not applicable										
Subgroup 2		T_C = +25°C								
Steady-state total dose irradiation (V_{GS} bias) 4/	1019	V_{GS} = -12V V_{DS} = 0								
Steady-state total dose irradiation (V_{DS} bias) 4/	1019	V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)								
End-point electricals:										
Breakdown voltage, drain to source	3407	V_{GS} = 0 I_D = -1 mA bias cond. C	$V_{(BR)DSS}$							
2N7523T1 & U2 2N7524T1 & U2				-30 -60		-30 -60		-30 -60		V dc V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	$V_{GS(th)1}$	-2.0	-4.0	-2.0	-4.0	-2.0	-5.0	V dc
Gate reverse current	3411	V_{GS} = -20 V V_{DS} = 0 bias cond. C	I_{GSSR1}		-100		-100		-100	nA dc
Gate forward current	3411	V_{GS} = 20 V V_{DS} = 0 bias cond. C	I_{GSSF1}		100		100		100	nA dc
Drain current	3413	V_{GS} = 0 bias cond. C V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)	I_{DSS1}		-10		-10		-10	µA dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-Irradiation limits		Post-Irradiation limits		Post-Irradiation limits		Unit
	Method	Conditions		R, F		R		F		
				Min	Max	Min	Max	Min	Max	
Static drain to source on-state voltage	3405	V_{GS} = -12 V cond. A pulsed (see 4.5.1) $I_D = I_{D2}$	$V_{DS(on)1}$							
2N7523T1					0.630		0.630		0.630	V dc
2N7523U2					0.784		0.784		0.784	V dc
2N7524T1					0.765		0.765		0.765	V dc
2N7524U2					0.952		0.952		0.952	V dc
Forward voltage source to drain diode	4011	V_{GS} = 0 $I_D = I_{D1}$	V_{SD}		-5.0		-5.0		-5.0	V dc

1/ For sampling plan, see MIL-PRF-19500.
2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in it's qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.
4/ Separate samples shall be pulled for each bias.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification inspection
	Method	Conditions	
Subgroup 1			12 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071	 Test conditions G or H Test conditions C or D	
Electrical measurements		See table I, subgroup 2	
Subgroup 2 1/			12 devices c = 0
Steady state reverse bias	1042	Test condition A; 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state gate bias	1042	Test condition B; 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Subgroup 4			Sample size N/A
Thermal impedance curves		See 4.2.1.1	
Subgroup 5			
Not applicable			
Subgroup 6			3 devices c = 0
ESD	1020	Not required for devices classified as ESD class 1.	
Subgroup 8			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	

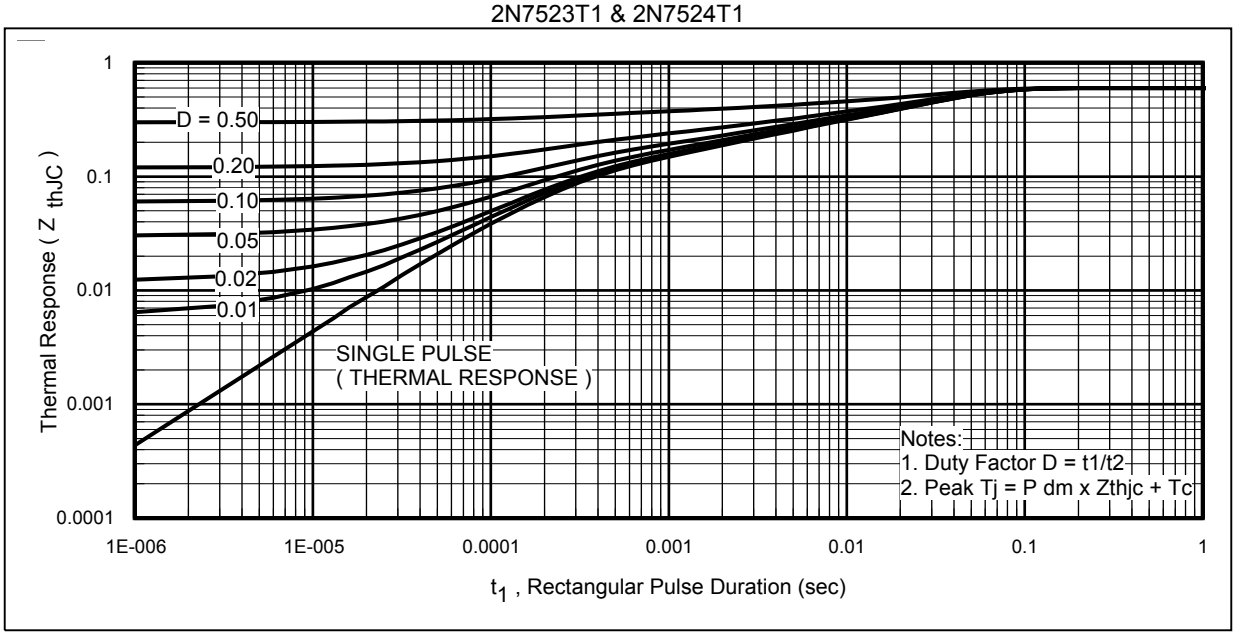
See footnotes at end of table.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only - Continued.

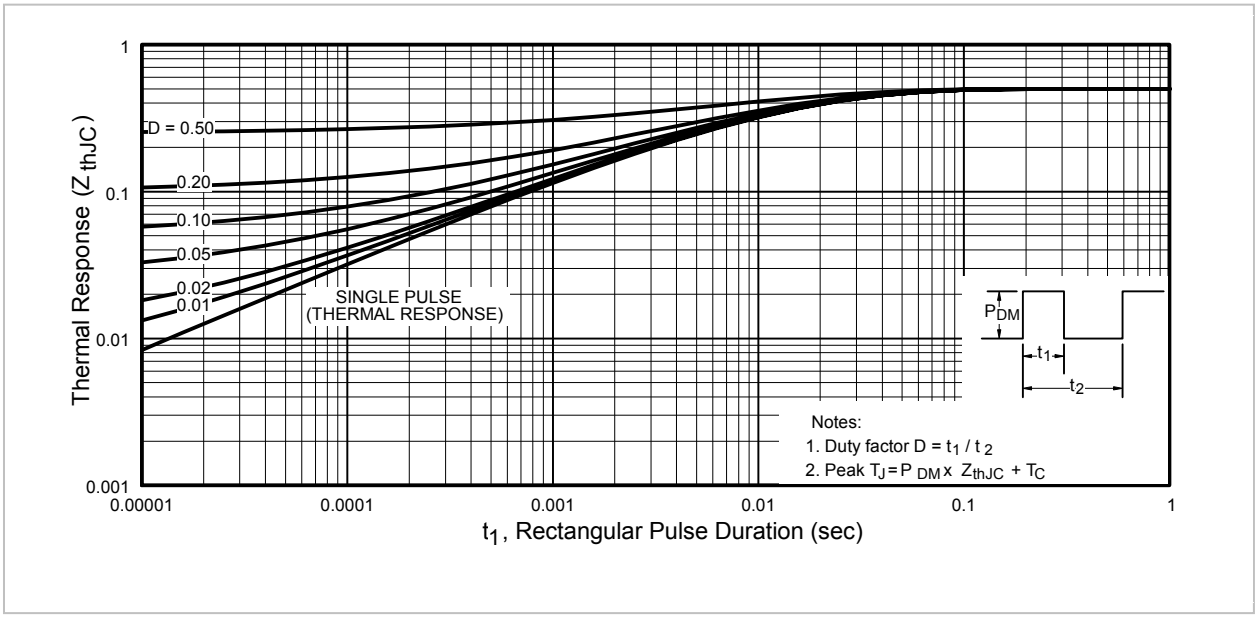
Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
Subgroup 9			3 devices c = 0
SEE 2/ 3/ 4/	1080	See figure 7	
Electrical measurements 5/		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
SEE irradiation		Fluence = 3E5 ±20 percent ions/cm^2 Flux = 2E3 to 2E4 ions/cm^2/sec Temperature = 25 ±5 °C	
		LET = 37.5 - 37.9 MeV-cm^2/mg Range = 33.1 - 36.0 microns Energy = 252.6 – 278.5 MeV	
2N7523T1, 2N7523U2		Insitu bias conditions: V_{DS} = -30 V and V_{GS} = 20 V	
2N7524T1, 2N7524U2		Insitu bias conditions: V_{DS} = -60 V and V_{GS} = 20 V	
		LET = 59.7MeV-cm^2/mg Range = 30.5 – 31.0 microns Energy = 314 - 320 MeV	
2N7523T1, 2N7523U2		Insitu bias conditions: V_{DS} = -30 V and V_{GS} = 15 V V_{DS} = -25 V and V_{GS} = 20 V	
2N7524T1, 2N7524U2		Insitu bias conditions: V_{DS} = -60 V and V_{GS} = 10 V V_{DS} = -45 V and V_{GS} = 15 V V_{DS} = -25 V and V_{GS} = 20 V	
		LET = 81.4 - 82.3 MeV-cm^2/mg Range = 27.0 - 28.4 microns Energy = 332 - 350 MeV	
2N7523T1, 2N7523U2		Insitu bias conditions: V_{DS} = -30 V and V_{GS} = 10 V V_{DS} = -25 V and V_{GS} = 15 V	
2N7524T1, 2N7524U2		Insitu bias conditions: V_{DS} = -60 V and V_{GS} = 10 V	
Electrical measurements 5/		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	

1/ A separate sample for each test shall be pulled.
2/ Group E qualification of testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.
3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.
4/ The sampling plan applies to each bias condition.
5/ Examine I_{GSS1} and I_{DSS1} before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2 may be performed at the manufacturer's option.

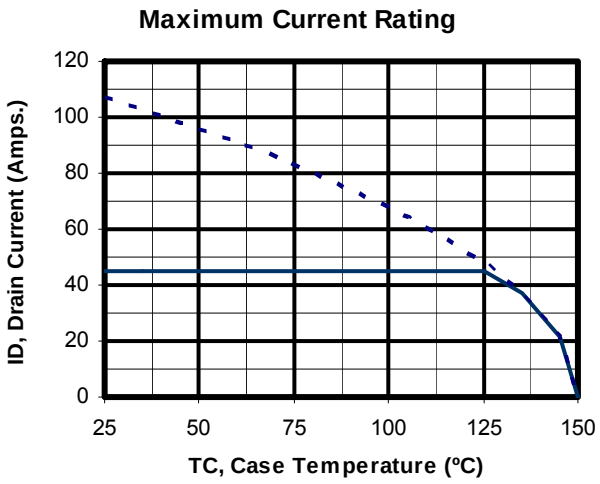
2N7523T1 & 2N7524T1



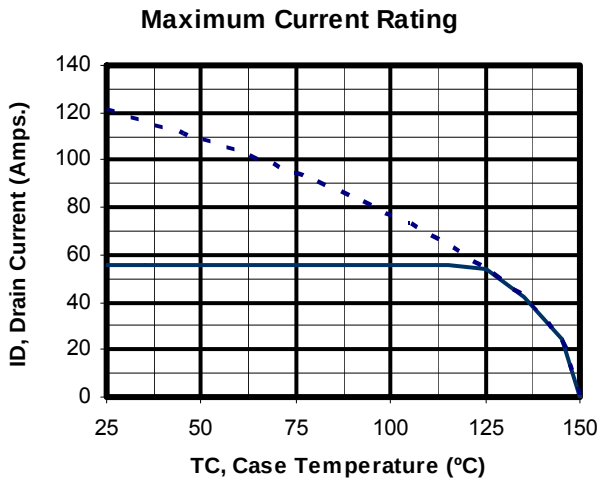
2N7523U2 & 2N7524U2



* FIGURE 3. Thermal impedance curves.



2N7523T1



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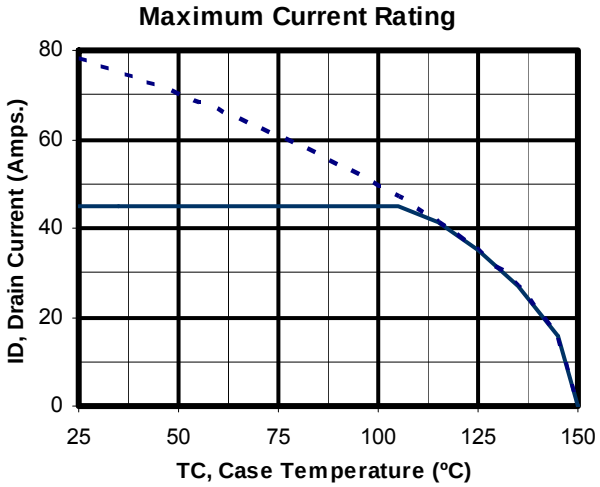
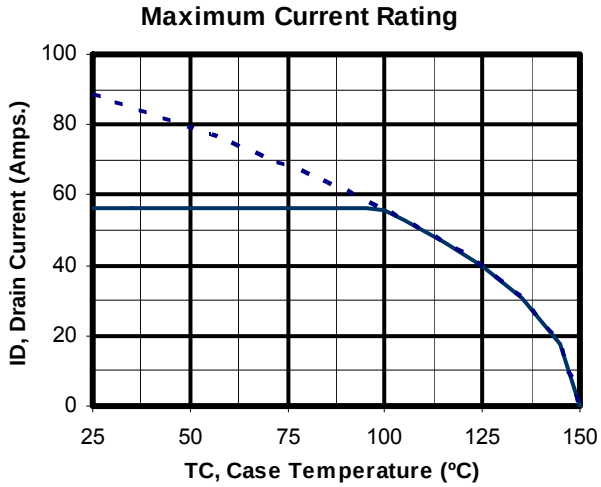


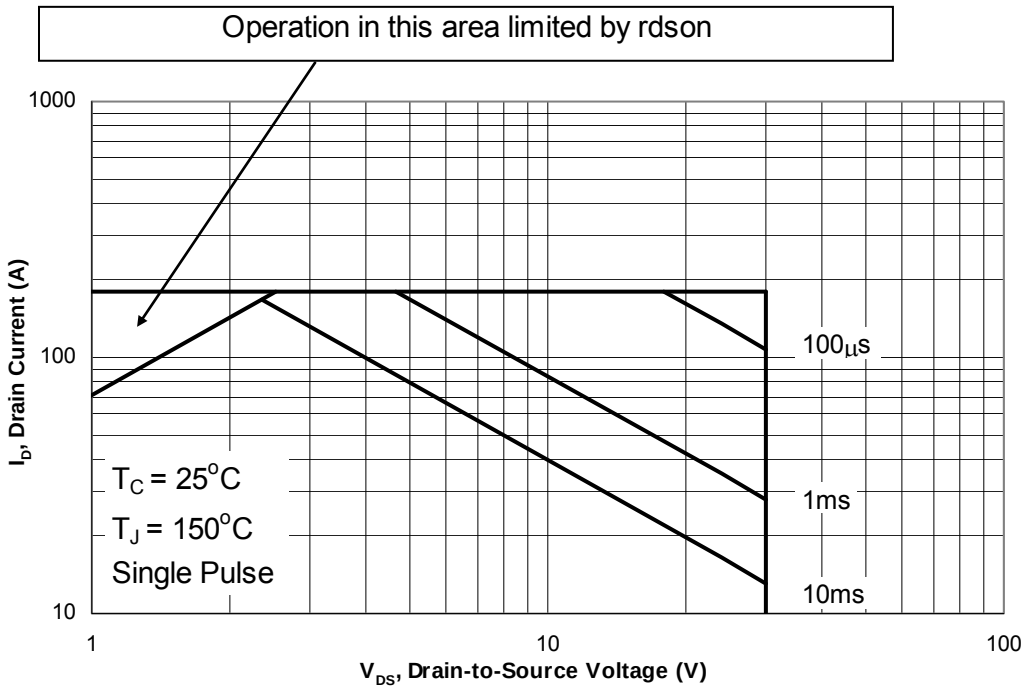
2N7524T1



2N7524U2

FIGURE 4. Maximum drain current vs case temperature graphs.

2N7523T1



2N7523U2

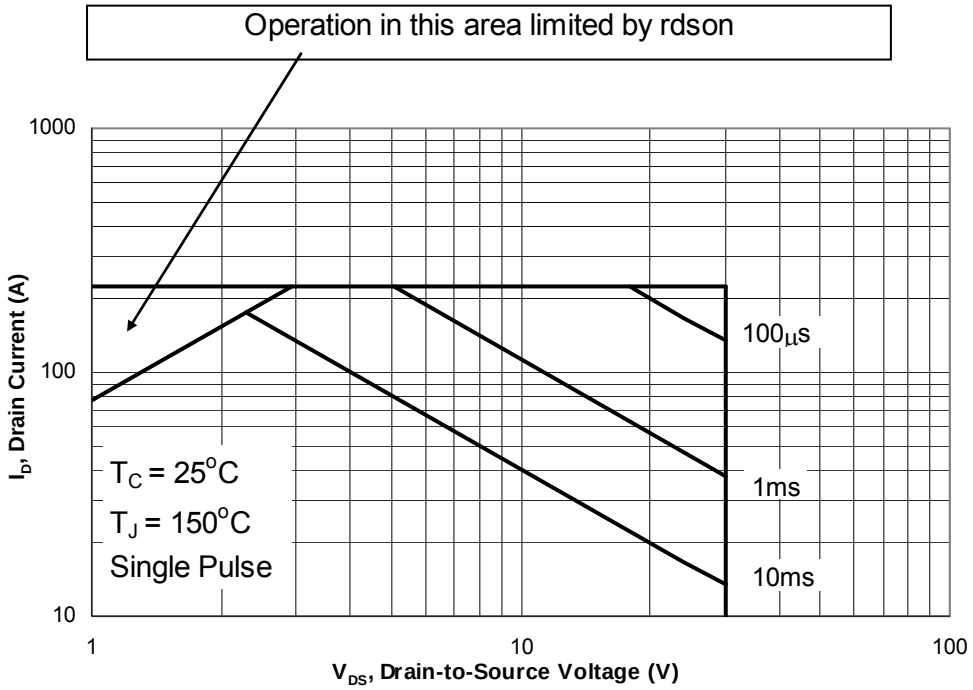
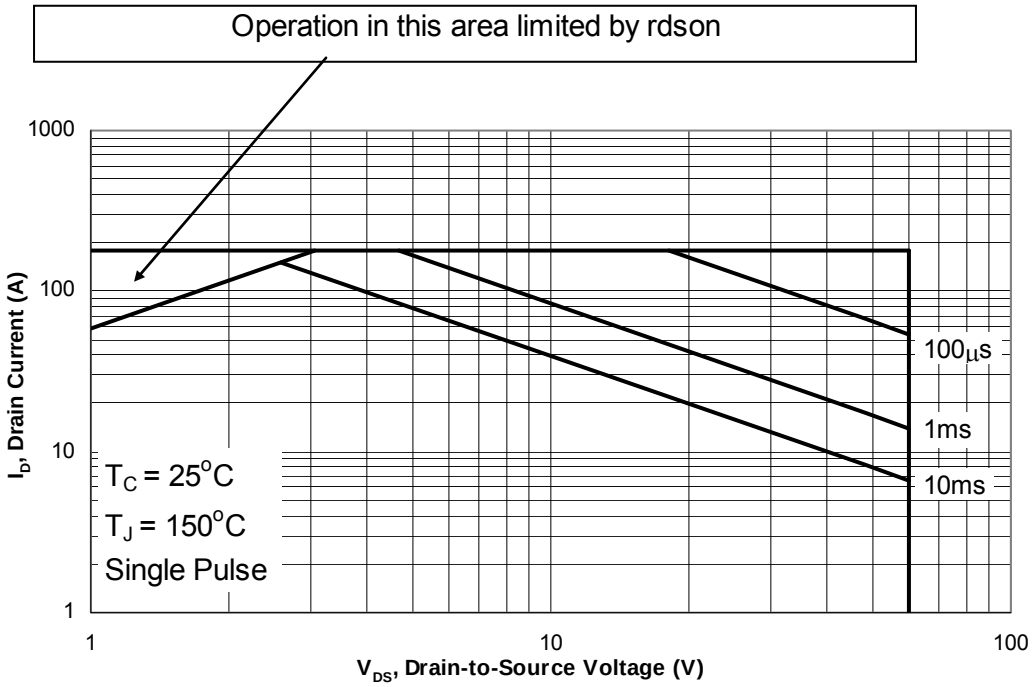


FIGURE 5. Safe operating area graphs.

2N7524T1



2N7524U2

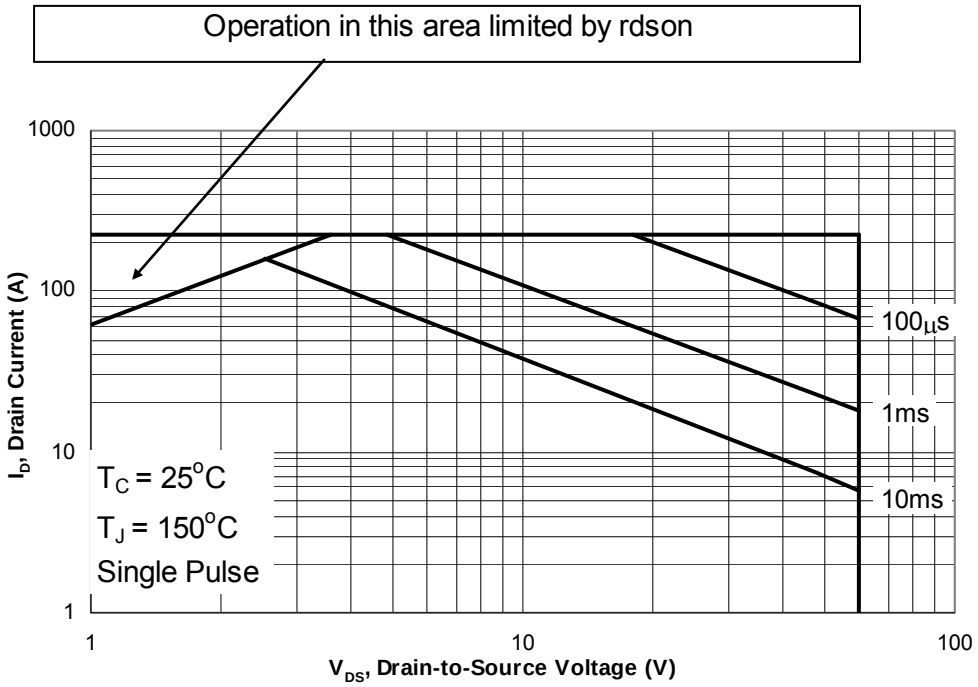
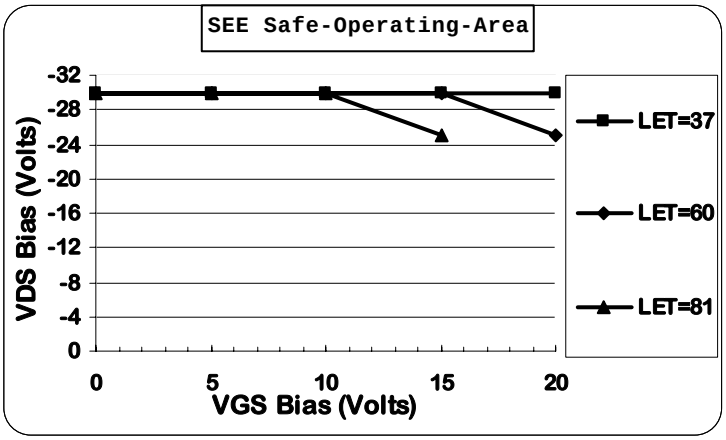


FIGURE 6. Safe operating area graphs.

2N7523T1 & 2N7523U2



2N7524T1 & 2N7524U2

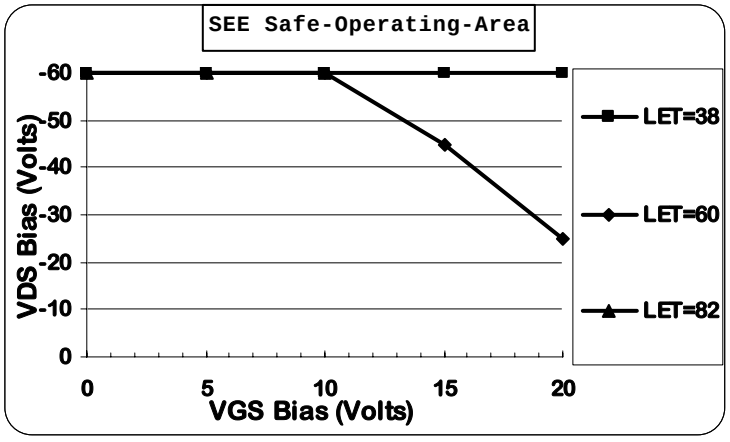


FIGURE 7. SEE safe operation area graphs.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead formation and finish (see 3.4.1).

d. Product assurance level and type designator.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types (military PIN)	Commercial PIN	
	TO-254AA	TO-276AC (SMD2)
2N7523T1	IRHMS59_Z60	
2N7523U2		IRHNA59_Z60
2N7524T1	IRHMS59_064	
2N7524U2		IRHNA59_064

6.5 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/741.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-3019)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil/ .