

The documentation and process conversion measures necessary to comply with this revision shall be completed by 26 March 2015.

INCH-POUND

MIL-PRF-19500/464H
26 January 2015
SUPERSEDING
MIL-PRF-19500/464G
22 May 2009

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, NPN, SILICON, POWER,
DEVICE TYPES 2N5685 AND 2N5686, JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for NPN silicon, power transistors. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for each device type as specified in [MIL-PRF-19500](#).

* 1.2 Package outlines. The device package outlines are as follows: TO-3 in accordance with [figure 1](#) for all encapsulated device types.

1.3 Maximum ratings. $T_C = +25^\circ\text{C}$, unless otherwise specified.

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T (1) $T_C = +100^\circ\text{C}$	V_{CB0}	V_{CE0}	V_{EB0}	I_B	I_C	T_J and T_{STG}	$R_{\theta JC}$
	<u>W</u>	<u>W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>°C</u>	<u>°C/W</u>
2N5685	300	171	60	60	5	15	50	-55 to +200	.584
2N5686	300	171	80	80	5	15	50	-55 to +200	.584

(1) Between $T_C = +25^\circ\text{C}$ and $T_C = +200^\circ\text{C}$ linear derating factor 1.715 W/°C.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



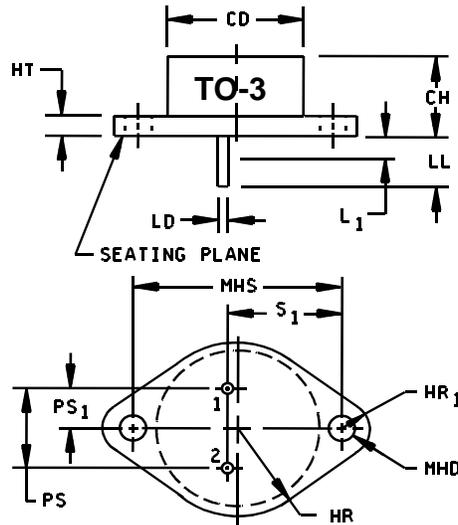
1.4 Primary electrical characteristics. Unless otherwise specified, $T_C = +25^\circ\text{C}$.

Type	h_{FE2} (1)		h_{FE3} (1)		$V_{BE(sat)}$ (1)		$V_{CE(sat)1}$ (1)		$V_{CE(sat)2}$ (1)	
	$V_{CE} = 2 \text{ V dc}$ $I_C = 25 \text{ A dc}$		$V_{CE} = 5 \text{ V dc}$ $I_C = 50 \text{ A dc}$		$I_C = 25 \text{ A dc}$ $I_B = 2.5 \text{ A dc}$		$I_C = 25 \text{ A dc}$ $I_B = 2.5 \text{ A dc}$		$I_C = 50 \text{ A dc}$ $I_B = 10 \text{ A dc}$	
	Min	Max	Min	Max	$\frac{V \text{ dc}}$		$\frac{V \text{ dc}}$		$\frac{V \text{ dc}}$	
					Min	Max	Min	Max	Min	Max
2N5685	15	60	5			2.0		1.0		5.0
2N5686	15	60	5			2.0		1.0		5.0

Type	C_{obo}		$ h_{fe} $		h_{fe}		Switching (see table 1 and figure 2 herein)			
	$V_{CB} = 10 \text{ V dc}$ $I_E = 0$ $0.1 \text{ MHz} \leq f \leq 1.0 \text{ MHz}$		$V_{CE} = 10 \text{ V dc}$ $I_C = 5 \text{ A dc}$ $f = 1 \text{ MHz}$		$V_{CE} = 5 \text{ V dc}$ $I_C = 10 \text{ A dc}$ $f = 1 \text{ kHz}$		t_{on}		t_{off}	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
	μF						μs		μs	
2N5685		1,200	2	20	15			1.5		3.0
2N5686		1,200	2	20	15			1.5		3.0

(1) Pulsed (see 4.5.1).

- * 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.
- * 1.5.1 JAN brand and quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", and "JANTXV".
- * 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.
 - * 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".
 - * 1.5.2.2 Second number symbols. The second number symbols for the transistor covered by this specification sheet are as follows: "5685" and "5686".
- * 1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.875		22.22	3
CH	.250	.450	6.35	11.43	
HR	.495	.525	12.57	13.34	
HR ₁	.131	.188	3.33	4.78	6
HT	.060	.135	1.52	3.43	
LD	.057	.063	1.45	1.60	4, 5, 9
LL	.312	.500	7.92	12.70	4, 5, 9
L ₁		.050		1.27	5, 9
MHD	.151	.165	3.84	4.19	7
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	
PS ₁	.205	.225	5.21	5.72	5
S ₁	.655	.675	16.64	17.15	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Body contour is optional within zone defined by CD.
4. These dimensions shall be measured at points .050 inch (1.27 mm) to .055 inch (1.40 mm) below seating plane. When gauge is not used, measurement shall be made at seating plane.
5. Both terminals.
6. At both ends.
7. Two holes.
8. The collector shall be electrically connected to the case.
9. LD applies between L₁ and LL. Lead diameter shall not exceed twice LD within L₁.
10. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
11. Terminal 1 is emitter; terminal 2 is base; case is collector.

FIGURE 1. Physical dimensions.

2. APPLICABLE DOCUMENTS

- * 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

- * 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

- * DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

- * (Copies of these documents are available online at <http://quicksearch.dla.mil/>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.7 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANTX and JANTXV levels). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurement
	JANTX and JANTXV levels only
(1) 3c	Thermal impedance (see 4.3.2)
11	h_{FE2} and I_{CEX1}
12	See 4.3.1
13	Subgroup 2 of table I herein; ΔI_{CEX1} = 100 percent of initial value or 1 μ A dc, whichever is greater; Δh_{FE2} = 25 percent of initial value.

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: $T_J = +187.5^\circ\text{C} \pm 12.5^\circ\text{C}$; $V_{CB} \geq 20$ V dc, $T_A \leq +100^\circ\text{C}$.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , t_{MD} and V_H where appropriate). See table II, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, appendix E table E-V, and table I herein. Electrical measurements (end-points) shall be in accordance with the table I, subgroup 2 herein.

- * 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JAN, JANTX and JANTXV) of [MIL-PRF-19500](#) and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
* B3	1037	$V_{CE} \geq 10$ V dc, ΔT_J between cycles $\geq +100^\circ\text{C}$, adjust power or current to achieve a $\Delta T_J = +100^\circ\text{C}$.

- * 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	2036	Test condition A, weight = 10 pounds, t = 15 s.
C5	3131	See 4.3.2, $R_{\theta JC} = .584^\circ\text{C/W}$.
* C6	1037	$V_{CE} \geq 10$ V dc, ΔT_J between cycles $\geq +100^\circ\text{C}$, adjust power or current to achieve a $\Delta T_J = +100^\circ\text{C}$.

- * 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance 2/	3131	See 4.3.2	$Z_{\theta JX}$			°C/W
Breakdown voltage collector to emitter 2N5685 2N5686	3011	Bias condition D; $I_C = 100$ mA dc, pulsed (see 4.5.1)	$V_{(BR)CEO}$	60 80		V dc V dc
Collector to emitter cutoff current 2N5685 2N5686	3041	Bias condition D $V_{CE} = 30$ V dc $V_{CE} = 40$ V dc	I_{CEO}		500	μ A dc
Collector to emitter cutoff current 2N5685 2N5686	3041	Bias condition A; $V_{BE} = 1.5$ V dc $V_{CE} = 60$ V dc $V_{CE} = 80$ V dc	I_{CEX1}		10	μ A dc
Emitter to base cutoff current	3061	Bias condition D; $V_{BE} = 5$ V dc, $I_C = 0$	I_{EBO}		1.0	mA dc
Collector to base cutoff current 2N5685 2N5686	3036	Bias condition D $V_{CE} = 60$ V dc $V_{CE} = 80$ V dc	I_{CBO1}		2.0	mA dc
Base to emitter saturated	3066	Test condition A; $I_C = 25$ A dc, $I_B = 2.5$ A dc, pulsed (see 4.5.1)	$V_{BE(sat)}$		2.0	V dc
Base to emitter non-saturated	3066	Test condition B; $I_C = 25$ A dc, $V_{CE} = 2$ V dc, pulsed (see 4.5.1)	V_{BE}		2.0	V dc
Collector to emitter saturated voltage	3071	$I_C = 25$ A dc; $I_B = 2.5$ A dc pulsed (see 4.5.1)	$V_{CE(sat)1}$		1.0	V dc
Collector to emitter saturated voltage	3071	$I_C = 50$ A dc; $I_B = 10$ A dc, pulsed (see 4.5.1)	$V_{CE(sat)2}$		5.0	V dc
Forward current transfer ratio	3076	$V_{CE} = 2$ V dc; $I_C = 5$ A dc, pulsed (see 4.5.1)	h_{FE1}	30		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued						
Forward current transfer ratio	3076	$V_{CE} = 2 \text{ V dc}; I_C = 25 \text{ A dc}$, pulsed (see 4.5.1)	h_{FE2}	15	60	
Forward current transfer ratio	3076	$V_{CE} = 5 \text{ V dc}; I_C = 50 \text{ A dc}$, pulsed (see 4.5.1)	h_{FE3}	5		
<u>Subgroup 3</u>						
High temperature operation:		$T_A = +150^\circ\text{C}$				
Collector to emitter cutoff current 2N5685 2N5686	3041	Bias condition A; $V_{BE} = 1.5 \text{ V dc}$ $V_{CE} = 60 \text{ V dc}$ $V_{CE} = 80 \text{ V dc}$	I_{CEX2}		5	mA dc
Low temperature operation:		$T_A = -55^\circ\text{C}$				
Forward current transfer ratio	3076	$V_{CE} = 2.0 \text{ V dc}; I_C = 25 \text{ A dc}$, pulsed (see 4.5.1)	h_{FE4}	7		
<u>Subgroup 4</u>						
Pulse response	3251	Test condition A, except test circuit and pulse requirements (see figure 2)				
Turn-on time		$V_{CC} = 30 \text{ V dc}; I_C = 25 \text{ A dc}$, $I_{B1} = 2.5 \text{ A dc}$	t_{on}		1.5	μs
Turn-off time		$V_{CC} = 30 \text{ V dc}; I_C = 25 \text{ A dc}$, $I_{B1} = - I_{B2} = 2.5 \text{ A dc}$	t_{off}		3.0	μs
Storage time		$V_{CC} = 30 \text{ V dc}; I_C = 25 \text{ A dc}$, $I_{B1} = - I_{B2} = 2.5 \text{ A dc}$	t_s		2.0	μs
Magnitude of common emitter small-signal short-circuit forward-current transfer ratio	3306	$V_{CE} = 10 \text{ V dc}; I_C = 5 \text{ A dc}$, $f = 1 \text{ MHz}$	$ h_{fe} $	2	20	

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u> - Continued						
Small-signal short-circuit forward-current transfer ratio	3206	$V_{CE} = 5 \text{ V dc}; I_C = 10 \text{ A dc}, f = 1 \text{ kHz}$	h_{fe}	15		
Open circuit output capacitance	3236	$V_{CB} = 10 \text{ V dc}; I_E = 0, 0.1 \text{ MHz} \leq f \leq 1 \text{ MHz}$	C_{obo}		1,200	pF
<u>Subgroup 5</u>						
Safe operating area (continuous dc)	3051	$T_C = +25^\circ\text{C}; t = 1 \text{ s}, 1 \text{ cycle (see figures 3 and 4)}$				
<u>Test 1</u>		$V_{CE} = 6 \text{ V dc}; I_C = 50 \text{ A dc}$				
<u>Test 2</u>		$V_{CE} = 30 \text{ V dc}; I_C = 10 \text{ A dc}$				
<u>Test 3</u> 2N5685		$V_{CE} = 50 \text{ V dc}; I_C = 560 \text{ mA dc}$				
2N5686		$V_{CE} = 60 \text{ V dc}; I_C = 640 \text{ mA dc}$				
Safe operating area (switching)	3053	Load condition C (unclamped inductive load) (see figure 5) $T_C = +25^\circ\text{C}$ duty cycle ≤ 10 percent $R_S = 0.1 \Omega; t_r = t_f \leq 500 \text{ ns}$				
<u>Test 1</u>		t_p approximately 5 ms (vary to obtain I_C); $R_{BB1} = 10 \Omega;$ $V_{BB1} = 20 \text{ V dc}; R_{BB2} = \infty;$ $V_{BB2} = 0 \text{ V}; V_{CC} = 50 \text{ V dc};$ $I_C = 20 \text{ A dc}; L = 1 \text{ mH};$ Sanford Miller CK - 50, 50 A .002 Ω (or equivalent)				
<u>Test 2</u>		t_p approximately 5 ms (vary to obtain I_C); $R_{BB1} = 100 \Omega;$ $V_{BB1} = 10 \text{ V dc}; R_{BB2} = \infty;$ $V_{BB2} = 0 \text{ V}; V_C = 50 \text{ V dc};$ $I_C = 1.5 \text{ A dc}; L = 80 \text{ mH};$ (2 each signal transformer CH06, 6A) 0.4 Ω (or equivalent)				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

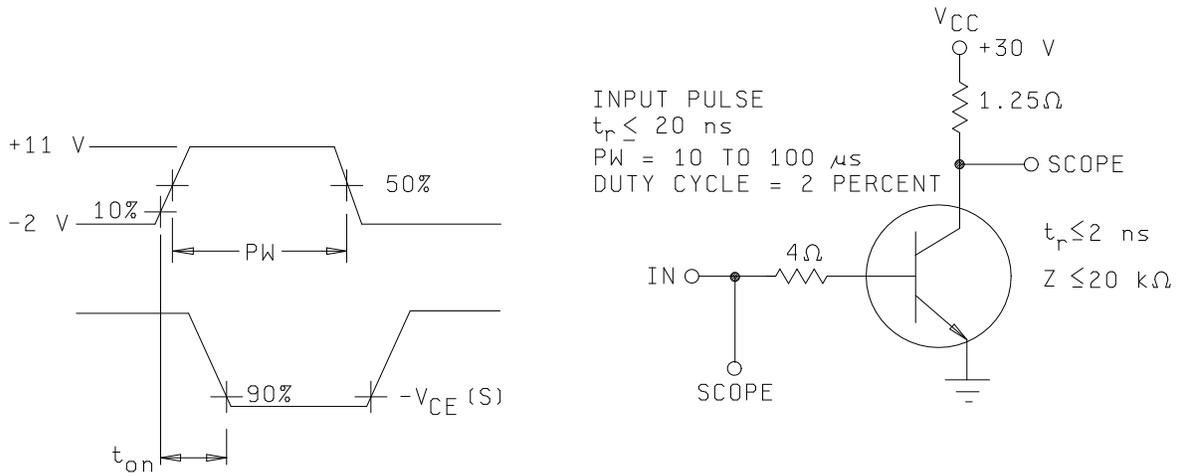
Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u> - Continued						
Safe operating area (switching)	3053	Clamped inductive load (see figures 6 and 7) $T_A = +25^\circ\text{C}$; $V_{CC} = 50\text{ V dc}$				
2N5685		Clamp voltage = 60 V dc				
2N5686		Clamp voltage = 80 V dc				
Electrical measurements		See table I , subgroup 2				

1/ For sampling plan, see [MIL-PRF-19500](#).

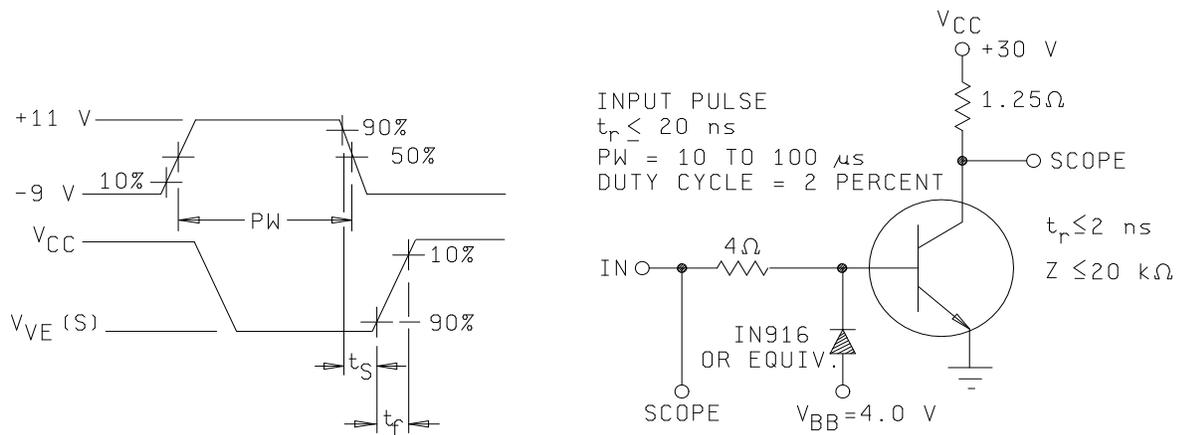
2/ This test required for the following end-point measurements only:
 Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).
 Group C, subgroups 2 and 6.
 Group E, subgroup 1.

* TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Test condition C, 500 cycles.	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 2</u>			45 devices c = 0
Blocking life	1048	Test temperature = +125°C; V _{CB} = 30 V dc; T = 1,000 hours.	
Electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 4</u>			
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition B.	



TURN-ON (t_{ON}) TIME TEST CIRCUIT



$t_{off} = t_s + t_f$

TURN-OFF (t_{OFF}) TIME TEST CIRCUIT

FIGURE 2. Switching time test circuits.

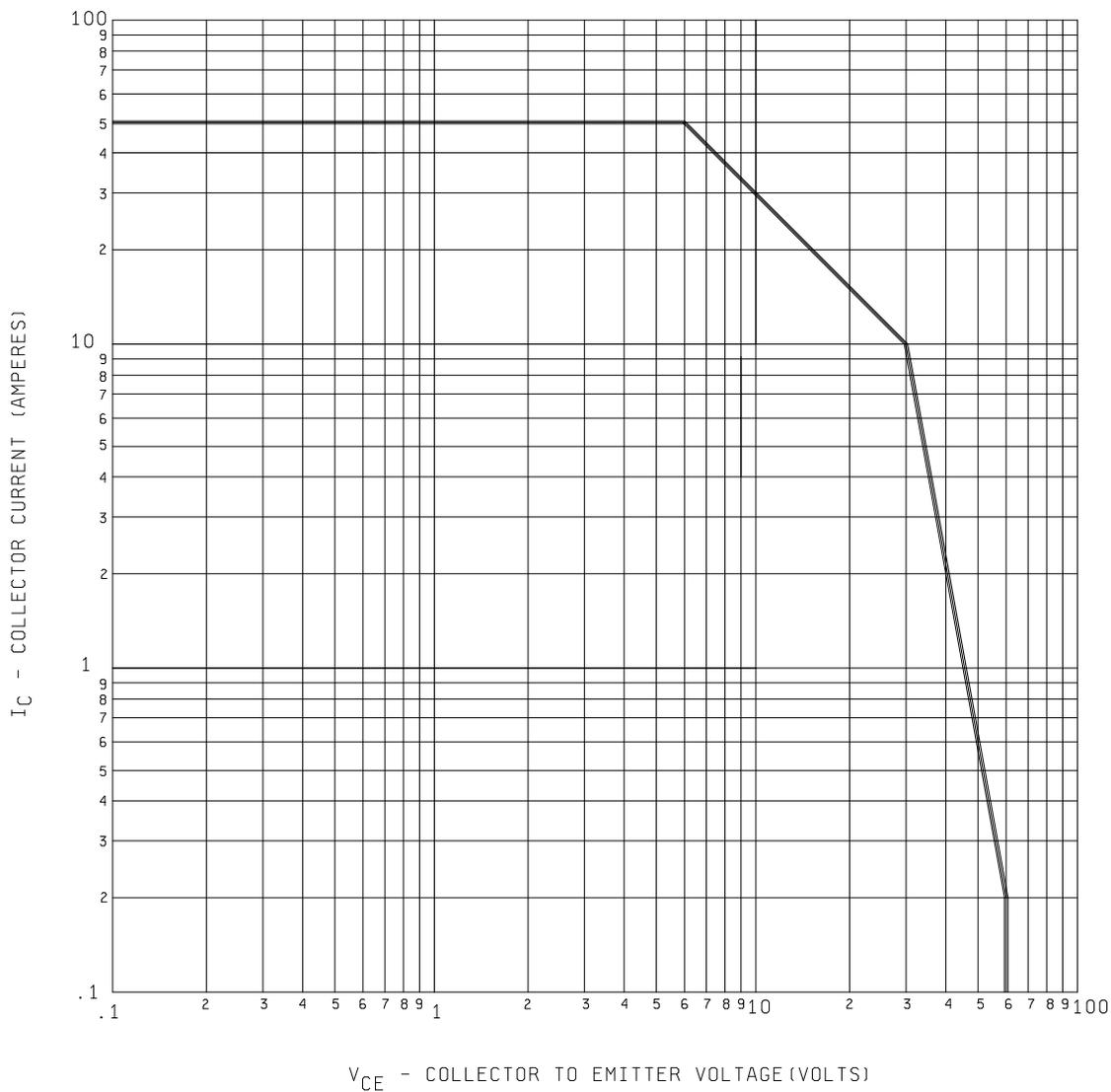


FIGURE 3. Maximum safe operating area graph continuous dc (2N5685).

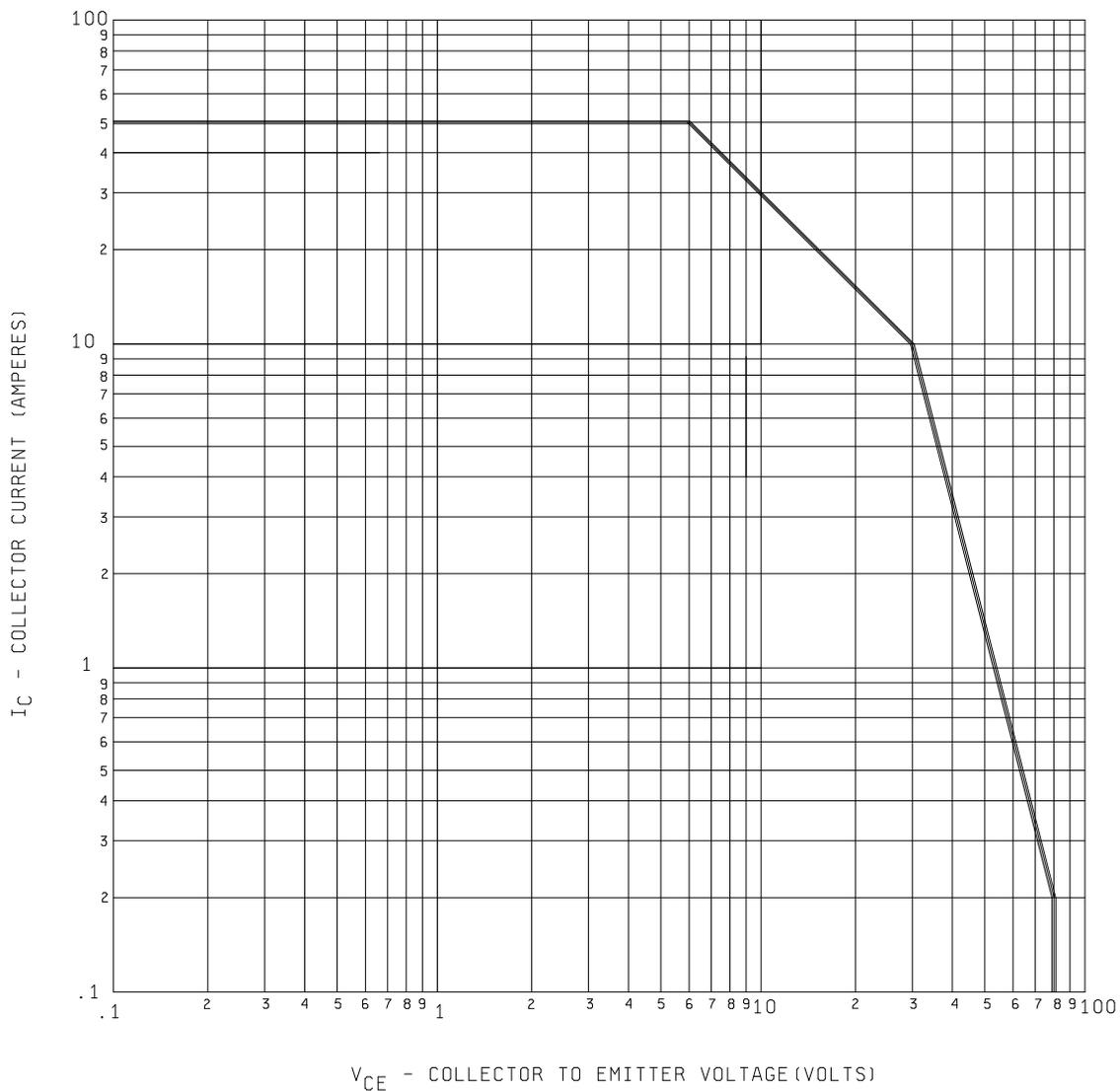


FIGURE 4. Maximum safe operating area graph continuous dc (2N5686).

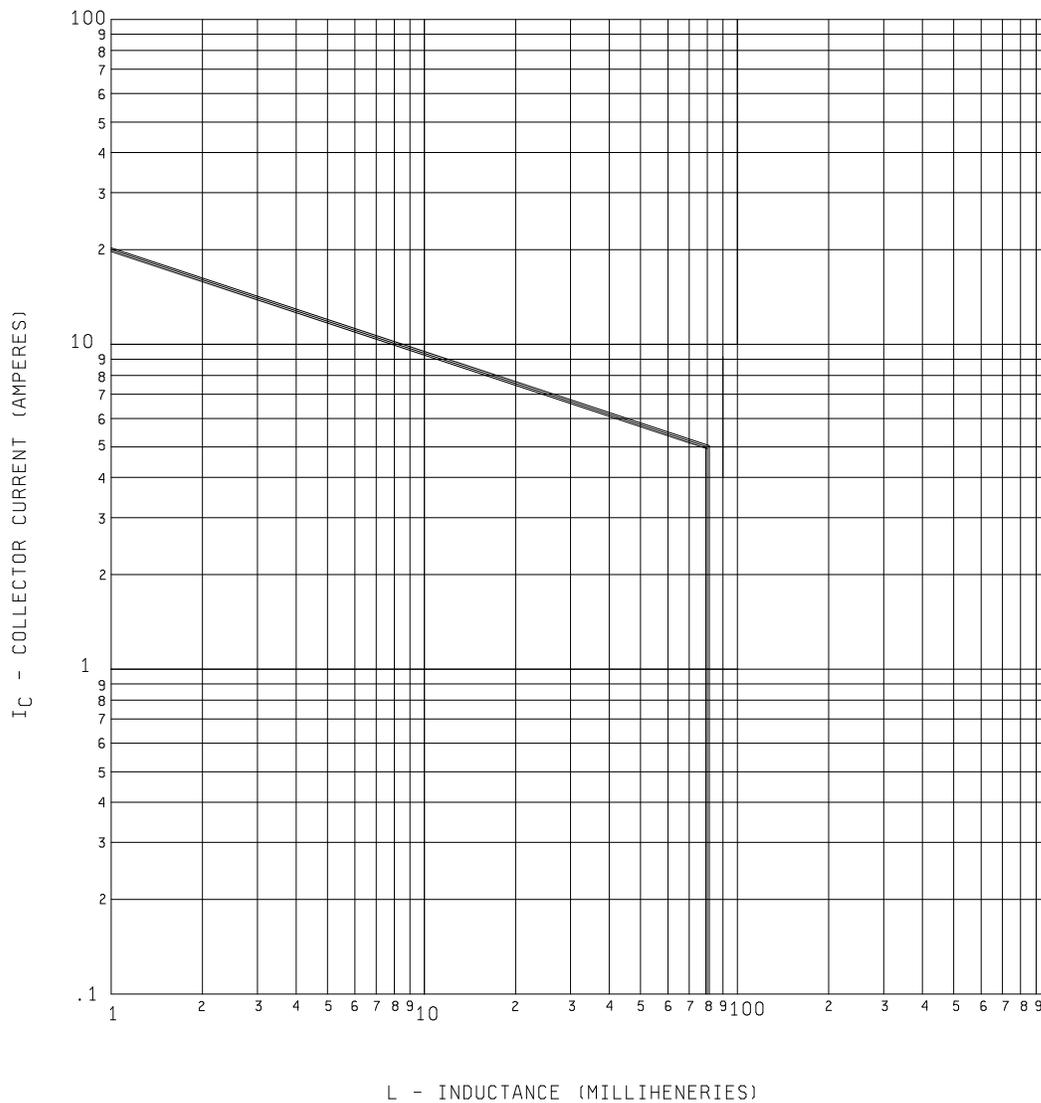
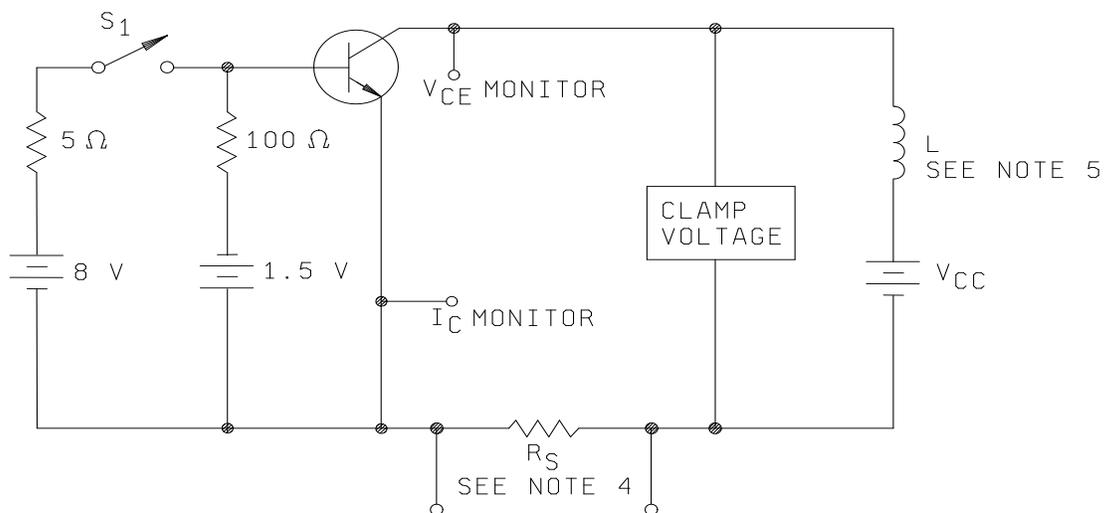


FIGURE 5. Safe operating area for switching between saturation and cutoff (unclamped inductive load).



Procedure:

1. With switch S₁ closed, set the specified test conditions.
2. Open S₁. Device fails if clamp voltage not reached.
3. Perform specified end-point tests.
4. R_S ≤ 0.1Ω, 12 W; 1percent tolerance maximum; (noninductive)
5. L = 2.0 mH (2 each 1 mH. Sanford Miller CK-50, 50 A). R = .002 Ω.

FIGURE 6. Clamp inductive sweep test circuit.

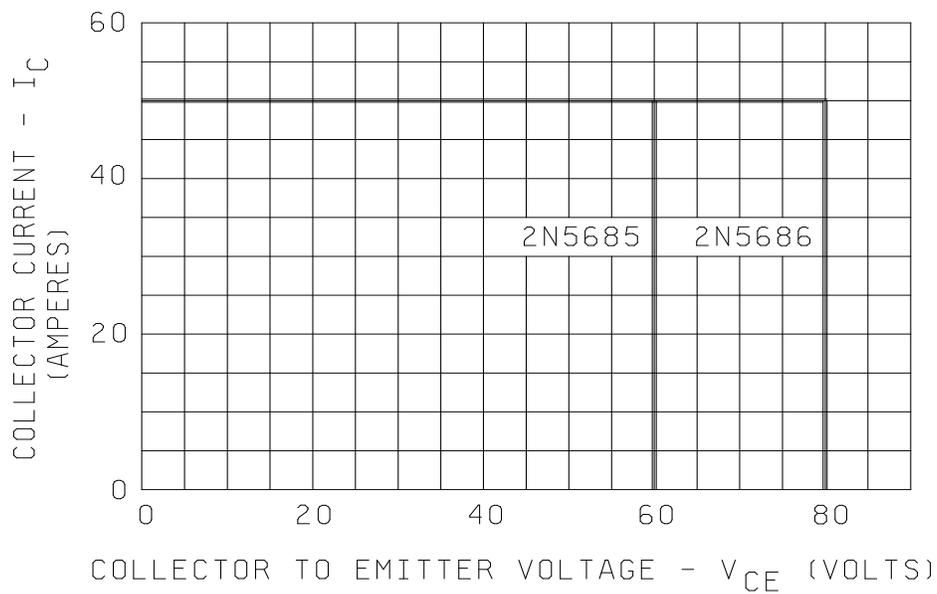


FIGURE 7. Safe operating area for switching between saturation and cutoff (clamped inductive load).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

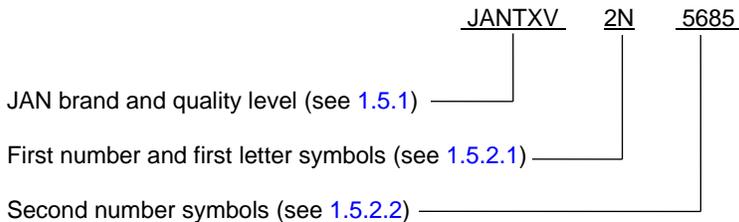
* 6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).

* d. The complete Part or Identifying Number (PIN), see 1.4 and 6.4.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

* 6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



* 6.5 List of PINs.

* 6.5.1 PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for types 2N5685	PINs for types 2N5686
JAN2N5685	JAN2N5686
JANTX2N5685	JANTX2N5686
JANTXV2N5685	JANTXV2N5686

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 85
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5961-2014-128)

Review activities:
 Army - AR, MI
 Air Force - 19, 70, 99

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.