The documentation and process conversion measures necessary to comply with this revision shall be completed by 10 February 2007.

INCH-POUND

MIL-PRF-19500/664B
10 November 2006
SUPERSEDING
MIL-PRF-19500/664A
5 November 2003

* PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED (TOTAL DOSE ONLY) TRANSISTORS, N-CHANNEL, SILICON, TYPES 2N7431U, 2N7432U, AND 2N7433U, JANTXVR, F, G, AND H; AND JANSR, F, G, AND H

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for an N-channel, enhancement-mode, MOSFET, radiation hardened (total dose only), power transistor. Two levels of product assurance are provided for each device type specified in MIL-PRF-19500, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). See 6.5 for JANHC and JANKC die versions.

1.2 Physical dimensions. See figure 1, SMD-2 (surface mount).

* 1.3 Maximum ratings. Unless otherwise specified, T_C = +25°C.

Type	P_T (1)	P_T T_A = +25°C (1)	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4)	I_{D2} T_C = +100°C (3)	I_S	I_{DM} (5)	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A(pk)	°C
2N7431U	300	2.5	0.42	60	60	±20	75.0	56.0	75.0	300	-55
2N7432U	300	2.5	0.42	100	100	±20	51.0	32.5	51.0	204	to
2N7433U	300	2.5	0.42	200	200	±20	43.0	27.0	43.0	172	+150

(1) Derate linearly by 2.4 W/°C for T_C > +25°C.
(2) See figure 2, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal construction.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(4) See figure 3, maximum drain current graph.
(5) I_{DM} = 4 X I_{D1} as calculated in note (3).

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil/.

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0 mA dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS}	Max $r_{DS(ON)}$ (1) V_{GS} = 12 V dc		E_{AS} at I_{D1}	I_{AS}
					T_J = +25°C at I_{D2}	T_J = +150°C at I_{D2}		
	V dc	V dc		µA dc	ohm	ohm	mJ	A
		Min	Max					
2N7431U	60	2.0	4.0	25	0.015	0.036	500	75.0
2N7432U	100	2.0	4.0	25	0.040	0.100	500	51.0
2N7433U	200	2.0	4.0	25	0.070	0.175	500	43.0

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

* DEPARTMENT OF DEFENSE SPECIFICATIONS

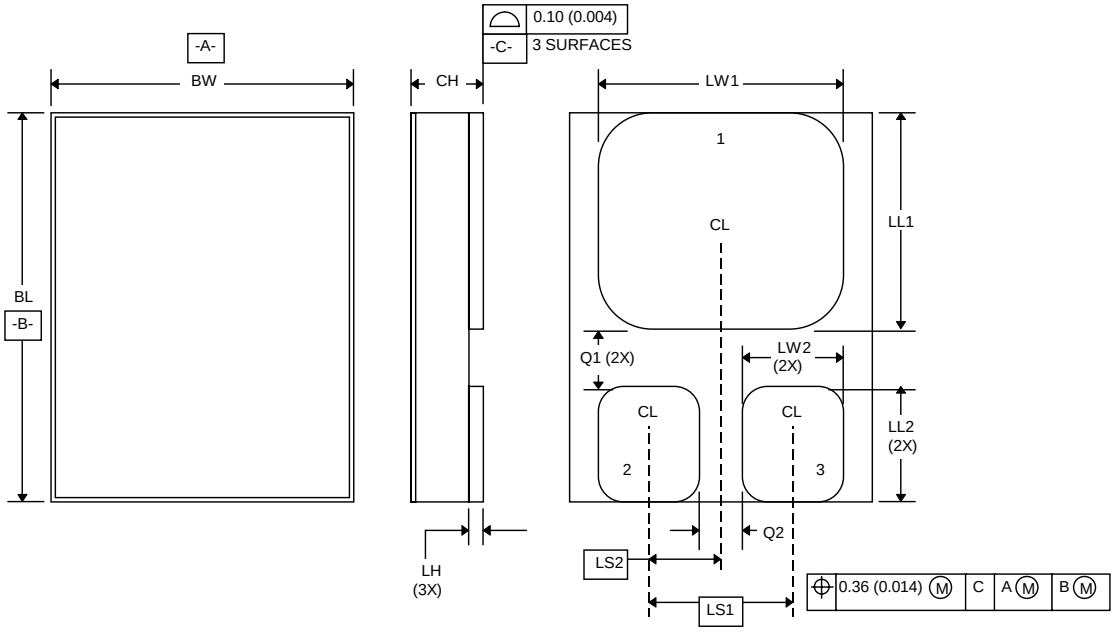
MIL-PRF-19500 - Semiconductor Devices, General Specification for.

* DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.684	.696	17.38	17.67
BW	.519	.531	13.19	13.48
CH		.142		3.60
LH	.010	.020	0.26	0.50
LW1	.434	.446	11.03	11.32
LW2	.134	.146	3.41	3.70
LL1	.469	.481	11.92	12.21
LL2	.151	.163	3.84	4.14
LS1	.240 BSC		6.10 BSC	
LS2	.120 BSC		3.05 BSC	
Q1	.035		0.89	
Q2	.050		1.27	
Term 1	Drain			
Term 2	Gate			
Term 3	Source			

Notes:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The lid shall be electrically isolated from the drain, gate and source.
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions for SMD-2 (surface mount package).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

I_{AS} ..... Rated avalanche current, nonrepetitive
nC ..... nano Coulomb.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 herein. Methods used for electrical isolation of the terminals shall employ materials that contain a minimum of 90 percent Al_2O_3 (ceramic).

3.4.1 Terminal material and finish. Terminal material shall be copper-tungsten. Terminal finish shall be solderable as defined in MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of terminal finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Internal construction. Multiple chip construction is not be permitted to meet the requirements of this specification.

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in paragraph 1.3, 1.4 and table I.

* 3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.7 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.7.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended.

a. Devices should be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq 100\ k\Omega$, whenever bias voltage is to be applied drain to source.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer , marking of the country of origin may be omitted from the body of the transistor but shall be retained on the initial container.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500.

* 4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV levels
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E_{AS} test (see 4.3.2)	Method 3470 of MIL-STD-750, E_{AS} test (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)
9	Subgroup 2 of table I herein. I_{DSS1}, I_{GSSF1}, I_{GSSR1},	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein. ΔI_{GSSF1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ± 10 μA dc or ± 100 percent of initial value, whichever is greater.	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein.
12	MIL-STD-750, method 1042, test condition A	MIL-STD-750, method 1042, test condition A
13	Subgroups 2 and 3 of table I herein. ΔI_{GSSF1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ± 10 μA dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ =± 20 percent of initial value $\Delta V_{GS(th)1}$ = ± 20 percent of initial value	Subgroups 2 and 3 of table I herein. ΔI_{GSSF1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ± 10 μA dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ =± 20 percent of initial value $\Delta V_{GS(th)1}$ = ± 20 percent of initial value

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1} and $V_{GS(th)1}$ shall be invoked.
(3) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 30 V minimum for t = 250 μs minimum.

4.3.2 Single pulse avalanche energy E_{AS}.

a. Peak current (I_{AS}) ..... $I_{AS} = I_{D1}$.

b. Peak gate voltage (V_{GS})..... 12 V.

c. Gate to source resistor (R_{GS})..... $25\Omega \leq R_{GS} \leq 200\Omega$.

d. Initial case temperature (T_C) ..... +25°C +10°C, -5°C.

e. Inductance..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right] \quad \left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right] \quad mH \text{ minimum}$

f. Number of pulses to be applied..... 1 pulse minimum.

g. Supply voltage (V_{DD}) ..... 25 V (50 V for 2N7433).

* 4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See table III, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. Alternate flow is allowed for quality conformance inspection in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and herein. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

* 4.4.2.1 Group B inspection, table E-VIA (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1051	Test condition G, 100 cycles.
B3	2075	See 3.4.2.
B3	2077	SEM qualification may be performed anytime prior to lot formation.
B4	1042	Intermittent operation life, condition D, 2000 cycles . No heat sink or forced air cooling on the device shall be permitted during the on cycle; t_{on} = 30 seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated, T_A = +175°C, t = 24 hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated, T_A = +175°C, t =120 hours minimum.
B5	2037	Bond strength; test condition A.

* 4.4.2.2 Group B inspection, table E-VIB (JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D, 2,000 cycles . No heat sink or forced air cooling on the device shall be permitted during the on cycle; t_{on} = 30 seconds minimum.
B3	2037	Test condition A.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable tests of table I, subgroup 2 herein.

	Subgroup	Method	Condition
	C2	2036	Not applicable.
*	C5	3161	Thermal resistance, see 4.3.3, $R_{\theta JC(max)}$ = 0.42°C/W.
	C6	1042	Intermittent operation life, condition D, 6,000 cycles . No heat sink or forced air cooling on the device shall be permitted during the on cycle; t_{on} = 30 seconds minimum.

4.4.4 Group D Inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

* TABLE I. Group A inspection.

	Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
	Subgroup 1						
	Visual and mechanical inspection	2071					
	Subgroup 2						
*	Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
	Breakdown voltage, drain to source	3407	V_{GS} = 0 V; I_D = 1 mA dc, bias condition C	$V_{(BR)DSS}$			
	2N7431U				60		V dc
	2N7432U				100		V dc
	2N7433U				200		V dc
	Gate to source voltage threshold	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)1}$	2.0	4.0	V dc
*	Gate current	3411	V_{GS} = +20 V dc, V_{DS} = 0	I_{GSSF1}		+ 100	nA dc
*	Gate current	3411	V_{GS} = -20 V dc V_{DS} = 0	I_{GSSR1}		-100	nA dc
	Drain current	3413	V_{GS} = 0 V dc, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS1}		25	µA dc
	Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)1}$			
	2N7431U					0.015	ohm
	2N7432U					0.040	ohm
	2N7433U					0.070	ohm
	Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A pulsed (see 4.5.1), $I_D = I_{D1}$	$r_{DS(on)2}$			
	2N7431U					0.018	ohm
	2N7432U					0.045	ohm
	2N7433U					0.077	ohm
	Forward voltage	4011	Pulsed (see 4.5.1), $I_D = I_{D1}$ V_{GS} = 0 V dc	V_{SD}			
	2N7431U					1.5	V dc
	2N7432U					1.8	V dc
	2N7433U					1.8	V dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 3						
High temperature operation:		$T_C = T_J = +125°C$				
Gate current	3411	V_{GS} = +20 and -20 V dc, bias condition C, V_{DS} = 0	I_{GSS2}		± 200	nA dc
Drain current	3413	V_{GS} = 0 V; bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		0.25	mA dc
Static drain to source On-state resistance	3421	V_{GS} = 12 V dc, pulsed (see 4.51), $I_D = I_{D2}$	$r_{DS(on)3}$			
2N7431U					0.030	ohm
2N7432U					0.085	ohm
2N7433U					0.140	ohm
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)2}$	1.0		V dc
Low temperature operation:		$T_C = T_J = +55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)3}$		5.0	V dc
Subgroup 4						
Forward transconductance	3475	I_D = rated I_{D2}, V_{DD} = 15 V (see 4.5.1)	g_{FS}			
2N7431U				18.0		S
2N7432U				16.0		S
2N7433U				9.0		S
Switching time test	3472	$I_D = I_{D1}$, V_{GS} = 12 V dc, R_G = 2.35Ω, V_{DD} = 50 percent of rated V_{DS}				
Turn-on delay time			$t_{d(on)}$			
2N7431U					27	ns
2N7432U					35	ns
2N7433U					50	ns
Rise time			t_r			
2N7431U					120	ns
2N7432U					150	ns
2N7433U					200	ns
Turn-off delay time			$t_{d(off)}$			
2N7431U					120	ns
2N7432U					150	ns
2N7433U					200	ns

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4 - Continued						
Fall time			t_f			
2N7431U					100	ns
2N7432U					130	ns
2N7433U					130	ns
Subgroup 5	3474					
Safe operating area test (high voltage)		See figures 4, 5, and 6, t_p = 10 ms minimum, V_{DS} = 80 percent of maximum rated V_{DS}, ($V_{DS} \leq 200$)				
Electrical measurements		See table I, subgroup 2				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B				
On-state gate charge			$Q_{g(on)}$			
2N7431U					270	nC
2N7432U					310	nC
2N7433U					290	nC
Gate to source charge			Q_{gs}			
2N7431U					60	nC
2N7432U					53	nC
2N7433U					42	nC
Gate to drain charge			Q_{gd}			
2N7431U					110	nC
2N7432U					110	nC
2N7433U					120	nC
Reverse recovery time	3473	di/dt ≤ 100 A/µs, $V_{DD} \leq 50$ V, $I_D = I_{D1}$	t_{rr}			
2N7431U					360	ns
2N7432U					520	ns
2N7433U					820	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ This test required for the following end-point measurements only:
Group B, subgroups 2 and 3 (JANTXV).
Group B, subgroups 3 and 4 (JANS).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection 1/ 2/	MIL-STD-750		Symbol	Preirradiation limits				Postirradiation limits				Unit
	Method	Conditions		R		F, G and H 3/		R		F, G and H 3/		
				Min	Max	Min	Max	Min	Max	Min	Max	
Subgroup 1												
Not applicable												
Subgroup 2		T_C = +25°C										
Steady-state total dose irradiation (V_{GS} bias) 4/	1019	V_{GS} = 12V, V_{DS} = 0										
Steady-state total dose irradiation (V_{DS} bias) 4/	1019	V_{DS} = 80 percent of rated V_{DS} (pre-irradiation), VGS = 0										
Pre and post electricals												
Breakdown voltage, drain to source	3407	V_{GS} = 0, I_D = 1 mA, bias cond. C	V_{BRDSS}									
2N7431U				60		60		60		60		V dc
2N7432U				100		100		100		100		V dc
2N7433U				200		200		200		200		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	$V_{GS(th)1}$									
2N7431U				2.0	4.0	2.0	4.0	2.0	4.0	1.25	4.5	V dc
2N7432U				2.0	4.0	2.0	4.0	2.0	4.0	1.25	4.5	V dc
2N7433U				2.0	4.0	2.0	4.0	2.0	4.0	1.25	4.5	V dc
Gate current	3411	V_{GS} = 20 V, V_{DS} = 0 bias cond. C	I_{GSSF1}		100		100		100		100	nA dc
Gate current	3411	V_{GS} = -20 V, V_{DS} = 0, bias cond. C	I_{GSSR1}		-100		-100		-100		-100	nA dc
Drain current	3413	V_{GS} = 0, bias cond. C, V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)	I_{DSS1}		25		25		25		50	µA dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

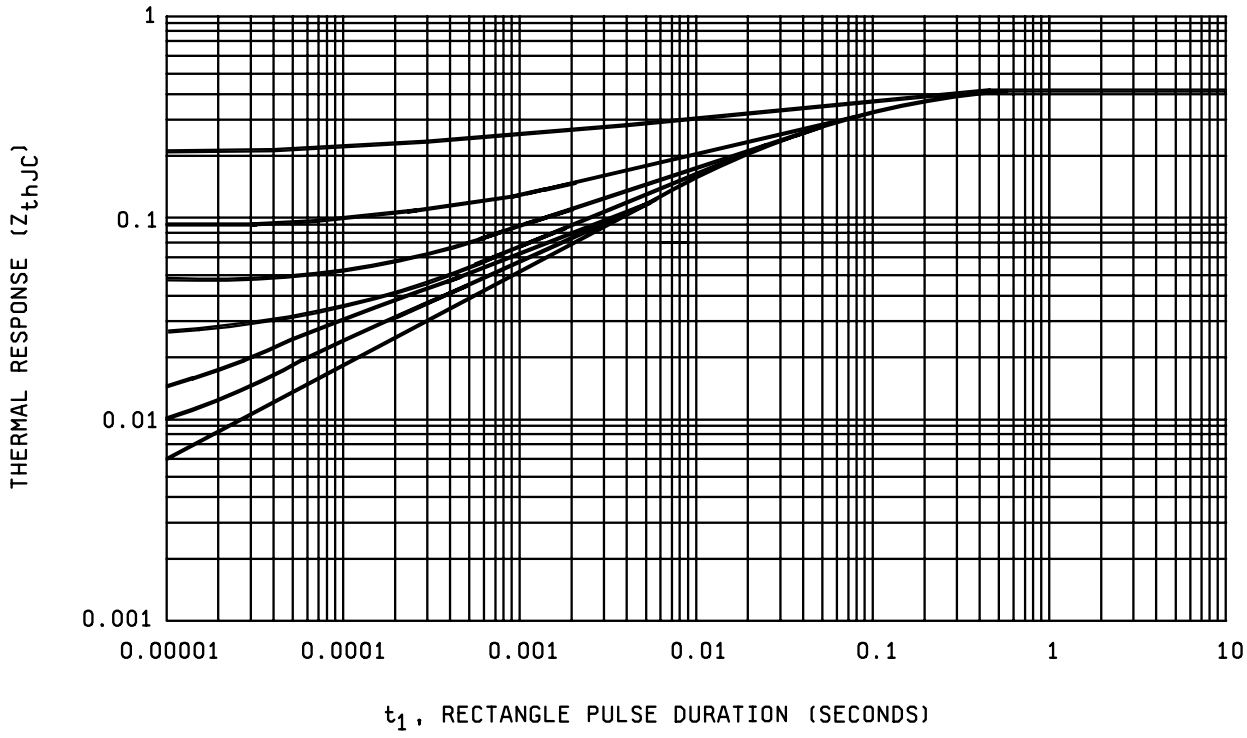
Inspection 1/ 2/	MIL-STD-750		Symbol	Preirradiation limits				Postirradiation limits				Unit
	Method	Conditions		R		F, G and H 3/		R		F, G and H 3/		
				Min	Max	Min	Max	Min	Max	Min	Max	
Static drain to source on-state voltage	3405	V_{GS} = 12 V, cond. A, pulsed (see 4.5.1), $I_D = I_{D2}$	$V_{DS(on)1}$									
2N7431U					0.840		0.840		0.840		1.400	V dc
2N7432U					1.300		1.300		1.300		1.852	V dc
2N7433U					1.890		1.890		1.890		2.970	V dc
Forward voltage source to drain diode	4011	V_{GS} = 0, $I_D = I_{D1}$	V_{SD}									
2N7431U					1.5		1.5		1.5		1.5	V dc
2N7432U					1.8		1.8		1.8		1.8	V dc
2N7433U					1.8		1.8		1.8		1.8	V dc

1/ For sampling plan, see MIL-PRF-19500.
2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D, QCI requirements may be used for any other specification utilizing the same die design.
3/ The H designation represent devices which pass end-points at 100k and 300k Rads (Si). The G designation represents devices which pass 100k, 300k and 600k Rads (Si) end-points. H must meet end-points for 100k, 300k, 600k and 1000k Rads (Si).
4/ Separate samples shall be pulled for each bias.
5/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

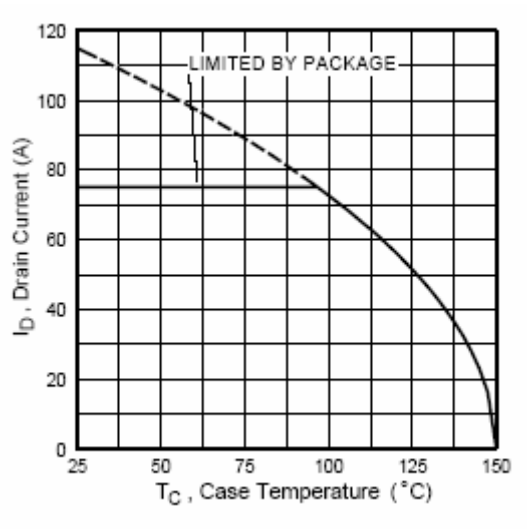
* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2.	
Subgroup 2 1/			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		See table I, subgroup 2.	
Steady-state gate bias	1042	Condition B, 1,000 hours.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 6			3 devices
ESD	1020	Not required for devices classified as ESD class 1.	
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	

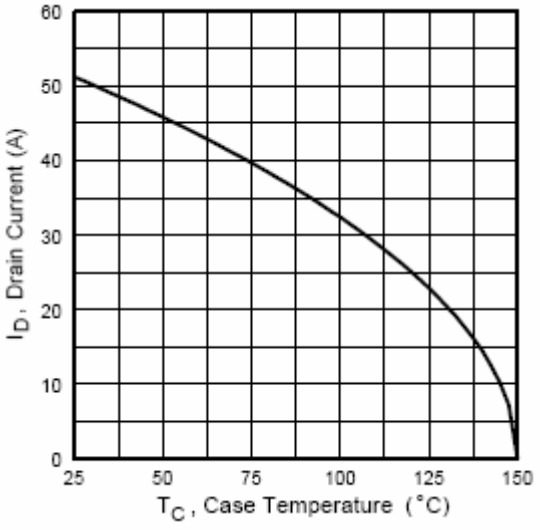
1/ A separate sample may be pulled for each test condition.



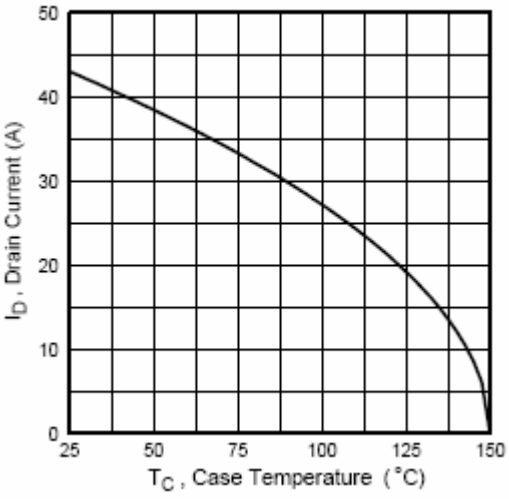
* FIGURE 2. Thermal impedance curve.



2N7431U

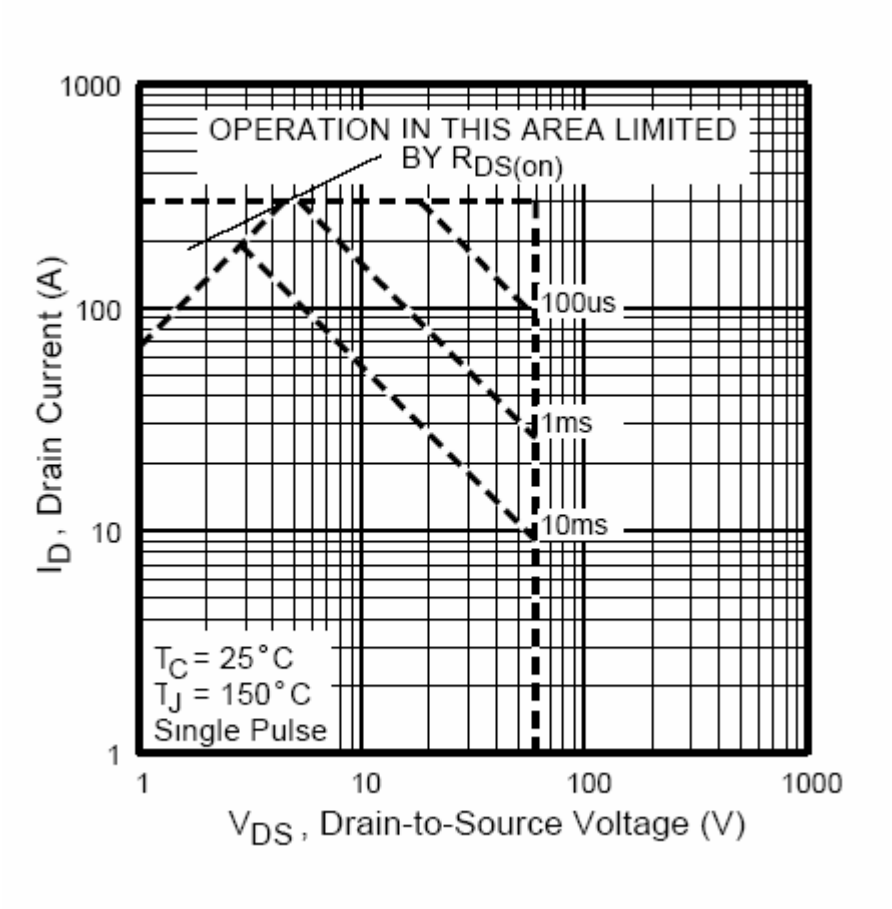


2N7432U



2N7433U

* FIGURE 3. Maximum drain current vs case temperature graphs.



* FIGURE 4. Safe operating area graph for 2N7431U.

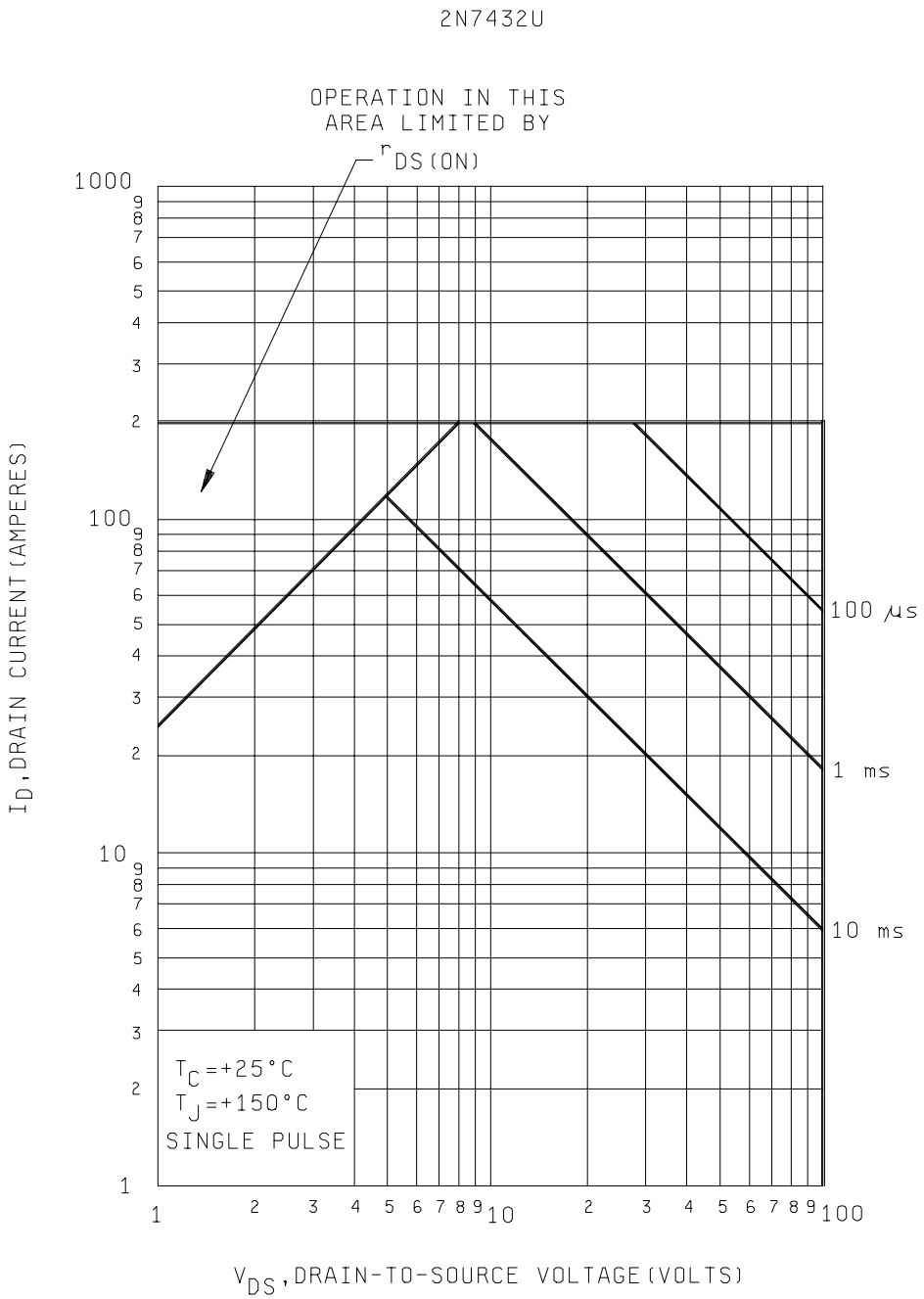


FIGURE 5. Safe operating area graph for 2N7432U.

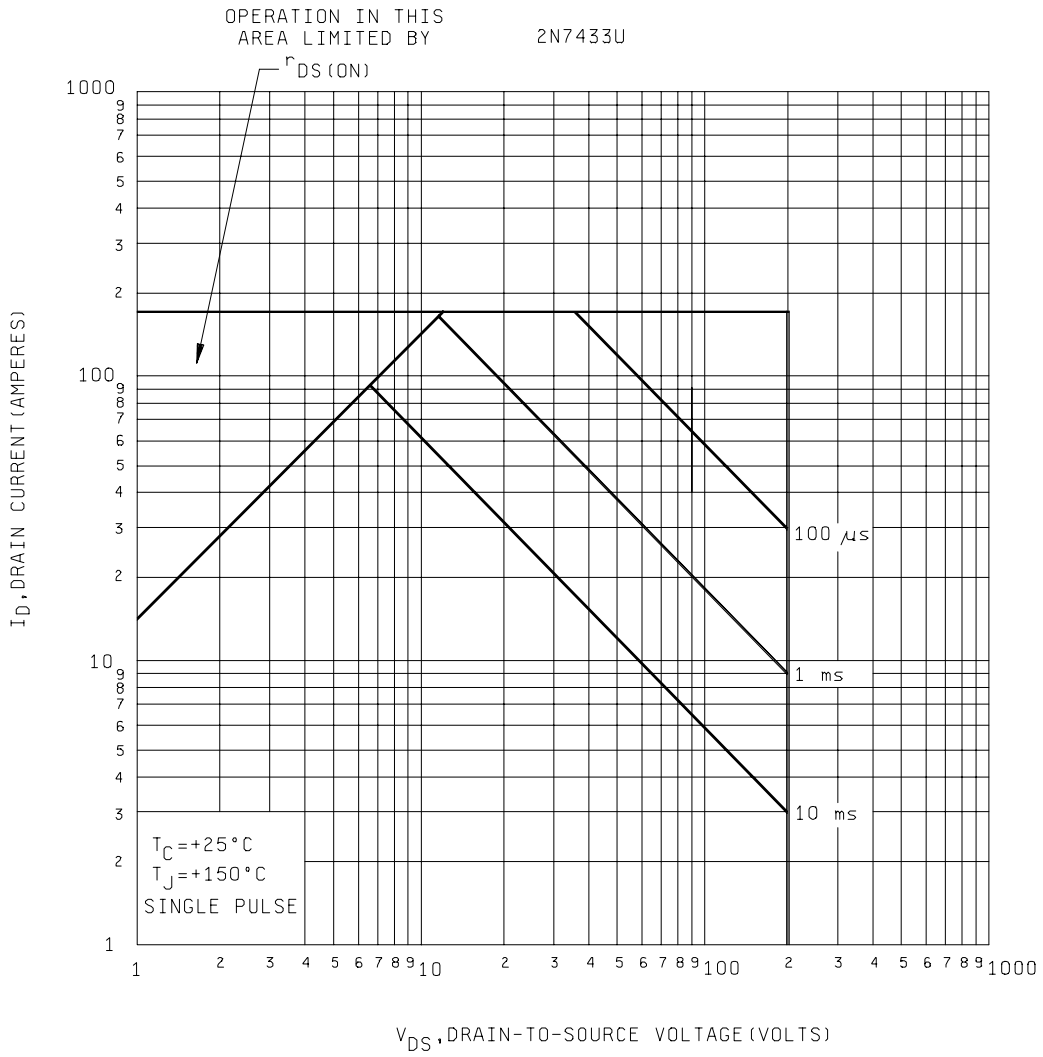


FIGURE 6. Safe operating area graph for 2N7433U.

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types Military PIN	Commercial PIN (1)
2N7431U 2N7432U 2N7433U	IRHNA_064 IRHNA_160 IRHNA_260

(1) IRHNA7: 100k RAD (Si)
IRHNA3: 300k RAD (Si)
IRHNA4: 600k RAD (Si)
IRHNA8: 1000k RAD (Si)

* 6.5 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/657.

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2006-063)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil/ .