

The documentation and process conversion measures necessary to comply with this document shall be completed by 20 November 2005.

INCH-POUND

MIL-PRF-19500/354J
 20 August 2005
 SUPERSEDING
 MIL-PRF-19500/354H
 5 March 2002

* PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, PNP, SILICON, LOW-POWER,
 TYPES 2N2604, 2N2604UB, 2N2605, AND 2N2605UB,
 JAN, JANTX, JANTXV, AND JANS, JANHC, JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP, silicon, low-power transistors for use in low noise level amplifier applications. Four levels of product assurance are provided for each encapsulated device type and two levels for each unencapsulated device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1 (TO-46), figure 2 (UB), and figures 3 and 4 die.

* 1.3 Maximum ratings unless otherwise specified, T_A = +25°C.

Types	V _{CBO}	V _{EBO}	V _{CEO}	I _c	T _J and T _{STG}
	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>mA dc</u>	<u>°C</u>
2N2604, UB	80	6	60	30	-65 to +200
2N2605, UB	70	6	60	30	-65 to +200

Type	P _T (1) T _A = +25°C	P _T (1) T _C = +25°C	P _T (1) T _{SP} = +25°C	R _{θJA} (2)	R _{θJC} (2)	R _{θJSP} (2)
	<u>mW</u>	<u>mW</u>	<u>mW</u>	<u>°C/W</u>	<u>°C/W</u>	<u>°C/W</u>
2N2604	400	400	N/A	437	175	N/A
2N2604UB	400	N/A	360	275	N/A	100
2N2605	400	400	N/A	437	175	N/A
2N2605UB	400	N/A	360	275	N/A	100

(1) For derating, see figures 5, 6, 7, and 8.

(2) For thermal impedance curves see figures 9, 10, 11, and 12.

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dsc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil>.

1.4 Primary electrical characteristics.

	h_{FE1}		h_{fe}		$ h_{fe} $	C_{obo}	$V_{BE(sat)}$	$V_{CE(sat)}$
	$V_{CE}=5\text{ V dc}$ $I_C=10\text{ }\mu\text{ dc}$		$V_{CE}=5\text{ V dc}$ $I_C=1\text{ mA dc}$ $f=1\text{ kHz}$		$V_{CE}=5\text{ V dc}$ $I_C=500\text{ }\mu\text{A dc}$ $f=30\text{ MHz}$	$V_{CB}=5\text{ V dc}$ $I_E=0$ $100\text{ kHz} \leq f \leq 1\text{ MHz}$	$I_C=10\text{ mA dc}$ $I_B=500\text{ }\mu\text{A dc}$	$I_C=10\text{ mA dc}$ $I_B=500\text{ }\mu\text{A dc}$
	<u>2N2604</u>	<u>2N2605</u>	<u>2N2604</u>	<u>2N2605</u>		<u>pF</u>	<u>V dc</u>	<u>V dc</u>
Min	40	100	60	150	1		0.7	
Max	120	300	180	450	8	6	0.9	0.3

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

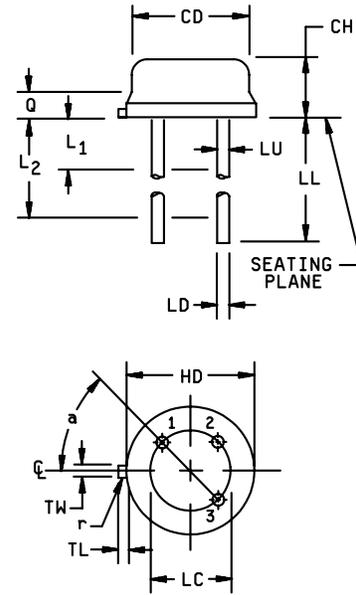
2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

* 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.065	.085	1.65	2.16	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		5
LD	.016	.021	0.41	0.53	6
LL	.500	1.750	12.70	44.45	6
LU	.016	.019	0.41	0.48	6
L1		.050		1.27	6
L2	.250		6.35		6
Q		.040		1.02	4
TL	.028	.048	0.71	1.22	3, 8
TW	.036	.046	0.91	1.17	3, 8
r		.010		0.25	9
α	45° TP		45° TP		5

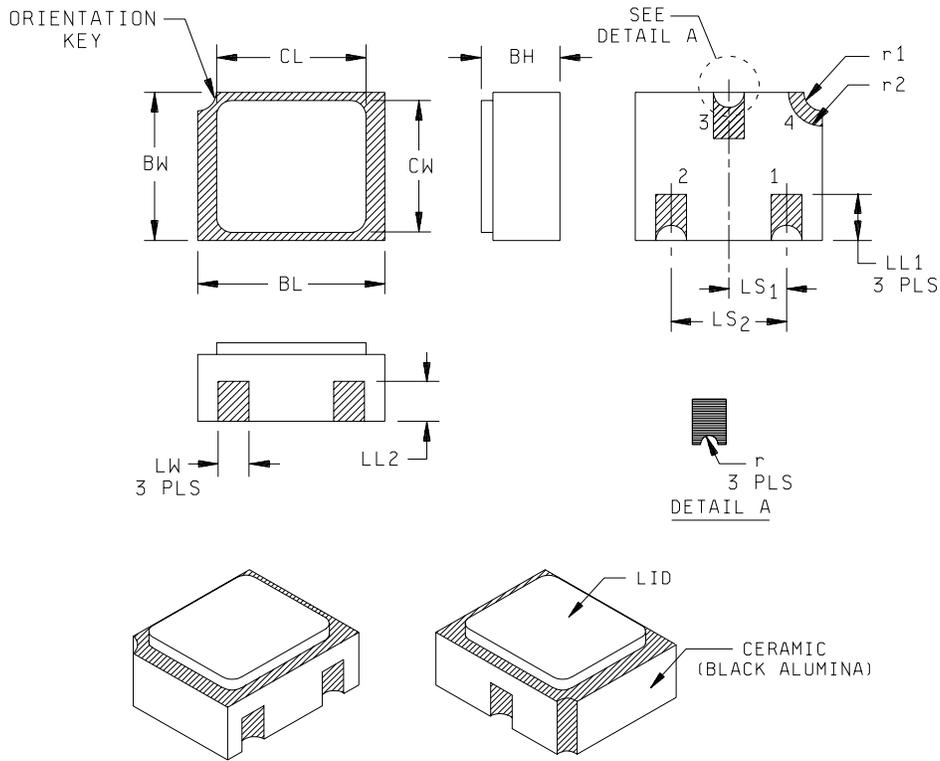


NOTES:

1. Dimensions are in inches. Lead 1 is emitter, lead 2 is base, and lead 3 is collector.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Leads at gauge plane $.054 +.001 -.000$ inch ($1.37 +0.03 -0.00$ mm) below seating plane shall be within $.007$ inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by the gauge and gauging procedure.
6. Symbol LU applies between L_1 and L_2 . Dimension LD applies between L_2 and LL minimum.
7. Lead number three is electrically connected to case.
8. Beyond r maximum, TW shall be held for a minimum length of $.011$ inch (0.28 mm).
9. Symbol r applied to both inside corners of tab.
10. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions – (TO-46).

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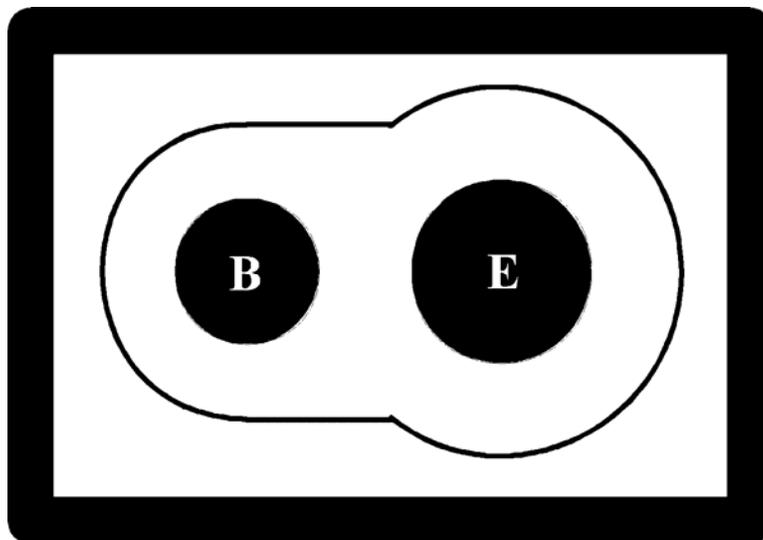


Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.96	
LL2	.017	.035	0.43	0.89	
LS1	.036	.040	0.91	1.02	
LS2	.071	.079	1.81	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r1		.012		.305	
r2		.022		.559	

NOTES:

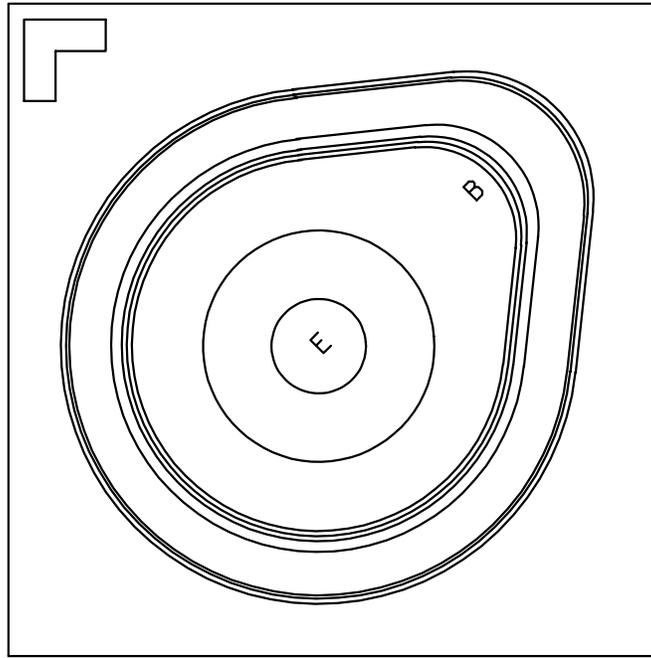
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 2. Physical dimensions, surface mount (UB version).



- | | |
|-------------------|---|
| 1. Chip size | .015 x .019 inch \pm .001 inch, (0.381 x 0.483 \pm 0.0254 mm). |
| 2. Chip thickness | .010 \pm .0015 inch, (0.254 \pm 0.381). |
| 3. Top metal | Aluminum 15,000Å minimum, 18,000Å nominal. |
| 4. Back metal | A. Gold 2,500Å minimum, 3,000Å nominal.
B. Eutectic Mount - No Gold. |
| 5. Backside | Collector. |
| 6. Bonding pad | B = .003 inch, (0.076 mm), E = .004 inch, (0.102 mm) diameter. |
| 7. Passivation | Si ₃ N ₄ (Silicon Nitride) 2kÅ min, 2.2kÅ nom. |

FIGURE 3. JANHC and JANKC A-version die dimensions.



Die size:	.018 x .018 inch (0.457 x 0.457 mm).
Die thickness:	.008 ±.0016 inch (0.203 ±0.0406 mm).
Base pad:	.0025 inch (0.0635 mm) diameter.
Emitter pad:	.003 inch (0.076 mm) diameter.
Back metal:	Gold, 6500 ±1950 Ang.
Top metal:	Aluminum, 19500 ±2500 Ang.
Back side:	Collector.
Glassivation:	SiO ₂ , 7500 ±1500 Ang.

FIGURE 4. JANHC and JANKC B-version die dimensions.

* 3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

$R_{\theta JA}$	Thermal resistance junction to ambient.
$R_{\theta JC}$	Thermal resistance junction to case.
$R_{\theta JSP}$	Thermal resistance junction to solder pads.
T_{SP}	Temperature of solder pads.
UB	Surface mount case outline (see figure 2).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 (TO-46), figure 2 (UB), and on figures 3 and 4 die.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

* 4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance (response) method 3131 of MIL-STD-750.	Thermal impedance (response) method 3131 of MIL-STD-750.
7	Optional	Optional
9	I_{CBO1} and h_{FE2}	Not applicable
10	24 hours minimum	24 hours minimum
11	I_{CBO1} ; h_{FE2} ; $\Delta I_{CBO1} = 100$ percent or 2 nA dc, whichever is greater; $\Delta h_{FE2} = \pm 15$ percent change of initial value.	I_{CBO1} and h_{FE2}
12	See 4.3.1	See 4.3.1
13	Subgroups 2 and 3 of table I herein; $\Delta I_{CBO1} = 100$ percent or 2 nA dc, whichever is greater; $\Delta h_{FE2} = \pm 15$ percent change of initial value.	Subgroup 2 of table I herein; $\Delta I_{CBO1} = 100$ percent or 2 nA dc, whichever is greater; $\Delta h_{FE2} = \pm 25$ percent change of initial value.
14	Required	Required

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

* 4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: $V_{CB} = 10 - 30$ V dc. Power shall be applied to achieve $T_J = +135^\circ\text{C}$ minimum using a minimum $P_D = 75$ percent of P_T maximum, T_A ambient rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J , and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.3.2 Screening (JANHNC and JANKC). Screening of JANHNC and JANKC die shall be in accordance with MIL-PRF-19500, "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHNC follows JANTX requirements.

4.3.3 Thermal response (ΔV_{BE} measurements). The ΔV_{BE} measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining V_H , V_{CE} , I_M , I_H , t_H , and t_{MD} . The ΔV_{BE} limit used in screen 3c of 4.3 herein and table I, subgroup 2 shall be set statistically by the supplier over several die lots and submitted to the qualifying activity for approval.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table VIa (JANS) of MIL-PRF-19500 and 4.4.2.1 herein. Electrical measurements (end-points) and delta requirements shall be in accordance with group A, subgroup 2 and 4.5.3 herein, delta requirements only apply to subgroups B4, and B5. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 herein and shall be in accordance with group A, subgroup 2 and 4.5.3 herein.

4.4.2.1 Group B inspection (JANS), table VIa of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
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B4	1037	$V_{CB} = 10 \text{ V dc}$, 2,000 cycles, adjust device current, or power, to achieve a minimum ΔT_J of $+100^\circ\text{C}$.
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B5	1027	$V_{CB} = 10 \text{ V dc}$; $P_D \geq 100$ percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.)
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Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table VIa, adjust T_A or P_D to achieve $T_J = +275^\circ\text{C}$ minimum.

Option 2: 216 hours minimum, sample size = 45, $c = 0$; adjust T_A or P_D to achieve a $T_J = +225^\circ\text{C}$ minimum.

* 4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
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1	1026	Steady-state life: 1,000 hours minimum, $V_{CB} = 10 \text{ V dc}$, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75$ percent of maximum rated P_T as defined in 1.3. $n = 45$ devices, $c = 0$. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
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2	1048	Blocking life, $T_A = +150^\circ\text{C}$, $V_{CB} = 80$ percent of rated voltage, 48 hours minimum. $n = 45$ devices, $c = 0$.
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3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$. $n = 22$, $c = 0$.
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4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.
- b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.3 herein; delta requirements only apply to subgroup C6.

* 4.4.3.1 Group C inspection (JANS), table VII of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E; (not applicable for UB devices).
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and applied thermal impedance curves.
C6	1026	1,000 hours at $V_{CB} = 10$ V dc; power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum and a minimum of $P_D = 75$ percent of maximum rated P_T as defined in 1.3 $n = 45$, $c = 0$. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

* 4.4.3.2 Group C inspection (JAN, JANTX, and JANTXV), table VII of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E; not applicable for UB devices.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3).
C6		Not applicable.

* 4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein; delta measurements shall be in accordance with the applicable steps of 4.5.3.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Noise figure. The noise figure shall be measured using commercially available test equipment and its associated standard test procedures.

4.5.3 Delta requirements. Delta requirements shall be as specified below:

Step	Inspection	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1	Collector-base cutoff current	3036	Bias condition D, $V_{CB} = 50 \text{ V dc}$	ΔI_{CB01} (1)	100 percent of initial value or 5 nA dc, whichever is greater.	
2	Forward current transfer ratio	3076	$V_{CE} = 5 \text{ V dc};$ $I_C = 500 \text{ uA dc};$ pulsed see 4.5.1	Δh_{FE2} (1)	± 25 percent change from initial reading.	

(1) Devices which exceed the table I limits for this test shall not be accepted.

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* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
Visual and mechanical examination <u>3/</u>	2071	n = 45 devices, c = 0				
Solderability <u>3/ 4/</u>	2026	n = 15 leads, c = 0				
Resistance to solvents <u>3/ 4/ 5/</u>	1022	n = 15 devices, c = 0				
Electrical measurements <u>4/</u>		Table I, subgroup 2				
Temp cycling <u>3/ 4/</u>	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal <u>4/ 6/</u> Fine leak Gross leak	1071	n = 22 devices, c = 0				
Bond strength <u>3/ 4/</u>	2037	Precondition T _A = +250°C at t = 24 hours or T _A = +300°C at t = 2 hours, n = 11 wires, c = 0				
Decap internal visual (design verification) <u>4/</u>	2075	n = 4 devices, c = 0				
<u>Subgroup 2</u>						
Thermal impedance	3131	See 4.3.3	ΔV_{BE}			mV
Collector to base cutoff current 2N2604 2N2605	3036	Condition D. V _{CB} = 80 V dc V _{CB} = 70 V dc	I _{CBO2}		10 10	μ A dc μ A dc
Collector - emitter breakdown voltage	3011	Bias condition D; I _C = 10 mA dc; pulsed (see 4.5.1)	V _{(BR)CEO}	60		V dc
Emitter - base cutoff current	3061	Bias condition D; V _{EB} = 6 V dc	I _{EBO2}		10	μ A dc
Collector - base cutoff current	3036	Bias condition D; V _{CB} = 50 V dc	I _{CBO1}		10	NA dc
Emitter - base cutoff current	3061	Bias condition D; V _{EB} = 5 V dc	I _{EBO}		2	NA dc
Collector - emitter cutoff current	3041	Bias condition C; V _{CE} = 50 V dc	I _{CES}		10	nA dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2 - Continued.</u>						
Forward current transfer ratio 2N2604 2N2605	3076	$V_{CE} = 5 \text{ V dc}; I_C = 10 \text{ } \mu\text{A dc}$	h_{FE1}	40 100	120 300	
Forward current transfer ratio 2N2604 2N2605	3076	$V_{CE} = 5 \text{ V dc}; I_C = 500 \text{ } \mu\text{A dc}$	h_{FE2}	60 150	180 450	
Forward current transfer ratio 2N2604 2N2605	3076	$V_{CE} = 5 \text{ V dc}; I_C = 10 \text{ mA dc}$	h_{FE3}	40 100	160 400	
Base - emitter voltage (saturated)	3066	Test condition A; $I_C = 10 \text{ mA dc};$ $I_B = 500 \text{ } \mu\text{A dc}$	$V_{BE(sat)}$	0.7	0.9	V dc
Collector - emitter voltage (saturated)	3071	$I_C = 10 \text{ mA dc};$ $I_B = 500 \text{ } \mu\text{A dc}$	$V_{CE(sat)}$		0.3	V dc
<u>Subgroup 3</u>						
High-temperature operation:		$T_A = +150^\circ\text{C}$				
Collector - base cutoff current	3036	Bias condition D; $V_{CB} = 50 \text{ V dc}$	I_{CBO2}		5	$\mu\text{A dc}$
Low-temperature operation:		$T_A = -55^\circ\text{C}$				
Forward current transfer ratio 2N2604 2N2605	3076	$V_{CE} = 5 \text{ V dc};$ $I_C = 10 \text{ } \mu\text{A dc}$	h_{FE4}	15 30		
<u>Subgroup 4</u>						
Small-signal short-circuit input impedance 2N2604 2N2605	3201	$V_{CE} = 5 \text{ V dc};$ $I_C = 1 \text{ mA dc}; f = 1 \text{ kHz}$	h_{ie}	1 2	10 20	$k\Omega$ $k\Omega$
Small-signal open-circuit reverse-voltage transfer ratio	3211	$V_{CE} = 5 \text{ V dc};$ $I_C = 1 \text{ mA dc};$ $f = 1 \text{ kHz}$	h_{re}		10×10^{-4}	

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4 - Continued.</u>						
Small-signal open-circuit output admittance 2N2604 2N2605	3216	$V_{CE} = 5 \text{ V dc};$ $I_C = 1 \text{ mA dc}; f = 1 \text{ kHz}$	h_{oe}		40 60	μmhos μmhos
Small-signal short-circuit forward-current transfer ratio 2N2604 2N2605	3206	$V_{CE} = 5 \text{ V dc};$ $I_C = 1 \text{ mA dc}; f = 1 \text{ kHz}$	h_{fe}	60 150	180 450	
Magnitude of common emitter small-signal short-circuit forward-current transfer ratio	3306	$V_{CE} = 5 \text{ V dc};$ $I_C = 0.5 \text{ mA dc};$ $f = 30 \text{ MHz}$	$ h_{fe} $	1	8	
Open circuit output capacitance	3236	$V_{CB} = 5 \text{ V dc}; I_E = 0;$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{obo}		6	PF
Noise figure	3246	$V_{CE} = 5 \text{ V dc}; I_C = 10 \mu\text{A dc};$ $R_g = 10 \text{ k}\Omega; f = 100 \text{ Hz}$	F_1		5	dB
Noise figure	3246	$V_{CE} = 5 \text{ V dc}; I_C = 10 \mu\text{A dc};$ $R_g = 10 \text{ k}\Omega; f = 1 \text{ kHz}$	F_2		3	dB
Noise figure	3246	$V_{CE} = 5 \text{ V dc}; I_C = 10 \mu\text{A dc};$ $R_g = 10 \text{ k}\Omega; f = 10 \text{ kHz}$	F_3		3	dB

1/ For sampling plan see MIL-PRF-19500.

2/ For resubmission of failed test in subgroup 1 of table I, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

4/ Not required for JANS devices.

5/ Not required for laser marked devices.

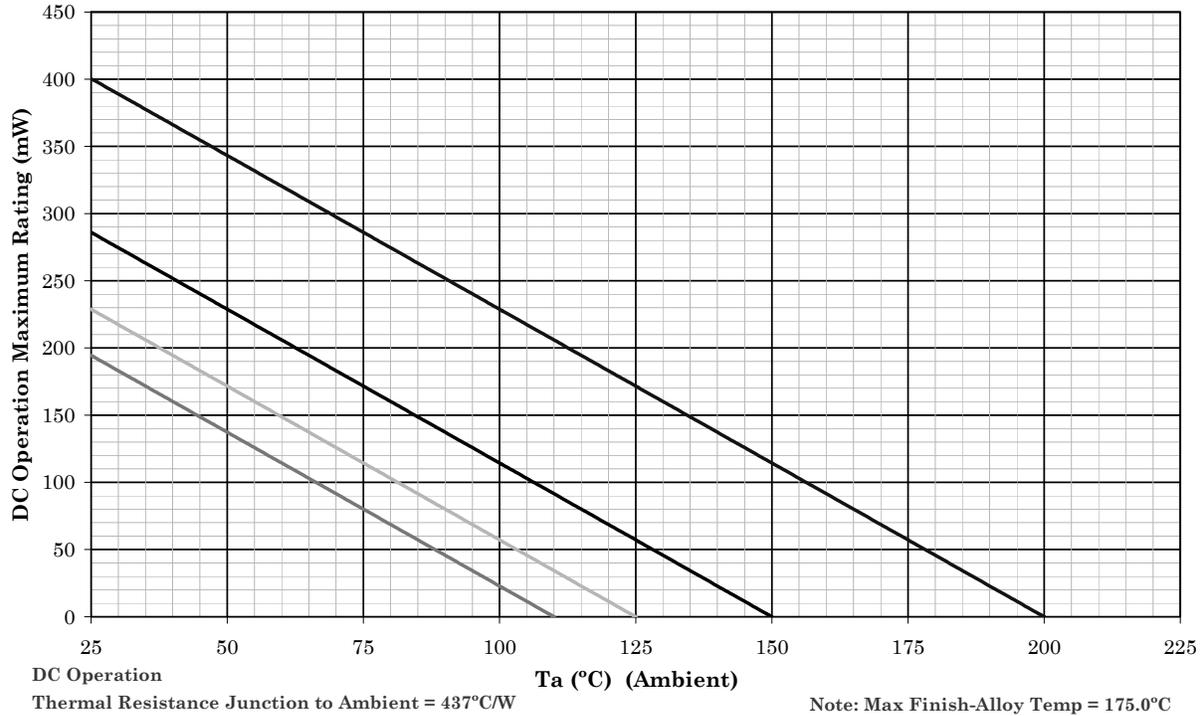
6/ This hermetic seal test is an end-point to temp-cycling in addition to electrical measurements.

* TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and 4.5.3 herein.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	Intermittent operation life: $V_{CB} = 10$ V dc, 6,000 cycles, adjust device current, or power, to achieve a minimum ΔT_j of $+100^\circ\text{C}$.	
Electrical measurements		See table I, subgroup 2 and 4.5.3 herein.	
<u>Subgroup 4</u>			
Thermal resistance	3131	$R_{\theta JS}$ need be calculated only.	15 devices, c = 0
Thermal response curves		The term "thermal response" is used here instead of "thermal impedance" because the active area is too small to be able to measure true thermal impedance accurately but is still useful for screening of die bond quality. ΔV_{BE} shall be recorded and conversion to $Z_{\theta JX}$ shall be made mathematically for the thermal impedance curves using the appropriate K-Factor. A histogram of thermal response (use $Z_{\theta JX}$ format) is required on 116 devices using the supplier proposed optimal test conditions and thermal response limit. The approved thermal response conditions and limit for $Z_{\theta JX}$ shall be used by the supplier in screening and for endpoint measurements as applicable. The approved thermal response conditions for $Z_{\theta JX}$ shall be used by the supplier for all conformance inspection. Each supplier shall submit a thermal response (using $Z_{\theta JX}$) log-log plot using the best device, the worst device and average device from the 116 devices histogram. These three thermal response plots will all reside on a single log-log graph and will extend from DC steady state down to at least 1ms of heating pulse time (equipment permitting).	Sample size N/A
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 6</u>			3 devices
Electrostatic discharge (ESD)	1020	Testing is not required for class 3 listing. Testing is required for a nonsensitive listing to prove capability.	
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition B.	

Temperature-Power Derating Curve

2N2604, 2N2605



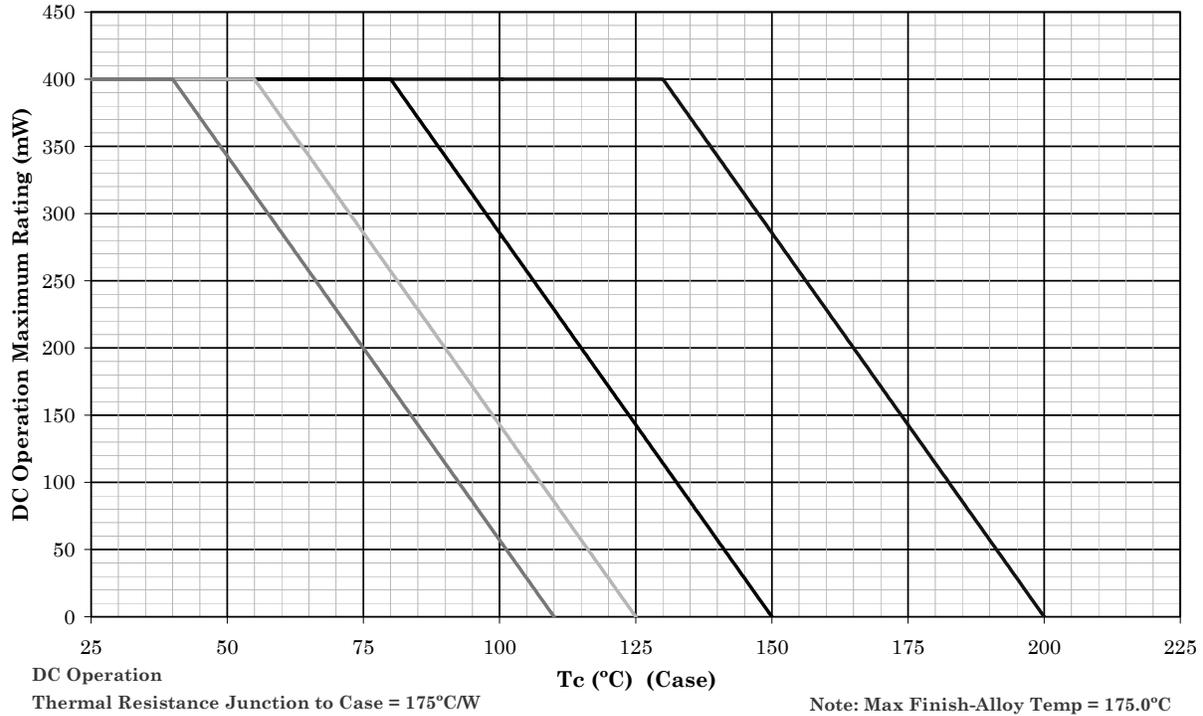
NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 5. Temperature-power derating for 2N2604 and 2N2605 (TO-46 package).

Temperature-Power Derating Curve

2N2604, 2N2605



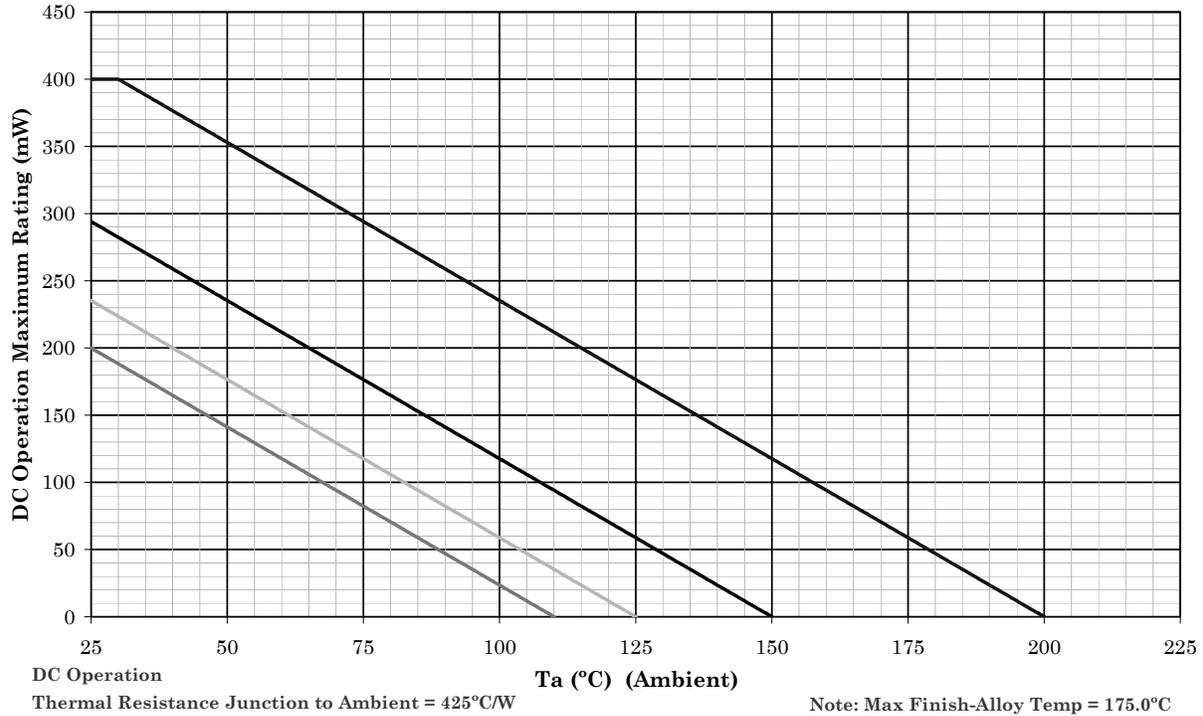
NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 6. Temperature-power derating for 2N2604 and 2N2605 (TO-46 package case mounted).

Temperature-Power Derating Curve

2N2604UB, 2N2605UB



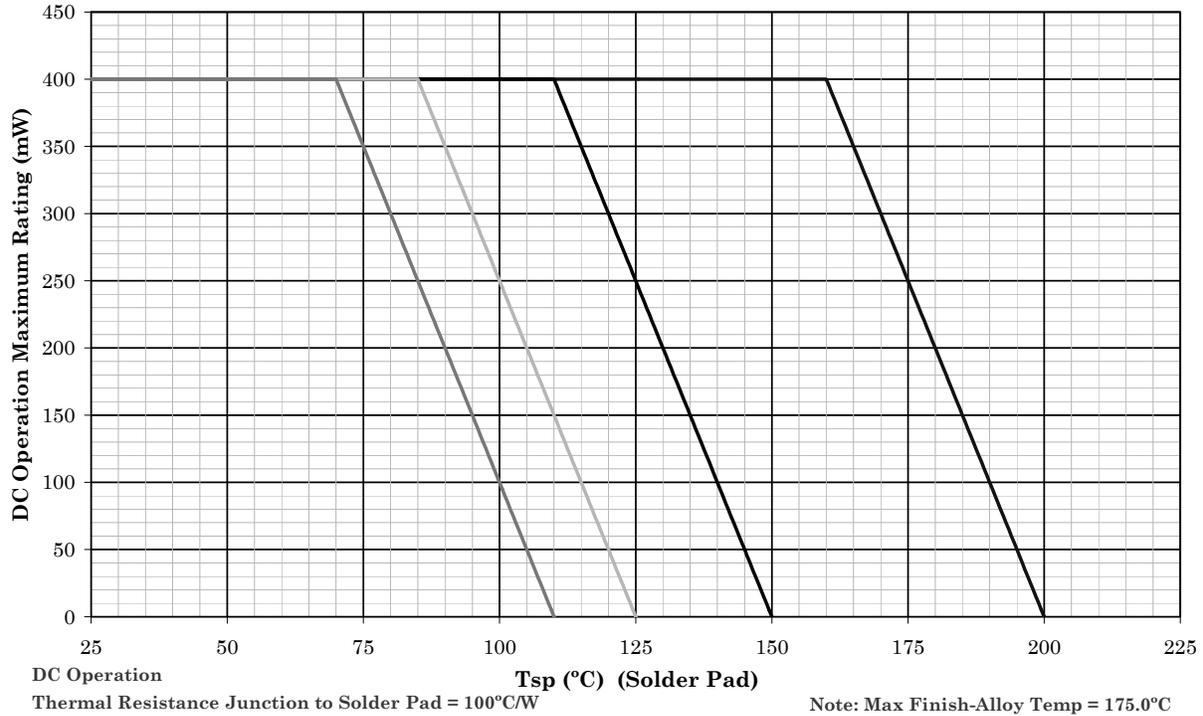
NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 7. Temperature-power derating for 2N2604UB and 2N2605UB (UB package PCB mounted in air).

Temperature-Power Derating Curve

2N2604UB, 2N2605UB

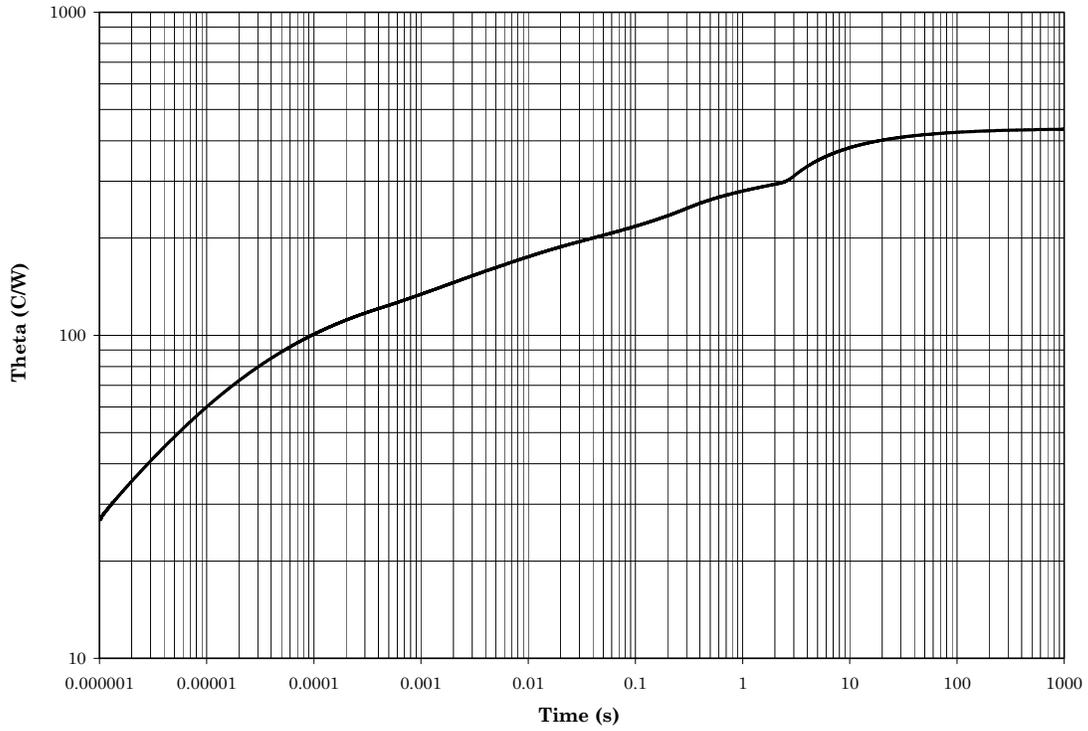


NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

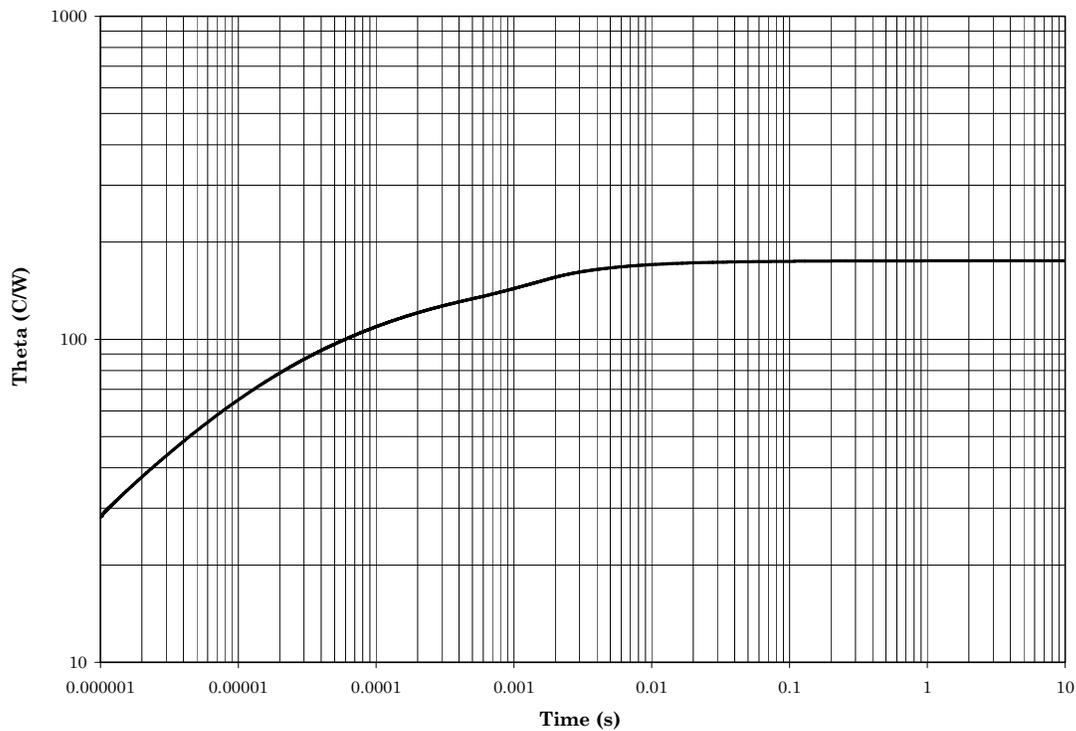
* FIGURE 8. Temperature-power derating for 2N2604UB and 2N2605UB (UB package solder pads to infinite sink).

Maximum Thermal Impedance



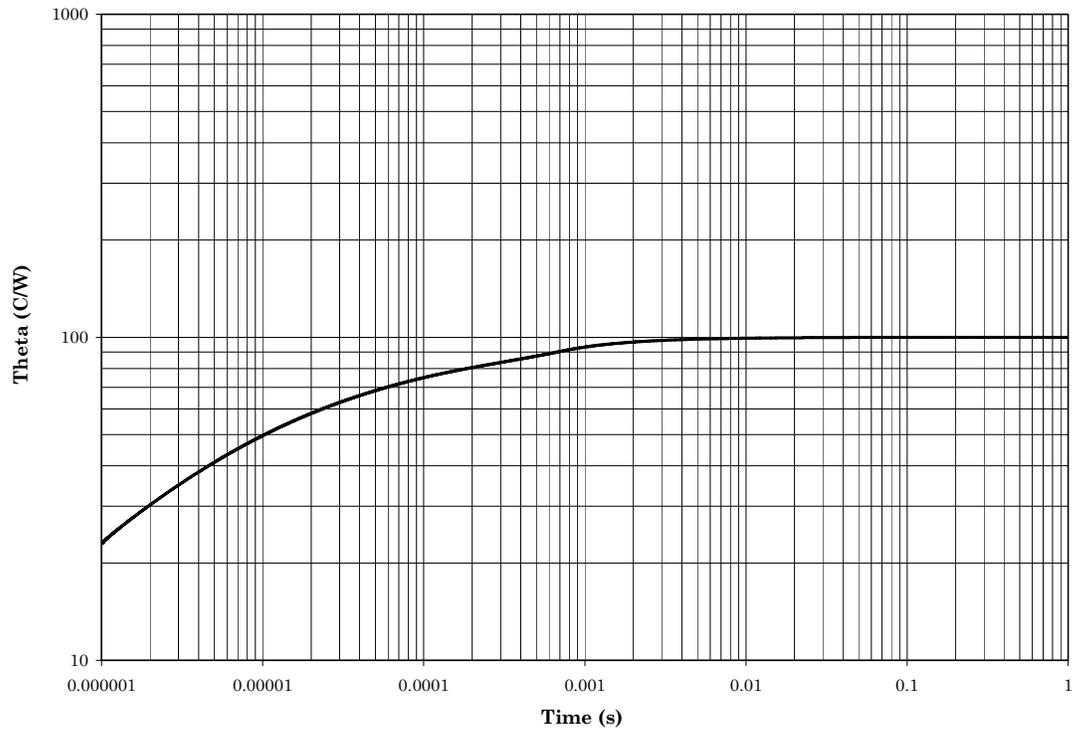
* FIGURE 9. Thermal impedance graph ($R_{\theta JA}$) for 2N2604 and 2N2605 (TO-46).

Maximum Thermal Impedance



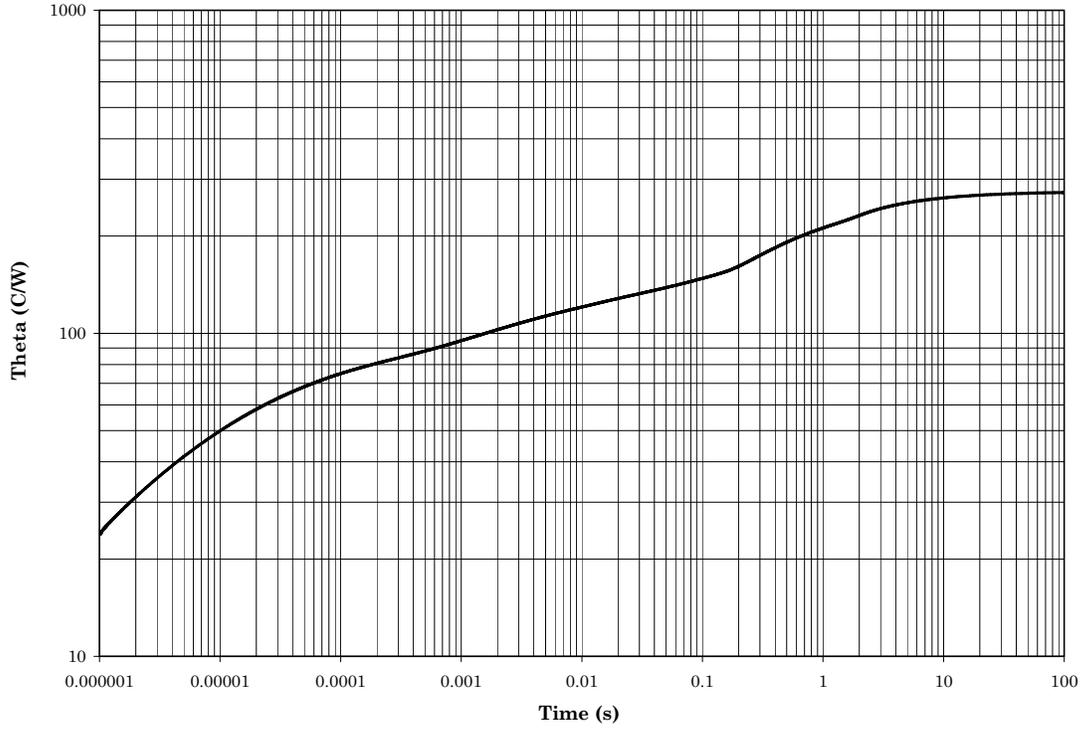
* FIGURE 10. Thermal impedance graph ($R_{\theta JC}$) for 2N2604, and 2N2605 (TO-46).

Maximum Thermal Impedance



* FIGURE 11. Thermal impedance graph ($R_{\theta JSP}$) for 2N2604UB and 2N2605UB (UB).

Maximum Thermal Impedance



* FIGURE 12. Thermal impedance graph ($R_{\theta JA}$) for 2N2604UB and 2N2605UB (UB).

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

* 6.4 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example, JANHCA2N2604) will be identified on the QPL.

JANHC and JANKC ordering information		
PIN	Manufacturer	
	43611	34156
2N2604 2N2605	JANHCA2N2604, JANKCA2N2604 JANHCA2N2605, JANKCA2N2605	JANHCB2N2604, JANKCB2N2604 JANHCB2N2605, JANKCB2N2605

6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-3010)

Review activities:
Army - AR, AV, MI
Navy - AS, MC
Air Force - 19

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