This document and process conversion measures necessary to comply with this revision shall be completed by 30 November 1995

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PERFORMANCE SPECIFICATION

HYBRID MICROCIRCUITS, GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

This document is a performance specification. It is intended to provide the device manufacturers an acceptable established baseline in order to support Government microcircuit applications and logistic programs. The basic document has been structured as a performance specification which is supplemented with detailed appendices. These appendices provide guidance to manufacturers on demonstrated successful approaches to meeting military performance requirements. These appendices are included as a benchmark and are not intended to impose mandatory requirements.

1. SCOPE

1.1 Scope. This specification establishes the general performance requirements for hybrid microcircuits, Multi-Chip Modules (MCM) and similar devices and the verification requirements for insuring that these devices meet the applicable performance requirements. Verification is accomplished through the use of one of two quality programs (Appendix A or Appendix B). The main body of this specification describes the performance requirements and the requirements for obtaining a Qualified Manufacturers List (QML) listing. The appendices of this specification are intended for guidance to aid a manufacturer in developing their verification program. Detail requirements, specific characteristics, and other provisions which are sensitive to the particular intended use shall be specified in the applicable device acquisition specification.

1.2 Description of this specification. The intent of this specification is to allow the device manufacturer the flexibility to implement best commercial practices to the maximum extent possible while still providing product which meets the military performance needs. Devices that are compliant to this specification are those that are capable of meeting the verification requirements outlined herein; and are built on a manufacturing line which is controlled by the manufacturer's quality management program and has been certified and qualified in accordance with the requirements herein. The certification and qualification requirements outlined herein are the requirements to be met by a manufacturer to be listed on the Qualified Manufacturers List (QML). The manufacturer may modify, substitute or delete the tests and inspections defined herein. This is accomplished by baselining a flow of tests and inspections that will assure that the devices are capable of meeting the generic verifications provided in this specification. This does not necessarily mean that compliant devices have been subjected to the generic performance verifications provided in this specification, just that compliant devices are capable of meeting them. It is the manufacturer's responsibility to insure that their devices are capable of meeting the generic performance verifications applicable to each specified product assurance level.

Appendices A and B define two quality management program that may be implemented by the manufacturer. Manufacturers who were certified under Options 1 or 2 of MIL-H-38534B have already implemented the Appendix A quality management program. Appendix B is a quality management approach utilizing a quality review board concept, hereafter referred to as the Technology Review Board (TRB) in this document, to modify the generic verification, design and construction criteria provided in this specification. This appendix is similar to MIL-H-38534B Option 4. Appendix C defines generic performance verifications. These verifications consist of a series of tests and inspections which may be used to verify the performance of devices. They may be used as is or modified as allowed by this specification. Manufacturers already certified under MIL-H-38534B have implemented the Appendix C verifications. Appendix D is to be used as a guide when characterization is necessary for new technologies and for standard technology qualification. This appendix may also be used as a guide in developing a test plan for new or existing products based on the tests and inspection of appendix C. Appendix E defines generic design and construction criteria relative to this technology, including rework limitations and major change testing guidance. Appendix F provides statistical sampling, and basic test and inspection procedures.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Defense Electronics Supply Center (DESC-ELD), Dayton, OH 45440, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

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1.3 Classification. Two quality levels are provided for in this specification. These classes are K and H, as defined below.

1.3.1 Class K. Class K is the highest reliability level provided for in this specification. It is intended for space applications.

1.3.2 Class H. Class H is the standard minimum military quality level.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. The following specification and standard form a part of this document to the extent specified herein. Unless otherwise specified, the issue of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-I-46058 - Insulating Compound, Electrical (For Coating Printed Circuit Assemblies)

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics

(Unless otherwise specified copies of military standards are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues are those cited in the solicitation.

Handbook H4/H8 - Commercial and Government Entity (CAGE) Handbook.

NAVSHIPS 0967-190-4010 - Manufacturer's Designating Symbols.

QML-38534 - Qualified Manufacturer's List of Custom Hybrid Microcircuits Qualified Under Military Specification MIL-H-38534

(Unless otherwise specified copies of military standards are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.3 Order of Precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated detail specifications, specification sheets, or MS standards), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Performance Requirements for Class K Devices. Class K devices shall be capable of meeting the class K tests and inspections of Appendices C and E. Verification of these Performance Requirements shall be performed as described in paragraph 4.

3.2 Performance Requirements for Class H Devices. Class H devices shall be capable of meeting the class H tests and inspections of Appendices C and E. Verification of these Performance Requirements shall be performed as described in paragraph 4.

3.3 General. The manufacturer of devices, in compliance with this specification, shall have and use production and test facilities and a verification program adequate to assure successful compliance with the provisions of this specification and the associated device acquisition specification. Adequacy of a device manufacturer to meet the requirements of this specification shall be determined by the Government qualifying activity. The individual item requirements shall be as specified in the associated device acquisition specification and herein. Only devices which meet all the performance requirements of this specification and the associated device acquisition specification and have been adequately verified shall be marked as compliant and delivered. Monolithic microcircuits may be built to the class H performance requirements of this specification. Facilities and programs listed on the Qualified Manufacturer's List (QML) may be used for the manufacture of other than compliant devices; however, any use or reference to compliant device marking, class K or H certification status or this specification in such a way as to state or imply equivalency (and thereby Government endorsement) in connection with noncompliant devices is prohibited and may be cause for revocation of certification or QML status (or both). Terms, definitions, methods, and symbols are per 6.3. Any military specification or standard referred to in this specification may be replaced by an equivalent commercial standard as determined by the preparing activity.

3.3.1 Implementation of Appendices C and E. The generic performance verifications of appendix C and the generic design and construction criteria of Appendix E shall be addressed by one of the following approaches:

a. As specified in Appendices C and E.

b. Demonstration to the qualifying activity of an alternate method which addresses the same quality and reliability concerns as defined herein or demonstration to the qualifying activity that the requirement is not applicable to the manufacturers technology or custom application.

c. Modification by an approved Technology Review Board (TRB) in accordance with Appendix B, using Appendix D as a guide, when appropriate.

NOTE: When using approach b above, Appendix D may be referred to for guidance. Furthermore, the following items shall be considered:

1. The nature and characteristics of the alternate method.

2. Supporting information and data.

3. Alternative test proposal(s) and data.

4. Assessment of worse case use conditions and process safety margin.

5. Test to failure data.

3.3.2 Device acquisition specification. The preferred device acquisition document for devices built in full compliance with this specification is a Standard Microcircuit Drawing (SMD). Monolithic microcircuits built in compliance with this document shall be documented on an approved SMD.

3.3.3 Design and Construction. The design and construction of compliant devices shall address the limitations and guidelines of Appendix E.

3.3.3.1 Lead finish. Appendix E provides the general interface requirements for lead finishes.

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3.3.4 Workmanship. Devices shall be manufactured, processed, and verified to meet the performance requirements of this specification, and with the production practices, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the Baseline Process Flow.

3.3.4.1 Rework and repair provisions. All rework and repair operations shall address the limitations and guidelines of Appendix E.

3.3.5 Marking of devices. Marking shall be in accordance with the requirements of this specification or the device procurement specification. The marking shall be legible and complete, and shall meet the resistance to solvents requirements of MIL-STD-883, method 2015. When mechanical or laser marking is performed it shall be clearly visible through those conformal coatings approved for use in MIL-I-46058 (see method 2015 of MIL-STD-883 if contrasting material or ink is used to highlight the trace). Mechanical or laser marked metal surfaces shall meet all applicable microcircuit finishes and shall not degrade the performance requirements of the device. Mechanical or laser marking shall be approved by the qualifying activity. If any special marking is used, it shall in no way interfere with the marking required herein, and shall be visibly separated therefrom. The following marking shall be included on each microcircuit unless otherwise specified.

a. Index point (see 3.3.5.2).

b. Part or Identifying Number (PIN) (see 3.3.5.1).

c. Lot identification code or date code (see 3.3.5.3).

d. Device manufacturer's identification (see 3.3.5.4).

e. Device manufacturer's designating symbol (see 3.3.5.5).

f. Country of origin (see 3.3.5.6).

g. Serialization, when applicable (see 3.3.5.7).

h. Special marking (see 3.3.5.8).

i. Certification mark (see 3.3.5.8.3).

j. ESD sensitivity identifier (see 3.3.5.8.2).

Unless otherwise specified, the certification mark, the PIN, the inspection lot identification code, and the ESD identifier shall be located on the top surface of flat packages or dual-in-line configurations and on either the top or the side of cylindrical packages (TO configurations and similar configurations).

3.3.5.1 Part or Identifying Number (PIN). Each Standard Microcircuit Drawing (SMD) microcircuit shall be marked with the complete PIN, as specified in the SMD. The number sequence for MIL-H-38534C is 5962-XXXXXZZHYY, where:

5962	-	XXXXX	ZZ	H	Y	Y
Federal stock class designator	RHA designator		Device type no. (see 3.3.5.1.1)	QML device class designator (see 3.3.5.1.2)	Case outline (see 3.3.5.1.3)	Lead finish designator (see 3.3.5.1.4)
_____	_____					

\/
Drawing number

3.3.5.1.1 Device type. The device type shall identify the circuit function as indicated in the SMD.

3.3.5.1.2 Device class designator. This device class designator shall be a single letter identifying the quality level in accordance with the SMD.

3.3.5.1.3 Case outline. The case outline shall be designated by a single letter assigned to each outline within each SMD.

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3.3.5.1.4 Lead finish. Lead frame or terminal material and finish shall be as specified (see Appendix E). The lead finish shall be designated by a single letter as follows:

Finish letter	Lead finish (see note)
A	hot solder dip
B	tin-lead plate
C	gold plate
X	finishes A, B, or C (see note)

NOTE: Finish letter "X" shall not be marked on the microcircuit or its packaging. This designation is provided for use in drawings, part lists, purchase orders, or other documentation where lead finishes A, B, and C are all considered acceptable and interchangeable without preference. For Government logistic support, the A lead finish will be acquired and supplied to the end user when the X is included in the PIN for lead finish. If the PIN is not available with the A lead finish, the same PIN will be acquired except with the C or B lead finish designator as determined by availability. Type C terminal material is a fired on metallization used with leadless chip carriers.

3.3.5.2 Index point. The index point, tab, or other marking indicating the starting point for numbering of leads or for mechanical orientation shall be as specified and shall be applied so that it is visible from above when the microcircuit is installed in its normal mounting configuration. The outline of an equilateral triangle (i.e., ▵), which may be used as an electrostatic identifier (see 3.3.5.8.2), may also be used as the pin 1 identifier.

3.3.5.3 Lot identification code (date code). Devices shall be marked by a unique code to identify the week of final seal. The first two numbers in the code shall be the last two digits of the number of the year, the third and fourth numbers shall be two digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero. Reading from left to right or from top to bottom, the code number shall designate the year and week, in that order (e.g., 8806 equals week 6 of 1988).

3.3.5.4 Manufacturer's identification. Devices shall be marked with the name or trade mark of the manufacturer. The identification of the equipment manufacturer may appear on the device only if the equipment manufacturer is also the device manufacturer.

3.3.5.5 Manufacturer's designating symbol. The manufacturer's designating symbol or CAGE code number shall be as listed on NAVSHIPS 0967-190-4010 or cataloging Handbook H4/H8. The designating symbol shall be used only by the manufacturer to whom it has been assigned and only on those devices manufactured at the manufacturer's plant. In the case of small devices, the manufacturer's designating symbol may be abbreviated by omitting the first "C" in the series of letters.

3.3.5.6 Country of origin. The manufacturer shall indicate the country of origin of the device. At the option of the manufacturer the country of origin marking may be omitted from the body of the device but shall be retained on the initial container.

3.3.5.7 Serialization. Serialization allows traceability of electrical tests results (variables data) to an individual device.

3.3.5.7.1 Class K serialization. Prior to the first recorded electrical measurement in screening, each class K device shall be marked with a unique serial number assigned consecutively. Lot records shall be maintained to provide traceability from the serial number to the specific incoming inspection lots from which the elements originated.

3.3.5.7.2 Class H serialization. Serialization of class H devices shall only be required when specified in the device acquisition specification.

3.3.5.8 Special marking. When the size of a package is insufficient to allow marking of special process identifiers on the top surface, the back side of the package may be used for these markings except the ESD identifier shall be marked on the top. Button cap flat packs with less than or equal to 16 leads may have the identifier marked on the ceramic. Back side marking with conductive or resistive ink shall be prohibited on nonconductive surfaces.

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3.3.5.8.1 Beryllium oxide package identifier. If a device package contains beryllium oxide, the device shall be marked with this designation: BeO.

NOTE: Packages containing beryllia will not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages will not be placed in acids that will produce fumes containing beryllium.

3.3.5.8.2 Electrostatic discharge (ESD) sensitivity identifier. ESD classification levels are defined as follows when tested in accordance with MIL-STD-883, method 3015.

ESD class designator	Prior designation category	Part marking	Electrostatic voltage
1	A	△	0-1,999 V
2	B	△ △	2,000-3,999 V
3	---	---	4,000 V

ESD class marking is not required. However at the manufacturers option devices not yet ESD classified may be marked as class 1 until testing determines the appropriate class. Devices previously classed by test as category A may be marked as class 1. Devices previously classified as category B may be marked as class 2.

3.3.5.8.3 Certification mark. All devices acquired to and meeting the requirements of this specification and the applicable associated device acquisition specification, and which are approved for listing on QML-38534 shall bear the "QML" certification mark for SMD controlled devices and the "CH" (compliant device) certification mark for non-SMD controlled devices. The certification mark shall be located preceding the date code. The certification mark abbreviation "Q" or "C" may be used for small devices. The "QML" or "CH" certification mark or the abbreviation "Q" or "C" shall not be used for any device acquired under contracts or orders which permit or require any changes to this specification. In the event that a lot fails to pass inspection, the manufacturer shall remove or obliterate the "QML" or "Q" or "CH" or "C" certification mark from the sample tested and also from the devices represented by the sample.

3.3.5.9 Marking option for controlled storage of class H. Where devices are subjected to testing and screening in accordance with some portion of the quality assurance requirements and stored in controlled storage areas pending receipt of orders requiring conformance to the same or a different level, the inspection lot identification code shall be placed on the device package along with the other markings specified in 3.3.5 sufficient to assure identification of the material. As an alternative, if the microcircuits are stored together with sufficient data to assure traceability to processing and inspection records, all markings may be applied after completion of all inspection to the specified level.

3.4 Item Requirements. The individual item requirements, including temperature range, for devices delivered under this specification shall be documented in the device acquisition specification.

3.4.1 Certification of Conformance. Manufacturers or suppliers, including distributors, who offer compliant devices described by this specification shall provide written certification, signed by the corporate officer who has management responsibility for the production of the devices, the devices are built, tested and handled in accordance with this specification and that they meet or exceed the performance requirements for the applicable class. The responsible corporate official may, by documented authorization, designate other responsible individuals to sign the certificate of conformance, but, the responsibility for conformity to the facts shall rest with the responsible corporate officer.

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4. VERIFICATION.

4.1 Responsibility for compliance. All items shall meet all requirements of section 3. The absence of any inspection requirements in the specification shall not relieve the contractor of the responsibility of insuring that all products or supplies submitted to the Government for acceptance comply with all requirements of the contract. Sampling inspection, as part of manufacturing operations, is an acceptable practice to ascertain conformance to requirements, however, this does not authorize submission of known defective material, either indicated or actual, nor does it commit the Government to accept defective material.

4.2 Quality Management Program. Manufacturers of compliant devices to this specification shall have in place or shall implement a quality management program, (see Appendix A or B). This system will be used to verify that devices meet the applicable Performance Requirements of paragraph 3. This system will be verified by the Qualifying Activity, see paragraph 4.5.

4.3 Baseline Process Flows. Manufacturers of compliant devices to this specification shall implement a baseline process flow detailing the processes, tests and inspections/monitors used by the manufacturer and the order in which they are performed. The point of entry where all materials or subassemblies enter the flow shall also be reflected. Appendices C and E provide generic verifications, design, and construction criteria for use in developing the manufacturer's baseline flows. The criteria and verifications identified in Appendices C and E may be modified using one of the approaches defined in paragraph 3.3.1. The baseline flow will be verified by the Qualifying Activity, see paragraph 4.5.

4.4 Quality management (QM) plan. The manufacturer's quality management plan reflects the major elements of the quality management program. The QM plan shall be available at, and continually effective in, the manufacturer's plant.

4.4.1 Self-audit program. As part of the QM plan, the manufacturer shall establish an independent self-audit program under the direction of the quality organization to assess the effectiveness of the manufacturer's quality assurance system, and ability to meet specification requirements. The results of these audits shall be available.

4.4.2 Change control procedures. As part of the QM plan, the manufacturer shall have a system which shall include procedures for notification of change that affects form, fit, and function, to all applicable acquiring activities.

4.5 Verifications for QML listing. Manufacturers of devices furnished as compliant to this specification shall obtain a Qualified Manufacturers List (QML) listing from the qualifying activity (DESC-ELS). The qualifying activity (QA) is as defined in 6.3.26. QA approval of the manufacturers quality management program, baseline process flows, and technology capability will result in the manufacturers receiving a QML certification and QML listing. The manufacturing processes and materials portion of the baseline flow (4.3) are listed on the QML. The qualifying activity shall provide procedures to obtain a QML certification and QML listing. This verification will require an on-site visit to the manufacturer's facility.

4.5.1 Verification audit. During the audit, the qualifying activity shall verify the adequacy of the manufacturer's quality management program to achieve at least the same level of quality as could be achieved by complying with Appendix A or B as applicable. The qualifying activity shall also verify the adequacy of the manufacturer's baselined process flow, assessing those flows' capability to produce product that can meet the generic performance verifications defined in Appendices C and D as applicable. Qualifying activity approval of the manufacturer's quality management system and baseline process flow results in QML certification, and is a mandatory precondition to QML listing.

4.5.1.1 On-site verification. The manufacturer shall make available to the qualifying activity all data needed to support the quality management program and procedures. Qualifying activity access to manufacturing and testing facilities and operators will be required. For first time qualification, on-site verifications will include all of the following areas: the manufacturer's quality management program, design program, baselined substrate fabrication, assembly and test processes, and facility control. Deficiencies and concerns shall be noted by the audit team during and exit critique and will be followed up with a written report.

4.5.1.2 QML certification. After verification and upon correction of all deficiencies and concerns, the qualifying activity shall issue a certificate and letter of QML certification to the manufacturer.

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4.5.2 Technology capability verification. The manufacturer shall demonstrate a comprehension of the capability of the manufacturing process and materials as related to quality, reliability, and producability in order to receive a QML listing. This demonstration shall be performed using test data, which shall be made available to the qualifying activity for review. This testing shall verify the technology's capability to withstand the generic performance verifications outlined in Appendix C as defined in the manufactuerer's baseline process flow. Manufacturer's of traditional technologies around which the technology qualification flow of D.6 was developed, may perform technology qualification using that criteria and test flow. Manufacturer's of new technologies shall demonstrate the adequacy of those test flows for their technology through characterization. Reference D.3, D.4, and D.5 for guidance related to technology characterization for specific technologies. Qualifying activity acceptance of this test data will result in the listing of the manufacturer on the QML.

5. PACKAGING. Packaging shall be as specified in the acquisition document.

6. NOTES.

6.1 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit application and logistic purposes. For maximum cost effectiveness while maintaining essential quality and reliability requirements, it is recommended that, for initial acquisitions for original equipment complements, the device class appropriate to the need of the application be acquired. For acquisition of spare parts for logistic support, it is recommended that, unless otherwise specified, all devices be acquired to class H requirements.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, and date of this specification.

b. Issue of DODISS to be cited in the solicitation.

c. PIN.

d. Title, number, and date of applicable device acquisition specification and identification of the originating design activity.

e. Device finishes.

f. Product assurance level (see 1.3).

g. Change notification (i.e., who to contact).

6.2.1 Optional acquisition data. The following items are optional and are only applicable when specified in the acquisition documents.

a. Requirements for failure analysis.

b. Special requirements.

c. Disposition of samples.

d. Requirement for qualification or Conformance Inspection (CI) and Periodic Inspection (PI) plan.

6.3 Terms, definitions, methods, and symbols. For the purposes of this specification, the terms, definitions, methods, and symbols of MIL-STD-883, MIL-STD-750, MIL-STD-1331, and those contained herein apply and may be used in applicable device acquisition specification wherever they are pertinent. The preparing activity shall interpret these definitions for use wherever pertinent. The item levels of part, subassembly, assembly, unit, group, set, and system, as well as the ancillary terms accessory and attachment, contained in MIL-STD-280, shall be applicable to this specification. To further describe a particular type of device, additional modifiers may be prefixed to the type name.

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6.3.1 Acquiring activity. The organizational element of the Government which contracts for articles, supplies, or services may authorize a contractor or subcontractor to be its agent. When this organizational element of the Government has given specific written authorization to a contractor or subcontractor to serve as agent, the agent shall not have the authority to grant waivers, deviations, or exceptions to this specification unless specific written authorization to do so has also been given by the Government organization which is the preparing activity, or qualifying activity. In the absence of a specific acquiring activity, the acquiring activity shall be an organization within the supplier's company that is independent of the group responsible for device design, process development or screening, or may be an independent organization outside the supplier's company.

6.3.2 Acquisition documents. Acquisition documents consist of the purchase order or contract, SMD, or specifications as applicable. The preferred device acquisition document for compliant devices is the SMD.

6.3.3 Antistatic materials. Antistatic materials which resist triboelectric charging, used as appropriate. Antistatic materials and plastic materials impregnated with antistatic agents (antistats) are antistatic if their surface resistivity is between 1×10^{9} and 1×10^{14} ohms/sq.

6.3.4 Baseline index of documents. The documents which establish the baseline for a given device manufacturer in satisfying the requirements of certification in accordance with this specification.

6.3.5 Baseline process flow. The manufacturer's baseline process flow is that flow of manufacturing processes, inspection and test processes, and material entry points into the flow that defines the manufacturer's specific technology flow. This flow begins with incoming material, goes through all manufacturing processes including in-processes monitors, completed device screening, and final acceptance verification of the product. The manufacturing processes and materials portion of the baseline process flow are the portions of the baseline that are listed on the QML. The total baseline flow is certified under QML certification.

6.3.6 Burn-in lot. The burn-in lot used for purposes of percent defective allowable (PDA) or pattern failure accountability (or both).

6.3.7 Chip on Board (COB). Multi component, actives (packaged and unpackaged) and passives, interconnected by a conductor network embedded in a ceramic (MIBS) or organic (PWB) substrate. A lamination process is used to fabricate the PWB and a co-fired ceramic process for the MIB. Level of interconnect is 2.0.

6.3.8 Compliant devices. Compliant devices are those that meet, without exception, the performance requirements of this specification, as well as the requirements of the device acquisition specification (SMD).

6.3.9 Compound bond. A bond placed on top of another bond, wire, ribbon, or other conductors not integral to the substrate.

6.3.10 Conductive materials. Conductive materials capable of electrostatic field shielding and having a volume resistivity of 1×10^{3} ohm-cm maximum or a surface resistivity less than 1×10^{5} ohms/sq may be used as appropriate.

6.3.11 Delta (Δ) limits. Delta limits, maximum changes in specified parameter readings which permit device acceptance on specified tests, shall be based on comparison of present measurements with specified previous measurements.

NOTE: When expressed as a percentage value, they shall be calculated as a proportion of previously measured values.

6.3.12 Dissipative materials. Dissipative materials having a surface resistivity between 1×10^{5} and 1×10^{9} ohms/sq shall be used as appropriate.

6.3.13 Electrostatic discharge sensitivity (ESDS). The level of susceptibility of devices to damage by static electricity, found by classification testing, is used as the basis for assigning an ESDS class.

6.3.14 Element. A constituent of a device that contributes directly to its operation (e.g., chip resistor, capacitor, diode, transistor, integrated circuit, surface acoustic wave (SAW), substrate, package, etc., incorporated into a device), is an element of the device.

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6.3.15 Film Microcircuit. A microcircuit consisting exclusively of elements which are film formed in-situ upon or within an insulating substrate.

6.3.16 Final seal. After manufacturing operations which complete the enclosure of a device following all allowable rework so that further internal processing cannot be performed, and for the purpose of seal date code identification and conformance inspection (CI) and periodic inspection (PI) testing, the final seal date code is used.

6.3.17 Flip chip bonding: Direct attachment of a bare die to a PCB through solder bumps on the surface of the die being placed in direct contact with the board. The solder bumps are located on the contact pads on the active side of the die, and the die is flipped over and placed in contact with the mating contacts on the board.

6.3.18 Hybrid microcircuit. A microcircuit that contains two or more of a single type or a combination of the following types of elements with at least one of the elements being active.

a. Film microcircuit (6.3.14).

b. Monolithic microcircuit (6.3.23).

c. Semiconductor element.

d. Passive chip or printed or deposited substrate elements.

6.3.19 Hybrid microcircuit type (device type). The term "hybrid microcircuit type" (device type) refers to a single specific device configuration. All samples of a hybrid microcircuit type are electrically and functionally interchangeable with each other; have the same electrical and environmental test limits; and use the same package, materials, piece parts, and assembly processes.

6.3.20 Inspection lots. Inspection lots consist of a quantity of devices of a single device type (required for group A) or several different circuit types (allowed for groups B, C, and D tests only) in a single package type and lead finish submitted at one time for final acceptance. All devices within each inspection lot shall be finally sealed in the same period not exceeding 13 weeks. Inspection lot identification shall be maintained from the time the lot is formed until the lot is accepted. Inspection lot traceability shall be maintained to the production lots from which it was formed.

6.3.21 Inspection lot formation. Inspection lot formation is required if the inspection lot is to be formally accepted by the lot related CI and PI testing of this specification or MIL-STD-883 method 5005. If the in-line process verification testing alternative is used, inspection lot formation is not required. For in-line process verification, process traceability must be maintained such that devices can be clearly identified to specific periods of in-line process testing.

6.3.22 Insulating materials. Insulating materials having a volume resistivity of 1×10^{12} ohm-cm minimum, or a surface resistivity of 1×10^{14} ohms/sq minimum may be used as required.

6.3.23 Known good die (KGD). A bare die of the same quality and reliability level as an equivalent packaged die.

6.3.24 Microelectronics. That area of electronic technology associated with or applied to the realization of electronic systems from extremely small electronic parts or elements.

6.3.25 Microcircuit. A small circuit having a high equivalent circuit element density, which is considered as a single part composed of interconnected elements on one or more substrates to perform an electronic circuit function. (This excludes printed wiring boards, circuit cards assemblies, and modules composed exclusively of discrete electronic parts mounted on a non-ceramic substrate or board.)

6.3.26 Monolithic microcircuit. A microcircuit consisting exclusively of elements formed in-situ or within a single semiconductor substrate with at least one of the elements formed within the substrate.

6.3.27 Multichip module (MCM). A hybrid microciruit that contains two or more microcircuits, each having greater than 100,000 junctions.

6.3.28 MCM-C (Ceramic). An MCM whose substrate is composed of a multilayer ceramic using thick-film technology.

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6.3.29 MCM-D (Dielectric). An MCM whose interconnection pattern is formed on deposited dielectrics and conductors to a substrate, typically by a thin-film process.

6.3.30 MCM-L (Laminated). An MCM having a substrate constructed using laminated multilayer printed wiring board technology.

6.3.31 MCM-Si (Silicon). Interconnections are formed using a silicon substrate, aluminum or copper conductors, and SiO_2 as the inorganic dielectric media.

6.3.32 MCM SEC (Standard evaluation circuit). A portion of the MCM design which could be used for testing to determine if the processes being used to construct the unit are adequate.

6.3.33 Noncontinuous production. Noncontinuous production occurs when devices are held by the manufacturer, with no additional assembly work performed, for more than 30 days.

6.3.34 Passive element. Planar resistors, capacitors, inductors and patterned substrates (single and multilayer) and nonplanar chip resistors, capacitors, inductors, and transformers.

6.3.35 Percent defective allowable (PDA). PDA is the maximum observed percent defective which will permit the lot to be accepted after the specified 100 percent test.

6.3.36 Printed circuit board (PCB). An interconnect board that uses copper conductors and plastic, laminate-based dielectrics.

6.3.37 Production lot. A production lot consist of a device type manufactured from the same basic raw materials on the same production line, processed under the same manufacturing techniques and controls using the same type of equipment. The production lot is formed at or prior to device kit preparation (i.e., release to manufacturing). In addition for class K devices, all materials shall be from the same incoming inspection lot for each element. If necessary, rework requirements may be satisfied with materials from a different incoming inspection lot.

6.3.38 Qualifying activity. The qualifying activity is the organizational element of the Government that grants certification and QML status. For the purpose of this document the Qualifying Activity shall be DESC-EL.

6.3.39 Semiconductor element. Transistor or diode.

6.3.40 Similar devices. For the purpose of CI and PI, one device type is similar to another when it meets all the following conditions:

a. Designed and manufactured identically using the same or fewer fabrication and assembly processes and materials.

b. Assembled with the same or fewer active and passive elements.

c. Subjected to the same screening except electrical testing.

d. Designed to generate the same or fewer functions (magnitude of functional attributes such as voltage, current, duty cycle, frequency, etc. may vary) using the same or less functional circuitry (e.g., a 4-bit A/D converter is similar to a 10-bit A/D converter, but not vice versa).

6.3.41 Tape automated bonding (TAB). The attachment of a bare die to a very fine pitch lead frame normally made of copper and polyimide. The top surface of the die is normally mechanically protected with a polymer coating.

6.3.42 Technology capability. Technology reliability and performance limits, normally determined through tests known to reveal failure modes/mechanisms; and through testing of critical characteristics of the technology that are known to impact performance and reliability. Testing performed to more severe test conditions than those used for screening and final acceptance testing of the device, or test-to-failure testing, are examples of testing performed specifically to determine a technology's capability. The data may also be produced through other means for mature technologies, e.g., production test data taken over time, design or product qualification test data accumulated for a specific program or customer, etc.

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6.3.43 Wafer lots. Wafer lots consist of microcircuit and semiconductor wafers formed into lots at the start of wafer fabrication for homogeneous processing as a group. Each lot is assigned a unique identifier or code to provide traceability and maintain lot integrity throughout the fabrication process. Wafer lot processing as a homogeneous group is accomplished by any of the following procedures, providing process schedules and controls are sufficiently maintained to assure identical processing in accordance with process instructions of all wafers in the lot:

a. Batch processing of all wafers in the wafer lot through the same machine process steps simultaneously.

b. Continuous or sequential processing (wafer by wafer or batch portions of wafer lot) of all wafers through the same machine or process steps.

c. Parallel processing of portions of the wafer lot through multiple machines or process stations on the same certified line, provided statistical quality control (SQC) assures and demonstrates correlation between stations and separately processed portions of the wafer lot.

6.4 Destructive tests. All mechanical or environmental tests (other than those listed in 6.5), shall be considered destructive initially, but may subsequently be considered nondestructive upon accumulation of sufficient data to indicate that the test is nondestructive. The accumulation of data from five repetitions of the specified tests on the same sample of product, without evidence of cumulative degradation or failure to pass the specified test requirements in any device in the sample, is considered sufficient evidence that the test is nondestructive. Any test specified as a 100 percent screen shall be considered nondestructive for the stress level and duration or number of cycles applied as a screen. Unless otherwise specified or subsequently determined to be otherwise, the following MIL-STD-883 tests shall be initially classified as destructive.

Internal visual and mechanical (method 2014) 1/	Die shear strength test
Bond strength (method 2011)	Total dose radiation hardness test
Solderability (except for lead finish A)	ESDS test
Moisture resistance	Lid torque test
Lead integrity (method 2004)	Adhesion of lead finish
Salt atmosphere	Vibration, variable frequency
SEM inspection for metallization	Internal water vapor test 2/
Steady state life test (accelerated)	Pin grid package lead pull (method 2028)

Notes 1/ This inspection is nondestructive when performed at preseal visual.
2/ Test samples may be delidded/relidded in accordance with Appendix E making these devices eligible for shipment. The manufacturer shall assure that proper precautions for handling, testing, and shipping have been taken by the RGA test laboratory.

6.5 Nondestructive tests. Unless otherwise specified, the following tests are classified as nondestructive:

Barometric pressure	Radiography
Steady state life (see note)	Particle impact noise detection (PIND)
Intermittent life (see note)	Physical dimensions
Hermeticity	Nondestructive bond pull test (method 2023)
External visual	Resistance to solvents
Internal visual (preseal)	Solderability (for lead finish A only)
Burn-in screen (see note)	

NOTE: When the test temperature exceeds the maximum specified junction temperature for the device (including maximum specified for operation or test), these tests shall be considered destructive unless otherwise specified.

6.6 Subject term (key word) listing.

Class H
Class K
QML
Qualification
SPC

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APPENDIX A

QUALITY MANAGEMENT PROGRAM

A.1 SCOPE

A.1.1 Scope. This appendix is intended to be used by manufacturers in developing their quality management program. The quality management program should demonstrate the methods used to assure conformance to the applicable requirements, including design, manufacturing, and verification. Compliance with this appendix is not mandatory, however, manufacturers must be able to demonstrate a quality management system that achieves at least the same level of quality as could be achieved by complying with this appendix.

A.1.2 Description of Appendix A. This appendix describes a quality management program to demonstrate and assure that design, manufacture, inspection, and testing of devices are adequate to assure compliance with the applicable requirements and quality standards for each device manufactured.

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A.2 APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

A.3 QUALITY MANAGEMENT PROGRAM

A.3.1 Design, processing, manufacturing, and testing instructions. The manufacturer should maintain documentation and instructions covering, as a minimum, these areas:

a. Conversion of customer requirements into manufacturer's internal instructions (see A.3.1.1).

b. Personnel training and testing (see A.3.1.2).

c. Inspection of incoming materials, utilities, and work in-process (see A.3.1.3).

d. Quality control operations (see A.3.1.4)

e. Performance verification operations (see A.3.1.5).

f. Design, processing, rework, tool and materials standards, and instructions (see A.3.1.6).

g. Cleanliness and atmosphere control in work areas (see A.3.1.7).

h. Change control of design, process, and documentation (see A.3.1.8).

i. Tool, gauge, and test equipment maintenance and calibration (see A.3.1.9).

j. Failure and defect analysis and data feedback (see A.3.1.10).

k. Corrective action and evaluation (see A.3.1.11).

l. Incoming, in-process, and outgoing inventory control (see A.3.1.12).

m. ESD handling control program (see A.3.1.13).

Detailed information regarding these items is stated in A.3.1.1 through A.3.1.13. These areas will normally be addressed by the manufacturer's standard drawings, specifications, process instructions, and other established manufacturing practices.

A.3.1.1 Conversion of customer requirements into manufacturer's internal instructions. These procedures should address the method by which customer requirements, as expressed in specifications, purchase orders, etc., are converted into working instructions for the manufacturer's personnel.

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A.3.1.2 Personnel training and testing. The procedures should address the and work training and testing practices employed to establish, evaluate, and maintain the skills of personnel engaged in reliability critical work including the form, content, and frequency of use.

A.3.1.3 Inspection operations. Procedures should address inspection operations specifying type of inspection, sampling and test procedures, acceptance and rejection criteria, and frequency of use.

A.3.1.4 Quality control operations. Procedures should address quality control operations specifying the type, procedures, rating criteria, action criteria, records, and frequency of use. The use of Statistical Quality Control (SQC) and Statistical Process Control (SPC) is strongly encouraged.

A.3.1.5 Performance verification operations. Procedures should address performance verification operations specifying the type, procedures, equipment, judgment, and action criteria, records, and frequency of use. The use of SQC and SPC is strongly encouraged.

A.3.1.6 Design, processing, manufacturing equipment, and materials instructions. Procedures should address device design, processing, manufacturing equipment, and materials described in drawings, standards, specifications, or other appropriate media covering the requirements and tolerances for all aspects of design and manufacturing including equipment test and prove-in, materials acquisition and handling, design verification testing and processing steps. As a minimum, detailed instructions should exist for the following items, and be adequate to assure that quantitative controls are exercised, that tolerances or limits of control are sufficiently tight to assure a reproducible high quality product, and that process and inspection records reflect the results actually achieved:

a. Incoming materials control (substrates, packages, active and passive chips or elements, wire, water purification, etc.).

b. Substrate fabrication operations.

c. Die, element, or substrate attachment.

d. Interconnect (e.g., wire bonding).

e. Rework.

f. Sealing.

A.3.1.7 Cleanliness and atmosphere control in work areas. Procedures should address instructions for cleanliness and atmosphere control in each work area in which unsealed devices, or parts thereof, are processed or assembled. Controlled work areas should be established in accordance with Federal Standard 209 or commercial equivalent. Action and absolute control limits (at which point work stops until corrective action is completed) based on historical data and criticalness of the process in each particular area should be established. A method for the identification and control of foreign material, equivalent to or better than the foreign material control program described in MIL-STD-883 method 2017, should be employed.

A.3.1.8 Change control. Procedures should address the methods and procedures for implementation and control of changes in device design, processing, and documentation; and for making change information available when applicable. This includes changes made for cost reduction and continuous improvement.

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A.3.1.8.1 Configuration control. Changes are categorized into three classifications.

Class	Description
I	Major changes
II	Minor changes
III	Editorial changes

All changes in design, substitution of materials or processes, or modifications to baselined documentation (i.e., all class I, II, and III changes) for any hybrid microcircuit should be processed in accordance with established change control procedures.

a. Class I: Class I changes detailed in Appendix E are those changes that may affect the performance, quality, reliability, or interchangeability of the product. Acquiring activity approval is required if specified by contract.

b. Class II changes are all changes except Class I and class III changes (e.g., conformance to the military specification revision, vendor metallization mask change, package height change within the envelope tolerances of the detail drawing, etc.). Control procedures and records should be kept available for on-site review. In addition, for class K devices minor design and process changes, records for each change should include the rationale, and/or evidence as appropriate that the performance, quality, reliability, or interchangeability of the product were not adversely affected.

c. Class III: Class III, editorial changes, are those changes to documentation necessary to insure the understanding and execution of the affected document (e.g., format changes, spelling, word identity, etc.). Change documentation history for class III type changes should be kept available for on-site review.

A.3.1.9 Tool and test equipment maintenance and calibration. Procedures should address the maintenance and calibration procedures, and the frequency of scheduled actions, for tools, gauges, and test equipment in accordance with the requirements of ANSI Z540-1 or equivalent.

A.3.1.10 Failure and defect analysis and data feedback. Procedures should address methods for identification, handling, and analysis of failed or defective devices.

A.3.1.11 Corrective action and evaluation. Procedures should address the process and responsibility for decisions regarding the necessity for corrective action as a result of failure or defect analysis, and for evaluation and approval of proposed corrective actions.

A.3.1.12 Incoming, in-process, and outgoing inventory control. Procedures should address methods and procedures which are used to control storage and handling of incoming materials, work in-process, and warehoused and outgoing product in order to achieve such factors as age control of limited-life materials; and prevent inadvertent mixing of conforming and nonconforming materials, work, or finished product. Each area should maintain identity of work in process. Procedures should exist for controlling the receipt of acquired materials and supplies. The procedures should address the following:

a. Withholding received materials or supplies from use pending completion of the required inspection or tests, or the receipt of necessary reports.

b. Segregation and identification of nonconforming material and supplies from conforming materials and supplies and removal of nonconforming subassemblies and parts.

c. Identification and control of limited-life materials and supplies.

d. Identification and control of raw materials.

e. Assurance that the required test reports, certification, etc., have been received.

f. Clear identification of materials released from receiving inspection and test to clearly indicate acceptance or rejection status of material pending review action.

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A.3.1.13 ESD handling control program. Procedures should address the ESD handling control program documentation. This includes methods, equipment and materials, training, packaging, handling, and procedures for handling ESD sensitive devices.

A.3.2 Records to be maintained. The records pertaining to production processes, incoming and in-process inspections are should be retained for a minimum of 3 years (7 years for class K) and those pertaining to performance verification retained for a minimum of 5 years (7 years for class K) after performance of the inspections. Records should be maintained as a minimum for:

a. Personnel training and testing (see A.3.2.3).

b. Inspection operations (see A.3.2.4).

c. Failure reports and analyses (see A.3.2.5)

d. Initial documentation and subsequent changes in designs, materials, or processing (see A.3.2.6).

e. Equipment calibrations (see A.3.2.7).

f. Process, utility, and material controls (see A.3.2.8).

g. Product lot identification (see A.3.2.9).

h. Product traceability

A.3.2.1 Computerized records. Computerized records are optional provided they clearly and objectively indicate that all requirements of MIL-H-38534 have been met. The computerized records for traceability, screening and conformance inspection should be readily accessible and available to Government personnel for review and an appropriate electronic or hard copy provided to the qualifying activity as required. Instructions for the keeping of computerized records should address the following:

a. Entry verification.

(1) Identification of each individual making entries.

(2) Verification of all manually entered data at the time of entry by the same operator.

(3) Identification of all entered data by time/date of date/entry sequence to protect against "out of sequence" entries. No recorded transactions should be deleted or changed.

b. Control procedure for lot history records.

(1) Modification of lot histories by additions (i.e., original entries plus corrective addenda).

(2) Ensuring all corrective addenda meet all the requirements of h.(1) above.

(3) Limitation and designation of operators that are permitted to access lot history computer records for corrective addenda. Documentation of security procedures to assure that limited access is maintained (e.g., restricted terminals, passwords, etc.).

(4) Backup and archival of computerized lot history records prior to lot shipment.

A.3.2.2 Altered records. Altered records should identify the following:

a. For changed data:

(1) Identification of individual making new entry.

(2) Maintain identity of all original data entries (no "white out").

(3) Justification noted for change and verification by a second party (e.g., QA) when change affects lot jeopardy (i.e., lot originally considered to be rejected is changed to pass status).

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b. For transferred data to new test record:

(1) Identification of individual transferring data.

(2) All original record entries should be transferred.

(3) New test records entries should be verified against the original record by a second party.

A.3.2.3 Personnel training and testing. Records should cover the nature of training or testing given (e.g., when it was given, how long it lasted, and who was trained and tested). An effective training program should address at least the following:

a. Identification of critical processes and performance verifications.

b. Conformance to manufacturer's in-house standards.

c. Formal training (e.g., classroom or on the job training supervised by a certified trainer).

d. Evaluation procedure to assure the proficiency of each individual.

e. Re-evaluation or retraining at the end of a designated period or when personnel performance indicates poor proficiency.

f. Use of only trained personnel in critical processes or inspections.

A.3.2.4 Inspection operations. Records of inspection operations should cover the tests or inspections made, the materials group (lot, batch, etc.) inspected, the controlling documentation, the date of completion of inspection, the amount of material tested, and acceptance, rejection, or other final disposition of the material.

A.3.2.5 Reports and analyses of defective devices and failures. Records of defective devices should cover the source from which each device was received, the test or operation during which failure occurred or defects were observed, and prior testing or screening history of the device, the date of receipt, and the disposition of the device. Records of failure and defect analyses should cover the nature of the reported failure or defect (failure or defect mode), verification of the failure or defect, the nature of any device discrepancies which were found during analysis (failure or defect mechanism), assignment of the failure-activating cause if possible, the date of completion of the analysis, identification of the group performing the analysis, disposition of the device after analysis, and the distribution of the record. The record should also address the relationship of observed failure or defect modes in related lots or devices and, where applicable, corrective action taken as a result of the findings.

A.3.2.6 Changes in design, materials, or processing. Records should cover:

a. The initial documentation and all changes.

b. The date upon which each change becomes effective for devices intended to be submitted for Conformance Inspection (CI) under this specification.

c. The first production, or CI lot (as applicable) within which product incorporating the change is included).

d. The documents authorizing and implementing changes.

e. For minor design and process changes to class K devices, the documents that justify the change as minor (see Appendix E).

A.3.2.7 Equipment calibrations. Records should cover the scheduled calibration intervals for each equipment item, the dates of completion of actual calibration, identification of the group performing the calibration, and certification of the compliance of the equipment with documented requirements after calibration, in accordance with ANSI Z540-1 or equivalent.

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A.3.2.8 Process, utility, and materials controls. Records should cover the implementation of tools such as control charts (e.g., X and R charts) or other means of indication of the degree of control achieved at the points in the material, utility, and assembly process flow documented in the manufacturing instructions. Records should also indicate the action taken when each out-of-control condition is observed, and the disposition of product processed during the period of out-of-control operation.

A.3.2.9 Production lot identification. Records should identify when each production or inspection lot was processed through each area. These records should identify for each production or performance verification lot (as applicable) of finished product, these items as a minimum:

a. The performance verifications performed and their results.

b. The serial numbers (when applicable) of all devices.

c. The date of completion of performance verifications.

d. Lot Identification.

e. The pertinent associated device acquisition specification under which verification was performed.

f. Final lot disposition(withdrawn, not accepted, accepted).

g. Acquiring activity source inspection consideration, when applicable.

h. The number of devices, by device type, at the time of seal.

i. By device type, the number of devices shipped and the number of devices in stock inventory.

A.3.3 Product assurance program plan (PAPP). The PAPP should consist of a volume or portfolio, or series of documents which is adequate to assure compliance of the manufacturer's product with the applicable specifications and quality standards. A summary of the manufacturer's approach to the above items that makes specific reference to the manufacturer's actual procedures is also a method of documenting the product assurance program plan. The documents authorizing and implementing changes should be maintained. Any difference in treatment of different product lines within a plant should be stated and explained in the PAPP, or separate PAPP's prepared for such different lines. The PAPP should contain, as a minimum, documentation covering the following items:

a. Functional block organization chart (see A.3.3.1).

b. Baseline process flowchart (see main body and A.3.3.2).

c. Procedures for conversion of customer requirements into internal instructions (see A.3.1.1).

d. Design guidelines (see A.3.3.3).

e. Design, material, and process change control documents (see A.3.1.8).

f. Failure and defect analysis and feedback documents (see A.3.1.10).

g. Corrective action and evaluation documents (see A.3.1.11).

h. Examples of assembly and verification travelers (see A.3.3.4).

i. Baseline index of documents (see A.3.3.5).

j. Manufacturer's self-audit (see A.3.3.6).

A.3.3.1 Functional block organization chart. This chart should show, in functional block-diagram form, the lines of authority and responsibility (both line and staff) for origination, approval, and implementation of all aspects of the product assurance program. Names of the incumbents are not necessary in this chart.

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A.3.3.2 Baseline process flowchart. The flow (see 4.3) should identify all major documents pertaining to the inspection of materials, the production processes, the production environments, and production controls which were used. The documents will be identified by name and number. Changes approved thereafter will be treated in accordance with the approved document change control procedures in A.3.1.8.

A.3.3.3 Design guidelines. Design guidelines used to design and/or verify the design of microcircuits intended to be submitted for acceptance inspection.

A.3.3.4 Examples of assembly and verification travelers. Screening and Conformance Inspection verification travelers should be maintained on a current basis. When in-line inspections replace end-of-line verifications (i.e., alternate group A or B) the traveler should includes evidence of required inspections. The travelers should include all manufacturer imposed tests. The traveler should include all the following minimum information, or provide direct traceability to it:

a. Name or title of operation and specification number of each process or test.

b. Identify PIN, date code, and manufacturer internal lot identification number.

c. Date of test and operator identification.

d. Calibration control number or equipment identification of all major equipment components used for test.

e. Quantity tested and rejected for each process or test and actual quantity tested if sampled.

f. Serial numbers of passing and failing devices when applicable.

g. Time in and out of process or test if critical to process or test results (i.e., burn-in and 96-hour window).

h. Specific major conditions of test that are verifiable by operator including times, temperature, rpm, etc.

i. The percent defective calculated and the pattern failure analysis for burn-in.

j. Burn-in or life test board serial number or test circuit identification number and revision.

k. All required variables data except for electrical tests (use attachments if applicable).

l. For electrical tests, test program number and revision, and identify when variables data is required.

A.3.3.5 Baseline Index of Documents. A list of the specification titles, document numbers, and revisions which make up the QML program. This is the baseline the manufacturer is certified to at the certification audit.

A.3.3.6 Manufacturer's self-audit. The manufacturer's self-audit program should identify key review areas, their frequency of audit, and the corrective action system to be employed when variations from approved procedures or specification requirements are identified.

A.4 SELF-AUDIT

A.4.1 Self-audit requirements. This portion of appendix A contains, details for implementation of the manufacturer's self-audit program. The intent of this self-audit program is to assure continued conformance to applicable requirements.

A.4.2 Definitions.

A.4.2.1 Self-audit. The performance of periodic surveys and reviews by the device manufacturer's designated personnel to evaluate compliance to military specifications, customer, and internal requirements.

A.4.2.2 Audit checklist. A form listing specific items which are to be audited.

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A.4.3 General guidance.

A.4.3.1 Self-audit representatives. The designated auditors should be independent from the area being audited. If the use of an independent auditor is not practical, then as a minimum another individual should be assigned to participate in the audit or review the results with the auditor from the area. The auditors should be trained in the area to be audited, in the applicable military specification requirement, and provided with an appropriate checklist for annotating deficiencies. Prior to the audit, the assigned auditor should review the previous audit checklist to assure corrective actions have been implemented and are sufficient to correct the deficiencies.

A.4.3.2 Audit deficiencies. All audit deficiencies should be documented on the appropriate checklist and a copy submitted to the department head for corrective action. All corrective actions should be agreed to by the quality organization or review board.

A.4.3.3 Audit follow-up. All audit reports should be filed and maintained. A procedure should be established to follow up on all audit deficiencies to assure that the corrective actions have been implemented in a timely manner. The system (e.g., management review) should also review the acceptability and timeliness of all corrective actions and determine if any deficiencies have repeated since the last required self-audit. If any deficiencies have occurred two or more times in the predetermined time period, additional corrective actions should be taken to assure immediate correction of the problem including notification of applicable organizations.

A.4.3.4 Audit schedules. The original audit frequency is established by the manufacturer normally not to exceed 1 year for each area.

A.4.3.5 Self-audit report. The manufacturer keeps the self-audit report on file for the established amount of time prescribed by the manufacturer's record retention requirements, and makes the self-audit report, deficiencies, and corrective actions taken available for review by the qualifying activity.

A.4.3.6 Self-audit areas. The self-audit will be performed to assure conformance to the checklist and military specification in at least the following areas:

Areas

Calibration	Training
Substrate Fabrication	Failure analysis
Qualification/CI and PI system	Assembly operations
Document control	Electrical test
Change control	Test methods
Incoming inspection	Environmental control
Inventory control and traceability	

A.4.3.7 Self-audit checklist. The audit checklist should be approved and maintained under document control. The checklist is intended to assure that the quality assurance system is adequate and followed by all personnel in each area.

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APPENDIX B

TECHNOLOGY REVIEW BOARD OPTION

B.1 SCOPE

B.1.1 Scope. This appendix defines a Quality Management (QM) Program for implementation of preventative techniques to assure product quality and reliability. Compliance with this appendix is not mandatory, however, manufacturers choosing to use this option must be able to demonstrate a review board system that achieves at least the same level of quality as could be achieved by complying with this appendix. This option allows a manufacturer to migrate from the conventional design and construction requirements and detection tests (e.g., screening, conformance and periodic inspection, and qualification) of MIL-H-38534 to alternative prevention methods with sufficient documentation. Alternative prevention methods include statistical process control (SPC), periodic process capability certification, design analysis, design robustness, off-line reliability assessment, etc. The documentation must show that the alternative methods ensure product compliance to the minimum quality and reliability requirements of this specification without performing the detection tests or adhering to the specific design and construction requirements. Using this specification as a baseline the manufacturer develops a QM program, which encompasses the entire manufacturing line being validated. This line is controlled by a technology review board (TRB), which can modify, substitute, or delete detection tests as appropriate for the technology or process. Techniques such as statistical process control and design of experiments are employed to ascertain process capabilities. Once alternative techniques are developed, periodic assessment is required to ensure that the processes continue to meet the required capabilities. The QM program also requires a program of continuous improvement to reduce overall product cost and improve quality and reliability. A customer compliance matrix (CCM) is generated for each product as part of the conversion of customer requirements process, and documents the means by which the end-item performance requirements will be met.

B.1.2 Description of Appendix B. This appendix is an optional appendix for use by manufacturers who wish to have their TRB certified by the Qualifying Activity (QA). This certification will then allow the TRB to make changes to the Verification Program (see Appendix C), without prior approval by the QA.

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B.2 APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

B.3 REQUIREMENTS

B.3.1 Terms, definitions, methods, and symbols. The terms, definitions, methods and symbols of this specification will apply.

B.3.1.1 Cpk. Cpk is a capability index that reflects process centering and variability with respect to specification requirements. The higher the Cpk number, the more capable the process.

B.3.1.2 Critical control parameters. Critical control parameters are parameters whose variability most affect a design, process, or material.

B.3.1.3 Customer compliance matrix (CCM). The CCM documents the relationship between each customer requirement for a specific product, and the method used to assure that customer requirements will be achieved. The CCM will document the correlation between alternative methods used by the manufacturer and the verification methods of Appendix B including any changes, and justification for any changes, made to the design requirements.

B.3.1.4 Design analysis. Design analysis is an evaluation of critical performance parameters and/or design data to determine a design/process/material combination that guarantees compliance to a specific requirement without testing.

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B.3.1.5 Design of experiments (DOE). DOE is a formal plan for conducting experiments which may be used to make achievement of a specific requirement less sensitive to process/material variability. Typical examples include: Taguchi, Central Composite Design, and factorial designs.

B.3.1.6 Design robustness. Design robustness is insensitivity of a design to uncontrollable variation so that it does not significantly affect the product or process once it is in routine operation.

B.3.1.7 Off-line reliability assessment. Off-line reliability assessment is the use of statistically based methods to monitor reliability data. This data may be used to control future adjustments to the design/process/material.

B.3.1.8 Periodic capability certification. Periodic capability certification is the calibration and certification of equipment and/or process steps for an individual parameter(s) such that it can be used as an alternative method to detection testing.

B.3.1.9 Quality function deployment (QFD). QFD is a technique for analysis of the interrelationships between different requirements. These interrelationships are evaluated in a decision making matrix developed through concurrent engineering.

B.3.1.10 Standard Evaluation circuit (SEC). An SEC is a test coupon/device that is representative of actual product. The SEC may be actual product or may be specifically designed to evaluate a particular process. The SEC should be processed using the same processes, equipment, and type of material as the product it represents.

B.3.1.11 Statistical process control (SPC). SPC utilizes statistical methods to monitor parameters (i.e., process or product) in order to provide early warning of a process fluctuation or shift. Appropriate actions must be taken to maintain a state of statistical control. SPC may be used as a tool to facilitate process improvement.

B.3.2 Quality Management (QM) Program.

B.3.2.1 General. A QM program should be developed and implemented by the manufacturer, documented in the QM Plan, and controlled by the TRB (see B.3.2.3). The QM program should ensure and demonstrate compliance to the minimum performance requirements of this specification and outline a program for continuous improvement. A device manufactured under this option should, as a minimum, be equivalent in form, fit, function, quality, and reliability to a device manufactured in accordance with Appendix C.

B.3.2.2 Implementation. Appendix C should be used as a baseline for the QM program. From that baseline, this option may be implemented incrementally by process, or by product line. After satisfying the minimum requirements for validation, a manufacturer may implement alternative methods for addressing the requirements contained in the baselined (Appendix C) flow while performing detection testing in accordance with Appendix C on the remainder of the processes. The minimum requirements for the QM program which should be reviewed during validation are as follows:

a. A Technology review board (see B.3.2.3).

b. A quality management plan (see B.3.2.4).

c. Process/material confirmation and capability achievement procedures including technology qualification test flows.

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B.3.2.3 Technology review board (TRB). The manufacturer should establish a technology review board and develop the necessary procedures to govern its operation. The manufacturer will be responsible for ensuring that the actions of the TRB result in products that meet all customer and performance requirements. As a minimum, these operating procedures should address the following:

a. Record retention.

b. Minimum organizational membership (see B.3.2.3.1).

c. TRB charter.

d. Responsibilities (see B.3.2.3.2).

e. System for recovery of data used in TRB decisions.

f. TRB meeting structure.

g. Decision making/approval procedures.

h. Distribution of TRB minutes.

B.3.2.3.1 TRB organizational structure. The following functions, as a minimum, should be represented on the manufacturer's TRB: design, material procurement, assembly, test, reliability, and quality assurance. Other personnel with decision making responsibilities affecting the product, its processes, or its production facility should participate as required. The manufacturer should identify those organizations that must be represented on the TRB. A responsible technical representative within each of these organizations should be identified to the qualifying activity.

B.3.2.3.2 TRB responsibilities. The TRB should oversee the manufacturer's qualified line, including the processes and materials that continue to be controlled under Appendix C. The TRB should be responsible for the following:

a. Developing, monitoring, maintaining and controlling the QM program and QM plan, and all supporting documents and data.

b. Managing QM plan implementation.

c. Monitoring and controlling the self audit program.

d. Managing and maintaining the quality improvement programs.

e. Overseeing the process/material confirmation and change control activities.

f. Overseeing the initial process/materials certification/qualification and subsequent maintenance thereof.

g. Reviewing and analyzing data (e.g., Cpk data, defect data, rate of assembly failures, rate of failure returns, and failure analysis results) and taking appropriate action to improve processes. When performance or reliability of shipped microcircuits is called into question, the TRB should provide quick evaluation, appropriate corrective action, and prompt notification of the problem to the qualifying activity.

h. Maintaining records of conditions found and actions taken.

i. Reporting status of the QM program to the qualifying activity (see B.3.2.3.4).

j. Approving alternative methods that modify, substitute, or delete existing methods (e.g., inspection, testing, screening, CI and PI, or design/construction procedures of this specification).

B.3.2.3.3 Records. Records of the TRB's membership, deliberations, and decisions should be maintained; dissenting opinions should be recorded. As a minimum, TRB minutes and associated data should be maintained for 5 years.

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B.3.2.4 Quality management (QM) plan. A plan should be developed that documents the manufacturer's quality management program. This replaces the quality assurance program plan (Appendix A of this specification). The QM plan should comprise of the following, as a minimum:

a. Functional organization chart, including organizational charters.

b. Flow charts for the product from design through delivery, including those processes that are controlled under Appendix C.

c. TRB charter and procedure (see B.3.2.3).

d. Alternative method correlation, confirmation, and implementation procedures and change control procedures (see B.3.2.5).

e. Conversion of customer requirements procedures (see B.3.2.6).

f. Design requirements and procedures (see B.3.2.7).

g. Quality improvement plan (see B.3.2.8).

h. Manufacturing process failure analysis program and corrective action plan (see B.3.2.9).

i. Supplier control procedures (see B.3.2.10).

j. Operator/inspector training program.

k. Cleanliness and atmosphere control program.

l. Index of certified baseline documents (see 6.3.4).

m. Self-audit program and audit results (see B.3.2.11).

n. A specific plan defining the manufacturer's SPC program within the manufacturing process to the requirements of JEDEC Publication 19.

B.3.2.5 Alternative method correlation, confirmation, and implementation procedures. This is the approach by which inspection/testing/screening/CI and PI or design/construction requirements within this specification should be modified, substituted, or deleted. The manufacturer should develop methods for confirmation and maintenance of process and material capability and for verification of design capability under this option. Test methods and design/construction requirements of this specification are intended to address worst case application environments for military product. Any alternate method used in lieu of testing, screening, or design/construction requirements should be approved by the manufacturer's TRB and should document the specific areas of correlation between the alternative method and the specification requirement it replaces (i.e., how it meets the specific application environments of this specification) or if the requirements does not apply to a particular technology (see 3.3.1).

B.3.2.5.1 Correlation, confirmation, and implementation. The following is a typical flow.

a. Identify candidate requirements of this specification for alternative method.

b. Using data, identify any correlations between the candidate requirement and potential alternative method(s).

c. Where correlations exist, develop and document alternative method(s).

d. Accumulate data off-line to confirm the capability of the alternative method(s) to assure meeting the requirement.

e. Submit alternative method(s) for TRB approval.

f. Implement the alternative method(s) as directed by the TRB.

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NOTE: If an alternative method is determined to no longer assure meeting the requirements of this specification, the product should be inspected/screened/tested in accordance with the previous TRB approved baseline, until the required capability is achieved.

B.3.2.5.2 Alternative methods. For each candidate process under this option, the manufacturer should specify and implement alternative methods that should be used to maintain each process/material capability such that it continues to meet the minimum performance requirements of this specification. Examples of alternative methods are design analysis (see B.3.1.4), DOE (see B.3.1.5), off-line reliability assessment (see B.3.1.7), periodic capability certification (see B.3.1.8), SPC (see B.3.1.11), embedded machine controls, manufacturer derived test methods, automated methods with feedback controls, etc.

B.3.2.5.2.1 Standard evaluation circuits. A manufacturer may utilize SEC's (see B.3.1.10) to evaluate the capability of alternative methods and monitor product performance. The SEC design should be approved by the TRB and controlled through the manufacturer's documentation system. SEC documentation should include construction, dimensions, intended application (i.e., the processes it evaluates), and minimum acceptable limits (e.g., mechanical or electrical values).

B.3.2.5.2.2 Periodic assessment of alternative methods. Alternative methods should be periodically assessed, as necessary (determined and documented by the TRB), to assure their continued effectiveness. This periodic assessment is a tool for the TRB to aid in monitoring and maintaining product quality. Methods for periodic assessment may include stress-to-failure tests, failure mode analysis, analytic prediction modeling, etc. If an alternative method is determined to no longer meet the initial requirement (i.e., Appendix C), the manufacturer should implement the appropriate previous TRB-approved baselined inspection/screening/testing/step.

B.3.2.5.3 Change control program. The manufacturer should develop a program that defines how changes are made to processes and materials.

B.3.2.6 Conversion of customer requirements. The manufacturer should develop a system by which customer requirements and all requirements of this specification are converted into working instructions. As part of the conversion of customer requirements process the manufacturer should generate a CCM (see B.3.1.3) for each product that documents the means by which the end-item quality, reliability, and customer/specification requirements should be met. Required process capabilities and specific internal documents used by the manufacturer to control, monitor, or assess processes and materials should be specified in the CCM. The CCM should be approved by the TRB and procuring activity. The TRB should ensure that the CCM is kept current.

B.3.2.7 Design requirements. The manufacturer should develop an approach for device design. The design approach should include the following:

a. Design guidelines/handbook. The design guidelines should define the manufacturer's qualified processes and materials as they relate to the design including the interactions between the application environment and affected materials/processes. Any design requirement not in accordance with this specification should be recorded. These guidelines should form the basis for all designs to be manufactured under the QM program.

b. Design models/procedures for worst case temperature and electrical extremes.

c. Rules check procedures, covering the following areas, as applicable:

   1. Design rules check (DRC) - geometric and physical.

   2. Electrical rules check (ERC) - shorts and connectivity.

   3. Reliability rules - Electromigration and current density, IR drops, latchup, single event upset (SEU), hot electrons, ESD, burnout, or backgating, as applicable.

   4. RHA rules - applicable radiation environments.

d. Thermal design verification procedures.

e. Reliability design verification procedures. Worst case circuit design.

f. Package design performance verification procedures.

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g. Feedback loop from design/material/process development activities into design guidelines.

B.3.2.8 Quality improvement program. The manufacturer should develop and implement a program for continuous quality and reliability improvement of processes.

B.3.2.9 Failure analysis and corrective action program. The manufacturer should develop the procedures for testing, analyzing, and taking corrective actions on failed parts from all stages of manufacturing, including field returns. The program should include the specific steps to be followed in order to correct any process that is out of control.

B.3.2.10 Supplier control program. The capability of supplied material may be validated through a supplier certification system. This system selects and monitors suppliers in order to guarantee that the supplied material should meet and maintain required capability levels (e.g., Cpk, ppm, etc.). Supplier certification is granted based on consistent proof that their product conforms to the specification requirements, through implementation of SPC and quality control systems analogous to those herein. Conventional element evaluation is not required when the elements are purchased from certified suppliers. Material may be procured from vendors who are not certified; such material should be evaluated in accordance with Appendix B of this specification or alternative methods approved by the TRB. The following are the minimum documentation requirements for each supplier controlled under this program:

a. A description of the vendor quality assurance plan with status update reports as required by the TRB.

b. A description of the procedure used by the vendor for notification of changes in materials or processes.

c. A quality assurance procedure that can be performed by either the vendor or the manufacturer, or a combination of the two.

B.3.2.11 Self audit program. The manufacturer should develop and implement a self audit program, in accordance with appendix A, to assess the effectiveness of the QM program. The self audit program should be approved, monitored, and controlled by the manufacturer's TRB.

B.3.3 Requirements for approval of qualified manufacturers. Qualification requires validation of the manufacturer's QM program and systems per the qualifying activity, and qualification of the manufacturer's processes and materials per the qualifying activity.

B.4 PERFORMANCE VERIFICATION

B.4.1 Responsibility for compliance. All items should meet all requirements of section B.3 of this appendix and section 5 of this specification.

B.4.2 General product requirements. All product manufactured and delivered in compliance with this appendix should be produced in accordance with the QM plan (see B.3.2.4).

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APPENDIX C

GENERIC PERFORMANCE VERIFICATIONS FOR HYBRID AND MULTICHIP MODULE TECHNOLOGIES

C.1 SCOPE

C.1.1 Scope. This appendix is intended to be used by manufacturers in developing their baseline flow of processes, tests, and inspections. This appendix provides an acceptable standard which may be used to verify the performance requirements of compliant devices. Compliance with this appendix is not mandatory, however, manufacturers must be able to demonstrate a test and inspection system that achieves at least the same level of quality as could be achieved by complying with this appendix. These standards may be used as is, or as modified in accordance with 3.3.1. For new technologies (i.e., MCMs, stacked die, etc.) Appendix D should be used as a guide in developing an acceptable test plan. This test plan should be based on the verifications of this appendix, modified as necessary. Appendix D also contains a flow used to qualify new and existing processes and materials. This appendix is adapted from Options 1 and 2 of MIL-H-38534B.

C.1.2 Description of appendix C. This appendix contains the standard testing and inspection approach to verifying the performance requirements of this specification. This approach is a four step approach consisting of an element evaluation program, a process control program, a screening program, and a Conformance Inspection (CI) and Periodic Inspection (PI) program.

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C.2 APPLICABLE DOCUMENTS

C.2.1 Government specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issue of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

MILITARY

MIL-S-19500 - Semiconductor Devices, General Specification for.

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-202 - Test Methods for Electronic and Electrical Component Parts.

MIL-STD-750 - Test Methods for Semiconductor Devices.

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

MIL-STD-977 - Test Methods and Procedures for Microcircuit Line Certification.

(Unless otherwise specified copies of military standards are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

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C.3 ELEMENT EVALUATION

C.3.1 Description of element evaluation. Element Evaluation is a methodology used to verify that procured materials and devices are adequate to perform as intended under the conditions experienced in the application. These evaluations should be completed on all materials purchased from outside sources, and prior to their use in production devices (see Table I). Element acquisition documents will identify element characteristics required to assure device performance and assembly process capability.

Note: When approved by the acquiring activity, elements may be assembled into the device prior to final element lot acceptance. However, the hybrid manufacturer will have a system, approved by the qualifying activity, to maintain traceability of all such elements for purposes of recall. This system should be employed only when a work stoppage situation is encountered or when a lengthy test is required. Element evaluation will be successfully completed prior to device shipment. The conditional acceptance system should address the following considerations:

a. Element quality and reliability history.

b. Device quality and reliability history.

c. Supplier history.

d. Supplier/manufacturer relationship.

e. Possible impact of element evaluation failure after assembly.

C.3.2 General.

C.3.2.1 Sequence of testing. Subgroups within a group (table) of tests may be performed in any sequence, but individual tests within a subgroup will be performed in the sequence indicated.

C.3.2.2 Sample selection. Samples will be randomly drawn from inspection lots or in-line production samples as applicable. The sample size columns in the evaluation tables give minimum quantities to be evaluated with applicable accept number enclosed in parentheses.

C.3.2.3 Class requirements. Class K and class H element evaluation requirements are identified by X's in the appropriate column locations of evaluation tables.

C.3.2.4 Location of element evaluation. Element evaluation may be performed at the element supplier facility (or other facility approved by the device manufacturer) or at the device manufacturing facility.

TABLE I. Element evaluation summary.

Element	Paragraph	Table or MIL-STD-883, method
Microcircuit and semiconductor dice	C.3.3	See table II
Passive elements	C.3.4	See table III
Saw elements	C.3.5	See table IV
Alternate ICD evaluation	C.3.6	N/A
Substrates	C.3.7	See table V
Packages	C.3.8	See table VI
Adhesives	C.3.9	Method 5011

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C.3.2.5 Characteristics. Characteristics to be verified will be those necessary for compatibility with the element acquisition documents and assembly procedures and at least those which cannot be verified after assembly, but could cause functional failure.

C.3.2.6 Protection from electrostatic discharge. Suitable handling precautions and grounding procedures will be taken to protect ESDS elements from accidental damage.

C.3.2.7 Electrical test specifications. Electrical test parameters, values, limits (including deltas when applicable), and conditions will be specified in the element acquisition documents.

C.3.3 Microcircuit and semiconductor dice. Microcircuit and semiconductor dice from each wafer lot will be evaluated in accordance with table II and C.3.3.1 through C.3.3.7.2. For class H devices, element evaluation testing is not required for JANHC or JANKC discrete semiconductors which have been tested in accordance with MIL-S-19500, appendix H. For class K devices, element evaluation is not required for JANKC discrete semiconductor devices which have been tested in accordance with MIL-S-19500, appendix H. Element evaluation is not required for MIL-I-38535 qualified die.

C.3.3.1 Subgroup 1, 100 percent electrical test of dice. Each die will be electrically tested, which may be done at the wafer level provided all failures are identified and removed from the lot when the dice are separated from the wafer. When wafer/die level testing requirements are not specified in the procurement documents the manufacturer/die supplier will choose the parameters, conditions, and limits to assure compliance with the electrical characteristics.

C.3.3.2 Subgroup 2, 100 percent visual inspection of dice. Each die will be visually inspected to assure conformance with the applicable die related requirements of MIL-STD-883, method 2010; MIL-STD-750, methods 2072 and 2073; and the element acquisition documents.

C.3.3.3 Sample evaluation of assembled dice.

C.3.3.3.1 Test samples. A sample of dice from each wafer lot will be evaluated in accordance with table II, subgroups 3 through 7 as applicable, and C.3.3.3.2 through C.3.3.7.2.

C.3.3.3.2 Test sample preparation. Test samples will be assembled into suitable packages such that the assembly methods and conditions the element will see during normal production assembly will be simulated.

C.3.3.4 Subgroups 3 and 4.

C.3.3.4.1 Sample size. The class K sample will consist of 3 die from each wafer and a total of at least 10 die from each wafer lot. The class H sample will consist of at least 10 die from each wafer lot.

C.3.3.4.2 Internal visual. Each sample will be visually inspected after assembly to assure conformance with the applicable requirements of MIL-STD-883, method 2010; MIL-STD-750, methods 2072 and 2073; and the element acquisition documents.

C.3.3.4.3 Electrical test. For interim, post burn-in, and final electrical tests, the minimum requirements for microcircuits and semiconductor dice will include static tests at each of the following:

a. +25°C.

b. Maximum rated operating temperature.

c. Minimum rated operating temperature.

NOTE: Final electrical tests satisfy end point electrical test requirements specified in preceding test methods and need not be repeated.

C.3.3.5 Subgroup 5.

C.3.3.5.1 Sample size. From each wafer lot, a sample of at least 5 die requiring 10 bond wires minimum will be selected.

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C.3.3.5.2 Wire bond strength testing. For wire bond strength testing:

a. A minimum of 10 wires consisting of die-to-package, die-to-die, or die-to-substrate bonds will be destructively pull tested. An equal number of bonds will be tested on each sample die.

b. For beam lead and flip-chips, five devices shall be tested.

c. The die metallization shall be acceptable if no failure occurs. If only one wire bond fails, another sample shall be selected in accordance with C.3.3.5.1 and subjected to subgroup 5 evaluation. If the second sample contains no failures, the bonding test results are acceptable and the lot of dice is acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the lot of dice shall be rejected.

d. The rejected wafer lot may be resubmitted to subgroup 5 evaluation if the failure was not due to defective die metallization.

C.3.3.6 Subgroup 6, scanning electron microscope (SEM).

C.3.3.6.1 Sample selection and reject criteria. Sample selection and reject criteria shall be in accordance with MIL-STD-883, method 2018. Alternatively, SEM testing may be performed on a sample of eight randomly selected dice from each wafer. In cases when dice are very large and comprise a large area of the wafer, the qualifying activity may approve other alternate sample selection plans.

C.3.3.7 Subgroup 7, radiation testing.

C.3.3.7.1 Class K sample size. The class K sample requires 3 dice from each wafer and a minimum of 10 dice from each wafer lot.

C.3.3.7.2 Radiation testing requirement. Radiation testing is required when applicable to the microcircuit device.

a. For dose rate and latchup, photo current and latch-up effects are functions of circuit configurations and thus should be simulated during tests.

b. The sample will be equally divided between MIL-STD-883, methods 1017 and 1019.

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TABLE II. Microcircuit and semiconductor dice evaluation requirements.

Subgroup	Class		Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	K	H		Method	Condition		
1	x	x	Element electrical			100 percent	C.3.3.1
2	x	x	Element visual	2010 2072 1/ 2073 1/		100 percent	C.3.3.2
3	x	x	Internal visual	2010 2072 1/ 2073 1/		10 (0)	C.3.3.3 C.3.3.4.2
4	x		Stabilization bake	1008	C	10 (0) 2/	C.3.3.3
	x		Temperature cycling	1010	C		
	x		Mechanical shock or Constant acceleration	2002 2001	C, Y1 direction B, Y1 direction		
	x		Interim electrical				C.3.3.4.3
	x		Burn-in	1015	240 hours minimum at +125°C		
	x		Post burn-in electrical				C.3.3.4.3
	x		Steady-state life	1005			
	x	x	Final electrical				C.3.3.4.3
5	x	x	Wire bond evaluation	2011		10(0) wires or 20(1) wires	C.3.3.3 C.3.3.5
6	x		SEM	2018		See method 2018	C.3.3.6
7	x		Radiation				C.3.3.7
	x		Dose rate and latch-up	1020		10 (0)	
	x		Total dose	1019		5 (0)	
	x		Neutron irradiation	1017		5 (0)	

1/ MIL-STD-750 methods.

2/ For Class K sample sizes see C.3.3.4.1.

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C.3.4 Passive elements. Passive elements from each inspection lot will be evaluated in accordance with table III and C.3.4.1 through C.3.4.6. This evaluation is not required when the elements are acquired from the Established Reliability series of military specifications and the element meets or exceeds the evaluation requirements of this specification and is listed on the QPL.

C.3.4.1 Subgroup 1, 100 percent electrical test of passive elements. Each passive element will be electrically tested at +25°C as specified in the element acquisition documents.

C.3.4.2 Subgroup 2, visual inspection of passive elements. Passive elements will be visually inspected to assure conformance with the applicable passive element related requirements of MIL-STD-883, method 2032, and the passive element acquisition documents.

a. Each class K passive element will be visually inspected.

b. Class H elements will be sample inspected using a sample size and (accept number) of 22 (0).

C.3.4.3 Test sample preparation for subgroups 3 and 4.

a. For class H and K passive elements, when assembly is required to perform electrical tests, test samples will be assembled into suitable packages such that the assembly methods and conditions the element will see during normal assembly will be simulated.

b. The total test sample will contain at least 20 wire bonds (an equal number on each element) if wire bonding assembly is applicable.

C.3.4.4 Sample electrical test of passive elements. Sample passive elements will be electrically tested at +25°C for the following characteristics (minimum):

a. Resistors: DC resistance.

b. Capacitors:

(1) Ceramic type: Dielectric withstanding voltage, insulation resistance, capacitance, and dissipation factor.

(2) Tantalum type: DC leakage current, capacitance, and dissipation factor.

(3) Metal insulation semiconductor type (MIS): DC leakage current, capacitance, dielectric withstanding voltage.

c. Inductors: DC resistance, inductance, and Q.

C.3.4.5 Visual examination. Elements will be visually examined for evidence of corrosion or damage attributable to the test and conditioning sequence.

C.3.4.6 Wire bond strength testing. Wire bond strength testing applies to elements which are wire bonded during the device assembly operation. The sample will include at least 5 elements and 10 bond wires minimum.

a. At least 10 wires, consisting of element-to-substrate, element-to-package, or element-to-element bonds will be destructively pull tested. An equal number of bonds will be tested on each sample element.

b. The element metallization will be acceptable if no failure occurs. If only one wire bond fails, a second sample will be selected and subjected to the test in accordance with C.3.4.6a. If the second sample contains no failures, the bonding test results and the element lot are acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the element lot will be rejected.

c. The element inspection lot may be resubmitted to evaluation if the failure was not due to defective element metallization.

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TABLE III. Passive element evaluation requirements.

Subgroup	Class		Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	K	H		Method	Condition		
1	x	x	Element electrical			100 percent	C.3.4.1
2	x		Visual inspection	2032		100 percent	C.3.4.2
		x		2032		22(0)	C.3.4.2
3	x		Stabilization bake	1008	C	10 (0)	C.3.4.3
	x		Temperature cycling	1010	C		
	x		Mechanical shock	2002	B, Y1 direction		
			or				
	x		Constant acceleration	2001	A, Y1 direction		
	x		Voltage conditioning				C.3.2.7
			or				
	x		Aging (capacitors)				
	x		Visual inspection	2017			C.3.4.5
	x	x	Electrical				C.3.4.4
4	x	x	Wirebond evaluation	2011		10(0) wires or 20(1) wires	C.3.4.3 C.3.4.6

C.3.5 Surface acoustic wave (SAW) element evaluation. SAW elements will be evaluated in accordance with table IV and C.3.5.1 through C.3.5.3.

C.3.5.1 RF probe test. Each SAW element will be RF probe tested as specified in the detail/acquisition specification. This RF probe test may be done at the wafer level provided all failures are identified and removed from the lot when the elements are separated from the wafer. RF probe testing will be performed at +25°C unless otherwise specified by the detail/acquisition specification.

C.3.5.2 Visual inspection. Each SAW element will be visually inspected to assure conformance with the requirements of MIL-STD-883, method 2032.

C.3.5.3 Wire bond evaluation. From each inspection lot of SAW elements, a randomly selected sample of at least two elements will be evaluated for wire bond pull strength. A minimum of 10 wires will be destructively pull tested in accordance with MIL-STD-883, method 2011. The SAW element metallization will be acceptable if no failure occurs. If only one wire fails, another sample will be selected and a minimum of 10 wires will be destructively pull tested in accordance with method 2011. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the lot of SAW elements will be rejected. The rejected lot may be resubmitted to wire bond evaluation if the failure was not due to defective metallization. With acquiring activity approval, destructive bond pull tests may be performed on test coupons which provide the specified test requirements. Test coupons must be processed with the same element production lot.

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TABLE IV. SAW element evaluation requirements.

Subgroup	Class		Test	MIL-STD-883		Quantity	Reference paragraph
	K	H		Method	Condition		
1	x	x	RF electrical probe			100 percent	C.3.5.1
2	x	x	Visual inspection	2032		100 percent	C.3.5.2
3	x	x	Wire bond evaluation	2011		10 (0) wires or 20 (1) wires	C.3.5.3

C.3.6 Alternate Integrated Circuit Die (ICD) Evaluation. Alternate ICD evaluation will be used only in cases where complex ICD testing is impractical outside the actual end item (i.e., device). The ICD sample built into devices must successfully complete evaluation prior to release of the balance of the incoming lot. Acquiring activity approval must be obtained prior to implementation of this alternate procedure. In lieu of packaged element evaluation tests in accordance with C.3.3, C.3.4, and C.3.5 ICD's may be assembled into devices and acceptance of these elements will be based on the ability of the device to meet all group A, subgroups 1, 2, and 3 (plus 4, 7, and 9 as applicable) electrical tests required for the device. A minimum of 10 ICD's (0 defects) will be assembled into at least 3 devices. Devices assembled for the purpose of element evaluation are deliverable provided all of the provisions of this specification are met. Element wire bond evaluation for ICD's may be accomplished using a second or additional sample of elements wire bonded for that purpose only. When the device build option for ICD evaluation is selected, the manufacturer will establish and maintain a sample plan or procedure to identify the sample prior to electrical test. In case of lot failure when alternative ICD evaluation is used, all of the device samples and the ICD inspection lot will be rejected. When the manufacturer chooses to analyze the failed devices to isolate the cause of failure and this analysis determines that the cause of failure is not related to the ICD being tested and that the ICD has been correctly stressed during the required screening and testing, then the ICD inspection lot may be accepted. If the ICD has not been correctly stressed, the failed device may be reworked or new sample replacement devices may be assembled.

C.3.7 Substrate evaluation. Substrates will be evaluated in accordance with table V and C.3.7.1 through C.3.7.5.3.3.

NOTE: Substrates fabricated by the device manufacturer using a qualified process will be exempt from this evaluation.

C.3.7.1 Definition. For the purpose of substrate evaluation, a substrate inspection lot will consist of homogeneous substrates having the same number of layers, manufactured using the same facilities, processes, materials, and vacuum deposited, plated or printed as one lot.

C.3.7.2 Electrical test parameters. Electrical test parameters, values, limits, and conditions will be as specified in the applicable detail/acquisition specification.

C.3.7.3 Subgroup 1, 100 percent electrical testing. Each substrate will be electrically tested at +25°C, if and as specified in the applicable detail/acquisition specification.

C.3.7.4 Subgroup 2, 100 percent visual inspection. Each substrate will be visually inspected to assure conformance with the applicable requirements of MIL-STD-883, method 2032, and the applicable detail/acquisition specification.

C.3.7.5 Subgroups 3, 4, and 5 general requirements. From each inspection lot of substrates, a randomly selected sample will be evaluated. With acquiring activity approval, destructive tests may be performed on test coupons which provide the required test data. The test coupons must be made with the same materials that were used in the manufacturing of the inspection lot and processed at the same time as the inspection lot.

C.3.7.5.1 Subgroup 3. A minimum of five samples will be submitted to subgroup 3 testing.

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C.3.7.5.1.1 Physical dimension. Inspect in accordance with MIL-STD-883, method 2016, and the applicable detail/acquisition specification.

C.3.7.5.1.2 Visual inspection. Inspect in accordance with MIL-STD-883, method 2032, and the applicable detail/acquisition specification.

C.3.7.5.1.3 Electrical. Substrates will be electrically tested at +25°C for the following characteristics (minimum). Requirements will be as specified in the applicable detail/acquisition specification.

a. Resistors: DC resistance.

b. Capacitors: Capacitance. As specified in the applicable detail/acquisition specification, test for dielectric withstanding voltage, insulation resistance, and dissipation factor.

c. For multilayered substrates, continuity and isolation testing will be performed to verify the interconnection of conductors as specified in the applicable detail/acquisition specification.

C.3.7.5.2 Subgroup 4. A minimum of three samples that have been subjected to, and passed, subgroup 3 testing will be submitted to subgroup 4 testing.

C.3.7.5.2.1 Conductor thickness. Measure conductor thickness in accordance with the applicable detail/acquisition specification. Conductor thickness will meet the requirements specified in the applicable detail/acquisition specification.

C.3.7.5.2.2 Conductor resistivity. Measure conductor resistivity in accordance with the applicable detail/acquisition specification. Conductor resistivity will meet the requirements specified in the applicable detail/acquisition specification.

C.3.7.5.2.3 Film adhesion. Perform film adhesion testing in accordance with MIL-STD-977, method 4500. The substrate and tape will show no evidence of peeling or flaking of metallization.

C.3.7.5.2.4 Solderability. For solderable substrates only, perform solderability testing if specified in the applicable detail/acquisition specification in accordance with the applicable detail/acquisition specification.

C.3.7.5.3 Subgroup 5. A minimum of two samples that have been subjected to, and passed, subgroup 3 testing will be submitted to subgroup 5 testing.

C.3.7.5.3.1 Temperature coefficient of resistance (TCR): When specified in the applicable detail/acquisition specification, perform TCR testing for resistors in accordance with MIL-STD-202, method 304. TCR will meet the requirements specified in the applicable detail/acquisition specification.

a. Thick film type: Test as a minimum, two resistors from each resistor paste sheet resistance value. One from the smallest and one from the largest area resistors at -55°C using a reference reading at +25°C, or temperatures as specified in the detail/acquisition specification.

b. Thin film type: Test as a minimum, the highest value resistor at +125°C using a reference reading at +25°C or temperatures as specified in the detail/acquisition specification.

c. If specified in the applicable detail/acquisition specification, TCR tracking testing will be performed. TCR tracking will meet the requirements specified in the applicable detail/acquisition specification.

C.3.7.5.3.2 Wire bond strength testing. For wire bondable substrates, perform wire bond strength testing in accordance with MIL-STD-883, method 2011. The sample will include at least 2 substrates and 10 bond wires minimum. For gold metallized class K substrates that at the device level are intended to contain aluminum wire bonds, aluminum wires will be placed as specified in the detail/acquisition specification and these wire bond samples will be baked for 1 hour at +300°C in either an air or an inert atmosphere prior to the performance of wire bond strength testing.

a. At least 10 wires, consisting of substrate to substrate bonds, will be destructively pull tested. An equal number of bonds will be tested on each sample substrate.

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b. The substrate metallization will be acceptable if no failure occurs. If only 1 wire bond fails, a second sample of a minimum of 10 wires will be prepared using the same wire type/size and the same type equipment as the failed bond(s). If the second sample contains one or more failures, or if more than one failure occurs in the first sample, then the substrate inspection lot will be rejected.

c. The substrate inspection lot may be resubmitted to evaluation if the failure(s) was not due to defective substrate metallization.

C.3.7.5.3.3 Die shear strength testing. Perform shear strength testing in accordance with MIL-STD-883, method 2019. At least two die per substrate will be attached and tested for each die attachment method, as specified in applicable detail/acquisition specification. If a failure occurs at less than the specified force and is not due to defective substrate materials, the lot will be resubmitted to die shear evaluation and the failure mode documented.

TABLE V. Substrate evaluation requirements.

Subgroup	Class		Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	K	H		Method	Condition		
1	x	x	Electrical testing			100 percent	C.3.7.3
2	x	x	Visual inspection	2032		100 percent	C.3.7.4
3	x	x	Physical dimensions	2016		5 (0)	C.3.7.5.1.1
	x	x	Visual inspection	2032			C.3.7.5.1.2
	x	x	Electrical				C.3.7.5.1.3
4	x	x	Conductor thickness or conductor resistivity			3 (0)	C.3.7.5.2.1 or C.3.7.5.2.2
	x	x	Film adhesion test				C.3.7.5.2.3
	x	x	Solderability				C.3.7.5.2.4
5	x	x	TCR			2 (0)	C.3.7.5.3.1
	x	x	Wire bond evaluation	2011		10 wires (0) 20 wires (1)	C.3.7.5.3.2
	x	x	Die shear evaluation	2019		2 (0)	C.3.7.5.3.3

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C.3.8 Package evaluation. Package cases or covers will be evaluated in accordance with table VI and C.3.8.1 through C.3.8.5. In addition, laser marked surfaces will be subjected to and pass subgroups 3, 5, and 6.

C.3.8.1 Definition. For the purpose of package evaluation, a package inspection lot will consist of homogeneous cases or covers of the same package type and outline dimensions (may differ only in lead length and lead count); manufactured using the same facilities and processes; and plated as one lot (if plating is applicable).

C.3.8.2 General.

a. From the initial package inspection lot, a randomly selected sample will be subjected to package evaluation.

b. Subgroups 1, 2, and 3 of table VI will be accomplished for each lot. The remainder of table VI will be accomplished periodically at intervals not exceeding 6 months for additional package inspection lots, except as noted in C.3.8.5 herein.

c. Subgroups 2, 3, and 4 of table VI apply to cases only. A quantity (accept number) of 15 (0) will apply to the number of terminals or leads to be tested. The leads will be randomly selected from three packages minimum.

C.3.8.3 Subgroup 1. Separately verify case and cover dimensional compliance with the element acquisition documents.

C.3.8.4 Subgroup 4. For metal cases with leads separated by an insulator, measure insulation resistance between the metal body of the case and the leads that are isolated from the case. This test does not apply to non-metallic cases. This test will be performed at 6-month intervals unless a change in insulator material is made for class H devices and on every incoming lot for class K devices.

C.3.8.5 Subgroups 5 and 6. Separately verify case and cover for compliance with subgroups 5 and 6. Corrosion in the internal cavity area will not be cause for rejection. This test will be performed one time only for class H and at 6-month intervals for class K unless a change in material or plating is made.

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TABLE VI. Package evaluation requirements.

Subgroup	Class K	Class H	Test	MIL-STD-883 Method	MIL-STD-883 Condition	Quantity (accept number)	Reference paragraph
1	x	x	Physical dimensions	2016		3 (0)	C.3.8.3
2	x	x	Solderability	2003	Soldering temperature +245°C ±5°C	3 (0)	C.3.8.2c
3	x	x	Thermal shock	1011	C	3 (0)	C.3.8.2
	x	x	High temperature bake	1008	1 hour at +150°C		
	x	x	Lead integrity	2004	B2 (lead fatigue) D (leadless chip carriers)		
				2028	(Pin grid array leads and rigid leads)		
	x	x	Seal	1014	A4 Unlidded cases		
4	x	x	Metal package isolation	1003	600 V dc 100 nA maximum	3 (0)	C.3.8.4
5	x	x	Moisture resistance	1004		5 (0)	C.3.8.5
6	x	x	Salt atmosphere	1009	A	5 (0)	C.3.8.5

C.3.9 Adhesive evaluation. The polymeric adhesives used in device applications will be subjected to and pass the evaluation procedures detailed in MIL-STD-883, method 5011.

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C.4 PROCESS CONTROL

C.4.1 Description of process control. Process control is a methodology used to detect defective processes prior to completion of assembly. This section outlines the requirements for process control on two processes though process control may be applied to other areas. The indicated processes will be controlled in accordance with table VII and C.4.2 through C.4.3.

TABLE VII. Process control summary.

Operation	Class		MIL-STD-883		Paragraph
	K	H	Method	Condition	
Wire Bonding	X X	X X	2011 2023		C.4.2
Seal	X		1014	A, 1×10^{-8} atm/cc He	C.4.3

C.4.2 Wire bonding.

C.4.2.1 General. A process machine operator evaluation will be performed:

a. When a machine is put into operation.

b. Periodically while in operation, not to exceed 4 hours.

c. When the operator is changed. Change of certified auto wirebond operators is allowed without machine reevaluation if all other machine conditions for evaluation are maintained.

d. When any machine part has been changed.

e. When any machine adjustment of the process parameters has been made.

f. When the spool of wire is changed.

g. When a new device type is started (unless the machine was evaluated using test samples that also simulate the new device type, see C.4.2.2).

C.4.2.2 Standard evaluation circuit (test coupon or test vehicle). Standard evaluation circuits (test coupons or test vehicles) that simulate the production device metal bonding system (e.g., thick film, thin film, aluminum bonding pads, plated gold) may be destructively evaluated in lieu of the product.

C.4.2.3 Process machines. Process machines not meeting the evaluation requirements will not be used.

C.4.2.4 Corrective action of process machine. A process machine may be returned to operation only after appropriate corrective action has been implemented and the machine has been evaluated and passed testing in accordance with table VII as required.

C.4.2.5 Data record. A data record will be maintained and identifiable to each machine, operator, shift, and date of test.

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C.4.2.6 Wire bonding.

C.4.2.6.1 Process machine/operator evaluation. Sample wires from three devices or a test sample will be destructively pull tested in accordance with MIL-STD-883, method 2011 and as follows:

a. Class H devices: A minimum of 10 wires total consisting of wire bonds to elements metalization bonding systems (e.g., thick film, thin film, aluminum bonding pads, plated gold) typical of device assembly operation will be tested.

b. Class K devices: A minimum of 15 wires total will be tested. As a minimum, wires tested will include one each from a typical transistor, diode, capacitor, and resistor die, and five wires from the header to the substrate, as applicable.

c. Requirements classes H and K: Evaluation results are acceptable if no failure occurs at less than the value given in table I of MIL-STD-883, method 2011. If any of the sample wires fail, the machine/operator will be deactivated and corrective action taken. When a new sample has been prepared, tested, and has passed this procedure, the machine/operator has been certified or recertified, it can be returned to service.

C.4.2.6.2 Lot sample bond strength. From each wire bonding lot, a sample of at least two devices will be nondestructively tested in accordance with MIL-STD-883, method 2023. This requirement does not apply to devices that are 100 percent nondestructively tested. Alternately, destructive pull testing in accordance with method 2011 may be performed. Devices with known visual wire bonding rejects will not be excluded from this sample.

a. A wire bonding lot consists of devices that are consecutively bonded using the same setup and wire, by one machine/operator (operator changes are allowed for autobonders) during the same period not to exceed 4 hours.

b. In each sample device, at least 15 wires will be tested, including 1 wire from each type of transistor, diode, capacitor, and resistor chips, 3 wires from each type of integrated circuit, and 5 wires connecting package leads, as applicable. If there are less than 15 wires in the device, all wires will be tested. Sample devices will be inspected for lifted wires. Lifted wires resulting from bond pull testing will be counted as nondestruct pull test failures.

c. The wire bonding lot will be acceptable if no failure occurs. If one wire/bond fails, another sample of two devices will be selected and 100 percent nondestructively tested. If the second sample contains no failures, the wire bonding lot is acceptable. If the second sample also contains failure(s), or more than one wire/bond fails in the first sample, the bonding machine/operator will be removed from the operation.

d. The failures will be investigated and appropriate corrective action will be implemented. The machine/operator will be recertified in accordance with C.4.2.6.1 before being returned to operation. All devices bonded since the previous certification (lot sample bond strength test) will be subjected to 100 percent nondestructive bond strength testing (class H).

e. For RF/microwave devices, test sample circuits that simulate the production device may be destructively evaluated in lieu of the product (see C.4.2.2). When test sample circuits are used, the data from this test will be used for SPC monitoring of the process/product.

C.4.3 Seal testing. All class K devices will receive fine leak testing, without pressurization (bomb) immediately after sealing and prior to any other test. Class K devices are sealed with a minimum 10 percent helium tracer gas atmosphere. If a failure occurs, the lid seal rework requirements will be followed.

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C.5 DEVICE SCREENING

C.5.1 Description of device screening. Screening is a series of tests and inspections performed on each device in each lot in order to eliminate products which do not meet the performance requirements. Each device will be subjected to and pass all of the applicable screening tests and inspections in accordance with Table VIII and C.5.2 through C.5.12.

C.5.2 General.

a. Additional tests and inspections may be performed where experience indicates justifiable concern for specific quality characteristics.

b. Electrical test parameters, values, limits (including deltas), and conditions will be as specified on the acquisition document.

c. All devices that fail any test criterion in the screening sequence will be removed from the lot at the time of observation or immediately at the conclusion of the test in which the failure was observed.

d. When PDA, pattern failure, or delta limits have been specified or other conditions for lot acceptance have been imposed, the required data will be recorded and maintained as a basis for lot acceptance.

e. Once rejected and verified as a device failure, rework and subsequent rescreening in accordance with the limitations of this specification may be performed.

C.5.3 Preseal burn-in test Preseal burn-in is optional, and performance requires the approval of the acquiring activity.

C.5.4 Nondestructive bond pull test for class K Devices. Nondestructive 100 percent bond pull test will be performed for class K devices. The total number of failed wires and the total number of devices failed will be recorded. The lot will have a PDA of 2 percent or one wire, whichever is greater based on the number of wires pulled in the wire bond lot or production lot. Failed lots may be resubmitted one time to 100 percent nondestructive bond pull test with a tightened PDA of 1.5 percent. The test will be performed in accordance with MIL-STD-883, method 2023. Devices from lots which have been subjected to the nondestructive 100 percent bond pull test and have failed the specified class K PDA requirement will not be delivered as class H product.

C.5.5 Internal visual inspection. Devices awaiting preseal inspection and accepted devices awaiting further processing will be stored in a dry, controlled environment until sealed as specified in MIL-STD-883, method 2017.

C.5.6 Visual inspection for damage. The manufacturer may inspect for damage after each thermal or mechanical screening step, or at any subsequent time in the screening sequence.

C.5.7 Particle impact noise detection (PIND) test. When approved by the acquiring activity, PIND testing will not apply to devices with internal conformal coating. PIND will be performed in accordance with test method 2020 of MIL-STD-883, condition A or B. The lot may be accepted on any of the five runs if the percentage of defective devices is less than 1 percent (or one device, whichever is greater). All defective devices will be removed after each run. Lots which do not meet the 1 percent PDA on the fifth run, or exceed 25 percent defectives cumulative, will be rejected.

C.5.8 Preburn-in electrical test.

a. Preburn-in electrical testing is optional except when delta limit measurements are required. However, devices may be tested to remove defects prior to further screening and to form a basis for application of PDA criteria.

b. This test need not include all device parameters, but will include those measurements most sensitive to and effective in removing electrically defective devices.

c. When delta limits are specified in the device acquisition specification, the measurements will be recorded, and traceability will be maintained from the device to the corresponding electrical test data.

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C.5.9 Burn-in. Burn-in will be performed on each device.

C.5.9.1 General.

a. Preburn-in (interim burn-in for class K) and post burn-in electrical parameters as specified in the device acquisition specification will be measured.

b. Burn-in electrical conditions will be as specified in the device acquisition specification.

c. Delta measurements will be made on parameters specified in the device acquisition specification.

C.5.9.2 Burn-in period.

a. Class K devices will be burned-in in accordance with the time-temperature regressions specified in MIL-STD-883, method 1015. The burn-in time will be equally divided into two successive burn-ins. Interim electrical tests in accordance with the device acquisition specification will be performed after the first burn-in to determine acceptable devices for the second burn-in.

b. Class H devices will be burned-in in accordance with the time-temperature regressions specified in MIL-STD-883, method 1015.

C.5.9.3 Failure analysis of burn-in screen failures for class K devices. Catastrophic failures (e.g., shorts or opens measurable or detectable at +25°C) after burn-in will be analyzed. Analysis of catastrophic failures may be limited to a quantity and degree sufficient to establish failure mode and cause. Failure analysis results will be documented and available to the Government representatives.

C.5.9.4 Lots resubmitted for burn-in. Burn-in lots that do not exceed twice the allowable PDA may be resubmitted for burn-in one time only. Resubmitted lots will be kept separate from new lots and will be inspected for all specified characteristics using a tightened inspection PDA equal to the next lower number in the PDA series. The number of pattern failures allowed will be the same as required for the original burn-in.

C.5.9.5 Burn-in acceptance criteria. At the option of the manufacturer, burn-in acceptance will be based on PDA or pattern failures. Either option or both may be applied to a burn-in lot as acceptance criteria (i.e., if a lot exceeds PDA requirements, then pattern failure analysis may be used to determine if the lot is acceptable).

C.5.9.5.1 General. Pattern failures are multiple device failures within a device burn-in lot with the same root cause of failure. The manufacturer will determine and document, prior to beginning burn-in, the criteria for the formation of burn-in lots (e.g., devices submitted to burn-in at one time, a production lot, or an inspection lot) for the purposes of PDA calculation. The burn-in lot will be ≥ 41 devices or all devices submitted to burn-in during a 1-week period, whichever is less. The manufacturer will not conduct burn-in in addition to that specified. Delta limits will be defined in the device acquisition specification when required. When the PDA or pattern failures applies to delta limits, the delta parameter values measured after burn-in (100 percent screening test) will be compared with the delta parameter values measured prior to that burn-in. Unless otherwise specified in the device acquisition specification, PDA, and pattern failure analysis will be applicable only to +25°C static tests (group A, subgroup 1).

C.5.9.5.2 PDA option.

C.5.9.5.2.1 PDA class H. For class H, the PDA will be 10 percent or one device, whichever is greater, regardless of burn-in lot size.

C.5.9.5.2.2 PDA class K. For class K, the PDA will be 2 percent or one device, whichever is greater, regardless of burn-in lot size. Class K PDA will be calculated on failures occurring during the second half of burn-in only.

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C.5.9.5.3 Pattern failure option.

C.5.9.5.3.1 Pattern failure option, class H. For class H devices, when acceptance is based on pattern failures, all multiple device static failures at +25°C must be analyzed to determine root cause. Multiple device failures with the same root cause (three or more depending on lot size) will be considered a "failure pattern". If a failure pattern is established, the lot will be rejected; otherwise, the lot will be accepted regardless of PDA. In all cases, lots with device failures that do not exceed the PDA are acceptable and do not require pattern failure analysis. The number of device failures with the same root cause that establish a failure pattern will be based on lot size, as follows:

Lot size (x)	Number of failures that establish a pattern
$x \le 20$	3
$21 \le x \le 40$	4
$40 < x \le 100$	5
$100 < x \le 300$	6
$300 < x \le 500$	11
$500 < x$	16

Example 1: Lot size is 25 with 4 device static failures at +25°C.

If all 4 device failures do not have the same root cause of failure (i.e., 3 or less failures with the same root cause), then no "failure pattern" exists and the passing 21 devices are acceptable.

If all 4 failures have the same root cause of failure, then a "failure pattern" exists and the lot should be rejected.

Example 2: Lot size is 400 with 15 device static failures at +25°C.

The lot is acceptable (i.e., 10 percent PDA allows 40 device failures).

Example 3: Lot size 400 with 41 device static failures at +25°C.

If 10 or less of the device failures are due to the same root cause, then a "failure pattern "does not exist and the lot is acceptable.

If 11 or more of the device failures are due to the same root cause, then a "failure pattern" has been established and the lot is unacceptable.

In all instances where analysis of the failed devices indicates that the failure mechanism is due to poor basic processing procedures, a basic design fault, or nonscreenable defects, the lot will be rejected.

C.5.9.5.3.2 Pattern failure option, class K. For class K, when acceptance is based on pattern failures, all multiple device static failures at +25°C must be analyzed to determine root cause. The lot will be stopped and placed on hold if:

a. Any two device failures within the burn-in lot have the same root cause of failure (i.e., pattern failure established), or

b. The total number of device failures in the burn-in lot exceeds 5 percent.

The lots may be reworked and recovered if the failure is due to:

a. A defect that can be effectively removed by rescreening the entire burn-in lot or,

b. Random type defects which do not reflect poor basic device design or poor basic processing procedures.

In all instances where analysis of the failed devices indicates that the failure mechanism is due to poor basic processing procedures, a basic design fault, or nonscreenable defects, the lot will be rejected.

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C.5.10 Final electrical test.

a. Final electrical testing will include all parameters, limits, and conditions of test which are specifically identified in the device acquisition specification as final electrical test requirements. As a minimum, final electrical testing will include group A, table IXa, subgroups 1, 2, and 3 (plus 4, 7, and 9 as applicable).

b. Final electrical testing satisfies end-point electrical test requirements specified in the preceding test methods, and need not be duplicated.

C.5.11 Seal (fine and gross leak).

a. For class K devices, the seal test may be performed in any sequence between the final electrical test and external visual, but it will be performed after all shearing and forming operations on the terminals.

b. For class H devices, the seal test will be performed in any sequence between the constant acceleration test and external visual, but it will be performed after all shearing and forming operations on the terminals.

c. For class K and H devices, all device lots (sublots) having any physical processing steps (e.g., solder dipping to the glass seal, etc.) performed following seal or external visual will be retested for hermeticity and visual defects. This will be accomplished by performing, and passing, as a minimum, a sample seal test (MIL-STD-883, method 1014) using an acceptance criteria of a quantity (accept number) of 45(0), and an external visual inspection (MIL-STD-883, method 2009) on the entire inspection lot (sublot). For devices with leads that are not glass sealed and that have a lead pitch less than or equal to 1.27 mm (0.050 inch), the sample seal test will be performed using an acceptance criteria of a quantity (accept number) of 15(0). If the sample fails the acceptance criteria specified, all devices in the inspection lot represented by the sample will be subjected to the fine and gross seal tests and all devices that fail will be removed from the lot for final acceptance.

C.5.12 External visual screen. The final external visual screen will be conducted in accordance with MIL-STD-883, method 2009 after all other 100 percent screens have been performed. The manufacturer will inspect the devices 100% or on a sample basis using a quantity/accept number of 116(0). If one or more rejects occur in this sample the manufacturer may double the sample size with no additional failures allowed or inspect the remaining devices 100% for failed criteria and remove the failed devices from the lot. If the doubled sample also fails, the manufacturer will be required to 100% inspect the remaining devices in the lot for the failed criteria. Reinspection magnification will be no less than that used for the original inspection for the failed criteria.

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TABLE VIII. Device screening.

Test inspection	MIL-STD-883		Requirements		Reference paragraph
	Method	Condition	Class K	Class H	
Preseal burn-in	1030		Optional	Optional	C.5.3
Nondestructive bond pull	2023		100 percent	N/A	C.5.4
Internal visual	2017		100 percent	100 percent	C.5.5
Temperature cycling or thermal shock	1010 1011	C A, minimum	100 percent N/A	100 percent or 100 percent	C.5.6
Mechanical shock or constant acceleration	2002 2001	B, (Y1 direction only) A, (Y1 direction only)	100 percent or 100 percent	100 percent or 100 percent	C.5.6
PIND	2020	A or B	100 percent	N/A	C.5.7
Electrical	In accordance with applicable device specification		100 percent	Optional	C.5.8
Burn-in	1015		100 percent	100 percent	C.5.9
Final electrical test	In accordance with applicable device specification		100 percent	100 percent	C.5.10
Seal a. Fine b. Gross	1014		100 percent	100 percent	C.5.11
Radiographic	2012		100 percent	N/A	
External visual	2009				C.5.12

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C.6 CONFORMANCE INSPECTION AND PERIODIC INSPECTION

C.6.1 Description of Conformance Inspection and Periodic Inspection. Conformance Inspection (CI) and Periodic Inspection (PI) is a series of tests and inspections performed on samples of devices which have passed screening. These tests and inspections are used to further verify the performance requirements on a sample basis. Sample testing is necessary due to the fact that many of these tests are either destructive, expensive, or time consuming. Group A is considered CI, wheras Groups B, C, and D and considered PI. CI and PI will consist of the tests and inspections specified herein. Devices will not be accepted or approved for delivery until all applicable CI and PI requirements have been met. The acquiring activity may approve delivery if groups A, B, C1, C3, and D testing have been completed and group C2, steady state life test, has commenced. The manufacturer will maintain traceability of all devices delivered to the acquiring activity prior to completion of CI and PI testing for the purpose of notification/recall in case of test failure.

C.6.2 General. CI and PI for a given device type is determined by selection of a requirements option flow (see table IX) at the time of contract negotiation and acceptance. The requirements option flow selected will determine the CI and PI requirements for the specific device manufactured. Where applicable, inspection lot sampling will be in accordance with appendix F of this specification. Except where the use of final electrical test rejects or simulation samples (i.e., test coupons or test vehicles) is allowed, all devices will have been previously screened and subjected to and passed all final electrical tests. Successful completion of CI and PI for a given product assurance level will satisfy the requirements for any lower level device manufactured on the same certified line. If a lot is withdrawn in a state of failing to meet requirements and is not resubmitted, it will be considered a failed lot and reported as such.

NOTE: The device manufacturer has the right to elect not to use any solution or solvent identified within this specification or related specifications that has also been identified by the American Congress of Government Industrial Hygienists as being a potential or suspect carcinogen. Where the device manufacturer elects not to use a material, he must notify the acquiring or qualifying activities and the customer in writing in clear, unambiguous language not subject to misinterpretation that this right has been exercised.

TABLE IX. CI and PI summary.

Requirement	Reference	Option 1 (in-line)	Option 2 (end-of-line)
General	Paragraph	C.6.3	C.6.4
Group A (CI)	Paragraph	C.6.3.1	C.6.4.1
	Table	IXa	IXa
Group B (PI)	Paragraph	C.6.3.2	C.6.4.2
	Table	N/A	IXb
Group C (PI)	Paragraph	C.6.3.3	C.6.4.3
	Table	IXc	IXc
Group D (PI)	Paragraph	N/A	C.6.4.4
	Table	N/A	IXd

C.6.2.1 Sample selection. The number of hybrid microcircuits to be tested will be chosen (independent of lot size) by the manufacturer in accordance with the applicable requirements of options 1 or 2 herein. Initial samples and resubmitted samples, when applicable, will be randomly selected from the inspection lot. Lot acceptance is based on an accept number of zero. If a failure occurs, the failed subgroup or test may be performed once using double the sample size or 100 percent with zero failures allowed. For group C inspection, limited sample quantities may be used to meet the requirements of C.6.1 for production start-up. When limited sampling is used for start-up, a subsequent full sample group C test will be performed within 6 months of initial group C or prior to exceeding the limited usage requirements of C.6.3.3.1c, whichever comes first.

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C.6.2.2 End point. Electrical end points will be measured and recorded when applicable.

C.6.2.3 Data. Test results will be recorded by inspection lot identification code or each inspection lot, when applicable. For in-line group B inspections where inspection lots are not applicable, data records or logs will be maintained and available for review by the qualifying and acquiring activities. A summary of attributes results for all tests and measurements will be part of the test report. Variable data will be provided when required by the device acquisition specification.

C.6.2.4 Nonfunctional Samples. Electrically rejected devices from the same inspection lot may be used in all subgroups when end point measurements are not required provided that the devices have been subjected to all device screening conditions through burn-in.

C.6.3 Option 1 (in-line inspection). Option 1 CI and PI will be satisfied by in-line inspections and tests in accordance with C.6.3.1 through C.6.3.4.

C.6.3.1 Group A electrical testing. Group A electrical testing will be performed in accordance with table IXa, C.6.3.1.1 through C.6.3.1.4 and the applicable device acquisition specification.

C.6.3.1.1 Group A general requirements. Group A subgroups will as a minimum, include the final electrical testing subgroups 1, 2, and 3 (plus 4, 7, and 9 as applicable) and any other subgroups required by the device acquisition specification. Each inspection lot or sublot will be tested. A procedure for performing group A inspection in accordance with one or more of the following methods will be available for review by the qualifying activity.

a. Sampling: A single sample may be used for all subgroup testing. Where the required size exceeds the lot size, 100 percent inspection will be allowed.

b. Sequence of test: Group A testing by subgroup or within subgroups may be performed in any sequence after subgroup 1 or alternate subgroups (see MIL-STD-883, method 1015) are performed.

C.6.3.1.2 End-of-Line sample testing.

a. Production performs all required final electrical screening tests.

b. Quality assurance or quality designate randomly pulls samples to the required quantity (accept number) and performs acceptance testing.

C.6.3.1.3 In-line sample testing. Test samples for each individual group A subgroup will be randomly selected from the inspection lot after 100 percent screening of that subgroup (or subgroups, in the event that multiple subgroups are tested at the same temperature in sequence with the same test program). All devices in the inspection lot or sublot will be available for selection as a test sample and a fully random sample will be selected from the total population of devices. In addition, a different operator will check the entire test setup and verify the use of the correct test program prior to testing the group sample.

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TABLE IXa. Group A electrical test.

Subgroup	Parameters	Quantity (accept number)
1	Static test at +25°C	116(0)
2	Static tests at maximum rated operating temperature	76(0)
3	Static tests at minimum rated operating temperature	45(0)
4	Dynamic test at +25°C	116(0)
5	Dynamic tests at maximum rated operating temperature	76(0)
6	Dynamic tests at minimum rated operating temperature	45(0)
7	Functional tests at +25°C	116(0)
8	Functional tests at maximum and minimum rated operating temperatures	76(0)
9	Switching tests at +25°C	116(0)
10	Switching tests at maximum rated operating temperature	76(0)
11	Switching tests at minimum rated operating temperature	45(0)

C.6.3.1.4 In-line verification testing.

a. For each test setup (and operator for manual testing) production will test a correlation unit to assure that the accuracy requirements of MIL-STD-883 are being met.

b. Testing will be performed using the verified setup.

c. At the completion of testing (or at least once each week) or following a change of operators for manual testing, Qualifying Activity (QA) or a QA designate verifies the production testing by:

(1) Visually inspecting to confirm that the correct test fixture, equipment, software, and procedures were used.

(2) Actual testing of a controlled, known good, device of the device type being tested, utilizing the fixtures, equipment, software, and procedure(s) that were used by production. Variables data for all applicable group A tests at +25°C will be read and recorded for the controlled unit. This data will be maintained with the lot.

(3) Failure of the verification test will, as a minimum, require engineering to perform a detailed review of hardware, software, setup, and parts. If the engineering review does not locate the problem, the verification unit will undergo failure analysis. The appropriate corrective action must then be taken based on the failure analysis results. The entire group of devices being considered for acceptance at the time of the failure may then be retested for the appropriate subgroup(s) acceptance one time only by repeating in-line verification testing. If the failure analysis does not specifically locate the problem, the lot may be reconsidered for acceptance one time only for 100 percent retesting of all of the devices to all of group A requirements and by repeating in-line verification testing.

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C.6.3.2 Group B inspection. Group B inspection will be satisfied by performing in-line inspection sample monitoring as follows. Electrically rejected devices or test vehicles or coupons may be used in all subgroup tests in lieu of actual product.

a. Physical dimensions: Randomly select devices from devices at final inspection such that as a minimum two devices of each package configuration presented for inspection are inspected each month. Confirm that all critical dimensions affected by the assembly process (e.g., package length, width, height, pin length, etc.) meet the requirements of the device acquisition specification. Critical dimensions unaffected by assembly processes may be inspected at final visual inspection or as a part of incoming (receiving) inspection.

b. Resistance to solvents: Each inspection lot of marking ink will be tested prior to acceptance in accordance with MIL-STD-883, method 2015. This series of tests will be performed on each type of surface which is used as the marking surface on completed devices (e.g., silver plate, abraded nickel plate, non-abraded nickel plate, etc.). One piece of each surface type will be tested in each solvent. Each week one device or element (lid or package) representative of each of the marking surfaces of each device marked during the week will be tested in accordance with MIL-STD-883, method 2015 except that only "solvent D" is required.

c. PIND: PIND testing is not required for class H devices. PIND testing for class K devices will be performed in accordance with MIL-STD-883, method 2020, condition A or B as specified in the device acquisition specification.

d. Internal visual and mechanical: Internal visual and mechanical inspection will be performed at preseal visual inspection in accordance with the requirements of MIL-STD-883, method 2014. As a minimum, one device of each device type received at preseal visual inspection each month will be inspected.

e. Bond strength: Wire bond strength in-line inspection will be performed as a part of wire bond certification and in accordance with MIL-STD-883, method 2011. Each wire bond process (i.e., thermosonic gold, ultrasonic aluminum, thermal compressions gold, etc.) will be tested weekly. Where more than one machine exists for a specific process, the test sample will be rotated between machines such that all machines are tested at least once during each 13 week period when in operation. At the time of certification, an additional minimum 10 wires total (15 wires for class K) will be bonded in the certification sample part(s). After completion of certification bond pulls, the parts with the additional 10 wires (15 wires for class K) intact will be preconditioned for 1 hour at +300°C minimum in either air or an inert atmosphere followed by destructive pull tests. Bond strength requirements (i.e., minimum pull forces) will be as specified in table IXb-1. No failures are allowed.

f. Die shear: Die shear testing will be performed on two devices as a part of group C inspection (i.e., first lot and any element attach changes). Die shear testing during group C will be performed in accordance with MIL-STD-883, method 2019.

g. Solderability: Solderability testing will be performed as a part of incoming inspection (i.e., package evaluation) as follows:

Packages will be temperature aged to one of the following conditions prior to performing the solderability test.

6 ±0.5 hours at T_A = +250°C, ±10°C
22 ±1 hours at T_A = +200°C, ±8°C
160 ±8 hours at T_A = +150°C, ±6°C

When the device process flow includes an operation in which the package lead finish is changed prior to delivery of the device (i.e., a solder coating is applied), this operation will be performed on the package evaluation sample packages subsequent to the temperature aging. Following the temperature aging (and the lead finish application, if applicable), the sample packages will be solderability tested in accordance with method 2003 including a 7- to 8-hour steam aging.

h. Seal: Seal tests will be performed in accordance with MIL-STD-883, method 1014. One-hundred percent testing will be performed on all devices between final electrical test and external visual.

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C.6.3.3 Group C inspection. Group C inspection will be performed only on the first inspection lot submitted for inspection and as required to evaluate or qualify changes. For QML qualification, refer to the qualifying activity. Group C inspection will be performed in accordance with table IXc under the PI column and as outlined herein.

NOTE: The qualifying activity may approve alternate test plans for small lots of devices for group C inspection.

C.6.3.3.1 General.

a. Group C sample selection: Samples for group C will be drawn from the first inspection lot submitted.

b. Subgroup sampling: Subgroup 1 samples (or electrical rejects or mechanical samples, see Appendix F) will be used for the subgroup 3 and subgroup 4 tests.

c. Limited usage samples: (See C.6.2.1 for group C production start-up). A minimum of five devices will be subjected to subgroups 1 and 2 when all of the following are met:

(1) A maximum of 500 devices in a single order against a contractor-prepared document.

(2) A maximum of 2000 devices acquired against a contractor-prepared document on a given equipment-acquisition contract or program.

(3) A maximum of 2000 devices acquired against a contractor-prepared document during a 12 month period for a given device and manufacturer.

C.6.3.3.2 Wire bond strength for option 1 PI product qualification. Two devices minimum will be tested to assure conformance to the applicable requirements of MIL-STD-883, method 2011. Sample criteria will be based on the number of wires pulled using a sample size (accept number) of 22(0) for class H and a sample size (accept number) of 45(0) for class K devices. If the 45(0) requirement for class K cannot be met with two devices then all wires in two devices will be pulled with a minimum of 22 wires being pulled with zero failures. Sample wires will include one wire from each type transistor, diode, capacitor, and resistor chip; 3 wires from each type of integrated circuit; and 5 wires from package leads as applicable. For test conditions F and H, test 3 dice for each method of interconnection, or all flip chips and beam lead dice, if less. The minimum allowable bond strength will be the post seal bond strength requirements of method 2011.

C.6.3.3.3 Element shear for option 1 PI product qualification. The element (die/chip) shear test will be performed to a quantity (accept number) 22(0) of the elements in the devices or all elements in the two sample devices, whichever is less. The shear sample will be uniformly divided among all element types (or all elements, if less) in the device and will be performed in a minimum of two devices. The sample will include typical resistor, capacitor, integrated circuit, and discrete semiconductor elements.

C.6.3.4 Nonconformance. Should failure occur in any of the above in-line inspections, an analysis to determine cause will be performed and corrective action, as necessary, will be imposed. The cause of failure, applicable corrective action, and disposition of product affected by the failure will be documented. This documentation will be available for qualifying and acquiring activity review.

C.6.4 Option 2 (end-of-line). Option 2 CI and PI will be satisfied by end-of-line inspections and tests in accordance with C.6.4.1 through C.6.4.5.

C.6.4.1 Group A electrical testing. Group A testing will be performed in accordance with table IXa, C.6.3.1 through C.6.3.1.4 and the applicable device acquisition specification.

C.6.4.2 Group B inspection. Group B inspection will be performed on each inspection lot for each package type and lead finish in accordance with table IXb and C.6.4.2.1 through C.6.4.2.7.

C.6.4.2.1 PIND test. Lots failing to pass this test will be subjected to 100 percent PIND testing. Corrective action will be initiated to determine the cause for the rejects.

C.6.4.2.2 Internal visual and mechanical. The criteria for internal visual and mechanical examination will be the general requirements for design and construction, the requirements of the device acquisition specification and confirmation that the actual device construction is in accordance with the design documentation on file.

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TABLE IXb. Group B testing (option 2 only).

Subgroup	Class K	Class H	Test	MIL-STD-883 Method	MIL-STD-883 Condition	Quantity/ (accept number)	Reference paragraph
1	x	x	Physical dimensions	2016		2 (0)	
2	x		PIND	2020	A or B	15 (0)	C.6.4.2.1
3	x	x	Resistance to solvents	2015		3 (0)	
4	x	x	Internal visual and mechanical	2014		1 (0)	C.6.4.2.2
5	x	x	Bond strength a. Thermocompression b. Ultrasonic or wedge c. Flip-chip d. Beam lead	2011	 C or D C or D F H	2 (0)	C.6.4.2.3
6	x	x	Die shear strength	2019		2 (0)	C.6.4.2.4
7	x	x	Solderability	2003	Solder temperature +245°C ±5°C	1 (0)	C.6.4.2.5
8		x	Seal a. Fine b. Gross	1014	 A or B C or D	15 (0)	C.6.4.2.6
9	x	x	ESD a. Electrical parameters b. ESDS c. Electrical parameters	3015	 Group A-1 Group A-1	3 (0)	C.6.4.2.7

C.6.4.2.3 Bond strength. Destructive wirebond pull tests will be performed in accordance with MIL-STD-883, method 2011 and as follows. Testing may be accomplished in-line anytime after device wire bonding.

a. Two devices will be preconditioned and tested.

b. Sample devices will be preconditioned for one hour minimum at +300°C minimum in either air or an inert atmosphere.

c. Sampling criteria will be based on the number of wires pull tested using a sample size (accept number) as follows:

(1) Class H: 22(0) wires, 11 wires each device (or all wires if less).

(2) Class K: 44(0) wires, 22 wires each device (or all wires if less).

d. Sample wire locations will include wires from the following device locations as applicable:

(1) One wire from each type transistor, diode, capacitor, and resistor chip/die.

(2) Three wires from each type integrated circuit.

(3) Five wires connecting to package leads.

e. The minimum allowable bond strength will be in accordance with table IXb-1.

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TABLE IXb-1. Bond strength requirements.

Gold or aluminum wire diameter, X (inches)	Minimum bond strength (grams)
X < 0.001	0.5
X = 0.001	1.0
0.001 < X ≤ 0.003	[MIL-STD-883 method 2011, table 1, post seal requirement] minus 1 gram
0.003 < X	[MIL-STD-883 method 2011, figure 2011-1, post seal requirement] minus 10 percent

C.6.4.2.4 Die shear strength. The element (die/chip) shear test will be performed to a quantity (accept number) of 22(0) of the elements in the devices or all elements in the two sample devices, whichever is less. The shear sample will be uniformly divided among all element types (or all elements, if less) in the device and will be performed in a minimum of two devices. The sample will include typical resistor, capacitor, integrated circuit, and discrete semiconductor elements.

C.6.4.2.5 Solderability. At least 15 leads (or all leads, if less) will be randomly selected, identified and tested.

C.6.4.2.6 Seal (fine and gross). This test is not required if the 100 percent seal test screening is performed between the final electrical test and external visual.

C.6.4.2.7 Electrostatic discharge (ESD). This test will be performed for initial qualification and product redesign as a minimum, or the device will be considered Class 1.

C.6.4.3 Group C inspection. Group C inspection will be in accordance with C.6.3.3 except table IXc, subgroup 4 tests are not required.

C.6.4.4 Group D inspection. Group D inspection will be performed on the first inspection lot submitted and at intervals not exceeding 26 weeks for additional inspection lots. Group D inspection will be performed in accordance with table IXd and C.6.4.4.1 through C.6.4.4.3.

NOTE: This testing may be accomplished during package evaluation at incoming inspection and need not be repeated.

C.6.4.4.1 Samples. Sealed empty packages that have been subjected to the handling and stress conditions of screening may be used for group D testing.

C.6.4.4.2 End point electrical measurements. End point electrical measurements are not required.

C.6.4.4.3 Lead integrity. Lead integrity testing will be performed on 15 leads minimum or all leads if there are fewer than 15 leads per device package.

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TABLE IXc. Group C testing.

Subgroup	Class K	Class H	Test	MIL-STD-883 conditions Method	PI	QML	Quantity (accept number)	Reference paragraph
1	x	x	External visual	2009			5(0)	
	x	x	PIND	2020	N/A	A or B, 1/ 5 passes		C.7.7.5.1
	x		Temperature cycling	1010	C, 20 cycles	C, 100 cycles		C.7.7.5.2
		x	Temperature cycling or	1010 or	C, minimum or	C, 100 cycles		C.7.7.5.2
		x	Thermal shock	1011	A, minimum	N/A		C.7.7.5.2
	x	x	Mechanical shock or	2002 or	B, Y1 direction,	B, Y1 direction,		C.7.7.5.3
	x	x	Constant acceleration	2001	or A1, Y1 direction	and B, Y1 direction		C.7.7.5.4
	x	x	Seal (fine and gross)	1014				
	x	x	PIND	2020	N/A	A or B, 1 pass		C.7.7.5.1
	x		Radiographic	2012	Y axis	N/A		
	x	x	Visual examination	1010				C.7.7.5.5
	x	x	End-point electrical	2/				C.7.7.5.6
2	x	x	Steady-state life test	1005	1000 hours at +125°C or equivalent in accordance with table I	1000 hours at +125°C or equivalent in accordance with table I	22(0) or 5(0) 3/	C.7.7.5.7
	x	x	End point electrical	2/				C.7.7.5.6
3	x	x	Internal water vapor content	1018 at +100°C			3(0) or 4/ 5(1) 4/	C.7.7.5.8
4	x	x	Internal visual and mechanical	2014	Option 1 only		2(0) 4/	C.7.7.5.9
	x	x	Wirebond strength	2011	Option 1 only			C.7.7.5.10 C.6.3.3.2
	x	x	Element shear	2019	Option 1 only		2(0)4/	C.7.7.5.11 C.6.3.3.3

See notes on following page

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1/ Manufacturer's option.
2/ In accordance with the applicable device specification.
3/ When group C, subgroup 2 is being performed for QML qualification or limited PI or class I changes only, a sample size (accept number) of 5(0) may be used.
4/ Subgroups 3 and 4 samples will have received subgroup 1 environmental exposure. Subgroup 3 samples may be used to perform subgroup 4 tests.

TABLE IXd. Group D package related tests.

Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	Method	Condition		
Thermal shock	1011	C	5(0)	
Stabilization bake	1008	+150°C, 1 hour	5(0)	
Lead integrity	2004 2028	B2 (lead fatigue) D (leadless chip carrier) (pin grid array leads and rigid leads)	1(0)	C.6.4.4.3
Seal a. Fine b. Gross	1014	 A or B C or D	5(0)	

C.6.4.5 Nonconformance. Lots which fail subgroup requirements of groups A, B, C, and D may be resubmitted in accordance with the provisions of C.6.4.5.1. A failed lot which is reworked or is rescreened (resubmittal to inadvertently missed process steps is not considered a rescreen) may not be resubmitted to the failed subgroups (and must be counted as a failure) for periodic groups B, C, and D PI coverages. The lot may be resubmitted only to the failed subgroup to determine its own acceptance. If a lot is not resubmitted or fails the resubmission, the lot will not be shipped and the compliant marking and all references to MIL-H-38534 will be removed.

C.6.4.5.1 Resubmission of failed lots. Resubmitted lots will be kept separate from new lots and will be clearly identified as resubmitted lots. When any lot submitted for CI and PI fails any subgroup requirement of groups A, B, C, and D tests, it may be resubmitted once for that particular subgroup at double the sample size with zero failures allowed. A second resubmission using double the initial sample size with zero failures allowed is permitted only if failure analysis is performed to determine the mechanism of failure for each failed device from the prior submissions and it is determined that failure is due to:

a. A defect that can be effectively removed by rescreening the entire lot, or

b. Random type defects which do not reflect poor basic device design or poor basic processing procedures.

In all instances where analysis of the failed devices indicates that the failure mechanism is due to poor basic processing procedures, a basic design fault, or nonscreenable defects, the lot will not be resubmitted.

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APPENDIX D

NEW TECHNOLOGY CHARACTERIZATION GUIDELINES AND QUALIFICATION FLOWS

D.1 SCOPE

D.1.1 Scope. This appendix provides guidance for characterizing new processes and technologies (D.3, D.4, D.5). This information currently provides general standard design , construction, and technology characterization criteria that can be applied to ceramic and plastic devices. The manufacturer is invited to use the standard verification criteria in Appendix C to whatever extent is meaningful during the development of element level, in-process, device screening, and final device acceptance verification flows. It is expected that the MCM manufacturer's final baseline verification flow will be based primarily on information gained through technology characterization and qualification. This appendix may be used to evaluate new technologies and processes in order to gain knowledge of the capability of those processes and materials. This knowledge may then be used to modify the standard test flow of Appendix C. This appendix also contains a standard qualification flow for traditional technologies (D.6). The manufacturer may develop it's own method of accomplishing this characterization and qualification provided that method addresses the performance requirements of this specification.

D.1.2 Description of Appendix D. This appendix will provide guidance to manufacturers of emerging technologies. This guidance will include generic design and construction criteria as well as characterization criteria. This appendix also contains qualification criteria for new processes and materials.

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D.2 APPLICABLE DOCUMENTS

D.2.1 Government specification and standard. The following specification and standard form a part of this document to the extent specified herein. Unless otherwise specified, the issue of these documents is that listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise specified copies of military standards are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

D.3 GENERAL GUIDELINES

D.3.1 QML listing of technologies. This appendix outlines standard approaches and tests for technology characterization and qualification. This information should be used by the manufacturer to baseline the manufacturer's technology in preparation for technology certification. Technology certification is granted by the certification body upon their verification and acceptance of a manufacturer's technology characterization/qualification methodologies and test data. Acceptance of this data and information by DESC as the certification body leads to listing on QML-38534 or QML-38535. The manufacturer decides whether to enter the QML program under MIL-I-38535 or MIL-H-38534, and the decision should be based on which QML program best suits the manufacturer's business. Typically, the MIL-H-38534 QML program is best suited for the manufacturer that procures the integrated circuits used in their devices, whereas MIL-I-38535 is best suited to manufacturers that fabricate the integrated circuits used in their devices.

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D.4 STANDARD DESIGN AND CONSTRUCTION CRITERIA

D.4.1 GENERAL DESIGN RULES. The following features are, where relevant, included in the design rules. The manufacturer develops test plans for each of these areas and has them approved in accordance with the manufacturer's quality management program requirements. All tests are completed, documented, analyzed, and retained as design history for future reference.

D.4.1.1 Model Verification. Evidence is provided that all models utilized in the design process are functional, predictable and accurate over the worst case temperature and electrical extremes. Examples of these models are: transistor behavioral, logic, rault, timing, simulation, fabrication, assembly and package.

D.4.1.2 Layout verification. Demonstration of the capability of the automated or manual procedures routinely used for design, electrical and reliability rule checking to catch all known errors singly and combinationally. These rules cover, as a minimum:

a. Design rules check (DRC): Geometric and physical.

(1) Description of components offered (L, C, R)

(2) Preferred substrate size.

(3) Layer to layer specifications.

(4) Minimum and maximum feature sizes

(5) Component orientation and placement.

(6) Limiting electrical stresses.

(7) Standard component configurations and limiting stresses.

(8) Layout data (including preferred bond-pad and test structure details).

b. Electrical rules check (ERC): shorts and opens, connectivity.

c. Reliability rules: e.g., electromigration and current density, I_R drops, latchup, single event upset (SEU), hot electrons, ESD, burnout backgating.

D.4.1.3 Performance verification. A performance verification device (i.e., a chip, substrate, or set of chips) is designed and constructed to assess the process capability to perform routing and to accurately predict post-routing performance. A demonstration is included that the actual measured performance for each function over temperature and voltage falls between the two worst case CAD simulation performance limits. All critical minimum geometric and electrical design rules are stressed via devices or structures located on the process/product monitors. The electrical stress requirements for the devices and interconnects on these structures are worst case conditions. Failure analysis is performed on all failed devices and structures, and actions are taken to correct any problems found.

D.4.1.4 Thermal design verification. Verification that functional elements are operating within their design temperature ratings when the device is operated at the specified maximum operating case temperature. Finite element analysis is an acceptable thermal design analysis technique. All active and passive elements are derated.

D.4.1.5 Testability and fault coverage verification. Testability verification is a demonstration of a design style and a design-for-test (DFT) methodology which, in conjunction with demonstrated CAD for test tools, can provide 99 percent or greater fault coverage on a design of reasonable complexity. The manufacturer should also address his approach for a testability bus to groups such as the Joint Test Action Group (JTAG). Fault coverage verification is a demonstration of the fault coverage measurement (fault simulation, test algorithm analysis, etc.) capability which is used to provide fault coverage statistics of the design that uses the demonstrated design style, DFT method, and CAD for test tools. Measurement of fault coverage is in accordance with the procedures defined in MIL-STD-883, Method 5012. For non-digital devices, the fault coverage measurement may not be applicable, but should be supplemented as measures of analog fault coverage become better defined. For devices with both analog and digital functions, this design criteria fully applies to the digital portions of the devices.

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D.4.1.6 Electrostatic discharge sensitivity (ESDS). The electrostatic sensitivity of devices is characterized by the manufacturer.

D.4.2 STANDARD WAFER/SUBSTRATE DESIGN AND FABRICATION CRITERIA. The substrate fabrication process is monitored and controlled using a combination of applicable process/product monitors (SEC, TCV, and parametric monitors). The fabrication sequence to produce finished substrates is established with processing limits for each fabrication step. The manufacturer baselines a specific technology or technologies for qualification of the substrate fabrication. A technology consists of the fabrication sequence, design rules, and electrical characteristics. Demonstration of substrate fabrication capability consists of the following supported with documentation and data:

D.4.2.1 Mask manufacturing and control. All procedures used to manufacture masks for fabrication are documented and controlled. All designs are checked for errors utilizing appropriate design rule checkers before start of the mask making. Before use, the mask is inspected for flaws and errors. The final photolithographic mask to be used for substrate fabrication is verified to comply with the critical dimensions. Measurements are made to show that the pattern sizes and positions are consistent with the design rules. All masks are maintained under an inventory control program which outlines the inspection and the release of masks to fabrication, recording of usage, cleaning cycles, and maintenance/repair. All conditions for removal of masks from inventory are documented.

D.4.3 STANDARD DESIGN AND PACKAGING/ASSEMBLY CRITERIA

D.4.3.1 Standard evaluation circuit (SEC). An SEC can be used to demonstrate process reliability for the technology. The SEC design documentation addresses the following: the design methodology, the software tools used in the design, the functions it is to perform, its size (i.e., utilized active element functions, active silicon area, chip density), and simulations of its performance. Documentation procedures for the SEC and standard production devices are the same so that correlation can be made. The SEC may be designed solely for its role as a quality and reliability monitoring vehicle, or it may be a product meant for system use. The SEC has an operating temperature range equivalent to the worst case temperature range of the product it is to represent, and any reference to minimum or maximum operating temperatures refer to the respective lower and upper limits of that range. The SEC addresses the following requirements:

D.4.3.1.1 Complexity. The SEC exercises the total functionality of the technology flow, is of a representative complexity, is representative of active element density and power dissipation, and is comprised of major element types.

D.4.3.1.2 Functionality. The SEC contains fully functional circuits capable of being tested, and screened in a manner that correlates to the actual product.

D.4.3.1.3 Design. The SEC is designed to stress the design capabilities of the process. The architecture of the SEC should be designed so that failures can be easily diagnosed.

D.4.3.1.4 Fabrication and assembly. The SEC is processed on the same fabrication and assembly line as the product that it is to represent.

D.4.3.1.5 Packaging. The SEC is packaged with the same packaging materials as the product it is to represent.

NOTE: A different SEC may be required whenever the design rules, materials, basic processes, or basic functionality of the technologies differ.

D.4.4 Packaging design and characterization. The design criteria and performance characteristics described herein are addressed for each package or packaging style. The device manufacturer takes final responsibility for package design/construction quality and reliability. Characterization is performed by either the device manufacturer, by an external lab, or by the package manufacturer. The device manufacturer addresses the testing described herein. The device manufacturer also takes responsibility for maintaining documented validation of all characterization methods used and supporting data.

D.4.4.1 Package thermal characterization. Packaging thermal resistance is determined. This value may be obtained by direct or indirect measurements, or by simulation tools or calculations. Test method 1012 of MIL-STD-883 may be used for this calculation. If the thermal resistance is obtained by a calculation or simulation tool, this procedure should be validated by the manufacturer. To validate such a method of theoretical estimation, a correlation is demonstrated between the theoretically estimated value and the actual measured value for at least one package of the same style with equal or greater pin count.

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D.4.4.2 Package electrical characterization. During electrical characterization the following parameters are addressed:

D.4.4.2.1 Ground and power supply impedance. The contribution by packages to ground and power supply noises is minimized. This is accomplished by either the use of documented package design rules, or through testing of packages. Packages are tested, either individually or by similarity, in accordance with method 3019 of MIL-STD-883.

D.4.4.2.2 Cross-coupling effects. The cross-coupling of wideband digital signals and noise between the pins of packages used for digital devices is minimized. This is accomplished either through the use of documented package design rules; or through testing the packages, either individually or by similarity, in accordance with method 3017 and 3018 of MIL-STD-883.

D.4.4.2.3 High voltage effects. Packages are designed such that the voltage applied to the package does not produce a surface or bulk leakage between adjacent package conductors (including leads or terminals). This is accomplished either through the use of documented design rules aimed at minimizing bulk or surface leakage; or through testing of the high voltage packages, either individually or by similarity, in accordance with method 1003 of MIL-STD-883.

D.4.4.2.4 Packaging material characterization. The thermal coefficient of expansion and purity of packaging materials are addressed during package design.

D.5 STANDARD VERIFICATION CRITERIA

D.5.1 Technology characterization/qualification.

D.5.1.1 Wafer/substrate technology characterization program. A technology characterization program contains those test structures needed to characterize a technology's susceptibility to intrinsic reliability failure mechanisms. The total program includes testing of the TCV to obtain technology capability benchmarks, testing of a parametric monitor during fabrication, and periodic wafer/substrate lot acceptance testing. The test structures necessary to monitor intrinsic reliability failure mechanisms may be stand-alone structures, or can appear on the parametric monitor, the SEC, or the device itself. The program indicates where the structures are located and how they are tested and analyzed. The technology characterization program is used for the following purposes: technology qualification, reliability monitoring, change verification, and technology certification.

D.5.1.2 Technology characterization vehicle (TCV). TCVs are randomly chosen and evenly distributed from three completed, homogeneous wafer/substrate lots in the technology and the fabrication technology to be characterized. These substrates have passed the substrate lot acceptance testing. Accelerated aging experiments are performed to produce an estimate of the mean-time-to-failure (MTTF) and a distribution of the failure times under worst case operating conditions and layout, consistent with the design rules for each wear-out mechanism. From the MTTF and distribution of failures, a worst case operating lifetime or worst case failure rate is predicted. The initial MTTF, failure distribution and acceleration factors are used as capability benchmarks for the technology to which subsequent technology characterization results are compared. To allow for the evaluation of the chip technology within the devices, the TCVs are packaged in a suitable package using the same packaging materials and assembly procedures as standard devices in the technology use. The packaging should not adversely affect the outcome of the test. The TCVs need not use a fully characterized package style since these packages will tend to have lead counts far in excess of those needed for intrinsic reliability studies. The packaging requirements for the TCV may be disregarded if the substrate level and packaged accelerated aging results show equivalence.

D.5.1.3 Parametric monitor. Parametric monitors are used for measuring electrical characteristics of each wafer/substrate type in a specified technology. The parametric monitor test structures can be incorporated into the grid (kerf), within a substrate, as a dedicated drop-in, or any combination thereof. Location of the parametric monitor test structures are optimally positioned to allow for the determination of the uniformity across the substrate. A suggested location scheme is one near the substrate center and one in each of the four quadrants of the substrate, at least two-thirds of a radius away from the center. Reject limits and procedures for parametric measurements including which parameters will be monitored routinely and which will be included in the SPC program are established and documented. Documentation of the parametric monitor also include parametric monitor test structure design, test procedure (including electrical measurement at temperature and the relationship between the measured limits and those determined in the manufacturer's device simulations), design rules, and process rules. Alternate measurement techniques, such as in-line monitors, can also be used and should be documented properly.

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D.5.1.4 Substrate acceptance plan. A substrate acceptance plan is developed and implemented based on electrical measurement of parametric monitors. This plan uses the parametric monitor and includes visual criteria when applicable. In addition, this plan addresses the concerns detailed in MIL-STD-883, method 2018 (e.g., metallization, step coverage). The use of method 2018 is encouraged, but alternate procedures utilizing parametric monitor data and in-line monitors can also be used. The plan can address acceptance by either a single substrate at a time, or by substrate lot acceptance. However, the plan always addresses the following concerns: small lots, large lots, and specialty lots.

D.5.2 Assembly/Packaging technology characterization. The assembly and packaging process capability is characterized by testing a suitable sample size of actual product or SEC's to the package characterization tests outlined in Tables X and XI. The sample size is determined by the manufacturer. The characterization test results are used to do the following: finalize the manufacturer's assembly (i.e., die attachment, wire/ribbon bonding, seal, molding, code marking, etc) and verification technology baseline flow; qualify the assembly/packaging technology, identify in-process monitors for prevention of failures and monitoring of critical technology parameters; and technology certification.

D.5.2.1 Assembly/Packaging technology benchmarking. A sufficient number of devices are randomly chosen from three completed lots of devices using the characterized technology. The devices are subjected to the baselined screening flow established for the technology (Appendix C). The number of device failures from these screening tests serve as a benchmark yield for the technology. Failure analysis is performed on the failed devices to determine each failure category and necessary corrective actions. Both the benchmark yield data and the failure analysis data are retained for future reference and technology comparisons.

Table X. Ceramic Assembly/Packaging Technology Characterization Tests.

Group Number	Process	Test	MIL-STD-883 Method or JEDEC Test Method
1	Element and substrate attach and interconnect	Temperature cycling (1000 cycles) Thermal shock (100 cycles) End-point electricals X-ray or ultrasonic inspection Visual inspection Bond strength Ball or die shear, stud pull	Method 1010, cond C Method 1011 Per device spec Method 2012 or 2030 Method 2010/2017/2032 Method 2011 Method 2019/2027
2	Element attach interconnect and seal	Mechanical shock Variable frequency vibration Constant acceleration Fine and gross leak Lid torque (glass seal) Visual inspection End point electricals	Method 2002, cond B Method 2007, cond A Method 2001 Method 1014 Method 2024 Method 1010 Per device spec
3	Package integrity and contamination	Internal water vapor PIND Internal visual	Method 1018 Method 202, cond A or B Method 2010/2017/2032
4	Post burn-in lead finish	Solderability	Method 2003 or 2022
5	Device marking	Resistance to Solvents	Method 2015
6	Final package test	High temperature storage	Method 1008, 1000 hrs 150C

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Table XI. Plastic Assembly/Packaging Technology Characterization Tests. 1/

Group Number	Process	Test	MIL-STD-883 Method/Condition or JEDEC Test Method
1	Die/substrate attach & Interconnect	In-line visual inspection In-line bond strength In-line die shear or stud pull Post-molding X-ray	Method 2010, 2017, 2032 Method 2011 Methods 2019 or 2027 Method 2012
2	Die/substrate attach, Interconnect, & Molding	X-ray Ultrasonic inspection Temperature cycling (1000 cycles) End-point electricals Ultrasonic inspection Thermal Shock (100 cycles) End-point electricals Ultrasonic inspection	Method 2012, (die mount & wire bond) Method 2030 Method 1010, Cond C per device specification Method 1011, Cond C per device specification
3	Device Marking	Resistance to Solvents	Method 2015
4	Post burn-in lead finish	Solderability	Method 2003 (245C ±5C) or Method 2022 (after worst case reburn)
5	Final package testing	High temperature storage	Method 1008, 1000 hrs @ 150C

1/ A "preconditioning" procedure is necessary to simulate board assembly of plastic surface mount devices. This procedure will include the moisture intake and reflow simulation. Exposure to soldering fluxes (possible source of corrosiveness) and to board cleaning agents is also an important part of the plastic surface mount device's preconditioning.

D.5.2.2 Package style verification. The device manufacturer documents how packaging (e.g., hermetic or plastic) used in the manufacture of products is verified. In particular, the documentation includes how packaging styles that offer similar characteristics are grouped together for verification and change control purposes. Table XII identifies key package characteristics for which testing is addressed on each packaging technology style.

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Table XII. Package Style characterization testing.

Group Number	Process	Test	MIL-STD-883 Method/Condition or JEDEC Test Method	Package
1	Dimensions	Physical dimensions	TM 2016	All
2a	Resistance to Moisture	Thermal Shock (15) Temperature cycles, (100 cycles) Moisture Resistance Visual Inspection Fine & Gross Leak	TM 1011, Cond C TM 1010, Cond C TM 1010 & TM 1004 criteria TM 1014	Ceramic
2b	Resistance to Moisture	Preconditioning Electrical testing Biased HAST (500 hrs, 130C, 85% RH) End-point electricals	See Note 1/ Per device specification JEDEC 22-B, 101 JEDEC 22-A, 112 per device specification	Plastic
3a	Susceptibility to Corrosion	Salt Atmosphere	TM 1009, Cond A	Ceramic
3b	Susceptibility to Leakage & Corrosion	Autoclave (no bias) (Pressure Pot) 2 Atm., 121C	JEDEC 22-B, 102 (data provided for 96 hrs and 168 hrs)	Plastic
4	Leads	Lead integrity	TM 2004, Cond A, B2 or D TM 2028 for pin grid array	All
5	Susceptibility to Moisture Induces Cracking at Reflow Solder	Moisture intake Reflow simulation Inspections for delaminations & cracks	168 hrs @ 85C/85% RH or bake + min guaranteed time @ 30C/60% RH Vapor phase (219C, no preheat) or infrared (240C max) Cross-section at 1000X or ultrasonic (CSAM)	Plastic Surface Mount
6	Safety	Flammability	UL94-V-0, ASTM2863-77	Plastic
7	Fungus Resistance	Fungus resistance	MIL-F-13927	Plastic

1/ The manufacturer defines a preconditioning procedure that simulates board assembly of plastic surface mount devices. This procedure includes as a minimum the moisture intake and reflow simulation tests of group 5. Exposure to soldering fluxes (possible source of corrosiveness) and to board cleaning agents is also recommended for preconditioning the devices.

D.5.3 SPC and in-process monitoring. An in-process monitoring system is used by the manufacturer to control key processing steps to ensure device yield and reliability. The monitoring system can utilize various test structures, methods and measurement techniques. The critical operations to be monitored are determined by the manufacturer based on experience and knowledge of the processes. The resulting data is analyzed by appropriate SPC methods to determine control effectiveness for substrate fabrication technologies. For assembly/packaging technologies, the resulting data is analyzed by an appropriate method, with SPC methods being the most preferred for determining control effectiveness.

D.5.4 Device screening. Where meaningful, the standard screening criteria in Appendix C can be utilized. However, final device screening flow should be based on technology characterization results.

D.5.5 Final device acceptance verifications. Where meaningful, the standard final device acceptance criteria in Appendix C can be utilized. However, final device acceptance test flow should be based on technology characterization results.

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D.6 QUALIFICATION

D.6.1 Description of Qualification. The following criteria has traditionally been used to qualify all processes and materials used in the manufacture of hybrid devices. It may not, however, be adequate for new technologies, in which case the remainder of Appendix D should be used for guidance when characterizing the technology. This criteria is intended to be used to characterize all process and materials used in the manufacture of the device. This criteria will be used to determine the acceptability of the processes and materials. All parts built using processes and materials that have succesfully completed characterization and have been verified by the Qualifying Activity are considered qualified.

D.6.2 Rework qualification. Devices containing any unqualified rework will not be shipped until the rework has been successfully qualified. The rework and repair provisions will apply.

D.6.2.1 Qualification of rework. If any rework is to be qualified, and unless otherwise allowed, the manufacturer will build a qualification lot of reworked devices in which certified rework processes are performed. Standard evaluation circuits may be used. Qualification of rework by this method will require qualifying activity approval of the test plan and ATT prior to assembly of the lot.

D.6.2.2 Delid/relid rework qualification procedures. If delid/relid rework is to be qualified, a qualification lot of delidded/relidded devices will be assembled that includes adequate devices for five qualification samples plus reserve units. Qualification of two or more delid/relid cycles require that the samples be delidded and relidded N+1 times to qualify "N" delid/relid cycles. The N+1 delid/relid rework operations will be performed on qualification devices that have been fully screened. In addition to the original screen, there will be N screens performed for N+1 delid/relid operations. The final screen will occur after the last delid/relid cycle. Note that one delid/relid qualification will require no additional delid/relid operation.

D.6.2.3 Alternate qualification procedures for die/wire bond rework. The manufacturer may elect to review the initial production lot(s) from which qualification samples are selected for the occurrence of certified rework processes. The devices containing the rework to be qualified will be among those selected for qualification. If the amount of rework that was performed does not meet the sample size requirements, then additional die/bond rework will be performed on the selected rework samples or more rework samples to meet the minimum sample size requirements. If the initial qualification does not cover all certified rework, then subsequent production lot(s) will be reviewed for the occurrence of the unqualified rework until all certified rework is qualified. Delid/relid rework will not be qualified by these procedures.

D.6.3 Qualified manufacturer's list (QML) qualification lot. The manufacturer may elect to perform the QML qualification in accordance with paragraph D.6.7 on an inspection lot of shippable product; or the manufacturer may choose to build a lot of devices specifically for QML qualification, and test them in accordance with paragraph D.6.7. Devices specifically built for QML qualification may either be actual product or standard evaluation circuits. Any actual products from the qualification lot are shippable as a compliant product after successful completion of qualification tests, subgroups 1, 3, 5, and 7 of table IXb, and table IXd tests.

D.6.4 Qualification test requirements. QML qualification will be accomplished by successful performance of group C testing as specified herein. For options 1 and 2, the group C testing will be the QML qualification tests and inspections specified in table IXc, under the QML column.

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D.6.5 Qualification to radiation hardness assurance (RHA) levels. Qualification to an RHA level will consist of qualification to the appropriate quality and reliability assurance level (class K or H) plus group E tests of MIL-STD-883, method 5005. Special qualification requirements were developed for a number of moderately hard microcircuits which obviated qualification inspection for class H, levels M and D. QPL-38510 provides a footnote for these microcircuits. RHA levels are defined as follows:

RHA level (see note below)

RHA level designator (see main body)	Radiation and total dose (KRad (Si))	Level neutron fluence (n/cm^2)
-	No RHA	No RHA
M	3	2×10^{12}
D	10	2×10^{12}
L	50	2×10^{12}
R	100	2×10^{12}
F	300	2×10^{12}
G	500	2×10^{12}
H	1000	2×10^{12}

NOTE: The device acquisition specification may allow for a higher neutron level.

Devices are considered to meet a specific RHA level if all dice used in the manufacture of the devices are acquired from wafers that have passed CI and PI to that RHA level, or a higher level. Where dice from such wafers are unavailable, a sample of the dice to be used will be packaged and tested in accordance with the requirements of MIL-STD-883, method 5005, group E for microcircuits or MIL-S-19500, group D for discrete devices. Samples must be taken from the specific wafer lot to be used in the device for class H or from each wafer to be used for class K. The manufacturer may elect to replace the element testing by testing of completed devices. The lot definitions, sampling procedures, and test methods of MIL-I-38535 and MIL-STD-883, method 5005, as related to group E, may be applied as an alternate test plan.

D.6.6 Qualification to electrostatic discharge sensitivity (ESDS) classes. Initial qualification to an ESDS class or requalification after redesign will consist of qualification to the appropriate quality and reliability level (class K or H) plus ESDS classification in accordance with method 3015 of MIL-STD-883. ESDS classification levels and associated marking are defined herein.

NOTE: Manufacturers may, at their option, classify devices as class 1 without performing the ESD sensitivity test based on their own history, judgment, or performance. ESD classification can be determined either by testing the devices using method 3015 or marking to the lowest electrostatic voltage class level of the active devices ESDS classified in accordance with MIL-I-38535 that are accessible to the leads of the devices. Support data (from device tests or ICD manufacturers' ESD results) will be retained by the device manufacturer for device types compliant with this specification.

D.6.7 QML-38534 qualification. All tests, test methods, test conditions, and limits will be in accordance with MIL-STD-883 and as specified herein. If a qualification lot is withdrawn due to (1) failing to meet qualification requirements or (2) lack of failure analysis, corrective action, and (3) no retesting is performed, the certification of the process or material (or both) to be covered by that qualification will be removed by the qualifying activity.

NOTE: The device manufacturer has the right to select not to use any solution or solvent identified within this specification or related specifications that has also been identified by the American Congress of Government Industrial Hygienists as being a potential or suspect carcinogen. Where the device manufacturer elects not to use a material, he must notify the acquiring or qualifying activities and the customer in writing in clear, unambiguous language not subject to misinterpretation that this right has been exercised.

D.6.7.1 Qualification eligibility. All processes to be qualified and which are to be included on QML-38534 must have been certified by the qualifying activity in accordance with 4.5.1.2.

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D.6.7.2 Test samples. Devices used for qualification will have been assembled using certified process (or as allowed by the Qualifying Activity) and screened in accordance with the applicable sections of C.6 herein. Qualification tests will be performed at facilities which have laboratory suitability granted by the qualifying activity. DESC Form EQC-42H, Device Product Baseline, or its equivalent, will be used to baseline the specific processes and materials utilized in the qualification device.

D.6.7.2.1 Standard evaluation circuits. The manufacturer may elect to design and build a functional standard evaluation circuit (device) in lieu of utilizing actual product. If qualification is to be performed on a lot of devices built specifically for QML qualification, the device will be representative of the physical complexity of the product that will be covered by its testing. Standard evaluation circuits will not be used for group C PI product qualifications.

D.6.7.2.2 Sample selection. The sample size for each test is listed in the corresponding subgroups of the group C table IXc. In addition for group C, subgroup 3, a minimum of three electrical rejects or representative mechanical samples will be reserved (see D.6.7.5.8). Except for designated rework and nonfunctional devices, test samples will be randomly selected from the inspection lot. The manufacturer will retain a sufficient number of test devices from the lot to designate reserve samples.

D.6.7.2.3 Rework samples. For approval of rework qualification, the rework sample will be prepared in accordance with the manufacturer's baselined rework procedure. Three out of five devices tested in group C, subgroup 1 will have undergone the rework to be qualified. Two out of the three (3(0)) devices tested in group C, subgroup 3 will contain the rework to be qualified. One of the two devices tested in group C, subgroup 4 will contain the rework to be qualified. The die and wire sample size requirements of C.7.7.5.10 and C.7.7.5.11 will be applied to reworked wirebonds and replaced die. Each rework method will be considered a different process.

D.6.7.2.4 Nonfunctional samples. Electrical rejects from final electrical testing in screening can be used in any subgroup of qualification tests where electrical testing is not required.

D.6.7.2.5 Disposition of samples. Samples destructively tested during qualification testing will be submitted to the qualifying activity with the qualification test report. Other devices in the qualification inspection lot will be disposed of.

D.6.7.3 Test failures.

D.6.7.3.1 Resubmission of failed samples or lots (or both). Unless otherwise specified (D.6.7.4.8.1), resubmission of failed samples or additional samples from the same production lot are not allowed unless such failures are due to equipment or operator errors in accordance with Appendix F. Notification of the qualifying activity is required.

D.6.7.3.2 Failures. All test failures will be reported to the qualifying activity, along with (if applicable) the resulting failure analysis and corrective actions needed to assess qualification status or alternatives.

D.6.7.4 Technology capability verifications. Table IXc under the QML column and D.6.7.4.1 through D.6.7.4.11 detail the testing requirements for qualification for both class H and class K devices.

D.6.7.4.1 PIND. The devices will show no evidence of loose particles. Any device showing loose particles when tested as specified herein will be analyzed. Failure of PIND will not jeopardize qualification provided the manufacturer demonstrates that the loose particle control is established and random samples, from product fabricated using the baselined process, are PIND tested after corrective action implementation. These random samples will have been screened (see C.5). The retest requirements will be determined based on the nature of the changes made as a result of the corrective action. Compliant class H will receive 100 percent PIND screening until the manufacturer demonstrates to the qualifying activity that these requirements are met.

D.6.7.4.1.1 Loose particle recovery. The loose particles that caused the failures will be recovered and analyzed for the cause and source. If the analysis fails to locate the particles causing failure, the device will be carefully delidded and examined in an attempt to locate the particles. Captured particles will be evaluated at 30X minimum and the offending portion of the process will be identified and corrected.

D.6.7.4.2 Temperature cycling. Thermal shock, MIL-STD-883, method 1011, will not be used as a substitute for temperature cycling for QML qualification.

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D.6.7.4.3 Mechanical shock. When QML qualification is being performed, constant acceleration is not an option in place of mechanical shock. Both tests are required for qualification.

D.6.7.4.4 Constant acceleration. For QML qualification, a stiffener plate (e.g., .125 inch (3.18 mm) aluminum) may be attached to the base of the package to prevent damage due to "oil canning" of the package. If conflicting design/process constraints warrant stress levels lower than the specified 10,000 g level, qualifying activity approval is required on a case-by-case basis. In this event the "g" level will be no lower than 7500 g and the "g" level that the manufacturer actually qualifies will be reflected on QML-38534.

D.6.7.4.5 Visual examination. The visual examination will be in accordance with the procedure given within MIL-STD-883, method 1010 or 1011.

D.6.7.4.6 Electrical requirements. Electrical end points will be measured (and recorded when required) before starting and after completion of all tests in subgroups 1 and 2 of group C tests. Electrical end-point limits, life test conditions, and intermediate measurement requirements will be specified as required by the applicable device acquisition specification. Test samples which require variable data will be serialized prior to tests.

D.6.7.4.7 Steady-state life test. Steady-state life testing will be performed on each initial lot of each device type. If group C, subgroup 2 testing is being performed for QML qualification only, the sample size will be five with zero failures allowed. In addition, if group C2 testing is being performed for QML qualification only, a 1000-hour bake at +150°C followed by end-point electrical testing may be performed in lieu of steady-state life testing.

D.6.7.4.8 Internal water vapor. An internal water vapor content sample of three devices (zero failures) or five devices (one failure) will be selected from the subgroup 1 sample. The use of electrical rejects or representative mechanical samples is permissible provided these samples have seen, as a minimum, the environmental exposures required in subgroup 1 (i.e., temperature cycle or thermal shock, mechanical shock or constant acceleration and seal tests as applicable). If the internal water vapor content exceeds 5000 ppmv at +100°C on more than one device, an additional 3(0) or 5(1) fully screened samples will be subjected to 10 cycles (20 cycles for class K) of MIL-STD-883, method 1010 temperature cycling, condition C, (or the optional 15 cycles of thermal shock, condition A for class H). Following temperature cycling (or thermal shock), the samples will be tested for internal water vapor content. The RGA data from both sets of testing will be submitted to the qualifying activity. Other gas species present in quantities greater than 100 parts per million volume (0.01 percent) will be reported. Different circuits in the same package and with an equal quantity (or fewer) elements and the same materials may be qualified by similarity to a qualified test sample that was processed and sealed in the same period.

D.6.7.4.8.1 Correlation testing for internal water vapor. At the manufacturer's option, if the initial test samples (three or five devices) fail internal water vapor, a second complete sample (see C.7.7.2.2) may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. An additional three samples will be held by the manufacturer until final disposition of the test report. If this test passes, the devices and data from both test submissions will be submitted to the qualifying activity for approval of internal water vapor criteria.

D.6.7.4.9 Internal visual and mechanical. In addition to the criteria of MIL-STD-883, method 2014, this inspection will verify that no damage has occurred to and no contamination is present on the elements and substrate.

D.6.7.4.10 Wire bond strength for QML qualification. Two devices minimum will be tested to assure the post seal bond strength requirements of MIL-STD-883, method 2011. The bond strength test will be performed on a sample size (accept number) of 15(0) bond wires for each wirebond process (including each rework method outlined in D.6.7.4.10.1 as a separate process) and material (wire metallization) present in the device. Each 15 piece sample of wires will contain an even distribution of all wire sizes that can be qualified by that sample. No failures will be allowed. Additional devices will be added, if necessary, to meet the required wire sample size. The test wires will be predesignated.

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D.6.7.4.10.1 Wire bond strength for QML rework qualification. Each of the following wirebond rework methods will be considered as separate methods requiring QML qualification:

a. Gold ball bonds on substrate wires.

b. Gold ball bonds on crescent bonds.

c. Gold ball bonds on top of gold ball bonds.

D.6.7.4.11 Element shear for QML qualification. Two devices minimum will be tested to assure the die shear strength requirements of MIL-STD-883, method 2019. The die shear test will be performed to a quantity (accept number) of 22(0) minimum of the elements in the devices or a quantity (accept number) of 5(0) elements for each element attach process (including element replacement as a separate process) and material present in the device. The materials considered will include the attach medium, element backing, and substrate/package attach area surface. Each five-piece sample of elements will contain an even distribution of all element sizes that can be qualified by that sample. No failures will be allowed. Additional devices will be added if necessary to meet the required element sample size. The test elements will be predesignated.

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APPENDIX E

GENERIC DESIGN AND CONSTRUCTION CRITERIA

E.1 SCOPE

E.1.1 Scope. This appendix is intended to present the generic design and construction criteria which will be addressed by the manufacturer. The criteria of this appendix may be modified as described in this specification. Compliance with this appendix is not mandatory, however, manufacturers must be able to demonstrate a design and construction system that achieves as least the same level of quality as could be achieved by complying with this appendix.

E.1.2 Description of Appendix E. This appendix will describe the generic design and construction criteria of this technology and is presented as requirements for conformance.

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E.2 APPLICABLE DOCUMENTS

E.2.1 Government documents.

E.2.1.1 Standard. The following standard forms a part of this document to the extent specified herein. Unless otherwise specified, the issue of this document is that listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise specified copies of military standards are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

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E.3 REWORK LIMITATIONS

E.3.1 Description of the rework limitations. This section describes a typical rework program, including limitation and testing required to insure that reworked devices are capable of meeting the performance requirements of this specification.

E.3.2 Rework and repair provisions. All rework and repair permitted on devices will be accomplished in accordance with procedures and safeguards documented in accordance with appendix A. This documentation will reflect the processes, procedures, and materials to be used including verification or test data. Each process or procedure will be designated as rework or repair. This documentation will indicate that a decision to rework is made solely by the manufacturer while a repair decision will be made with the concurrence of the customer except for repairs permitted by this specification. A typical example of rework is the removal of a defective element and replacement with a new element. An example of repair is the use of an organically attached molytab to replace a previously alloy attached semiconductor element.

E.3.2.1 General rework and repair provisions.

a. All temperature excursions during any rework or repair will not exceed the baselined rework or repair limitations. Time and temperature limits will be specified.

b. Touch-up of package sealing surface plating on delidded packages is not permitted.

c. The minimum distance between the glass to metal seals and the package sealing surface will be at least .040 inch (1.02 mm) after final seal to prevent damage to lead seals by welding adjacent to them. (Applies to seam welding only.)

d. For class H devices, any device that is reworked or repaired after preseal visual inspection will be subjected to full screening or rescreening as applicable. If a device has not been subjected to a given required screen prior to rework or repair, then that device must be subjected to that screen after rework or repair. If a device has been subjected to a given screen prior to rework or repair, then rescreening applies as follows:

   (1) Preseal visual inspection. Inspect for general damage (low magnification in accordance with MIL-STD-883, method 2017 and method 2032) which might have been caused by the rework or repair and perform a complete method 2017 or method 2032 inspection of the reworked or repaired element or area (e.g., replaced die, wirebonds, etc.).

   (2) Temperature cycle or shock, mechanical shock or centrifuge, seal, and external visual. Rescreen all rework or repair devices 100 percent.

   (3) Burn-in. Devices delidded to rework package seal failures do not require burn-in rescreen. Devices which have had elements replaced or have been wirebonded or rewirebonded require 100 percent burn-in rescreen.

e. For class K devices, any device which is reworked or repaired after 100 percent nondestructive bond pull (or preseal burn-in, when applicable) will be subjected to full screening or rescreening as applicable. If a device has not been subjected to a given required screen prior to rework or repair, then that device must be subjected to that screen after repair or rework. Full screening is required after any rework or repair operation involving unlidded (includes delidded) devices with clarification as follows:

   (1) Preseal burn-in (when applicable) will be repeated if the rework or repair involves any active element replacement or wire bonding (or wire rebonding) of any active element.

   (2) Nondestructive bond pull is only required on wires that were replaced or rebonded provided the device has already been subjected to the 100 percent bond pull screen.

   (3) Devices delidded for rework or repair after post seal burn-in.

   When preseal burn-in option is included in the baseline, the subsequent post seal burn-in rescreen may be reduced to 240 hours minimum. When preseal burn-in option is not included in the baseline the subsequent post seal burn-in rescreen may be reduced to 240 hours minimum provided that the rework or repair does not involve any active element replacement or wire bonding (or wire rebonding) of any active element.

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f. When flux is required for rework or repair, the specific flux and detailed procedures for its use and subsequent special cleaning operations will be documented and approved in accordance with Appendix A.

g. Replacement elements will not be bonded onto the chip element they are to replace.

h. Rework of a wafer (i.e., the strip and redeposition of a layer in order to correct a nonconformance to a specification limit) will not be allowed. Additional etch to correct a nonconformance to a specification limit, photoresist strip and recoat, or processing to continue or finish incomplete processing, will not be considered rework. For class K, additional deposition of oxidation, glassivation, or any interconnect layers (e.g., polysilicon, aluminum, etc.) will not be allowed.

E.3.2.2 Element wire rebonding. Wire rebonding of elements other than substrates, thick film elements, capacitors, and package posts will be permitted with the following limitations:

a. No scratched, voided, or discontinuous paths or conductor patterns on an element will be repaired by bridging with or addition of bonding wire or ribbon.

b. All rebonds will be placed on at least 50 percent undisturbed metal (excluding probe marks that do not expose underlying oxide). No more than one rebond attempt at any design bond location will be permitted. No rebonds will touch an area of exposed oxide caused by lifted or blistered metal. Bond-offs required to clear the bonder after an unsuccessful bond attempt need not be visible, will not be cause for reject and will not be counted as a rebond. For class K, the total number of rebond attempts (exclusive of element replacement or tuning wire replacement) will be limited to a maximum of 10 percent of the total number of bonds in the device. The 10 percent limit on rebond attempts may be rounded to the nearest whole number to the 10 percent value.

E.3.2.3 Substrate, thick film elements, capacitors, and package post wire rebonding or repair. Wire rebonding on substrates and package posts will be permitted with the following limitations:

a. Scratched, open, or discontinuous substrate metallization paths or conductor pattern on a substrate, not caused by poor adhesion, may be repaired by bridging with or by addition of bonded conductors having current carrying capacity at least 3.5 times the maximum calculated operating load current for the conductor or 3.5 times the current capacity of the wire bond connection terminating on the damaged conductor path. The quantity of repairs will be limited to one for each one-half square inch or fraction thereof of substrate area. This repair is not applicable to thick film elements, capacitors, or package posts.

b. No rebonds will be made over intended bonding areas in which the top layer metallization has lifted, peeled, or has been damaged such that underlying metallization or substrate is exposed at the immediate bond site.

E.3.2.4 Compound bonding. Compound bonding is permitted only as follows:

a. When required for design, rework, or repair, gold compound bonds will be limited to one bond over the original bond, wire, or ribbon.

b. Only monometallic compound bonds of the same size wire or ribbon are permitted (i.e., the original bond wire and that used for compound bonding must be the same material).

c. For rework or repair, the maximum number of compound bonds will not exceed 10 percent of the total number of wires.

d. For rework or repair, a corrective action system must be utilized in order to reduce the number of compound bonds.

e. For rework or repair, all compound bonds will be 100 percent nondestructive pull tested in accordance with MIL-STD-883, method 2023.

f. A compound bond will not be used to connect two wires.

g. All compound bonds will meet the visual criteria in MIL-STD-883, method 2017.

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E.3.2.5 Element replacement. Element replacement will be permitted with the following limitations:

a. Any polymer attached element may be replaced two times at a given location on any device. Any element attached with polymer to metal other than substrate metallization (e.g., pedestals, ribs, carriers, etc.) may be replaced four times at a given location. The number of polymer attached tuning element replacements will be defined in the manufacturers' baseline documentation, and approved by the qualifying activity.

b. Any metallic attached element may be replaced one time at a given location.

c. Any metallic attached element onto a plated tab where the tab is attached to a substrate with a higher temperature metallic attach process may be replaced two times.

d. Substrates may be removed, replaced, or put into a new package one time. This restriction does not apply to substrates attached into a package using mechanical fasteners.

E.3.2.6 Seal rework. The use of polymers to effect, improve, or repair any package seal will not be permitted.

E.3.2.6.1 Lid seal rework. It will be permissible to perform seal rework without delidding on devices that fail fine leak testing one time, only if tracer gas is included during the original sealing operation and under all of the following conditions:

a. Fine leak testing, without pressurization (bomb), must be performed immediately after sealing prior to any other test.

b. Devices will be stored in a nitrogen environment for a maximum of 4 hours between initial seal and reseal without replacing the cover.

c. Devices will be submitted to a predetermined vacuum bake prior to reseal.

d. Solder sealed packages may not be reworked in accordance with this procedure.

NOTE: The above leak testing will not be used as a substitute for the fine leak testing.

E.3.2.6.2 Other seal rework. It will be permissible to rework other seals (e.g., feedthroughs, connectors, seal plugs, windows, etc.) at metal-to-metal interfaces on unlidded devices.

E.3.2.7 Delidding of devices. Devices may be delidded and relidded for rework or repair provided the delid-relid procedures, controls, and resulting data are baselined. The number of delid-relid cycles allowed will be in accordance with E.3.2.7.1 or E.3.2.7.2. Delid-relid history (i.e., traceability by lot number or serial numbers) will be maintained by the device manufacturer.

E.3.2.7.1 Solder sealed devices. Class H solder sealed devices may be delidded-relidded one time. Class K solder sealed devices may not be delidded-relidded.

E.3.2.7.2 Welded devices. Only seam sealed, overlapping pulse welded, or laser welded packages designed for delid-relid may be delidded-relidded. Devices may be delidded-relidded N times, with N = 2 maximum for class K.

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E.4 DESIGN AND CONSTRUCTION

E.4.1 Description of Design and Construction. This section describes a typical design and construction program used to ensure that these devices will be capable of meeting of the performance requirements of this specification.

E.4.2 Design and construction. Device design and construction will be in accordance with the requirements specified herein and the device acquisition specification or SMD. The design will be capable of passing all applicable tests and screens (see Appendix C or D).

E.4.2.1 Package. Devices will be hermetically sealed in glass, metal, or ceramic (or combinations of these) packages. The following provisions apply to package construction and sealing:

a. No adhesive or polymeric materials will be used for package lid, or feedthrough, attach (or seal) or rework/repair.

b. Polymer impregnations or secondary seal (backfill, coating, or other uses or organic or polymeric materials to effect, improve, or rework/repair the seal) on the device package will not be permitted.

c. Flux will not be used in the final sealing process.

d. In the case of final lid seal using a welding process, sufficient distance will be maintained between the lid seal and any glass-to-metal seal so as to preclude damage or degradation of the glass-to-metal seal.

e. Package materials will be selected such that thermal expansion rate mismatches between different materials do not compromise package integrity or hermeticity during applicable temperature excursions.

E.4.2.2 Polymeric materials. The cure temperature of polymeric materials will not be exceeded after completion of final seal. Polymeric materials will meet the requirements of MIL-STD-883, method 5011. For materials outside the scope of method 5011, the manufacturer will develop an alternative plan.

E.4.2.3 External metals. External metal surfaces, other than seal weld areas, will meet the applicable corrosion resistance requirements, or will be plated to do so.

E.4.2.4 Other external materials. External parts, elements, or coatings including markings will be non-nutrient to fungus and will not blister, crack, flow, or exhibit defects that adversely affect storage, operation, or environmental capabilities of the device under the specified test and operating conditions.

E.4.2.5 Design and manufacturing documentation. Design, topography, schematic circuit information, manufacturing flowcharts, and process control documents for all devices will be available for review by the acquiring activity and the qualifying activity. This documentation will depict the physical and electrical construction of the device. Each device will be traceable to a specific part, drawing, or type number, and to the production lot and inspection lot codes under which devices are manufactured and tested (so that revisions can be identified).

E.4.2.5.1 Schematic diagrams. The device schematic diagram, logic diagram, or combination thereof, will be available with sufficient detail to represent all electrical elements functionally designed into the device together with their values (when applicable). For complex devices or those with redundant detail, the overall device may be represented by a logic diagram in combination with schematic details.

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E.4.2.6 Internal conductors. Internal thin film conductors on elements (metallization stripes, contact areas, bonding interfaces, etc.) and internal wires (wires, ribbons, etc.) will be designed such that no properly fabricated conductor will experience current in excess of the maximum value calculated by the manufacturer to preclude damage or degradation to the conductors, except by design (e.g., internal fuses). The following conditions will be considered when calculating the maximum current:

a. Calculate the current density at the point of maximum current density (i.e., greatest current per unit cross section) for the specified device type.

b. Use a current value equal to the maximum continuous current (at full fanout for digitals or at maximum load for linears) or equal to the simple time-averaged current obtained at maximum rated frequency and duty cycle with maximum load, whichever results in the greater current value at the point of maximum current density. This current value will be determined at the maximum recommended supply voltage and with the current assumed to be uniform over the entire conductor cross-sectional area.

c. Use the minimum allowed metal thickness in accordance with manufacturing specifications and controls including appropriate allowance for thinning experienced in the metallization step (via). The thinning factor over a metallization step is not required unless the point of maximum current density is located at the step.

d. Use the minimum allowable actual conductor widths (not mask widths) including appropriate allowance for narrowing or undercutting experienced in metal etching.

e. Do not include areas of barrier metals and nonconducting material in the calculation of conductor cross-section.

E.4.2.7 Device finishes. Tin is prohibited as a final finish and as an undercoat. The use of tin-lead finish is acceptable provided that the lead content is a minimum of 2 percent by weight.

E.4.2.7.1 Internal element finishes. Finishes on interior elements (e.g., bonding pads, posts, tabs) will be such that they meet lead bonding requirements and any applicable design and construction requirements.

E.4.2.7.2 External element finishes. Finishes of all external leads or terminals and all external metallic package/lid elements will meet the applicable corrosion resistance requirements.

E.4.2.7.3 External lead finish. Lead finish thickness measurements will be taken halfway between the seating plane and the tip of the lead. The finish system on all external leads or terminals will conform to one of the following:

a. Hot solder dip. The hot solder dip will be homogeneous with a minimum thickness of 60 microinches (1.52 µm) for round leads and, for other shapes, a minimum thickness at the crest of the major flats of 200 microinches (5.08 µm) solder (SN60 or Sn63). For leadless chip carrier devices, the solder will cover a minimum of 95 percent of the metallized side castellation or notch and metallized areas above and below the notch (except the index feature if not connected to the castellation). Terminal area intended for device mounting will be completely covered. The hot solder dip on leads is applicable to either 1 or 2 below:

(1) Over a finish in accordance with entry c or d below. the solder will extend within .030 inch (0.76 mm) of the lead or package interface, or beyond the effective seating plane for packages with standoffs.

(2) Over the basis metal or other finishes. When applied over the basis metal, or over underplate or finishes other than as specified in entry c or d, solder will cover the entire lead to the glass seal or point of emergence of the lead or metallized contact through the package wall.

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b. Tin-lead plate. Tin-lead plate will have in the plated deposit 2 percent to 50 percent by weight lead (balance nominally tin) co-deposited. As plated tin-lead will be a minimum of 300 microinches thick and will contain no more than 0.05 percent by weight co-deposited organic material (measured as elemental carbon). Tin-lead plating may be fused by heating above its liquidus temperature. Fused tin-lead will be a minimum of 200 microinches thick. Tin-lead plate is applicable:

(1) Over a finish in accordance with entry c below, or

(2) Over the basis metal.

c. Nickel plate or undercoating. Electroplated nickel or electroless nickel phosphorous nickel undercoating or finishes will be 50 to 350 microinches (1.27 µm to 8.89 µm) thick measured on major flats or diameters. Electroless nickel will not be used as the undercoating on flexible or semiflexible leads and will be permitted only on rigid leads or package elements other than leads (see MIL-STD-883 method 2004 for definitions of flexible and semiflexible leads).

d. Gold plate. Gold plating will be a minimum of 99.78 percent gold, and only cobalt will be used as the hardener. Gold plating will be a minimum of 50 microinches (1.27 µm) and a maximum of 225 microinches (5.72 µm) thick. Gold plating will be permitted only over nickel plate or undercoating in accordance with entry c above.

E.4.2.8 Thermal design. Thermal design analysis will be performed and will establish as a minimum that functional device elements are operating within their design temperature ratings when the device is operated at the specified maximum operating case temperature. Finite element analysis is an acceptable thermal design analysis technique. All active and passive elements will be derated.

E.4.2.9 Electrical circuit design. Worst case circuit design analysis will be performed and include the following evaluations as a minimum (applicable to the design):

a. Electrical element stress over the specified operating temperature range will be within the specified derating criteria under worst case temperature conditions.

b. Evaluated to meet the Group A CI test limits at worse case operating temperature conditions, as applicable.

E.5 Major changes. This sections describes how to handle major changes to devices or processes.

E.5.1 Class I, major changes. A thorough description of the proposed change, acceptable engineering data, and a suggested test plan designed to demonstrate that the changed product will continue to meet the acquisition document requirements including performance, quality, reliability, or interchangeability will be generated. The manufacturer will proceed with the change after approval of the test plan. To minimize the need for additional tests due to insufficient details or data regarding the proposed changes, it is recommended that the test plan be discussed with the acquiring or qualifying activity prior to commencing the test program. Test guidelines for each major change listed herein are provided in table XI for product design changes (column CI and PI) and baselined process changes (column QML). The subgroup designations in table XI correspond with the subgroups designated in tables IXa, IXb, IXc, and IXd of Appendix B. Tests will be performed on samples of the first devices or subassemblies manufactured incorporating the changes. Upon completion of the prescribed test program, the results will be recorded and available for review. At the manufacturer's option, devices incorporating the change may be manufactured and tested prior to approval; however, all shipments of these changed devices will be withheld until formal documented approval is granted by the acquiring or qualifying activity. Changes representative of those which are subject to the requirement are:

a. Substitution of substrate material (e.g., alumina versus BeO).

b. Substitution of materials or inks deposited on the substrate (e.g., (1) conductor: gold versus copper; (2) resistor: ruthenium base versus carbon) or deposit method: (e.g., thinfilm versus thickfilm).

c. Cumulative change of nominal process time of deposited materials exceeding 25 percent or nominal process temperature exceeding +50°C or 10 percent, whichever is greater, since the last qualification or major change notification.

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d. Cumulative changes to substrate mask design that reduce nominal design dimensions, spacing or isolation more than ±25 percent, or changes to electrical parameters of the deposited elements beyond the design limits since the last qualification or major change notification.

e. Substitution of trimming method (e.g., abrasive versus laser).

f. Increase in substrate fabrication multi-layer conductor levels more than one conductor level from QML Listing.

g. Substitution of attach material (e.g., epoxy A versus epoxy B) or of attachment method (e.g., epoxy versus eutectic) for device elements.

h. Change in the baselined process temperature for element or substrate attachment which exceeds +25°C or 10 percent, whichever is greater.

i. Substitution of die type (e.g., 2N2484 versus 2N2905) or other element types (e.g., tantalum versus ceramic capacitors or thinfilm versus thickfilm resistors) mounted on the substrate.

j. Increase in element attach area more than 50 percent from QML listing.

k. Substitution of baselined wire bond method (e.g., ultrasonic versus thermal compression) or wire size changes greater than 1.0 mil.

l. Any change in specified material composition or purity of the wire.

m. Increase in substrate attach perimeter more than 50 percent of QML listing.

n. Substitution of package configuration (e.g., platform versus bathtub), lid or covers (e.g., step lid versus drawn cover) or plating material.

o. Substitution of package or lid base material (e.g., nickel versus stainless steel).

p. Changes to finished device dimensions exceeding SCD, or SMD envelope tolerances.

q. Substitution of seal method (e.g., seam weld versus laser weld), or seal material (e.g., SnAg versus AuSn).

r. Change in the baselined seal process time, temperature, or vacuum of more than 10 percent, or sealing atmosphere except for the addition of helium.

s. Increase in package seal perimeter more than 50 percent from QML listing.

t. Increase in lead count for QML listing per package type.

u. Changes to the baselined product flowchart in which element evaluation, screening, CI and PI options, and any operations are added or deleted, except for additional inspections and SPC operations.

v. Addition of new processes or materials to QML.

w. Assembly operation or test facility move.

x. Class I changes as defined in MIL-STD-480.

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TABLE XIII. Testing guidelines for major product/process changes. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Major changes or substitutions	Recommended test subgroups of tables IXa, IXb, IXc, and IXd (unless otherwise noted)		Variable data required (subgroups)	
	CI & PI	QML	CI & PI	QML
a. Substitution of substrate material	C1	C1 -> C4	N/A	C4
b. Substitution of material deposited on substrate				
(1) conductor	A, B5, B6	A, C1 -> C4	B5, B6	C4
(2) resistor	A	A		
(3) deposit method	A, B5, B6, C2	A, C1 -> C4	B5, B6,C2	C4
c. Process/time/temperature changes	A, B5	Same as CI & PI	C2	C2
d. Substrate mask design	A1, B4, C2	N/A	C2	N/A
e. Substitution of trim method	A, C2	Same as CI & PI	C2	C2
f. Increase in multi-layer conductor levels, more than one level	B5, B6	C1 -> C4	B5, B6	C4
g,h. Substitution of attach material or process temperature	C1 -> C3	C1 -> C4 (no wirebond)	C3	C4
i. Substitution of die type	A, C2	N/A	C2	N/A
j. Increase in element area from QML listing	N/A	C1 -> C4 (no wirebond)	N/A	C4
k1. Substitution of baselined wirebond method	N/A	C1 -> C4 (no die shear)	N/A	C4
k2. Wire size change	C1, -> B5	C1 -> C4 (no die shear)	B5	C4
l. Substitution of wirebond material	C1 -> B5	C1 -> C4 (no die shear)	B5	C4
m. Increase in substrate perimeter from QML listing	N/A	C1 -> C4	N/A	C3
n. Substitution of package configuration, etc.	B1, C1 -> C3	C1 -> C3	N/A	C3
o. Substitution of package, lid base material	B1, C1 -> C3	C1 -> C3	C3	C3

See footnotes at end of table

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TABLE XIII. Testing guidelines for major product/process changes - Continued.
1/ 2/ 3/ 4/ 5/ 6/ 7/

Major changes or substitutions	Recommended test subgroups of tables IXa, IXb, IXc, and IXd (unless otherwise noted)		Variable data required (subgroups)	
	CI & PI	QML	CI & PI	QML
p. Change to finished device dimensions	Notify acquiring activity	N/A	N/A	N/A
q,r. Substitution of seal method, profile or seal material	C1 -> C3	C1 -> C3	C3	C3
s. Increase in package seal perimeter from QML listing	N/A	C1 -> C3	N/A	C3
t. Increase in lead count per package type	See Table VI C3 8/	See Table VI C3 8/	C3	C3
u. Change to baselined product flowchart	N/A	Notify qualifying activity	N/A	N/A
v. Addition of new process or material	N/A	Notify qualifying activity	N/A	N/A
w. Assembly operation or test facility move	N/A	Notify qualifying activity	N/A	N/A
x. Class I change, MIL-STD-480	Notify qualifying activity	Notify qualifying activity	N/A	N/A

1/ Sampling will be in accordance with table IXa, IXb, IXc, and IXd of this specification.
2/ All electrical parameter testing will be in accordance with the device acquisition specification or drawing or SMD.
3/ Data histograms providing a parametric data summary may be submitted in place of variables data.
4/ The acquiring or qualifying activity (or both) may add or reduce testing as warranted by detail specification requirements, unique design, or process circumstances after notification by the manufacturer.
5/ The acquiring activity will determine testing requirements for design changes affecting class K devices.
6/ Notification is required at the time of acceptance of new order or delivery on existing order when changes are made to devices acquired to Specification Control Drawings.
7/ -> implies specified subgroups testing will be sequential.
8/ Excluding subgroups 5 and 6.

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APPENDIX F

STATISTICAL SAMPLING, TEST AND INSPECTION PROCEDURES

F.1 SCOPE

F.1.1 Scope. This appendix contains statistical sampling qualification procedures and general test and inspection procedures used throughout this specification.

F.1.2 Description of Appendix F. This appendix contains general information and guidance to be used by manufacturers when testing and inspecting devices.

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F.2 APPLICABLE DOCUMENTS

F.2.1 Government documents.

F.2.1.1 Standard. The following standard forms a part of this document to the extent specified herein. Unless otherwise specified, the issue of this document is that listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise specified copies of military standards are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

F.3 GENERAL STATISTICAL SAMPLING

F.3.1 Definitions. The following definitions will apply for all statistical sampling procedures:

a. PDA series: The PDA series is defined as the following decreasing series of PDA values: 50, 30, 20, 15, 10, 7, 5, 3, 2, 1.5, 1, 0.7, 0.5, 0.3, 0.2, 0.15, 0.1.

b. Tightened PDA inspection: Tightened PDA inspection is defined as inspection performed using the next PDA value in the PDA series which is lower than that specified.

c. Acceptance number (c): The acceptance number is defined as zero.

d. Rejection number (r): Rejection number is defined as one or more.

F.3.2 Symbols. The following symbols will apply for all statistical sampling procedures:

a. c: Acceptance number.

b. r: Rejection number.

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F.4 STATISTICAL SAMPLING PROCEDURES AND TABLE

F.4.1 General. Statistical sampling will be conducted using a sample size (accept number) method as specified in table XIV herein. The procedures specified herein are suitable for all quality conformance requirements.

F.4.1.1 Selection of samples. Samples will be randomly selected from the inspection lot or inspection sublots. For continuous production, the manufacturer, at his option, may select the sample in a regular periodic manner during manufacture provided the lot meets the formation of lots requirement.

F.4.1.2 Failures. Failure of a unit for one or more tests of a subgroup will be charged as a single failure.

F.4.2 Single-lot sampling method. CI and PI information (sample sizes and number of observed defectives) will be accumulated from a single inspection lot to demonstrate conformance to the individual subgroup criteria.

F.4.2.1 Sample size. The sample size for each subgroup will be determined from table XIV and will meet the specified sample size (accept number).

F.4.2.2 Acceptance procedure. If zero failures are found in the initial sample of the required sample size, the lot will be accepted. If the observed number of defectives from the initial sample is greater than zero, a second sample of double the initial sample size may be selected from the original sub(lot). The sub(lot) may be accepted if zero defectives are observed in this double-size sample.

F.4.2.3 One-hundred percent inspection. Inspection of 100 percent of the lot will be allowed, at the option of the manufacturer, for any or all subgroups other than those which are called "destructive". If the observed percent defective for the inspection lot exceeds the specified PDA series value for the sample size specified, the lot will be considered to have failed the appropriate subgroup. One-hundred percent sampling is required where lot size is smaller than the required sample size with zero defectives allowed. Resubmission of lots tested on a 100 percent inspection bases will also be on a 100 percent inspection basis and in accordance with the tightened PDA inspection criteria.

TABLE XIV. Sample size (accept number) sampling plan. 1/ 2/ 3/

PDA series	50	30	20	15	10	7	5	3	2
	Minimum sample size (accept number)								
Accept number c = 0, r ≥ 1	5(0)	8(0)	11(0)	15(0)	22(0)	32(0)	45(0)	76(0)	116(0)

PDA series	1.5	1	0.7	0.5	0.3	0.2	.15	0.1
	Minimum sample sizes (accept number)							
Accept number c = 0, r ≥ 1	153(0)	231(0)	328(0)	461(0)	767(0)	1152(0)	1534(0)	2303(0)

1/ Sample sizes are based upon the Poisson exponential binomial limit.
2/ In this specification lot tolerance percent defective (LTPD) has been replaced with sample size (accept number) where the accept number is zero. Where reference is made by unrevised test methods of MIL-STD-883 to an LTPD value, that value will be found in the PDA series and the sample size will be the value immediately below the PDA series value. The accept number will always be zero.
3/ Minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percent defective equal to the specified sample size (accept number) will not be accepted (single sample).

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F.5 GENERAL TEST AND INSPECTION REQUIREMENTS

F.5.1 Procedure in case of test equipment failure or operator error. Whenever a device is believed to have failed as a result of faulty test equipment or operator error, the failure will be entered in the test record which will be retained for review along with a complete explanation verifying why the failure is believed to be invalid.

NOTE: ESD failures will be counted as rejects and not attributed to equipment or operator error for screening, group A and end-point electrical tests of screening, CI and PI, and Qualification and MIL-STD-883, method 5005.

F.5.1.1 Procedure for sample tests. When it has been established that a failure is due to test equipment failure or operator error and it has been established that the sample device has been damaged or degraded, a replacement device from the same inspection lot may be added to the sample. The replacement device will be subjected to all those tests to which the discarded device was subjected prior to its failure and to any remaining specified tests to which the discarded device was not subjected prior to its failure. The manufacturer, at his cwn risk, has the option of replacing the failed device and continuing with the tests before the validity of the test equipment failure or operator error has been established.

F.5.1.2 Procedure for screening tests. When it has been established that a lot failure during screening test is due to operator or equipment error and it has been established that the remaining product has not been damaged or degraded, the lot or surviving portion of the lot, as the case may be, may be resubmitted to the corrected screening test in which the error occurred. Failures verified as having been caused by test equipment failure or operator error will not be counted in the PDA calculation (when applicable).

F.5.1.3 Failure and corrective action reports. When the procedures of F.5.1.1 and F.5.1.2 are utilized in continuing sample tests or resubmitting lots for screening tests, the manufacturer will document the results of his failure investigations and corrective actions.

F.6 TRACEABILITY.

F.6.1 Material and element traceability. Traceability will be such that for each device, all adhesives and coatings will be traceable to a material production lot, inspection lot, or other specified grouping. All elements and materials used will be traceable to their incoming inspection lots. For class K, records will be maintained to provide traceability from the device serial number to the specific wafer lot from which each semiconductor and microcircuit element originated.

F.6.2 Process traceability. Each device, or each group of devices which have been fabricated as a common batch, will be identifiable through means of production travelers or similar documentation such that the complete manufacturing history, including rework, will be recorded. The records should include, as a minimum, the performance date of all identified production process steps, the specification, number of production process steps, and the identification of the operator performing the process steps. The records will be retained for a minimum of 5 years (7 years for class K) after delivery of the devices.

F.6.3 Production lot traceability. The manufacturer will maintain production lot traceability.

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