

The documentation and process conversion measures necessary to comply with this revision shall be completed by 19 November 2015.

INCH-POUND

MIL-PRF-19500/569A
19 August 2015
SUPERSEDING
MIL-S-19500/569
26 April 2010

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT, N-CHANNEL,
SILICON, TYPES 2N6966, 2N6967, 2N6968, 2N6969,
JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for N-channel, enhancement-mode, MOSFET, power transistor intended for use in high density power switching applications. Four levels of product assurance are provided for each encapsulated device type (JAN, JANTX, JANTXV, and JANS).

1.2 Package outlines. The device package outlines are as follows: similar to TO-66 in accordance with [figure 1](#).

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Type	P_T (1)	P_T	V_{DS}	V_{DG}	V_{GS}	I_{D1} (2) (3)	I_{D2} (2)
	$T_C = +25^\circ\text{C}$	$T_C = +25^\circ\text{C}$ (free air)				$T_C = +25^\circ\text{C}$	$T_C = +100^\circ\text{C}$
	<u>W</u>	<u>W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>
2N6966	70	5	100	100	± 20	15	13
2N6967	70	5	200	200	± 20	13	8
2N6968	70	5	400	400	± 20	7.5	5
2N6969	70	5	500	500	± 20	6	4

Type	I_S	I_{DM} (4)	T_J and T_{STG}	V_{ISO} 100,000 feet altitude	Max $r_{DS(on)}$ (1) $V_{GS} = 10 \text{ V dc}$, $I_D = I_{D2}$		$R_{\theta JC}$ max
					$T_J = +25^\circ\text{C}$	$T_J = +150^\circ\text{C}$	
	<u>A dc</u>	<u>A (pk)</u>	<u>$^\circ\text{C}$</u>		<u>ohms</u>	<u>ohms</u>	<u>$^\circ\text{C/W}$</u>
2N6966	-15	± 60	-55 to +150		0.085	0.13	1.8
2N6967	-13	± 50	-55 to +150		0.18	0.27	1.8
2N6968	-7.5	± 30	-55 to +150	400	0.55	1.04	1.8
2N6969	-6.0	± 24	-55 to +150	500	0.85	1.62	1.8

See notes on next page.

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1.3 Maximum ratings - Continued.

- (1) Derate linearly 0.56 W/°C for $T_C > +25^\circ\text{C}$;
- (2) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal wires and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

- (3) $I_{DM} = 4 \times I_{D1}$ as calculated in note 2.

1.4 Primary electrical characteristics. Unless otherwise specified, $T_C = +25^\circ\text{C}$.

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0 \text{ V}$ $I_D = 1 \text{ mA dc}$	$V_{GS(th)1}$ $V_{DS} \geq V_{GS}$ $I_D = 0.25 \text{ mA}$	Max I_{DSS1} $V_{GS} = 0 \text{ V}$ $V_{DS} = 80 \text{ percent}$ $\text{of rated } V_{DS}$	Max $r_{DS(on)1}$ (1) $V_{GS} = 10 \text{ V dc}$ $I_D = I_{D2}$	
				$T_J = +25^\circ\text{C}$ at I_{D1}	$T_J = +150^\circ\text{C}$ at I_{D2}
	<u>V dc</u>	<u>V dc</u> Min Max	<u>µA dc</u>	<u>ohms</u>	<u>ohms</u>
2N6966	100	2.0 4.0	25	0.085	0.13
2N6967	200	2.0 4.0	25	0.18	0.27
2N6968	400	2.0 4.0	25	1.0	1.04
2N6969	500	2.0 4.0	25	1.5	1.62

- (1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".

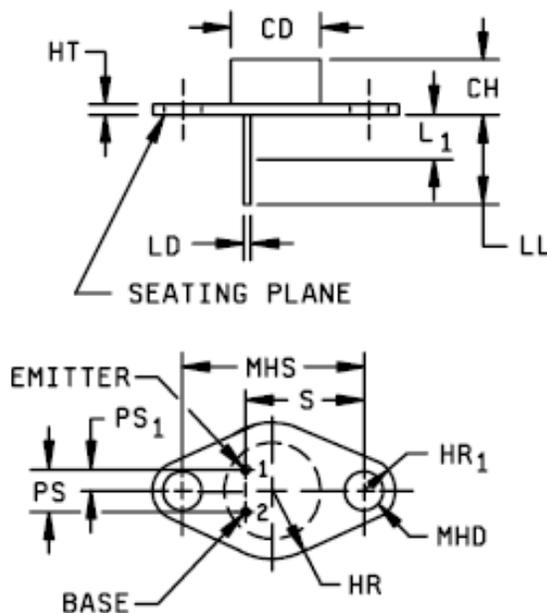
1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

1.5.2.2 Second number symbols. The second number symbols for the transistor covered by this specification sheet are as follows: "6966", "6967", "6968", and "6969".

1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

Dimensions					Notes
Symbol	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.620		15.76	
CH	.250	.340	6.35	8.64	
HR		.350		8.89	
HT	.050	.075	1.27	1.91	
HR ₁	.115	.145	2.92	3.68	4
LD	.028	.034	.71	.86	4, 6
LL	.360	.500	9.14	12.70	
L ₁		.050		1.27	6
MHD	.142	.161	3.61	4.08	4
MHS	.950	.970	24.13	24.53	
PS	.190	.210	4.83	5.33	3
PS ₁	.093	.107	2.36	2.73	3
S	.570	.590	14.48	14.99	
Notes	1, 2, 5, 7				



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. These dimensions should be measured at points .050 inch (1.27 mm) \pm .005 inch (0.13 mm) \pm .000 inch (0.00 mm) below seating plane. When gauge is not used, measurement will be made at the seating plane.
4. Two places.
5. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
6. Lead diameter shall not exceed twice LD within L₁.
7. Lead number 1 is the emitter, lead 2 is the base, case is the collector.
8. In accordance with ASME Y14.5M, diameters are equivalent to \varnothing x symbology.

FIGURE 1. Physical dimensions (similar to TO-66).

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <http://quicksearch.dla.mil/>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

nC nano coulomb.
I_{AS} Rated avalanche current, non-repetitive.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#) (similar to TO-66).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Internal construction. Multiple chip construction is not permitted to meet the requirements of this specification.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of electrostatic charge. The following handling practices shall be followed:

- a. Devices shall be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.8 Electrical test requirements. The electrical test requirements shall be the subgroups specified in 4.4.2 and 4.4.3 herein.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTX and JANTXV levels
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, (see 4.3.2) optional	Method 3470 of MIL-STD-750, (see 4.3.2) optional
(3) 3c	Method 3161 of MIL-STD-750, (see 4.3.3)	Method 3161 of MIL-STD-750, (see 4.3.3)
9	I_{GSSF1} , I_{GSSR1} , I_{DSS1}	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(th)1}$, subgroup 2 of table I herein: $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater.	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(th)1}$, subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A, t = 240 hours	Method 1042 of MIL-STD-750, test condition A; or t = 48 hours minimum at +175°C min
13	Subgroups 2 and 3 of table I herein; $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(th)1} = \pm 20$ percent of initial value.	Subgroup 2 of table I herein; $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(th)1} = \pm 20$ percent of initial value.

- (1) At the end of the test program, I_{GSSF1} , I_{GSSR1} and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} and $V_{GS(th)1}$ shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and TXV levels do not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply $V_{GS} = 30$ V minimum for $t = 250$ μ s minimum.

4.3.2 Single pulse unclamped inductive switching.

- a. Peak current, I_D Rated I_{D1} .
- b. Peak gate voltage, V_{GS}10 V.
- c. Gate to source resistor, R_{GS} $25 \leq R_{GS} \leq 200$.
- d. Initial case temperature+25°C +10, -5°C.
- e. Inductance100 μ H minimum.
- f. Number of pulses to be applied1 pulse minimum.
- g. Supply voltage V_{DD} 50 V.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (and V_H where appropriate). (See figure 2 herein.) Measurement delay time (t_{MD}) = 70 μ s max. See [table II](#), group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#), and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with appendix E, table E-V of [MIL-PRF-19500](#) and [table I](#) herein. Electrical measurements (end-points) shall be in accordance with the inspections of [table I](#), subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#).

4.4.2.1 Group B inspection, appendix E, table E-VIA (JANS) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1051	Test condition G.
B4	1042	Test condition D; the heating cycle shall be 1 minute minimum.
B5	1042	Accelerated steady-state operation life; test condition A, $V_{DS} =$ rated $T_A = +175^\circ\text{C}$, $t = 120$ hours minimum. Read and record $V_{(BR)DSS}$ (pre and post at 1 mA = I_D . Read and record I_{DSS} (pre and post). Deltas for $V_{(BR)DSS}$ shall not exceed 10 percent and I_{DSS} shall not exceed 25 μ A. Accelerated steady-state gate stress; condition B, $V_{GS} =$ rated, $T_A = +175^\circ\text{C}$, $t = 24$ hours.
B5	2037	Bond strength; test condition D.

4.4.2.2 Group B inspection, appendix E, table E-VIB (JAN, JANTX and JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B2	1051	Test condition G.
B3	1042	Test condition D. The heating cycle shall be 1 minute minimum.
B3	2037	Test condition D. All internal bond wires for each device shall be pulled separately.
B4	2075	See 3.4.2 .

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-VII of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	1056	Test condition A.
C2	2036	Test condition A; weight = 10 lbs., t = 15 s.
C5	3161	See 4.3.3 .
C6	1042	Test condition D; The heating cycle shall be 1 minute minimum.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

TABLE I. Group A inspection.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal response <u>2</u> /	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source	3407	$V_{GS} = 0$ V dc, $I_D = 1$ mA dc, condition C	$V_{(BR)DSS}$			V dc
2N6966				100		
2N6967				200		
2N6968				400		
2N6969				500		
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ $I_D = 0.25$ mA dc	$V_{GS(th)1}$	2.0	4.0	V dc
Gate current	3411	$V_{GS} = +20$ V dc, $V_{DS} = 0$, bias condition C	I_{GSSF1}		± 100	nA dc
Gate current	3411	$V_{GS} = -20$ V dc, $V_{DS} = 0$, bias condition C	I_{GSSR1}		± 100	nA dc
Drain current	3413	$V_{GS} = 0$ V dc $V_{DS} = 80$ percent of rated V_{DS} ; bias condition C	I_{DSS1}		25	μA dc
Static drain to source on-state resistance	3421	$V_{GS} = 10$ V dc, pulsed (see 4.5.1); condition A, $I_D =$ rated I_{D2} (see 1.3)	$r_{DS(on)1}$			ohms
2N6966					0.085	
2N6967					0.18	
2N6968					0.55	
2N6969					0.85	
Static drain to source on-state resistance	3421	$V_{GS} = 10$ V dc, pulsed (see 4.5.1); condition A, $I_D =$ rated I_{D1} (see 1.3)	$V_{DS(on)}$			V
2N6966					1.70	
2N6967					2.40	
2N6968					4.13	
2N6969					5.10	

See footnotes at end of table.

TABLE I. Group A inspection – Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> – Continued						
Forward voltage (source drain diode)	4011	Condition C, $V_{GS} = 0 \text{ V}$, $I_D = I_{D1}$	V_{SD}			V
2N6966				.85	2.5	
2N6967				.8	2.0	
2N6968				.8	2.0	
2N6969				.8	2.0	
Forward transconductance	3475	Pulsed (see 4.5.1)	gFS			S
2N6966				6	18	
2N6967				6	18	
2N6968				4	12	
2N6969				4	12	
<u>Subgroup 3</u>						
High temperature operation:		$T_C = T_J = +125^\circ\text{C}$				
Gate current	3411	Bias condition C $V_{GS} = \pm 20 \text{ V dc}$ $V_{DS} = 0 \text{ V dc}$	I_{GSS2}		± 200	nA dc
Drain current	3413	Bias condition C $V_{GS} = 0 \text{ V dc}$ $V_{DS} = 80 \text{ percent of rated } V_{DS}$	I_{DSS2}		0.25	mA dc
2N6966						
2N6967						
2N6968						
2N6969						
Static drain to source on-state resistance	3421	$V_{GS} = 10 \text{ V dc}$ pulsed (see 4.5.1); $I_D = \text{rated } I_{D2}$	$r_{DS(on)2}$			ohms
2N6966					0.13	
2N6967					0.27	
2N6968					1.04	
2N6969					1.62	
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ $I_D = 0.25 \text{ mA dc}$	$V_{GS(th)2}$	1.0		V dc

See footnotes at end of table.

TABLE I. Group A inspection – Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> – Continued						
Low temperature operation:		$T_C = T_J = -55^\circ\text{C}$				
Gate to source voltage threshold	3403	$V_{DS} \geq V_{GS}$ $I_D = 0.25 \text{ mA dc}$	$V_{GS(th)3}$		5.0	V dc
<u>Subgroup 4</u>						
Switching time test	3472	$I_D = \text{rated } I_{D2}$ (see 1.3); $V_{GS} = 10 \text{ V dc}$, Gate drive impedance = 7.5Ω				
Turn-on delay time			$t_{d(on)}$			ns
2N6966		$V_{DD} = 34 \text{ V dc}$			30	
2N6967		$V_{DD} = 75 \text{ V dc}$			30	
2N6968		$V_{DD} = 175 \text{ V dc}$			35	
2N6969		$V_{DD} = 200 \text{ V dc}$			35	
Rise time			t_r			ns
2N6966		$V_{DD} = 34 \text{ V dc}$			60	
2N6967		$V_{DD} = 75 \text{ V dc}$			60	
2N6968		$V_{DD} = 175 \text{ V dc}$			30	
2N6969		$V_{DD} = 200 \text{ V dc}$			30	
Turn-off delay time			$t_{d(off)}$			ns
2N6966		$V_{DD} = 34 \text{ V dc}$			80	
2N6967		$V_{DD} = 75 \text{ V dc}$			80	
2N6968		$V_{DD} = 175 \text{ V dc}$			90	
2N6969		$V_{DD} = 200 \text{ V dc}$			90	
Fall time			t_f			ns
2N6966		$V_{DD} = 34 \text{ V dc}$			30	
2N6967		$V_{DD} = 75 \text{ V dc}$			60	
2N6968		$V_{DD} = 175 \text{ V dc}$			35	
2N6969		$V_{DD} = 200 \text{ V dc}$			30	
<u>Subgroup 5</u>						
Safe operating area test	3474	See figure 3; $V_{DS} = 80$ percent of rated V_{DS} ; $t_p = 10 \text{ ms}$				
Electrical measurements		See table I , subgroup 2				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection ^{1/}	MIL-STD-750		Symbol	Limits		Unit	
	Method	Conditions		Min	Max		
<u>Subgroup 6</u>							
Not applicable							
<u>Subgroup 7</u>							
Gate charge	3471	Condition A and B					
Test 1							
Minimum off-state gate charge			$Q_{g(th)}$	2.7	8.0	nC	
Test 2			$Q_{g(on)}$	30	77	nC	
On-state gate charge			$Q_{gm(on)}$	51	130	nC	
Test 3							
Maximum on-state gate charge			V_{GP}	4	8	V dc	
Test 4							
Gate plateau voltage charge			Q_{gs}	4.6	13	nC	
Test 5							
Gate to source charge			Q_{gd}	13	40	nC	
Test 6							
Gate to drain charge			t_{rr}			ns	
Reverse recovery time	3473	di/dt = 100 A/μs $V_{DD} \leq 30$ V, $I_D = I_{D1}$					
2N6966						400	
2N6967						650	
2N6968						800	
2N6969						1000	

^{1/} For sampling plan, see [MIL-PRF-19500](#).

^{2/} This test required for the following end-point measurements only:
 Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).
 Group B, subgroups 3 and 4 (JANS).
 Group C, subgroup 6.
 Group E, subgroup 1.

TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycle	1051	Condition G, 500 cycles	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 2</u> ^{1/}			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 4</u>			sample size N/A
Thermal impedance curves		See MIL-PRF-19500	
<u>Subgroup 5</u>			3 devices c = 0
Barometric pressure (reduced) 400 and 500 V only	1001	Test condition C $V_{ISO} = V_{DS}$, $I_{(ISO)} = .25$ mA (max)	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	

^{1/} A separate sample for each test may be pulled.

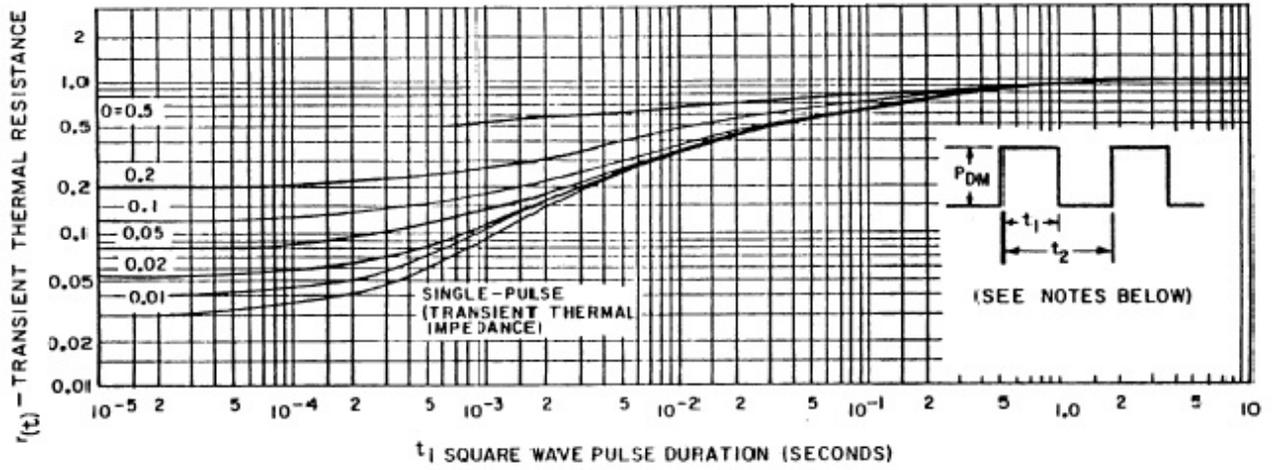


FIGURE 2. Thermal response curves.

2N6966

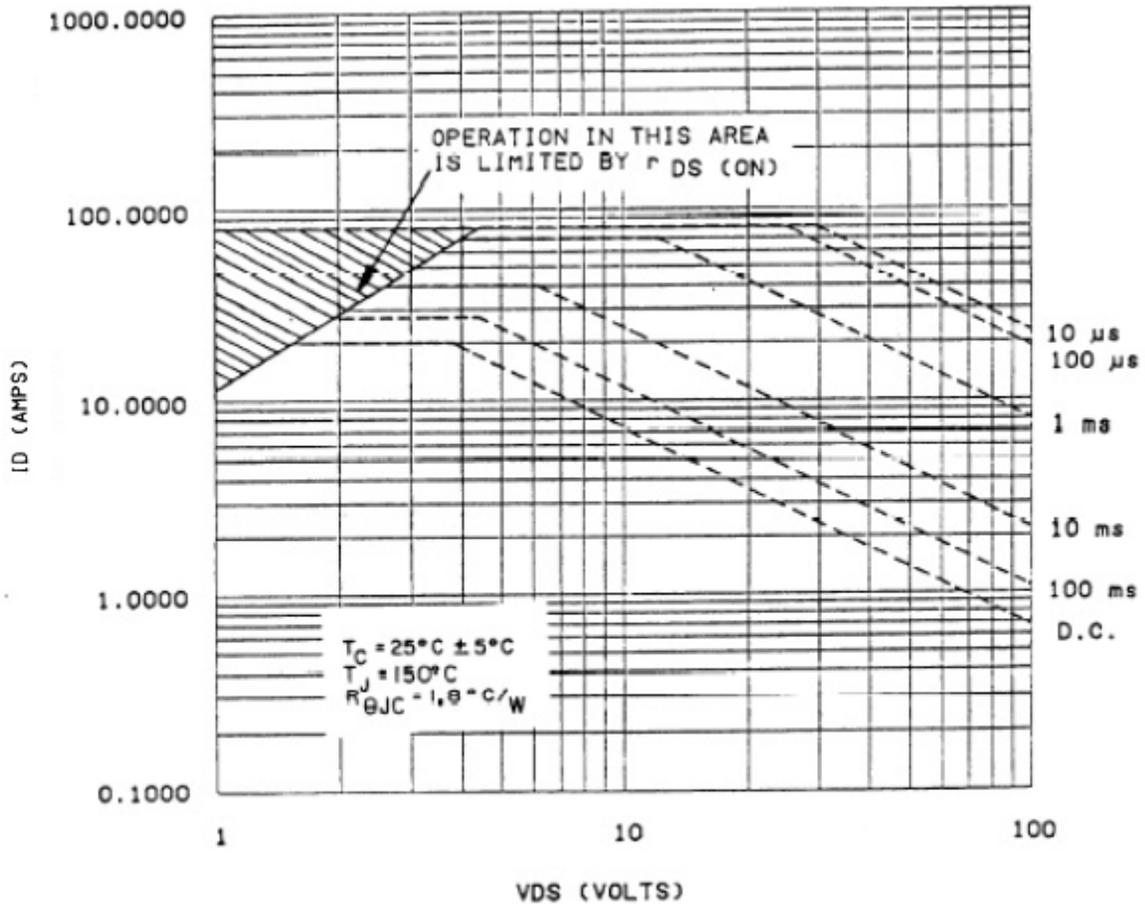


FIGURE 3. Safe operating area.

2N6967

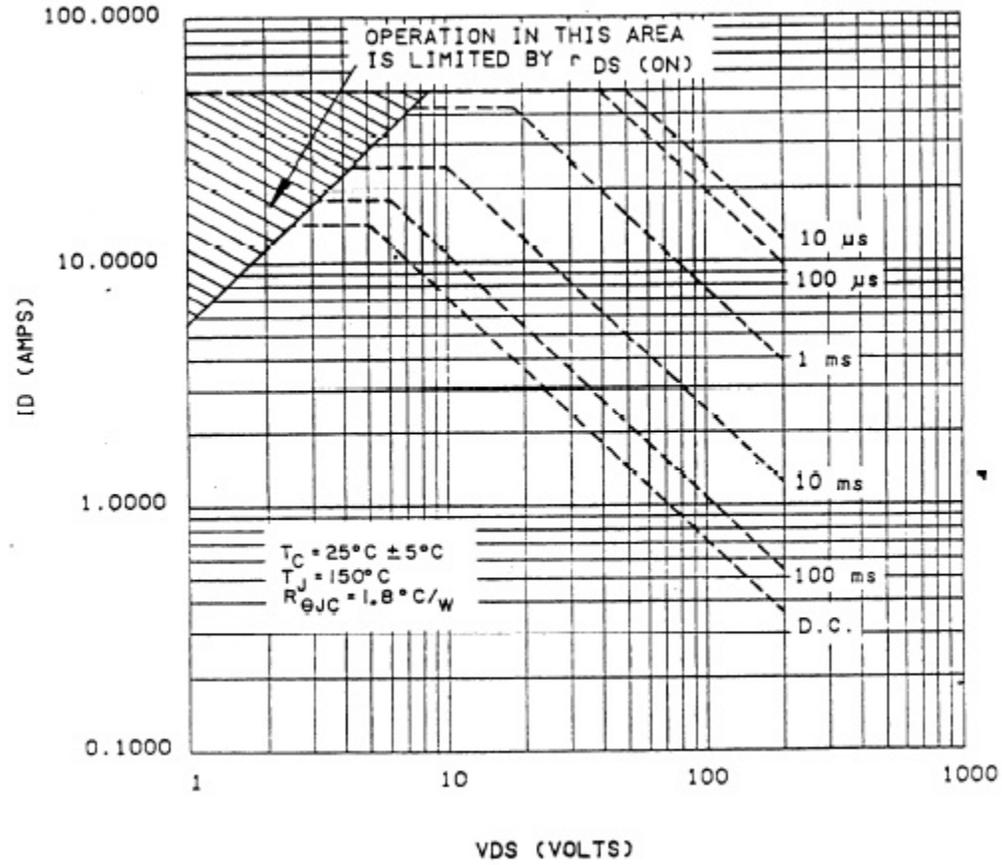


FIGURE 3. Safe operating area - Continued.

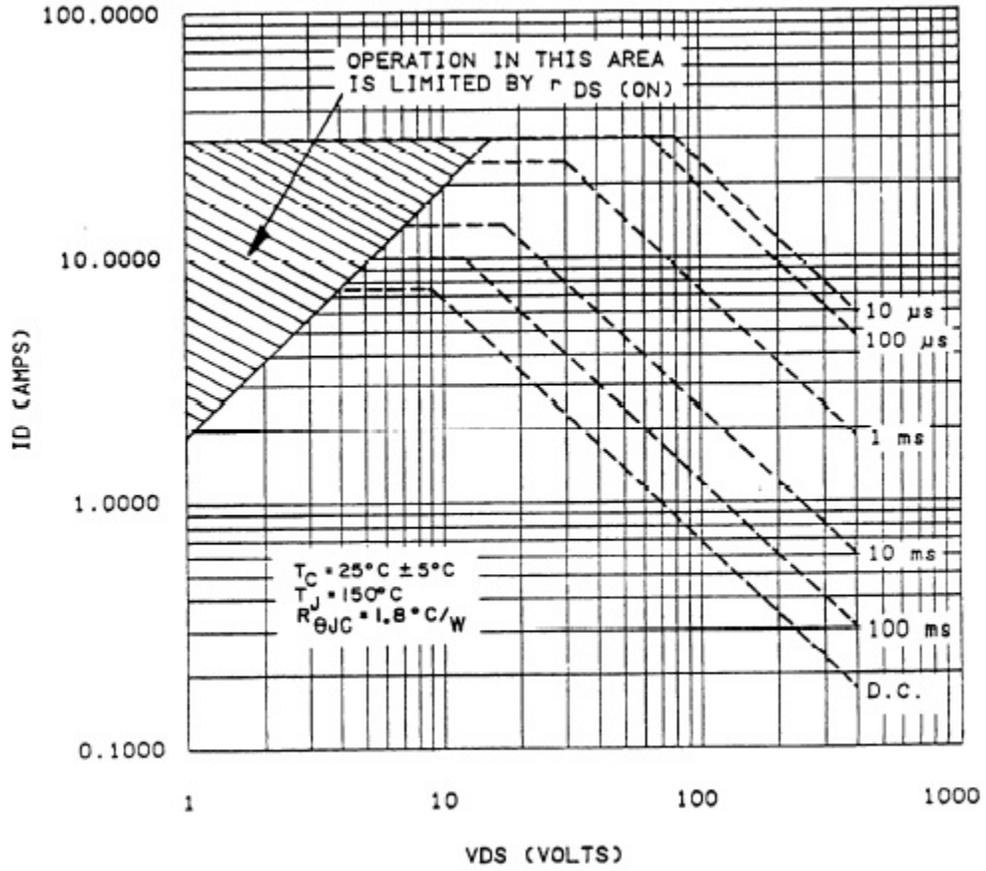


FIGURE 3. Safe operating area - Continued.

2N6969

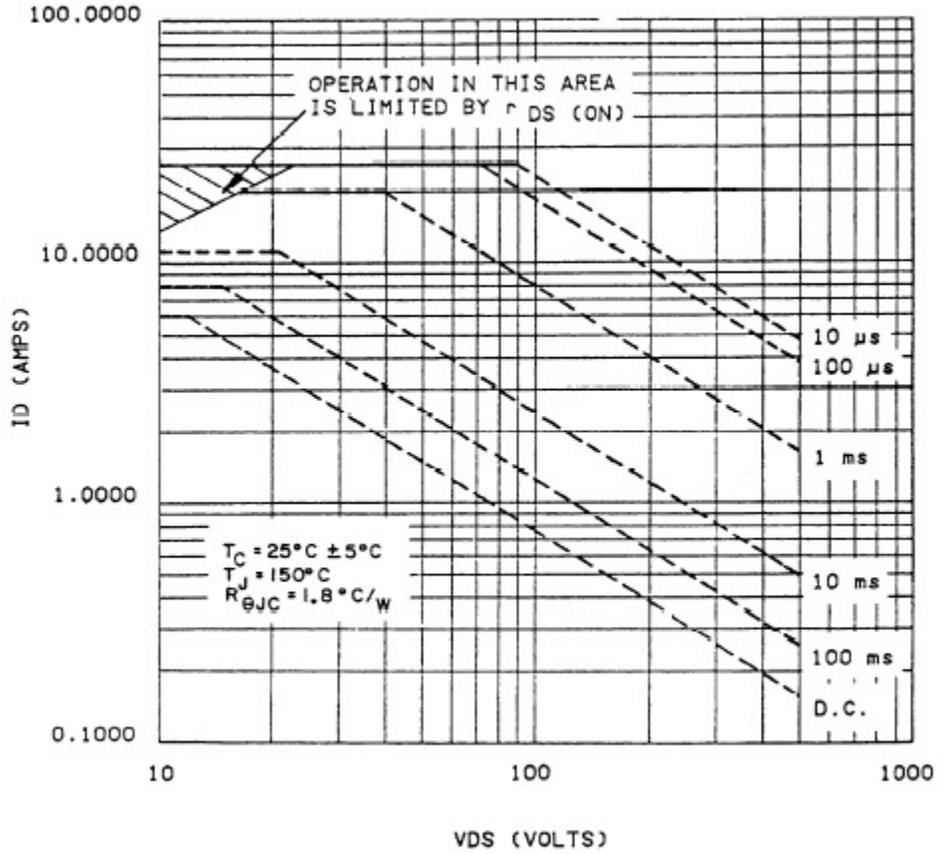


FIGURE 3. Safe operating area - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.6.

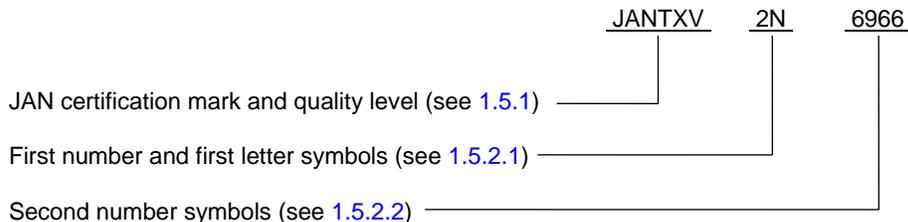
6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's PIN. This information in no way implies that manufacturers' PIN's are suitable as a substitute for the military PIN.

PIN	Commercial types
2N6966	IRFJ140
2N6967	IRFJ240
2N6968	IRFJ340
2N6969	IRFJ440

6.5 PIN construction example.

6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



6.6 List of PINs.

6.6.1 List of PINs for unencapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN2N6966	JANTX2N6966	JANTXV2N6966	JANS2N6966
JAN2N6967	JANTX2N6967	JANTXV2N6967	JANS2N6967
JAN2N6968	JANTX2N6968	JANTXV2N6968	JANS2N6968
JAN2N6969	JANTX2N6969	JANTXV2N6969	JANS2N6969

6.7 Changes from previous issue. The margins of this specification are not marked with asterisks due to the extent of the changes.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 85
 NASA - NA
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5961-2015-078)

Review activities:
 Army – AR, SM
 Navy – AS, CG, MC, OS, SH
 Air Force - 19, 70, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.