

The documentation and process conversion measures necessary to comply with this revision shall be completed by 9 August 2008.

INCH-POUND

MIL-PRF-19500/732A
 9 May 2008
 SUPERSEDING
 MIL-PRF-19500/732
 14 November 2005

PERFORMANCE SPECIFICATION SHEET

* SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED
 (TOTAL DOSE AND SINGLE EVENT EFFECTS)
 TRANSISTORS, P-CHANNEL, SILICON,
 TYPES 2N7519U3, 2N7519U3C, 2N7519T3, 2N7520U3, 2N7520U3C, AND 2N7520T3,
 JANTXVR, F AND JANSR, F

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a P-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). See 6.5 for JANHC and JANKC die versions.

* 1.2 Physical dimensions. See figure 1, TO-257AA (T3) and figure 2, SMD.5 TO-276AA (U3 or with ceramic lid, U3C).

* 1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Type	P _T (1) T _C = +25°C	P _T T _A = +25°C	R _{θJC} (2)	V _{DS}	V _{DG}	V _{GS}	I _{D1} (3) (4) T _C = +25°C	I _{D2} (3) (4) T _C = +100°C	I _S	I _{DM} (5)	T _J and T _{STG}
	<u>W</u>	<u>W</u>	<u>°C/W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A(pk)</u>	<u>°C</u>
2N7519U3, 2N7519U3C	75	1.56	1.67	-30	-30	±20	-22	-18	-22	-88	-55 to +150
2N7520U3, 2N7520U3C	75	1.56	1.67	-60	-60	±20	-21	-13.3	-21	-84	
2N7519T3	75	1.56	1.67	-30	-30	±20	-20	-18	-20	-80	
2N7520T3	75	1.56	1.67	-60	-60	±20	-20	-13	-20	-80	

(1) Derate linearly 0.6 W/°C for T_C > +25°C.

(2) See figure 3, thermal impedance curves.

(3) The following formula derives the maximum theoretical I_D specs. I_D is limited by package and device construction to 20 A for TO-257AA and to 22 A for TO-276AA:

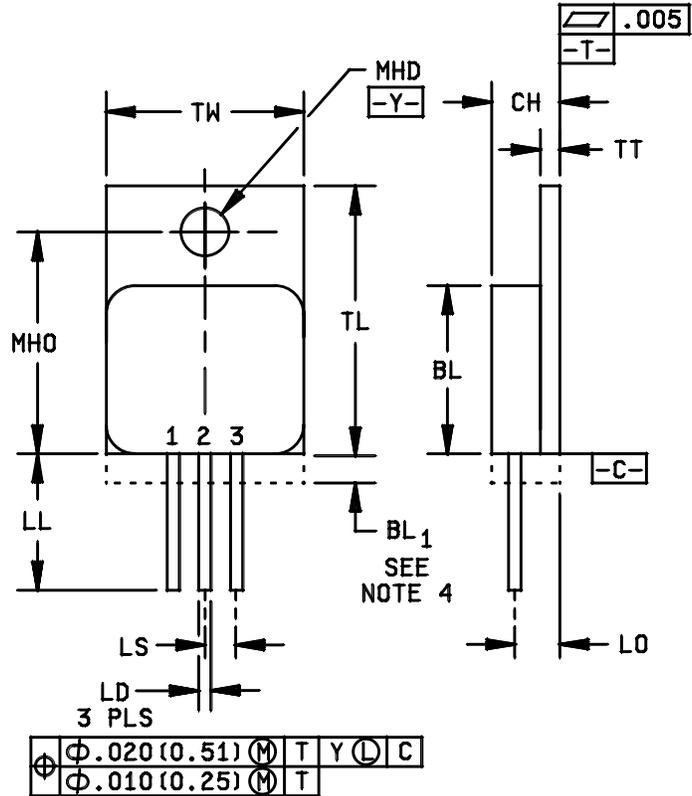
$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

(4) See figure 4, maximum drain current graph.

(5) I_{DM} = 4 X I_{D1} as defined in note (3).

Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dsc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil/>.

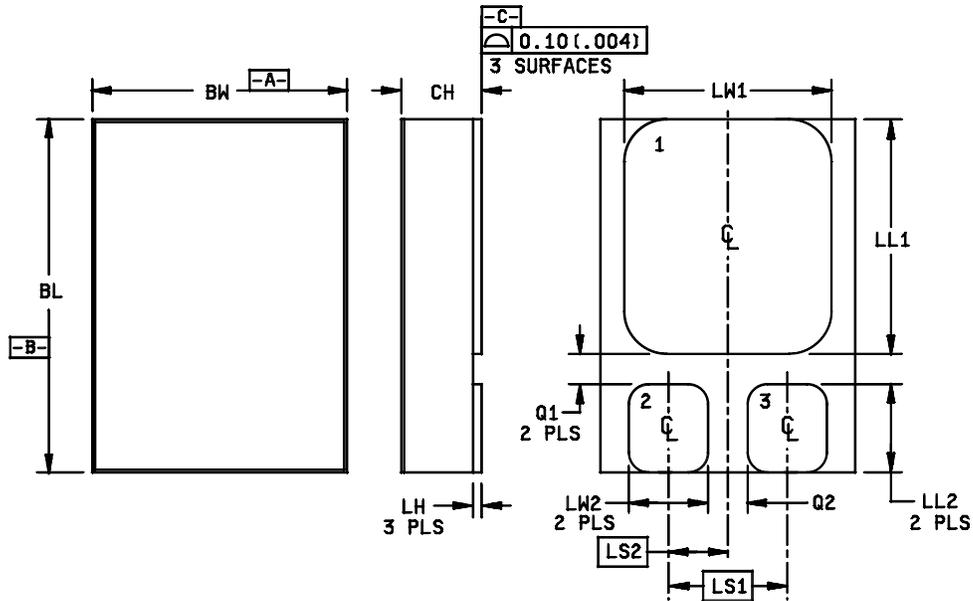
Dimensions				
Ltr	Inches		Millimeters	
	Min	Max	Min	Max
* BL	.410	.430	10.41	10.92
BL ₁		.033		0.84
CH	.190	.200	4.83	5.08
LD	.025	.035	0.64	0.89
LL	.600	.650	15.24	16.51
LO	.120 BSC		3.05 BSC	
LS	.100 BSC		2.54 BSC	
MHD	.140	.150	3.56	3.81
MHO	.527	.537	13.39	13.64
TL	.645	.665	16.38	16.89
TT	.035	.045	0.89	1.14
TW	.410	.420	10.41	10.67
Term 1	Drain			
Term 2	Source			
Term 3	Gate			



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from the case.
4. This area is for the lead feed-thru eyelets (configuration is optional, but will not extend beyond this zone).
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

* FIGURE 1. Physical dimensions for TO-257AA (2N7519T3 and 2N7520T3).



Ltr.	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
* CH (for U3)		.124		3.15
* CH (for U3C)		.134		3.40
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
4. Terminal 1 - Drain, Terminal 2 - Gate, Terminal 3 - Source.

* FIGURE 2. Physical dimensions for SMD.5 TO-276AA (2N7519U3, 2N7519U3C, 2N7520U3, and 2N7520U3C).

* 1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min V _{(BR)DSS} V _{GS} = 0 I _D = 1.0 mA dc	V _{GS} (TH)1 V _{DS} ≥ V _{GS} I _D = 1.0 mA dc		Max I _{DSS1} V _{GS} = 0 V _{DS} = 80 percent of rated V _{DS}	Max r _{DS(on)} (1) V _{GS} = 12 V dc		E _{AS} at I _{D1}	I _{AS}
					T _J = +25°C at I _{D2}	T _J = +150°C at I _{D2}		
	V dc	V dc		μA dc	ohm	ohm	mJ	A
		Min	Max					
2N7519U3, 2N7519U3C	-30	-2.0	-4.0	-10	0.070	0.091	152	-22
2N7520U3, 2N7520U3C	-60	-2.0	-4.0	-10	0.085	0.170	110	-21
2N7519T3	-30	-2.0	-4.0	-10	0.072	0.094	200	-20
2N7520T3	-60	-2.0	-4.0	-10	0.087	0.180	134	-20

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

* 2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

* 3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figures 1 (T3, TO-257AA) and 2 (U3 and U3C, surface mount TO-276AA) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.5.1 Handling. MOS devices shall be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate shall be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.2 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. See the design safe operation area figures herein. Electrical measurements (end-points) shall be in accordance with table III herein.

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4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV level
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)
(1) 9	Subgroup 2 of table I herein; I _{GSSF1} , I _{GSSR1} , I _{DSS1}	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein; I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(on)1} , V _{GS(TH)1} . Δ I _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. Δ I _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. Δ I _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein; I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(on)1} , V _{GS(TH)1}
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein; Δ I _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. Δ I _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. Δ I _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δ r _{DS(on)1} = ± 20 percent of initial value. Δ V _{GS(TH)1} = ±20 percent of initial value.	Subgroups 2 and 3 of table I herein; Δ I _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. Δ I _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. Δ I _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δ r _{DS(on)1} = ±20 percent of initial value. Δ V _{GS(TH)1} = ±20 percent of initial value.

- (1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and V_{GS(th)1} shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply $V_{GS} = -24$ V minimum for $t = 250$ μ s minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

- a. Peak current (I_{AS}) $I_{AS(max)}$.
- b. Peak gate voltage (V_{GS}) 12 V.
- c. Gate to source resistor (R_{GS}) $25\Omega \leq R_{GS} \leq 200\Omega$.
- d. Initial case temperature (T_C) $+25^\circ\text{C} +10^\circ\text{C}, -5^\circ\text{C}$.
- e. Inductance (L)..... $\left[\frac{2E_{AS}}{(I_{DI})^2} \right] \left[\frac{(V_{BR} - V_{DD})}{V_{BR}} \right] \text{mH minimum}$.
- f. Number of pulses to be applied 1 pulse minimum.
- g. Supply voltage (V_{DD}) 25 V.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μ s max. See table III, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.2.1 Group B inspection, table E-VIA (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Inspection</u>
B3	1051	Test condition G, 100 cycles.
B3	2077	Scanning electron microscope (SEM) qualification may be performed anytime prior to lot formation.
B4	1042	Condition D, 2,000 cycles. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5	1042	Test condition B, $V_{GS} = \text{rated}$ $T_A = +175^\circ\text{C}$, $t = 24$ hours.
B5	1042	Test condition A, $V_{DS} = \text{rated}$; $T_A = +175^\circ\text{C}$; $t = 120$ hours.
* B5	2037	Bond strength, test condition D.
B6	3161	See 4.3.3, $R_{\theta JC(\text{max})} = 1.67^\circ\text{C/W}$.

4.4.2.2 Group B inspection, table E-VIB (JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Inspection</u>
B2	1051	Test condition G, 25 cycles. (45 total, including 20 cycles performed in screening).
B3	1042	Test condition D, 2,000 cycles. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5 and B6		Not applicable.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Inspection</u>
C2	2036	Test condition A, weight = 10 lbs., $t = 10$ s (applicable to TO-257AA only).
C5	3161	See 4.3.3, $R_{\theta JC(\text{max})} = 1.67^\circ\text{C/W}$.
C6	1042	Test condition D, 6,000 cycles. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

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* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance 2/	3161	See 4.3.3	Z _{θJC}		1.6	°C/W
2N7519U3, 2N7520U3 2N7519U3C, 2N7520U3C 2N7519T3, 2N7520T3					1.5	°C/W
Breakdown voltage, drain to source	3407	V _{GS} = 0 V dc, I _D = -1 mA dc, bias condition C	V _{(BR)DSS}			
2N7519U3, 2N7519T3 2N7519U3C				-30		V dc
2N7520U3, 2N7520T3 2N7520U3C				-60		V dc
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS} , I _D = -1 mA dc	V _{GS(TH)1}	-2.0	-4.0	V dc
Gate reverse current	3411	V _{GS} = +20 V dc, bias condition C, V _{DS} = 0	I _{GSSF1}		+100	nA dc
Gate reverse current	3411	V _{GS} = -20 V dc, bias condition C, V _{DS} = 0	I _{GSSR1}		-100	nA dc
Drain current	3413	V _{GS} = 0 V dc, bias condition C, V _{DS} = 80 percent of rated V _{DS}	I _{DSS1}		-10	μA dc
Static drain to source on-state resistance	3421	V _{GS} = -12 V dc, condition A, pulsed (see 4.5.1), I _D = I _{D2}	r _{DS(on)1}			
2N7519U3, 2N7519U3C 2N7520U3, 2N7520U3C 2N7519T3 2N7520T3					0.070 0.085 0.072 0.087	Ω Ω Ω Ω
Forward voltage	4011	Pulsed (see 4.5.1), I _D = I _{D1} , V _{GS} = 0 V dc	V _{SD}		-5.0	V

See footnotes at end of table.

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* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u>						
High temperature operation:						
Gate reverse current	3411	$T_C = T_J = +125^\circ\text{C}$ $V_{GS} = -20\text{ V dc and } +20\text{ V dc,}$ bias condition C, $V_{DS} = 0$	I_{GSS2}		± 200	nA dc
Drain current	3413	$V_{GS} = 0\text{ V dc,}$ bias condition C, $V_{DS} = 80\text{ percent of rated } V_{DS}$	I_{DSS2}		-25	$\mu\text{A dc}$
Static drain to source on-state resistance	3421	$V_{GS} = -12\text{ V dc,}$ pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)3}$			
2N7519U3, 2N7519U3C					0.084	Ω
2N7520U3, 2N7520U3C					0.136	Ω
2N7519T3					0.086	Ω
2N7520T3					0.139	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS},$ $I_D = -1\text{ mA dc}$	$V_{GS(TH)2}$	-1.0		V dc
Low temperature operation:						
Gate to source voltage (threshold)	3403	$T_C = T_J = -55^\circ\text{C}$ $V_{DS} \geq V_{GS},$ $I_D = -1\text{ mA dc}$	$V_{GS(TH)3}$		-5.0	V dc
<u>Subgroup 4</u>						
Forward transconductance	3475	$I_D = \text{rated } I_{D2},$ $V_{DD} = -15\text{ V}$ (see 4.5.1)	gFS			
2N7519U3, 2N7519U3C, 2N7519T3				12		S
2N7520U3, 2N7520U3C, 2N7520T3				10		S
Switching time test	3472	$I_D = \text{rated } I_{D1},$ $V_{GS} = -12\text{ V dc,}$ $R_G = 7.5\Omega,$ $V_{DD} = 50\text{ percent}$ of rated V_{DS}				
Turn on delay time			$t_{d(on)}$		25	ns
Rise-time			t_r			
2N7519U3, 2N7519U3C, 2N7519T3					100	ns
2N7520U3, 2N7520U3C, 2N7520T3					65	ns
Turn-off delay time			$t_{d(off)}$			
2N7519U3, 2N7519U3C, 2N7519T3					50	ns
2N7520U3, 2N7520U3C, 2N7520T3					75	ns
Fall time			tf			
2N7519U3, 2N7519U3C, 2N7519T3					70	ns
2N7520U3, 2N7520U3C, 2N7520T3					50	ns

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 5; $t_p = 10$ ms, $V_{DS} = 80$ percent of rated V_{DS}				
Electrical measurements		See table I, subgroup 2 herein.				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B	$Q_{G(on)}$			
2N7519U3, 2N7519U3C, 2N7519T3					45	nC
2N7520U3, 2N7520U3C, 2N7520T3					45	nC
On-state gate charge			Q_{GS}			
2N7519U3, 2N7519U3C, 2N7519T3					20	nC
2N7520U3, 2N7520U3C, 2N7520T3					18	nC
Gate to drain charge			Q_{GD}			
2N7519U3, 2N7519U3C, 2N7519T3					13	nC
2N7520U3, 2N7520U3C, 2N7520T3					13	nC
Reverse recovery time	3473	$di/dt \leq 100A/\mu s$, $I_D = I_{D1}$	t_{rr}			
2N7519U3, 2N7519U3C, 2N7519T3		$V_{DD} \leq 30$ V			75	ns
2N7520U3, 2N7520U3C, 2N7520T3		$V_{DD} \leq 50$ V			100	ns

1/ For sampling plan, see MIL-PRF-19500.

2/ This test required for the following end-point measurements only:

- Group B, subgroups 3 and 4 (JANS).
- Group B, subgroups 2 and 3 (JANTXV).
- Group C, subgroup 2 and 6.
- Group E, subgroup 1.

* TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-Irradiation Limits		Post-Irradiation Limits		Post- Irradiation Limits		Unit
	Method	Conditions		R, F		R		F		
				Min	Max	Min	Max	Min	Max	
<u>Subgroup 1</u>										
Not applicable										
<u>Subgroup 2</u>		$T_C = +25^\circ\text{C}$								
Steady-state total dose irradiation (V_{GS} bias) 4/	1019	$V_{GS} = -12\text{V}$ $V_{DS} = 0$								
Steady-state total dose irradiation (V_{DS} bias) 4/	1019	$V_{GS} = 0$ $V_{DS} = 80$ percent of rated V_{DS} (pre- irradiation)								
End-point electricals:										
Breakdown voltage, drain to source	3407	$V_{GS} = 0$ $I_D = -1$ mA bias condition C	$V_{(BR)DSS}$							
2N7519U3, 2N7519U3C, 2N7519T3				-30		-30		-30		V dc
2N7520U3, 2N7520U3C, 2N7520T3				-60		-60		-60		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	$V_{GS(th)1}$	-2.0	-4.0	-2.0	-4.0	-2.0	-5.0	V dc
Gate reverse current	3411	$V_{GS} = -20$ V $V_{DS} = 0$ bias condition C	I_{GSSR1}		-100		-100		-100	nA dc
Gate forward current	3411	$V_{GS} = 20$ V $V_{DS} = 0$ bias condition C	I_{GSSF1}		100		100		100	nA dc
Drain current	3413	$V_{GS} = 0$ bias condition C $V_{DS} = 80$ percent of rated V_{DS} (pre- irradiation)	I_{DSS1}		-10		-10		-10	μA dc

See footnotes at end of table.

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* TABLE II. Group D inspection - Continued.

Inspection <u>1/</u> <u>2/</u> <u>3/</u>	MIL-STD-750		Symbol	Pre-Irradiation Limits		Post-Irradiation Limits		Post-Irradiation Limits		Unit
	Method	Conditions		R, F		R		F		
				Min	Max	Min	Max	Min	Max	
Static drain to source on-state voltage 2N7519U3 2N7519U3C 2N7520U3 2N7520U3C 2N7519T3 2N7520T3	3405	$V_{GS} = -12$ V condition A pulsed (see 4.5.1) $I_D = I_{D2}$	$V_{DS(on)1}$		1.296		1.296		1.296	V dc
					1.157		1.157		1.157	V dc
					1.296		1.296		1.296	V dc
					1.131		1.131		1.131	V dc
Forward voltage source to drain diode	4011	$V_{GS} = 0$ $I_D = I_{D1}$	V_{SD}		-5.0		-5.0		-5.0	V dc

- 1/ For sampling plan, see MIL-PRF-19500.
- 2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.
- 3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package, or in any qualified package, that the manufacturer has data to correlate the performance to the designated package.
- 4/ Separate samples shall be pulled for each bias.

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* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles	
Hermetic seal	1071	Test conditions G or H	
Fine leak		Test conditions C or D	
Gross leak			
Electrical measurements		See table I, subgroup 2	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	

See footnotes at end of table.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only - Continued.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
<u>Subgroup 11</u>			3 devices c = 0
SEE <u>2/ 3/ 4/</u>	1080	See figure 6	
Electrical measurements <u>5/</u>		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I, subgroup 2	
SEE irradiation		Fluence = $3E5 \pm 20$ percent ions/cm ² Flux = $2E3$ to $2E4$ ions/cm ² /sec Temperature = 25 ± 5 °C	
2N7519U3, 2N7519U3C and 2N7519T3		LET = 37.5 - 37.9 MeV-cm ² /mg; range = 33.1 - 36.0 microns; energy = 252.6 - 278.5 MeV In situ bias conditions: $V_{DS} = -30$ V and $V_{GS} = 20$ V	
2N7520U3, 2N7520U3C and 2N7520T3		In situ bias conditions: $V_{DS} = -60$ V and $V_{GS} = 20$ V	
2N7519U3, 2N7519U3C and 2N7519T3		LET = 59.7 MeV-cm ² /mg; range = 30.5 - 31.0 microns; energy = 314 - 320 MeV Insitu bias conditions: $V_{DS} = -30$ V and $V_{GS} = 15$ V $V_{DS} = -25$ V and $V_{GS} = 20$ V	
2N7520U3, 2N7520U3C and 2N7520T3		In situ bias conditions: $V_{DS} = -60$ V and $V_{GS} = 10$ V $V_{DS} = -45$ V and $V_{GS} = 15$ V $V_{DS} = -25$ V and $V_{GS} = 20$ V	
2N7519U3, 2N7519U3C and 2N7519T3		LET = 81.4 - 82.3 MeV-cm ² /mg; range = 27.0 - 28.4 microns; energy = 332 - 350 MeV In situ bias conditions: $V_{DS} = -30$ V and $V_{GS} = 10$ V $V_{DS} = -25$ V and $V_{GS} = 15$ V	
2N7520U3, 2N7520U3C and 2N7520T3		In situ bias conditions: $V_{DS} = -60$ V and $V_{GS} = 10$ V	
Electrical measurements <u>5/</u>		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I, subgroup 2	

1/ A separate sample for each test shall be pulled.

2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

4/ The sampling plan applies to each bias condition.

5/ Examine I_{GSSF1} , I_{GSSR1} , and I_{DSS1} before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

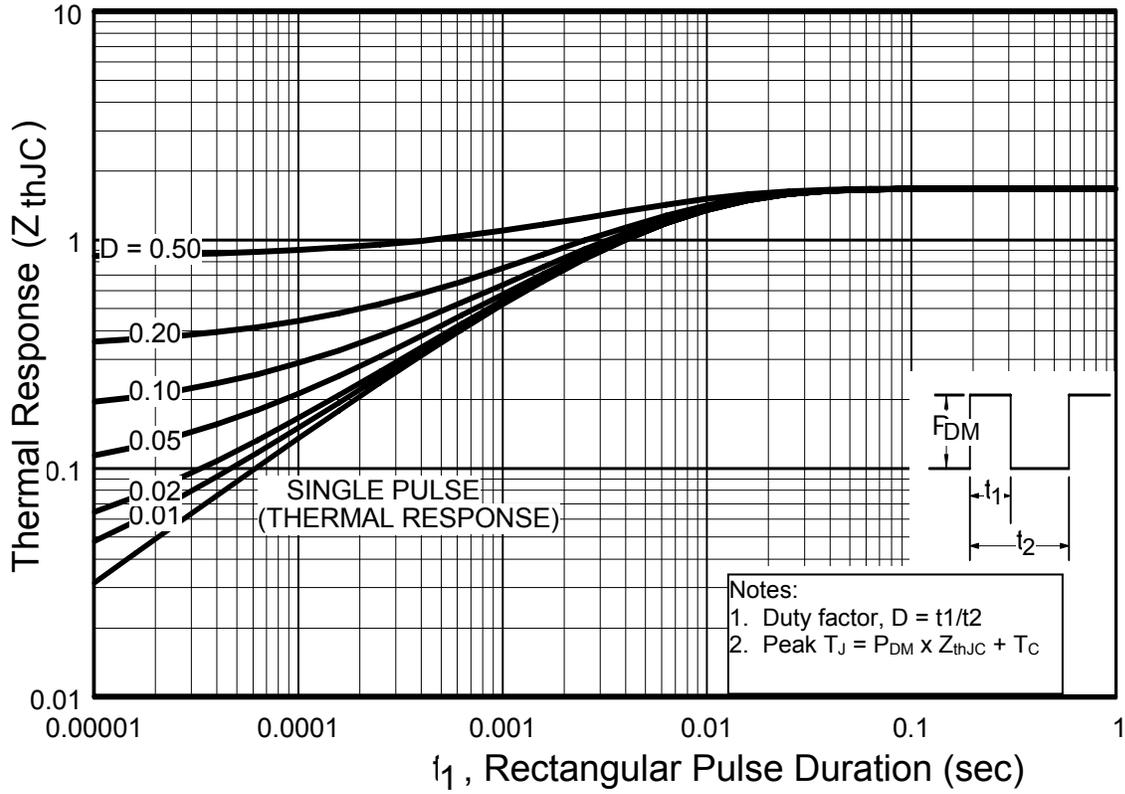
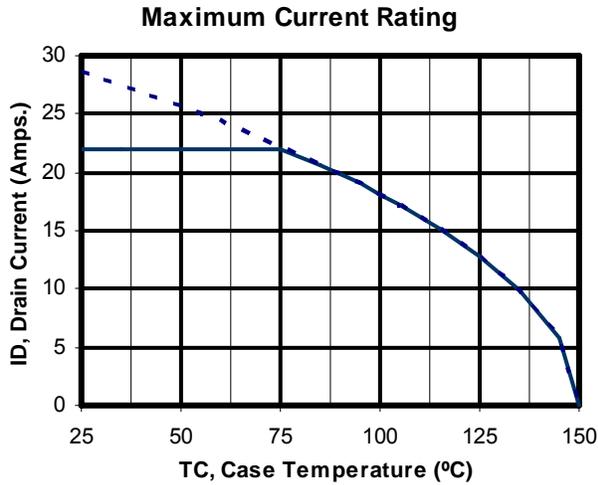


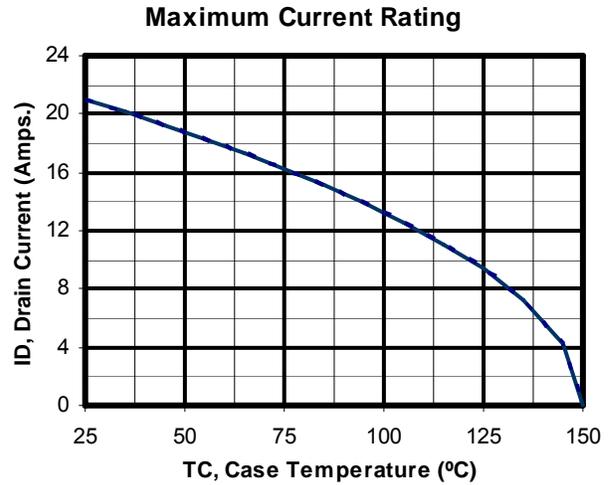
FIGURE 3. Thermal impedance curves.

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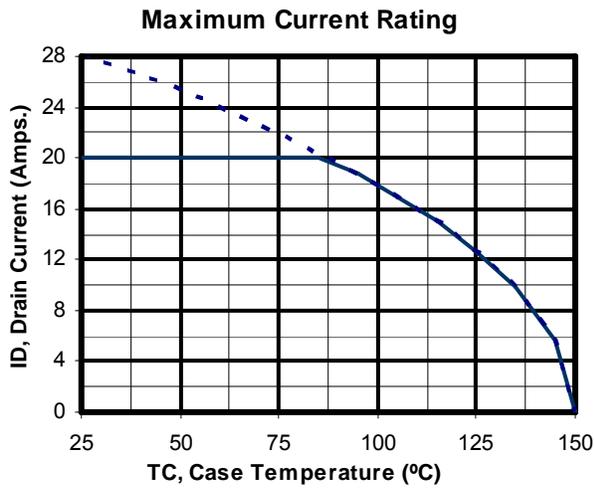
2N7519U3, 2N7519U3C



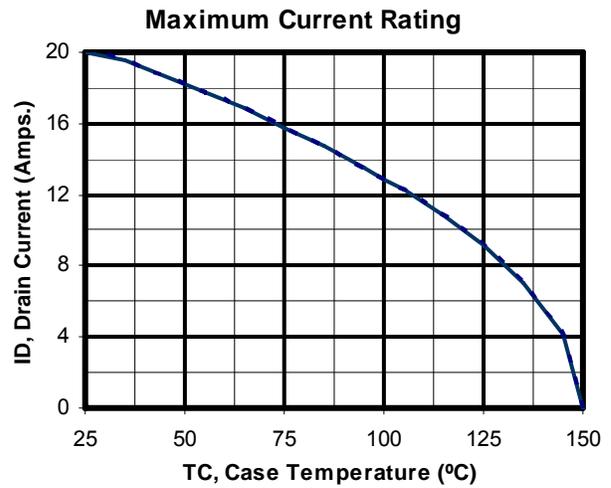
2N7520U3, 2N7520U3C



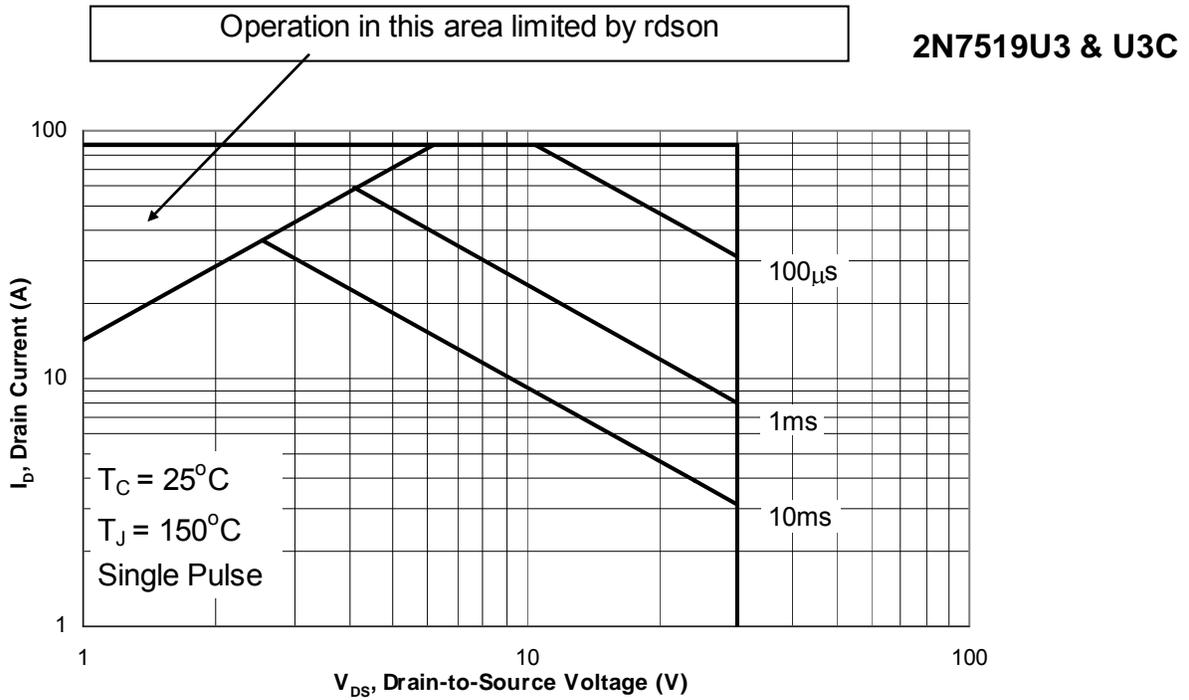
2N7519T3



2N7520T3

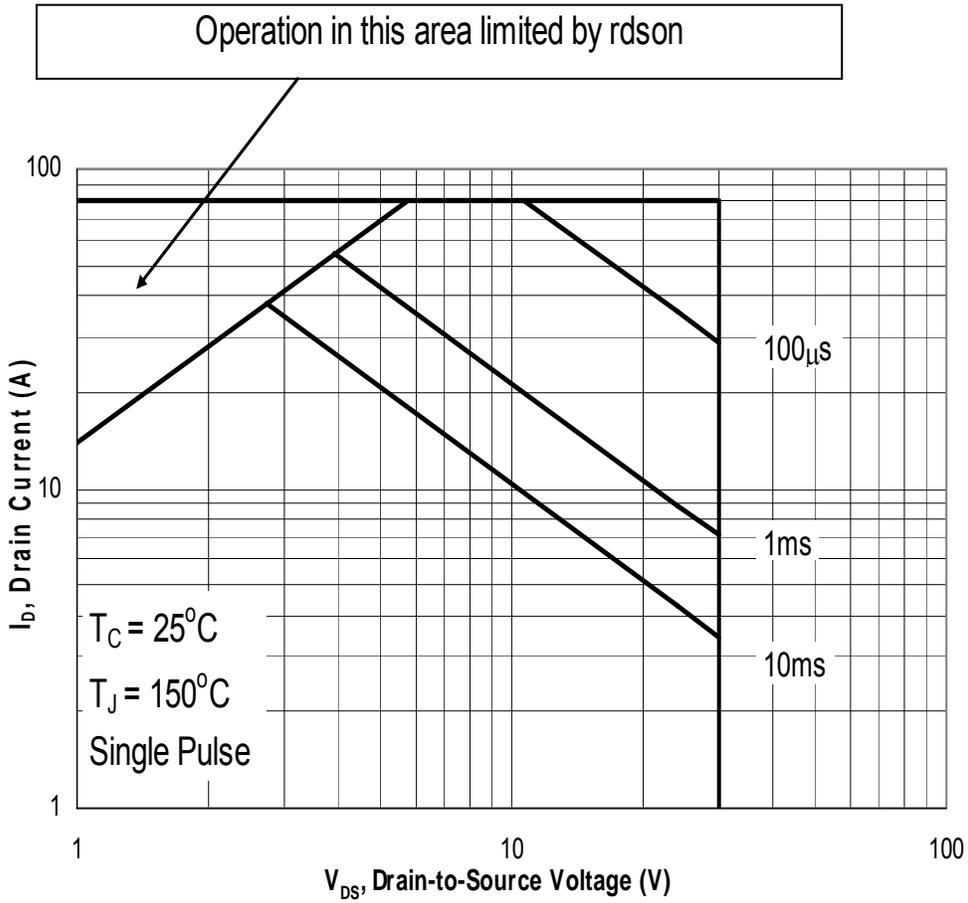


* FIGURE 4. Maximum drain current versus case temperature graphs.

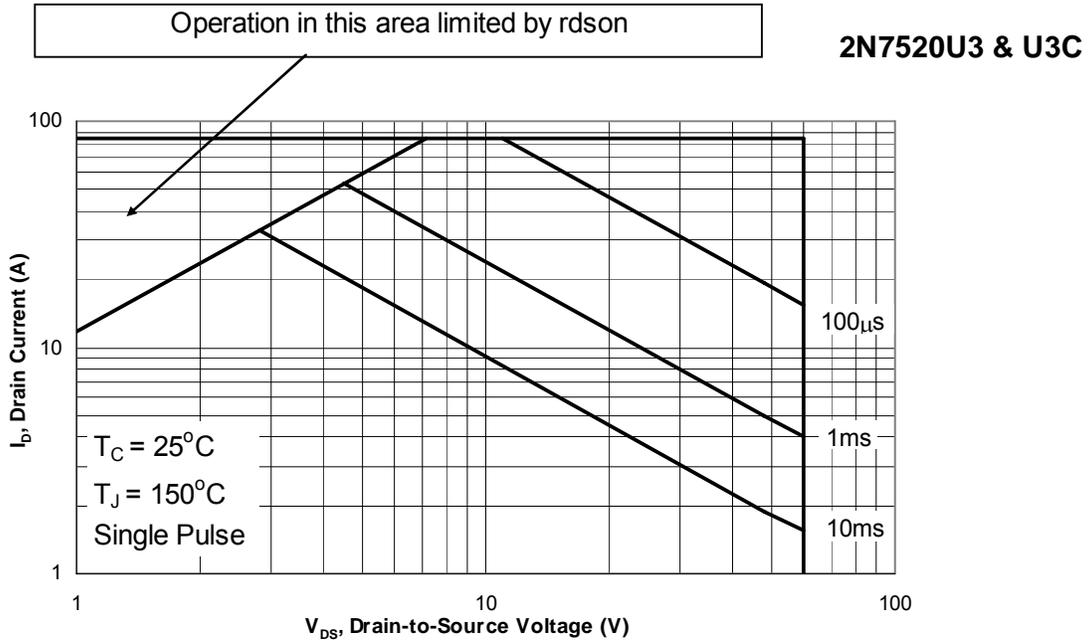


* FIGURE 5. Safe operating area graph.

2N7519T3

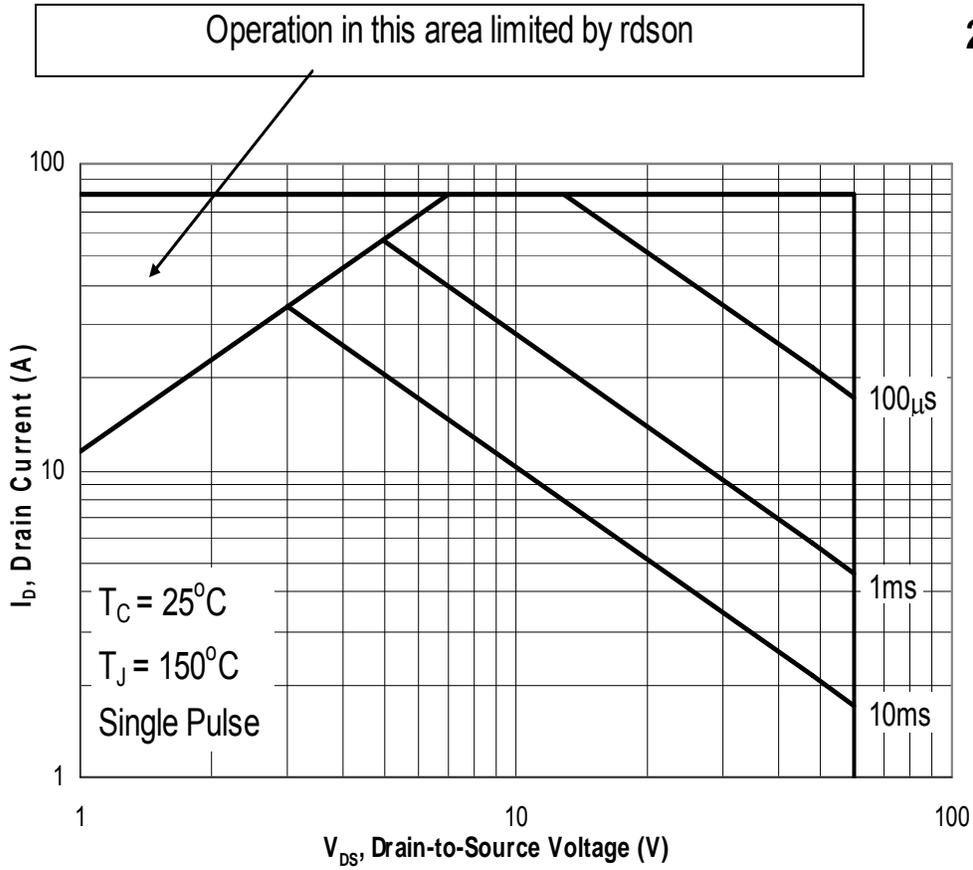


* FIGURE 5. Safe operating area graph. - Continued.

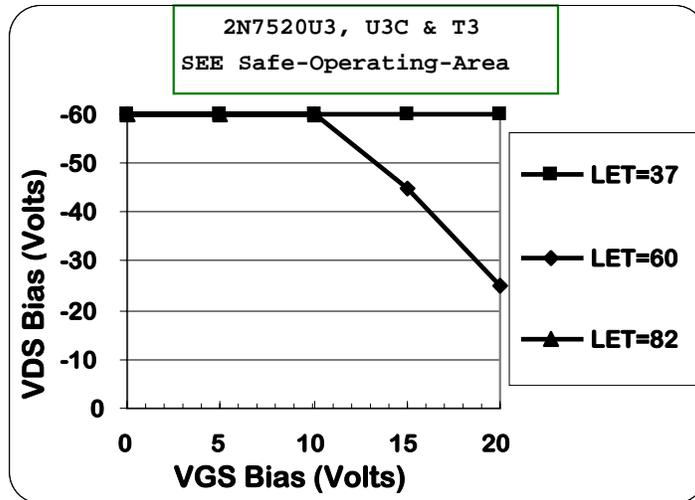
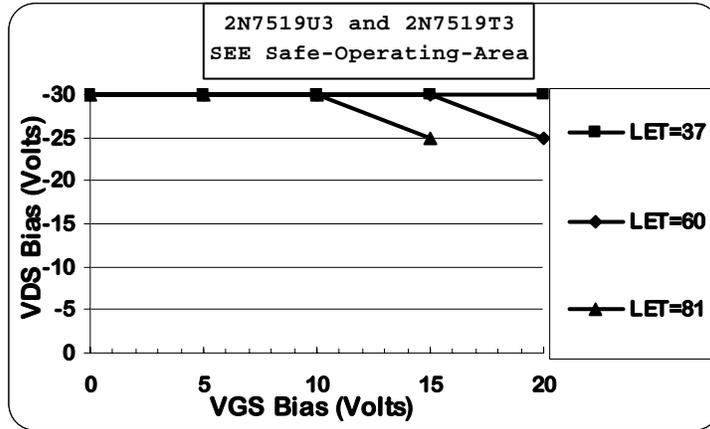


* FIGURE 5. Safe operating area graph. - Continued.

2N7520T3



* FIGURE 5. Safe operating area graph. - Continued.



* FIGURE 6. SEE safe operation area graphs.

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

* (This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

* 6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <http://assist.daps.dla.mil>.

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* 6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types (military PIN)	Commercial PIN		
	TO-257AA	TO-276AA (SMD-0.5)	TO-276AA (SMD-0.5) with Ceramic Lid
2N7519U3		IRHNJ597Z30	
2N7520U3		IRHNJ597034	
2N7519T3	IRHYS597Z30CM		
2N7520T3	IRHYS597034CM		
2N7519U3C			IRHNJC597Z30
2N7520U3C			IRHNJC597034

6.5 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/741.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 11
 NASA - NA
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5961-2008-050)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://assist.daps.dla.mil/>.