

The documentation and process conversion measures necessary to comply with this revision shall be completed by 6 December 2007.

INCH-POUND

MIL-PRF-19500/707A  
 6 September 2007  
 SUPERSEDING  
 MIL-PRF-19500/707  
 6 February 2002

\* PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED  
 (TOTAL DOSE AND SINGLE EVENT EFFECTS)  
 TRANSISTOR, N-CHANNEL, SILICON, TYPES 2N7500U5, 2N7501U5, AND 2N7502U5,  
 JANTXVR AND JANSR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

\* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

\* 1.1 Scope. This specification covers the performance requirements for a N-Channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum rating ( $E_{AS}$ ) and maximum avalanche current ( $I_{AS}$ ). See 6.5 for JANHC and JANKC die versions.

1.2 Physical dimensions. See figure 1, (surface mount, LCC-18).

\* 1.3 Maximum ratings.  $T_A = +25^\circ\text{C}$ , unless otherwise specified.

Type	$P_T$ (1) $T_C = +25^\circ\text{C}$	$P_T$ $T_A = +25^\circ\text{C}$	$R_{\theta JC}$ (2)	$V_{DS}$	$V_{DG}$	$V_{GS}$	$I_{D1}$ (3) (4) $T_C = +25^\circ\text{C}$	$I_{D2}$ (3) (4) $T_C = +100^\circ\text{C}$	$I_{DM}$ (5)	$I_S$	$T_J$ and $T_{STG}$
	<u>W</u>	<u>W</u>	<u>°C/W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>A dc</u>	<u>°C</u>
2N7500U5	25	1.25	5.0	130	130	$\pm 20$	9.0	6.0	36.0	9.0	-55
2N7501U5	25	1.25	5.0	200	200	$\pm 20$	6.3	4.0	25.2	6.3	to
2N7502U5	25	1.25	5.0	250	250	$\pm 20$	5.0	3.2	20.0	5.0	+150

(1) Derate linearly 0.2 W/°C for  $T_C > +25^\circ\text{C}$ ;

(2) See figure 2, thermal impedance curves.

(3) The following formula derives the maximum theoretical  $I_D$  limit.  $I_D$  is limited by package design.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

(4) See figure 3, maximum drain current graph.

(5)  $I_{DM} = 4 \times I_{D1}$ , as defined in note (3).

\* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dsc.dla.mil](mailto:Semiconductor@dsc.dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil/>.

\* 1.4 Primary electrical characteristics at  $T_C = +25^\circ\text{C}$ .

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 1.0\text{mA}$ dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ $I_D = 1.0\text{ mA}$ dc	Max $I_{DSS1}$ $V_{GS} = 0$ $V_{DS} = 80$ percent of rated $V_{DS}$	Max $r_{DS(on)}$ (1) $V_{GS} = 12\text{V}$ , $I_D = I_{D2}$		$E_{AS}$
				$T_J = +25^\circ\text{C}$	$T_J = +150^\circ\text{C}$	
	<u>V dc</u>	<u>V dc</u> Min    Max	<u><math>\mu\text{A}</math> dc</u>	<u><math>\Omega</math></u>	<u><math>\Omega</math></u>	<u>mJ</u>
2N7500U5	130	2.5    4.5	10	0.130	0.300	87
2N7501U5	200	2.5    4.5	10	0.270	0.621	94
2N7502U5	250	2.5    4.5	10	0.450	0.990	93

(1) Pulsed (see 4.5.1).

## 2. APPLICABLE DOCUMENTS

\* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

\* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

## \* DEPARTMENT OF DEFENSE SPECIFICATIONS

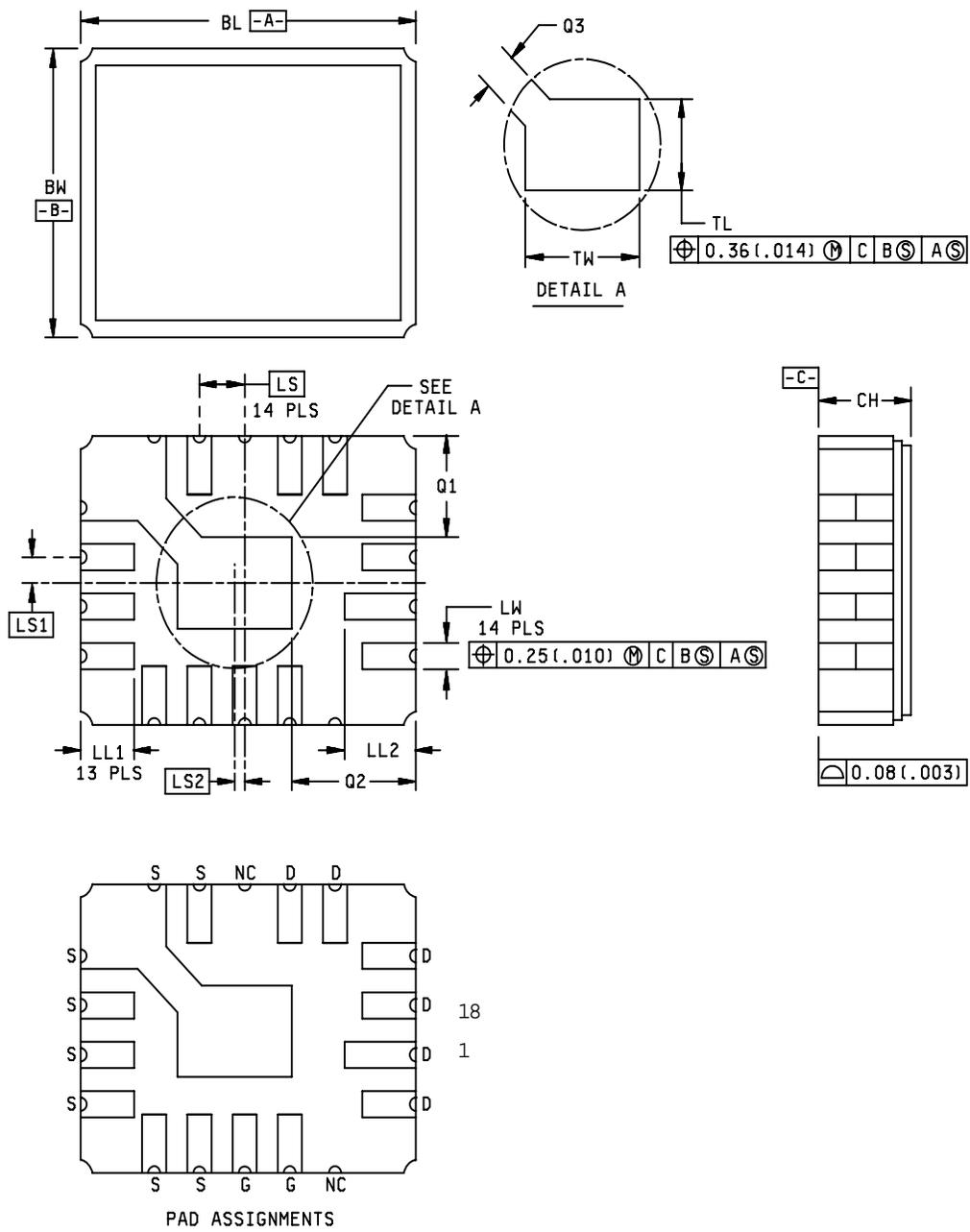
MIL-PRF-19500 - Semiconductor Devices, General Specification for.

## \* DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

\* (Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



\* FIGURE 1. Physical dimensions for LCC-18.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.345	.360	8.77	9.14
BW	.280	.295	7.12	7.49
CH	.095	.115	2.42	2.92
LL <sub>1</sub>	.040	.055	1.02	1.39
LL <sub>2</sub>	.055	.065	1.39	1.65
LS	.050 BSC		1.27 BSC	
LS <sub>1</sub>	.025 BSC		.635 BSC	
LS <sub>2</sub>	.008 BSC		.203 BSC	
LW	.020	.030	0.51	0.76
Q <sub>1</sub>	.105 REF		2.67 REF	
Q <sub>2</sub>	.120 REF		3.05 REF	
Q <sub>3</sub>	.045	.055	1.15	1.39
TL	.070	.080	1.78	2.03
TW	.120	.130	3.05	3.30

\*

## NOTES:

1. Dimensions are in inches.
- \* 2. Millimeters are given for general information only.
- \* 3. Dimensions and tolerancing shall be in accordance with ASME Y14.5M.

\* FIGURE 1. Physical dimensions for LCC-18 - Continued.

### 3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (LCC-18) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.5.1 Handling. Metal oxide semiconductor (MOS) devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source,  $R \leq$  or 100 k $\Omega$ , whenever bias voltage is applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3 and 1.4 herein.

3.7 Electrical test requirements. The electrical test requirements shall be the subgroups as specified in group A, table I herein.

\* 3.8 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

#### 4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

\* 4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

\* 4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. See the design safe operation area figures herein.

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\* 4.3 Screening (JANS, JANTX, and JANTXV). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS	JANTX and JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E <sub>AS</sub> test (see 4.3.2)	Method 3470 of MIL-STD-750, E <sub>AS</sub> test (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)
9	Subgroup 2 of table I herein I <sub>GSSF1</sub> , I <sub>GSSR1</sub> , and I <sub>DSS1</sub> as a minimum	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I <sub>GSSF1</sub> , I <sub>GSSR1</sub> , I <sub>DSS1</sub> , r <sub>DS(ON)1</sub> , V <sub>GS(TH)1</sub> , subgroup 2 of table I herein. ΔI <sub>GSSF1</sub> = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI <sub>GSSR1</sub> = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI <sub>DSS1</sub> = ±10 μA dc or ±100 percent of initial value, whichever is greater.	I <sub>GSSF1</sub> , I <sub>GSSR1</sub> , I <sub>DSS1</sub> , r <sub>DS(ON)1</sub> , V <sub>GS(TH)1</sub> , subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein ΔI <sub>GSSF1</sub> = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI <sub>GSSR1</sub> = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI <sub>DSS1</sub> = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr <sub>DS(ON)1</sub> = ±20 percent of initial value. ΔV <sub>GS(TH)1</sub> = ±20 percent of initial value.	Subgroups 2 of table I herein ΔI <sub>GSSF1</sub> = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI <sub>GSSR1</sub> = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI <sub>DSS1</sub> = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr <sub>DS(ON)1</sub> = ±20 percent of initial value. ΔV <sub>GS(TH)1</sub> = ±20 percent of initial value.

- (1) At the end of the test program, I<sub>GSSF1</sub>, I<sub>GSSR1</sub>, and I<sub>DSS1</sub> are measured.
- (2) An out-of-family program to characterize I<sub>GSSF1</sub>, I<sub>GSSR1</sub>, I<sub>DSS1</sub>, and V<sub>GS(TH)1</sub> shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

\* 4.3.1 Gate stress test. Apply  $V_{GS} = 24$  V minimum for  $t = 250$   $\mu$ s minimum.

\* 4.3.2 Single pulse avalanche energy ( $E_{AS}$ ).

- a. Peak current,  $I_{AS} = I_{D1}$ .
- b. Inductance,  $L = (2 * E_{AS} / (I_{D1})^2) * ((V_{BR} - V_{DD}) / V_{BR})$  mH minimum.
- c. Gate to source resistor,  $R_{GS}: 25 \Omega \leq R_{GS} \leq 200 \Omega$ .
- d. Supply voltage,  $V_{DD} = 25$  V dc, except  $V_{DD} = 50$  V dc for 2N7502U5.
- e. Initial case temperature,  $T_C = +25^\circ$  C,  $-5^\circ$  C,  $+10^\circ$  C.
- f. Gate voltage,  $V_{GS} = 12$  V dc.
- g. Number of pulses to be applied: 1 pulse minimum.

\* 4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining  $I_M$ ,  $I_H$ ,  $t_H$ ,  $t_{SW}$ , (and  $V_H$  where appropriate). Measurement delay time ( $t_{MD}$ ) = 70  $\mu$ s max. See table III, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTX and JANTXV) of MIL-PRF-19500, and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

\* 4.4.2.1 Group B inspection, table E-VIA (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B3	2077	Scanning electron microscope (SEM).
B4	1042	Intermittent operation life, condition D, 2,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} =$ rated; $T_A = +175^\circ$ C, $t = 24$ hours minimum; or $T_A = +150^\circ$ C, $t = 48$ hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} =$ rated; $T_A = +175^\circ$ C, $t = 120$ hours minimum; or $T_A = +150^\circ$ C, $t = 240$ hours minimum.

4.4.2.2 Group B inspection, table E-VIB (JANTX and JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D, 2,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Terminal strength is not applicable.
* C5	3161	See 4.3.3, $R_{\theta JC} = 5.0$ °C/W.
* C6	1042	Intermittent operation life, condition D, 6,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

\* 4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.5.1 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. See the design safe operating area figures herein. End-point measurements shall be in accordance with table III.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

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\* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
* Thermal impedance <u>2/</u>	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage drain to source	3407	$V_{GS} = 0V$ , $I_D = 1 \text{ mA dc}$ , bias condition C	$V_{(BR)DSS}$			
2N7500U5				130		V dc
2N7501U5				200		V dc
2N7502U5				250		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ , $I_D = 1 \text{ mA dc}$	$V_{GS(TH)1}$	2.5	4.5	V dc
* Gate current	3411	$V_{GS} = +20V \text{ dc}$ , bias condition C, $V_{DS} = 0V$	$I_{GSSF1}$		+100	nA dc
* Gate current	3411	$V_{GS} = -20V \text{ dc}$ , bias condition C, $V_{DS} = 0V$	$I_{GSSR1}$		-100	nA dc
Drain current	3413	$V_{GS} = 0V \text{ dc}$ , bias condition C, $V_{DS} = 80 \text{ percent of rated } V_{DS}$ ,	$I_{DSS1}$		10	μA dc
Static drain to source on-state resistance	3421	$V_{GS} = 12V \text{ dc}$ , condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$			
2N7500U5					0.130	Ω
2N7501U5					0.270	Ω
2N7502U5					0.450	Ω
Forward voltage	4011	$V_{GS} = 0V \text{ dc}$ , condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	$V_{SD}$		1.5	V dc

See footnotes at end of table.

\* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 3</u>						
High temperature operation		$T_C = T_J = +125^\circ\text{C}$				
Gate current	3411	$V_{GS} = \pm 20\text{V dc}$ , bias condition C, $V_{DS} = 0\text{V}$	$I_{GSS2}$		$\pm 200$	nA dc
Drain current	3413	$V_{GS} = 0\text{V dc}$ , bias condition C, $V_{DS} = 80$ percent of rated $V_{DS}$	$I_{DSS2}$		25	$\mu\text{A dc}$
Static drain to source on-state resistance	3421	$V_{GS} = 12\text{V dc}$ , condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)3}$			
2N7500U5					0.247	$\Omega$
2N7501U5					0.540	$\Omega$
2N7502U5					0.945	$\Omega$
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ , $I_D = 1\text{ mA dc}$	$V_{GS(TH)2}$	1.5		V dc
Low temperature operation		$T_C = T_J = -55^\circ\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$ , $I_D = 1\text{ mA dc}$	$V_{GS(TH)3}$		5.5	V dc
<u>Subgroup 4</u>						
Forward transconductance	3475	$I_D = I_{D2}$ , $V_{DD} = 15\text{ V dc}$ (see 4.5.1)	$g_{FS}$			
2N7500U5				5.0		S
2N7501U5				4.2		S
2N7502U5				4.0		S
Switching time test	3472	$I_D = I_{D2}$ , $V_{GS} = 12\text{ V dc}$ , $R_G = 7.5\ \Omega$ , $V_{DD} = 50$ percent of rated $V_{DS}$				
Turn-on delay time			$t_{D(on)}$		25	ns
Rise time			$t_r$		100	ns
Turn-off delay time			$t_{D(off)}$		35	ns
Fall time			$t_f$		40	ns

See footnotes at end of table.

\* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 4, $t_p = 10$ ms min. $V_{DS} = 80$ percent of max. rated $V_{DS}$				
Electrical measurements		See table I, subgroup 2				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B, $I_D = I_{D1}$ , $V_{GS} = 12$ V dc $V_{DD} = 50$ percent of rated $V_{DS}$				
On-state gate charge 2N7500U5			$Q_{G(ON)}$	48	nC	
2N7501U5				47	nC	
2N7502U5				28	nC	
Gate to source charge 2N7500U5			$Q_{GS}$	16	nC	
2N7501U5				12	nC	
2N7502U5				7.4	nC	
Gate to drain charge 2N7500U5			$Q_{GD}$	18	nC	
2N7501U5				16	nC	
2N7502U5				12	nC	
Reverse recovery time	3473	$di/dt = -100$ A/ $\mu$ s, $V_{DD} \leq 50$ V $I_D = I_{D1}$	$t_{rr}$			
2N7500U5				250	ns	
2N7501U5				274	ns	
2N7502U5				287	ns	

1/ For sampling plan, see MIL-PRF-19500.

2/ This test required for the following end-point measurements only:

Group B, subgroups 2 and 3 (JANTX/JANTXV).

Group B, subgroups 3 and 4 (JANS).

Group C, subgroup 6.

Group E, subgroup 1.

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\* TABLE II. Group D inspection.

Inspection <u>1/ 2/ 3/</u>	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Unit
	Method	Conditions		R		R		
				Min	Max	Min	Max	
<u>Subgroup 1</u>								
Not applicable								
<u>Subgroup 2</u>		$T_C = + 25^\circ\text{C}$						
Steady-state total dose irradiation ( $V_{GS}$ bias) <u>4/</u>	1019	$V_{GS} = 12 \text{ V}; V_{DS} = 0 \text{ V}$						
Steady-state total dose irradiation ( $V_{DS}$ bias) <u>4/</u>	1019	$V_{GS} = 0 \text{ V}; V_{DS} = 80 \text{ percent of rated } V_{DS} \text{ (preirradiation)}$						
End-point electricals								
Breakdown voltage, drain to source 2N7500U5 2N7501U5 2N7502U5	3407	$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}; \text{ bias condition C}$	$V_{(BR)DSS}$	130 200 250		130 200 250		V dc V dc V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}; I_D = 1 \text{ mA}$	$V_{GS(th)1}$	2.5	4.5	2.0	4.5	V dc
Gate current	3411	$V_{GS} = +20 \text{ V}; V_{DS} = 0 \text{ V}; \text{ bias condition C}$	$I_{GSSF1}$		100		100	nA dc
Gate current	3411	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; \text{ bias condition C}$	$I_{GSSR1}$		-100		-100	nA dc
Drain current	3413	$V_{GS} = 0 \text{ V}; V_{DS} = 80 \text{ percent of rated } V_{DS} \text{ (preirradiation); bias condition C}$	$I_{DSS}$		10		10	$\mu\text{A dc}$
* Static drain to source on-state voltage 2N7500U5 2N7501U5 2N7502U5	3405	$V_{GS} = 12 \text{ V}; I_D = I_{D2}; \text{ condition A, pulsed (see 4.5.1)}$	$V_{DS(on)}$		0.492 0.888 1.286		0.492 0.888 1.286	V dc V dc V dc
Forward voltage source drain diode	4011	$V_{GS} = 0 \text{ V}; I_D = I_{D1}; \text{ bias condition C}$	$V_{SD}$		1.5		1.5	V dc

1/ For sampling plan see MIL-PRF-19500.

2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other performance specification utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ Separate samples shall be pulled for each bias.

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\* TABLE III. Group E inspection (all quality levels) - for qualification only.

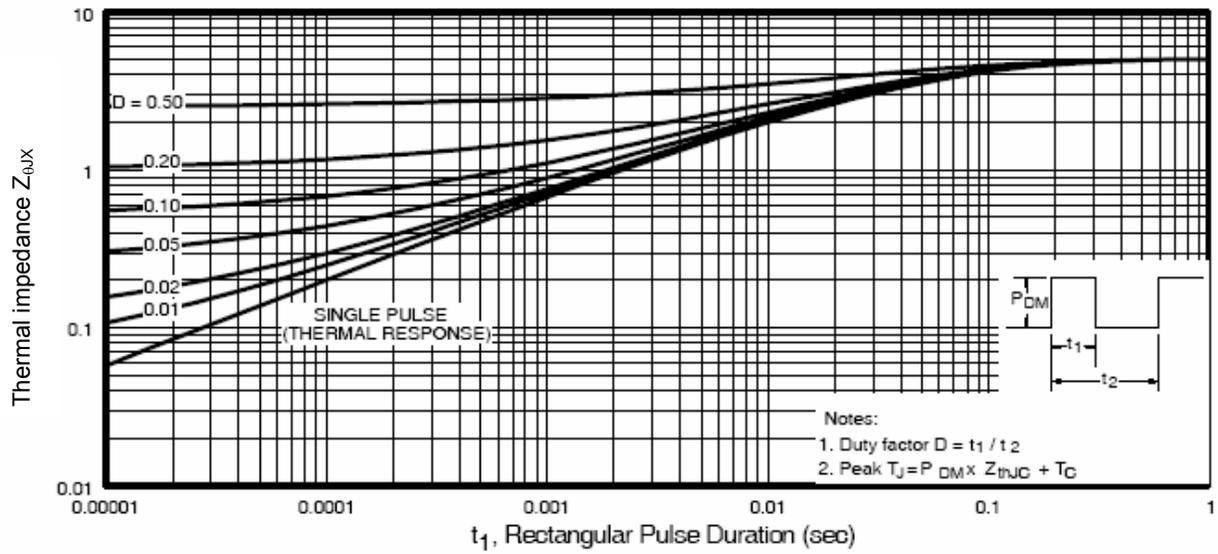
Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state gate bias	1042	Test condition B; 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state reverse bias	1042	Test condition A; 1,000 hours	
Electrical measurements		See table I, subgroup 2	
<u>Subgroup 4</u>			Sample plan N/A
Thermal resistance		See MIL-PRF-19500.	
<u>Subgroup 5</u>			3 devices, c = 0
Barometric pressure 2N7501U5, 2N7502U5 only	1001	Test condition C, see 1.3.	
<u>Subgroup 6</u>			3 devices
ESD	1020	Not required for devices classified as ESD class 1.	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	

See footnotes at end of table.

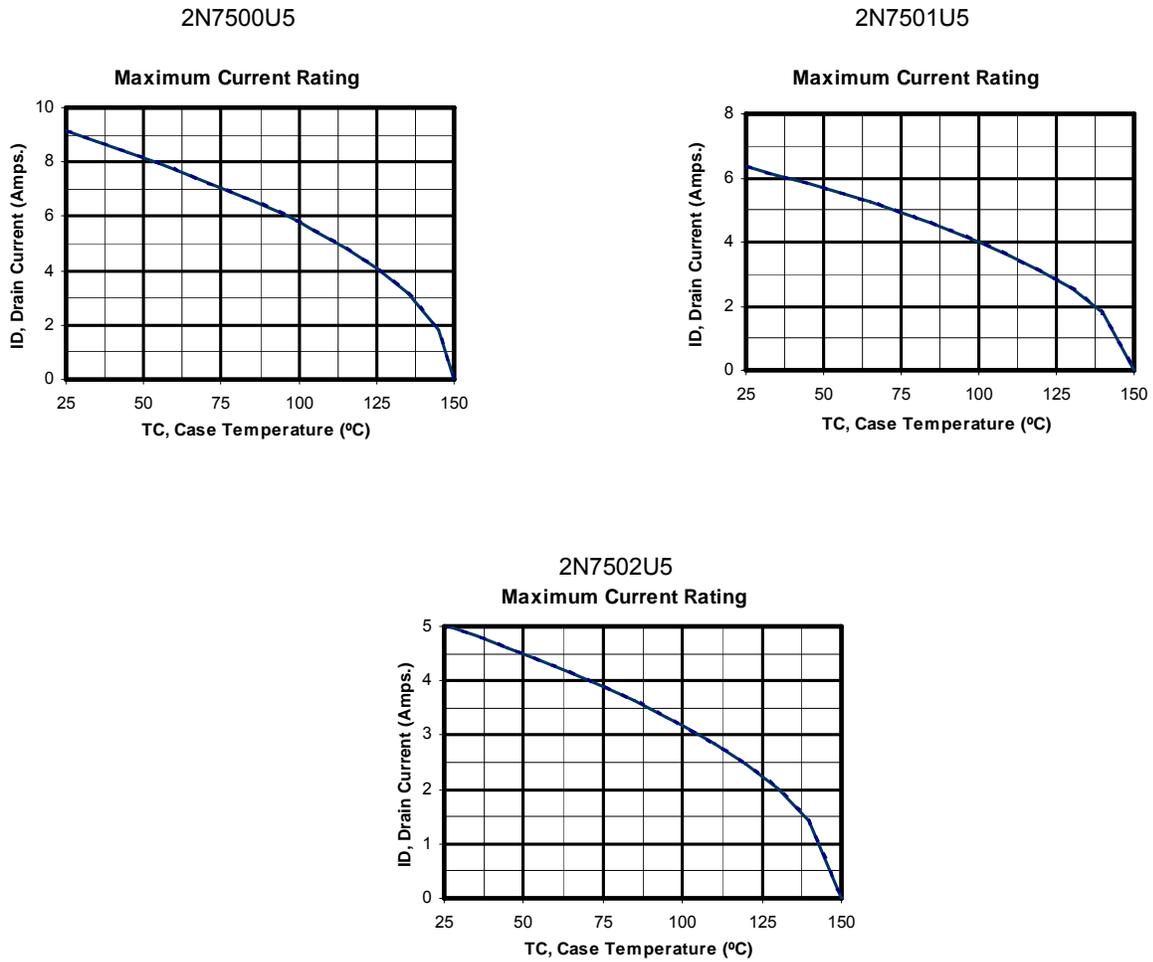
\* TABLE III. Group E inspection (all quality levels) - for qualification only - Continued.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 11</u> SEE <u>2/ 3/ 4/</u> Electrical measurements <u>5/</u> SEE Irradiation	1080	See figure 5  $I_{GSS1}$ and $I_{DSS1}$ in accordance with table I, subgroup 2  Fluence = $3E5 \pm 20$ percent ions/cm <sup>2</sup> Flux = $2E3$ to $2E4$ ions/cm <sup>2</sup> /sec, temperature = $25 \pm 5$ °C  LET = 37 MeV-cm <sup>2</sup> /mg, range = 39 microns, energy = 305 MeV In situ bias conditions: $V_{DS} = 130$ V and $V_{GS} = -20$ V In situ bias conditions: $V_{DS} = 200$ V and $V_{GS} = -20$ V In situ bias conditions: $V_{DS} = 250$ V and $V_{GS} = -20$ V  LET = 60 MeV-cm <sup>2</sup> /mg, range = 32 microns, energy = 340 MeV In situ bias conditions: $V_{DS} = 130$ V and $V_{GS} = -10$ V $V_{DS} = 100$ V and $V_{GS} = -15$ V $V_{DS} = 50$ V and $V_{GS} = -20$ V In situ bias conditions: $V_{DS} = 200$ V and $V_{GS} = -10$ V $V_{DS} = 185$ V and $V_{GS} = -15$ V $V_{DS} = 120$ V and $V_{GS} = -20$ V In situ bias conditions: $V_{DS} = 250$ V and $V_{GS} = -15$ V $V_{DS} = 240$ V and $V_{GS} = -20$ V  LET = 82 MeV-cm <sup>2</sup> /mg, range = 28 microns, energy = 350 MeV In situ bias conditions: $V_{DS} = 130$ V and $V_{GS} = 0$ V $V_{DS} = 120$ V and $V_{GS} = -5$ V $V_{DS} = 30$ V and $V_{GS} = -10$ V In situ bias conditions: $V_{DS} = 200$ V and $V_{GS} = -5$ V $V_{DS} = 150$ V and $V_{GS} = -10$ V $V_{DS} = 50$ V and $V_{GS} = -15$ V $V_{DS} = 25$ V and $V_{GS} = -20$ V In situ bias conditions: $V_{DS} = 250$ V and $V_{GS} = -5$ V $V_{DS} = 225$ V and $V_{GS} = -10$ V $V_{DS} = 175$ V and $V_{GS} = -15$ V $V_{DS} = 50$ V and $V_{GS} = -20$ V	3 devices
Electrical measurements <u>5/</u>		$I_{GSS1}$ and $I_{DSS1}$ in accordance with table I, subgroup 2	

- 1/ A separate sample for each test shall be pulled.
- 2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other performance specifications utilizing the same structurally identical die design.
- 3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.
- 4/ The sampling plan applies to each bias condition.
- 5/ Examine  $I_{GSS1}$  and  $I_{DSS1}$  before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

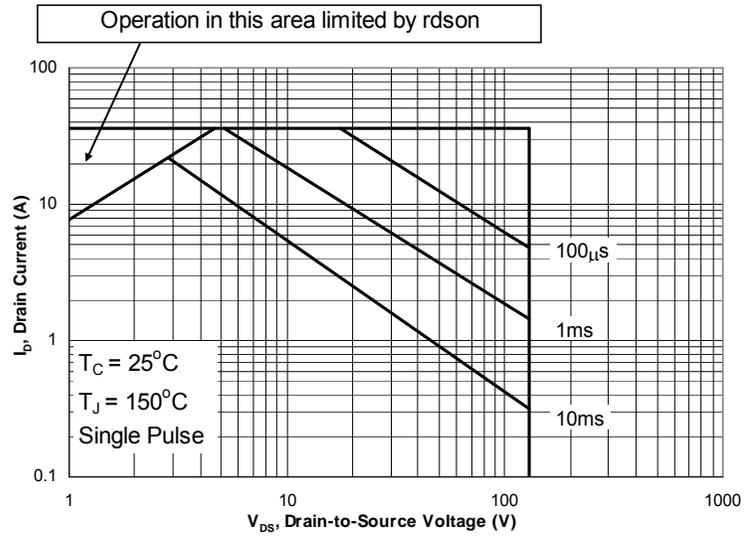


\* FIGURE 2. Thermal impedance curve.



\* FIGURE 3. Maximum drain current versus case temperature graphs.

2N7500U5



\* FIGURE 4. Safe operating area graph.

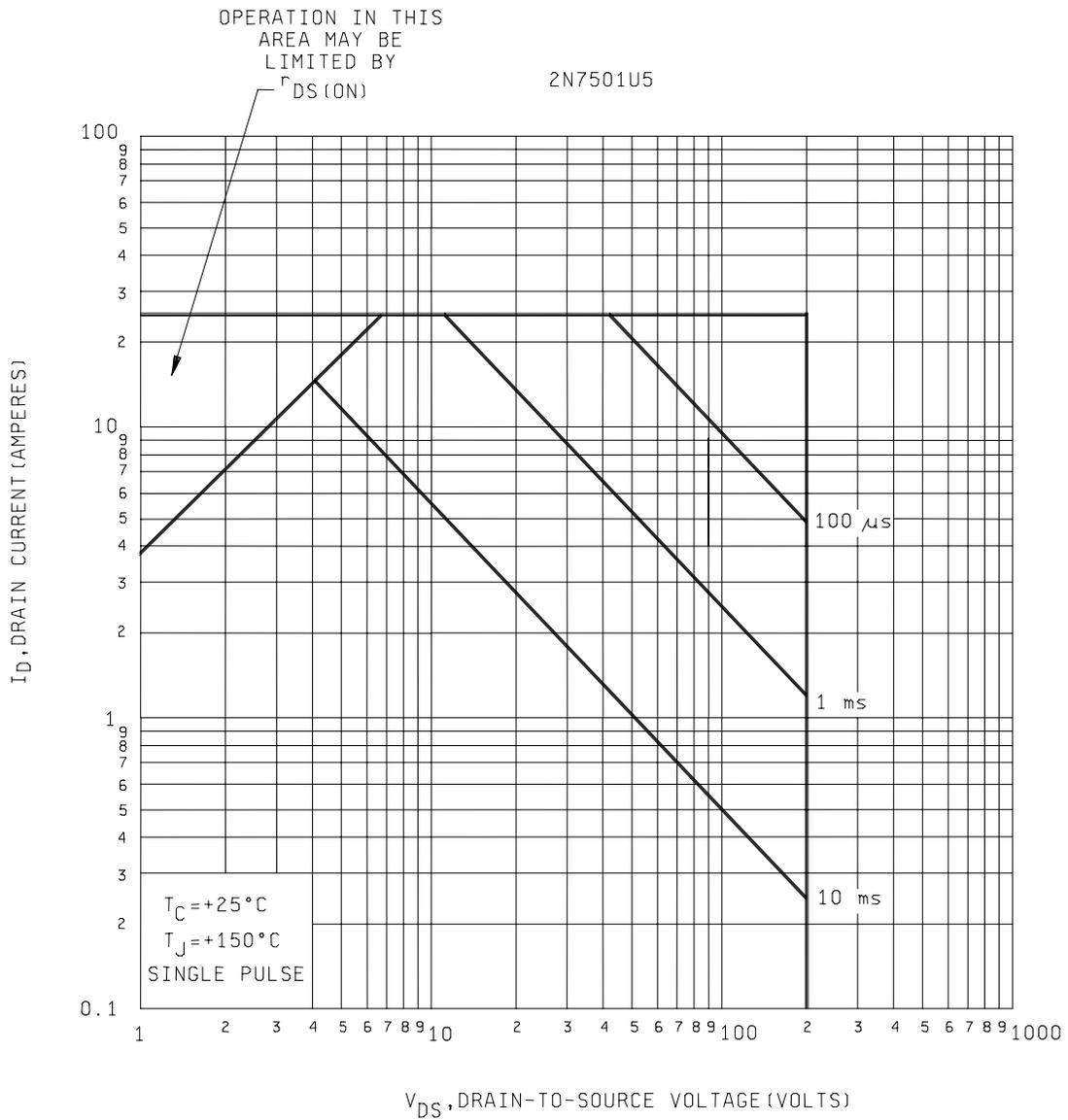
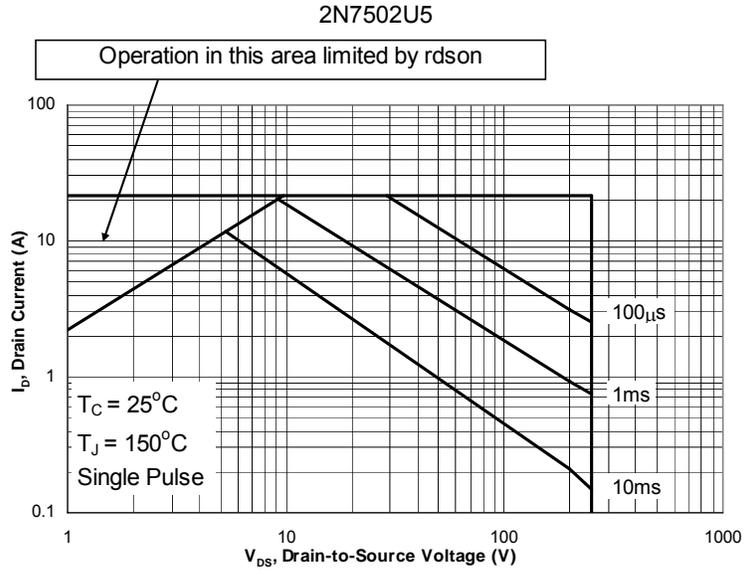


FIGURE 4. Safe operating area graph - Continued.



\* FIGURE 4. Safe operating area graph - Continued.

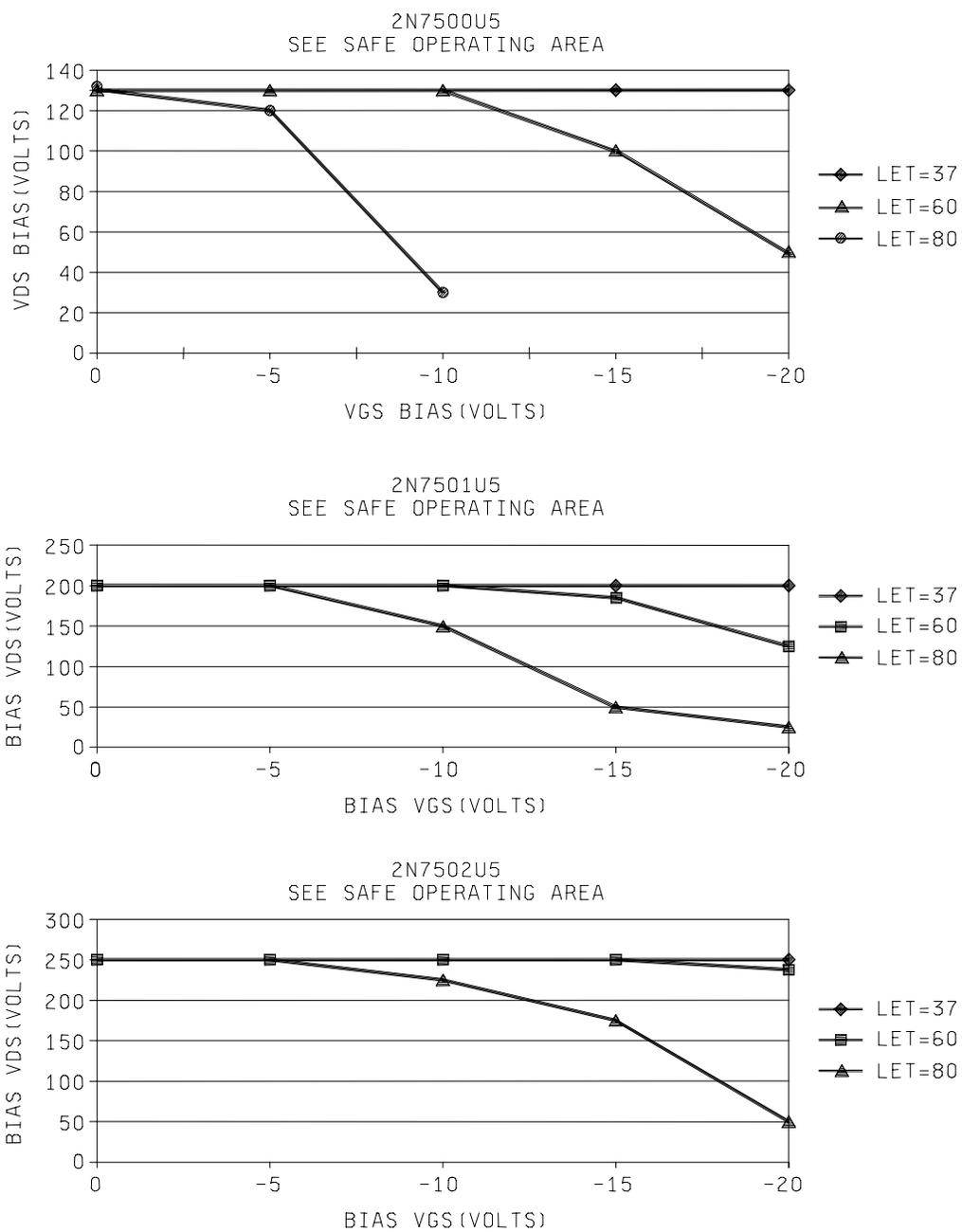


FIGURE 5. SEE safe operating area graph.

5. PACKAGING

\* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

\* (This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

\* 6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

\* 6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

\* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil).

6.4 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Generic P/N	Military P/N
IRHE57133SE	2N7500U5
IRHE57230SE	2N7501U5
IRHE57234SE	2N7502U5

\* 6.5 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/741.

\* 6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:  
Army - CR  
Navy - EC  
Air Force - 11  
NASA - NA  
DLA - CC

Preparing activity:  
DLA - CC  
  
(Project 5961-2007-048)

Review Activities:  
Army - AV, MI  
Air Force - 71, 99

\* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://assist.daps.dla.mil/> .