

MILITARY SPECIFICATION  
 CAPACITORS, FIXED, CERAMIC DIELECTRIC,  
 (TEMPERATURE STABLE AND GENERAL PURPOSE), HIGH RELIABILITY,  
 GENERAL SPECIFICATION FOR

This amendment forms a part of MIL-C-123B, dated 6 August 1990,  
 and is approved for use by all Departments and Agencies of the  
 Department of Defense.

PAGE 3

\* TABLE IV, delete in its entirety and substitute:

\*TABLE IV. Termination.

Leaded capacitors		Nonleaded capacitors	
Symbol	Termination type	Symbol	Termination type
A	Copper-iron-zinc alloy (194 alloy)	G	Silver-nickel-gold
C	Copper, solder coated, 60 microinches minimum	M	Palladium/silver alloy
W	Copper clad steel, solder coated, 60 microinches minimum	R	Palladium/silver alloy, solder coated
		S	Guarded, solder coated <sup>1/</sup> <sup>2/</sup>
		T	Guarded, solder dipped
		W	Base metallization - barrier metal - tinned (tin or tin-lead alloy) <sup>3/</sup>
		Y	Base metallization - barrier metal - tin
		Z	Base metallization - barrier - solder plated (tin/lead alloy with a minimum of 4 percent lead)

- <sup>1/</sup> A guarded termination is one in which the interelectrode metallization is separated from the final finish by a barrier or guard metal; e.g., copper or nickel, etc.  
<sup>2/</sup> Capacitors with termination types T or Z may, with procuring agency approval, be remarked with termination type S.  
<sup>3/</sup> Capacitors with termination types S, T, Y, or Z may, with procuring agency approval, be remarked with termination type W."

PAGE 5

3.4.1, first two sentences, delete in their entirety and substitute: "Capacitors supplied to this specification shall have a minimum dielectric thickness of 0.8 mil for 50 volt rated capacitors or 1 mil for capacitors with ratings above 50 volts, and a maximum dielectric constant of 2400 (see figure 1). Dielectric thickness is the actual measured thickness of the fired ceramic dielectric layer."

PAGE 6

3.8, line three: Delete "until rupture and the level recorded".

\* 3.9f, delete in its entirety and substitute:

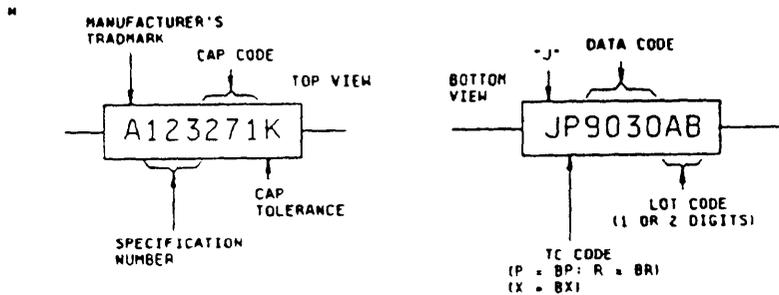
"f. Extraneous particles, such as solder spikes or solder balls, shall not exceed .015 inch (0.38 mm) in any dimension, nor shall the total encapsulation thickness be reduced to less than the thickness T or  $T_R$  as defined in 3.9c. Total encapsulation thickness is the combined measurement of the encapsulation thickness on either side of the particle."

PAGE 7

3.15, line two: Delete "of EIA standard RS-469" and substitute "specified herein".

PAGE 13

FIGURE 3, example 6, delete in its entirety and substitute:



Example 6 "

PAGE 16

4.3.1, after last sentence, add the following: "All test temperatures above 25°C shall have a tolerance of +4°C, -0°C unless otherwise specified herein."

PAGE 20

TABLE IX, under visual examination test, add the following test:

"Post termination, unencapsulated destructive physical analysis	3.15	4.6.11	Table XV-1, group 1
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PAGE 21

TABLE X, inspection column, subgroup 1, thermal shock and voltage conditioning, and voltage conditioning at 85°C tests: Add "3/" (two places).

TABLE X, sampling procedure column, subgroup 3: Delete "XIII" and substitute "XV-1".

TABLE X, bottom of table, after footnote 2/, add the following:

"3/ The DWV post test is not applicable if optional voltage conditioning was performed at 250 percent or more of the rated voltage."

PAGE 24

\* TABLE XIII, title, delete and substitute the following: "Pretermination destructive physical analysis sample size."

TABLE XV, PDA last 48 hours during voltage conditioning at +125°C heading: Add "1/".

TABLE XV, after table, add the following:

"1/ For optional voltage conditioning, the time required for meeting the PDA shall be calculated with the T(test) PDA equation in 4.6.6.2.2."

4.6.6.2.2, delete in its entirety and substitute the following:

"4.6.6.2.2 Optional voltage conditioning (see 3.10). The manufacturer, with approval from the qualifying activity, may perform an optional voltage conditioning test instead of the standard voltage conditioning test of 4.6.6.2.1. All conditions of 4.6.6.2.1 apply, with the exception of the voltage applied, the test time, and the time required for meeting the PDA. The accelerated condition selected for the optional voltage conditioning shall be used for the duration of the test. At no time shall a combination of standard and optional voltage conditioning be allowed on the same samples. The minimum time duration, T(test) minimum, and the time required for meeting the PDA, T(test) PDA, shall be calculated as follows:

$$T(\text{test}) \text{ minimum} = \frac{1344}{(E \text{ test}/E \text{ rated})^3}$$

$$T(\text{test}) \text{ PDA} = \frac{384}{(E \text{ test}/E \text{ rated})^3}$$

Where:  $2 \times E \text{ rated} \leq E \text{ test} \leq 4 \times E \text{ rated}$   
T(test) minimum = Minimum test time in hours  
T(test) PDA = Time required for meeting the PDA  
E test = Applied voltage  
E rated = Rated voltage of the capacitor"

\* 4.6.11, line two, delete in its entirety and substitute: "examined in accordance with 4.6.11.1 (group 1), 4.6.11.2 (group 2), and table XV-1."

\* Following 4.6.11, add the following new paragraphs and table:

"4.6.11.1 Group 1.

4.6.11.1.1 Leaded capacitors. After lead attachment and before encapsulation, or after removing the encapsulation. Group 1 samples shall be inspected for lead attachment, other assembly-related defects in accordance with appendix A of EIA-469, and the applicable criteria of appendix B of this specification.

4.6.11.1.2 Nonleaded capacitors. To be performed after the application of the final termination coating. The criteria of appendix C of this specification shall be used.

4.6.11.2 Group 2.

4.6.11.2.1 Leaded capacitors. Without removing the encapsulation. Group 2 samples shall be inspected in accordance with appendix B of EIA-469 and for the following encapsulation defects:

- a. Voids between the encapsulant and the capacitor body or lead wires.
- b. Cracks or voids in the encapsulation. There shall be no voids in the encapsulant greater in diameter than 50 percent of the encapsulant wall thickness.

4.6.11.2.2 Nonleaded capacitors. The group 2 samples shall be inspected in accordance with paragraphs 5.1.7 through 5.1.9 of EIA-469. Primary metallization shall only be included if it was not included in the chip lot in-process DPA.

MIL-C-123B  
AMENDMENT 3

TABLE XV-1. Destructive physical analysis sample size.

Lot size	Minimum sample size 1/	
	Group 1 2/	Group 2 3/
1 - 500	5	3
501 - 10,000	10	4
10,001 - 35,000	25	7
35,001 - 500,000	40	10

1/ No failures allowed.

2/ See 4.6.11.1.

3/ See 4.6.11.2

PAGE 31

4.6.15, delete in its entirety and substitute:

"4.6.15 Voltage-temperature limits (see 3.19). The temperature of each capacitor shall be varied as specified in table XVI. Capacitance measurements shall be made at the frequency and voltage specified in 4.6.7. The dc rated voltage need only be applied to the capacitor in each of steps E through G until voltage stability is reached and the capacitance measurement is made. Capacitance measurements shall be made at each step specified in table XVI and at a sufficient number of intermediate points between steps B and G to establish a true characteristic curve. Capacitance measurements at each temperature shall be taken at 5 minute intervals and shall be stopped and recorded when two successive readings indicate a capacitance change of less than one percent."

PAGE 32

\* 4.6.16.1c, delete in its entirety and substitute:

"c. Final measurements: On completion of the above test, remove capacitors from the chamber and allow 3 hours, 30 minutes,  $\pm 30$  minutes to dry and stabilize at  $+25^{\circ}\text{C}$  before performing the insulation resistance (IR), through a 100 kilohm resistor at  $1.3 \pm 0.25$  volts, and capacitance in accordance with 4.6.10 and 4.6.7, respectively."

PAGE 34

4.6.19d, delete in its entirety and substitute:

"d. Capacitors shall be subjected to the voltage and circuit specified in 4.6.6.2.1. In the event of a fuse failure, the procedure specified in 4.6.6.2.1 shall apply."

PAGE 50

30.2.2d, first sentence, delete and substitute:

"Edge chip-outs shall not be greater in depth than .003 inch (0.08 mm) with respect to either plane."

FIGURE C-7, delete in its entirety and substitute:

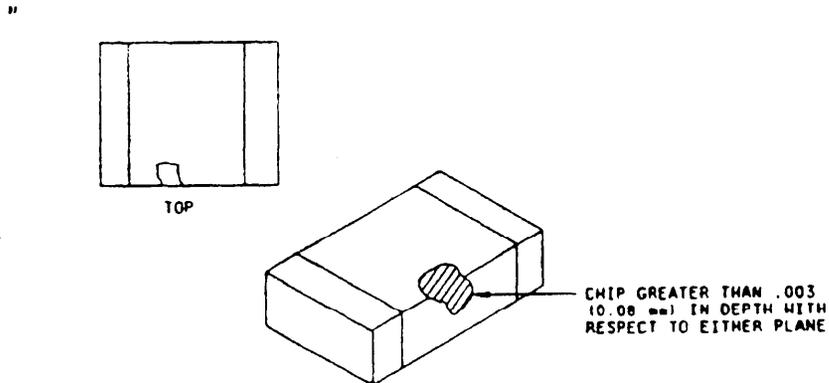


FIGURE C-7. Chip-outs. "

40.1, line three: Delete "until rupture occurs" and substitute "until the limits specified in table XIV are exceeded." Last sentence, delete in its entirety.

40.2, delete in its entirety and substitute:

"40.2 Axial devices. Firmly clamp both leads into the test fixture. Gradually apply an increasing force (see figure D-1) until the limits specified in table XIV are exceeded."

40.3b, first sentence: Delete "until a rupture occurs" and substitute "until the limits specified in table XIV are exceeded."

40.3c: Delete in its entirety.

FIGURE D-1, delete in its entirety and substitute:

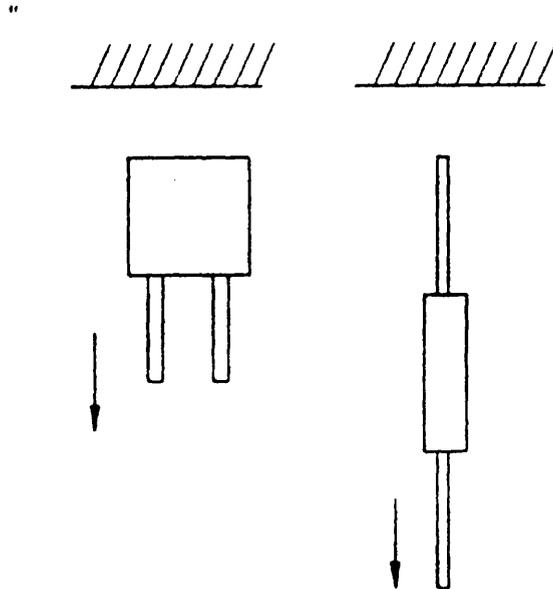


FIGURE D-1. Lead-pull direction."

The margins of this amendment are marked with an asterisk to indicate where changes (additions, modifications, corrections, deletions) from the previous amendment were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous amendment.

CONCLUDING MATERIAL

Custodians:

Air Force - 19  
NASA - NA

Review activities:

Army - ER  
Navy - EC  
Air Force - 85  
DLA - ES

Preparing activity:

NASA - NA

Agent:

DLA - ES

(Project 5910-1920)