

The document and process conversion measures necessary to comply with this revision shall be completed by 1 September 2006.

INCH-POUND

MIL-P-50884D
w/AMENDMENT 2
29 May 2006
SUPERSEDING
MIL-P-50884D
w/AMENDMENT 1
13 September 2002
(See 6.6)

MILITARY SPECIFICATION

PRINTED WIRING BOARD, FLEXIBLE OR RIGID-FLEX, GENERAL SPECIFICATION FOR

Inactive for new design after 28 February 1999.
For new design use MIL-PRF-31032.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification establishes the performance and qualification requirements for flexible and rigid-flex printed wiring boards with or without plated through holes (see 6.1). Verification is accomplished through the use of one of two methods of product assurance ([appendix A](#) or [appendix B](#)). Detail requirements, specific characteristics, and other provisions which are sensitive to the particular intended use are specified in the applicable master drawing.

1.2 Classification. Printed wiring boards are classified by 1.2.1 and 1.2.2.

1.2.1 Type. Printed wiring boards are of the types shown, as specified (see 3.1.1).

- Type 1 – Singled-sided flexible printed wiring board (see 6.4.2.1) with or without shields or stiffeners.
- Type 2 – Double-sided flexible printed wiring board (see 6.4.2.2) with or without shields or stiffeners with or without plated-through holes.
- Type 3 – Multilayer flexible printed wiring board with plated holes (see 6.4.2.3) and with or without shields or stiffeners.
- Type 4 – Multilayer rigid and flexible printed wiring board with plated-through holes (see 6.4.2.4).
- Type 5 – Bonded rigid and/or flexible printed wiring board combinations without plated-through holes (see 6.4.2.5).

1.2.2 Flexibility class. The flexibility class is identified by a single letter, A or B, designating the printed wiring board class.

- Class A – Capable of withstanding flexing during installation.
- Class B – Capable of withstanding continuous flexing for the number of cycles specified (see 3.1.1).

Comments, suggestions, or questions on this document should be addressed to: Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990 or emailed to 5998.Documents@dsc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil>.

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1.2.3 Flexible base material. The printed wiring board flexible base material type should be identified by the base material designators of the applicable flexible base material specification as required by the master drawing (see 3.1.1).

1.2.4 Rigid base material type (designs with stiffeners). The printed wiring board rigid base material type should be identified by the base material designators of the applicable base material specification as required by the master drawing (see 3.1.1).

1.3 Description of this specification. The main body contains general provisions and is supplemented by detailed appendices. Appendices A and B describe the two product assurance programs that can be implemented by the manufacturer. Appendix A contains the traditional QPL product assurance program. Appendix B is an optional quality management approach using a technical review board concept addressed in MIL-PRF-31032, to modify the generic verification criteria provided in this specification. Appendix C provides statistical sampling, and basic test and inspection procedures. Appendix D is optional and can be used when producing printed wiring boards designed to superseded design standards (see 6.4.1 and D.4.2). Appendix D may also be used as a guide in developing a test plan for legacy or existing designs based on the tests and inspections of appendix A. Appendix E is optional and describes an alternative procedure used to evaluate oxidation levels on solderable surfaces. The procedure involves using electrochemical reduction techniques to determine the type and quantity of oxide on plated-through holes.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC-T-50 – Terms and Definitions for Interconnecting and Packaging Electronic Circuits. (DoD adopted).

(Application for copies should be addressed to the IPC – Association Connecting Electronics Industry, 3000 Lakeside Drive, Suite 309 S, Bannockburn, IL 60015-1249 or <http://www.ipc.org>.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General requirements. The manufacturer of printed wiring boards, in compliance with this specification, shall use, or have access to production and verification facilities adequate to assure successful compliance with the provisions of this specification and the associated master drawing. Only printed wiring boards which are verified and meet all the applicable performance requirements herein and the design, construction, and material requirements of the associated master drawing shall be certified as compliant and delivered.

3.1.1 Master drawing. Printed wiring boards delivered under this specification shall be of the material, design, and construction specified on the applicable master drawing.

3.1.2 Conflicting requirements. In the event of conflict between the requirements of this specification and other requirements of the applicable master drawing, the precedence in which documents shall govern, in descending order, is as follows:

- a. The applicable master drawing (see 3.1.1). Additional acquisition requirements (see 6.2) may be provided in the order or contract. Any deletion of any of the performance requirements or performance verifications of this specification not approved by the qualifying activity, will result in the printed wiring board being deemed noncompliant with this specification.
- b. This specification.
- c. The applicable design standard (see 3.1.1, A.3.3 as applicable).
- d. Specifications, standards, and other documents referenced in section 2.

3.1.3 Terms and definitions. The definitions for all terms used herein shall be as specified in IPC-T-50 and those contained herein (see 6.4, and appendices A, B, C, D, and E).

3.2 Qualification. Printed wiring boards furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable Qualified Products List (QPL) at the time of award of contract (see A.4.5 and 6.3). In addition, the manufacturer shall certify (for QPL) or receive certification from the qualifying activity (for QPL/Qualified Manufacturer's List (QML)) that the product assurance requirements of 3.3 have been met and are being maintained.

3.2.1 QPL. The qualification requirements for the QPL product assurance level shall be in accordance with [appendix A](#).

3.2.2 QPL/QML. The qualification requirements for the QPL/QML product assurance level shall be in accordance with [appendix B](#).

3.3 Product assurance requirements. This document contains two different methods of product assurance for printed wiring board compliance. The two levels of printed wiring product assurance are QPL (see 3.3.1) and QPL/QML (see 3.3.2) as defined below.

3.3.1 QPL product assurance. A product assurance program for QPL printed wiring board furnished under this specification shall satisfy the requirements of [appendix A](#). Product assurance procedures (see A.4.5.5.2) shall be made available to the qualifying activity no later than 6 months after the date of this specification in order for the manufacturer to be retained on [QPL No. 50884](#). The product assurance procedures shall, as a minimum, consist of the items outlined in [A.4.5.5.2](#).

3.3.2 QPL/QML product assurance. A product assurance program for QPL/QML printed wiring board furnished under this specification shall satisfy the requirements of [appendix B](#).

3.4 Letters of interpretation and policy. Letters of interpretation and policy applicable to this document shall be approved in writing by the preparing activity. All letters of interpretation and policy applicable to MIL-P-50884 written prior to the current date of this document are not applicable to this revision. All subsequent letters of interpretation and policy letters are valid only until the next document change action (amendment or revision).

3.5 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.6 Certification of conformance. Unless otherwise specified by the contract or order (see 6.2), a certificate of conformance for compliant printed boards shall be forwarded to the acquiring activity (see 6.4.4). When a certificate of conformance for compliant printed boards is supplied, it shall include the following information, as a minimum:

- a. Manufacturer's name and address.
- b. Customer's name and address.
- c. Manufacturer's CAGE (Commercial and Government Entity) code.
- d. Printed board description, including classification (type and base material), specification number with revision and amendment level, master drawing or other identification number, and the applicable design standard.
- e. Lot date code.
- f. Quantity of printed boards in shipment from manufacturer.
- g. Statement certifying printed board conformance to this specification, the master drawing, and the contract or order.
- h. The date of transaction.
- i. The name of the company official approving the certificate of conformance. The manufacturer shall have a method for authenticating the approval of certificates of conformance for printed boards compliant to this specification.

3.7 Qualifying activity on-site audit. Manufacturers listed on [QPL-50884](#) will be required to undergo periodic on-site audits of their facilities by the qualifying activity. The manufacturer shall demonstrate to the qualifying activity that controls have been implemented to assure compliance to the requirements of this specification. The qualifying activity reserves the right to perform on-site audits of any other facilities, such as contracted services, that the manufacturer uses for producing printed boards to this specification.

3.8 Workmanship. Printed wiring boards shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [A.4.5](#) or [B.4.1](#)).
- b. Inspection of product for delivery (see [A.4.6](#) or [B.4.3.a](#)).
- c. Periodic conformance inspection (see [A.4.7](#) or [B.4.3.b](#)).

4.2 Printed wiring board performance verification.

4.2.1 QPL. Printed wiring board performance verification inspection shall consist of inspections on the production printed wiring boards and the quality conformance test circuitry or test coupons referenced in [appendix A](#).

4.2.2 QPL/QML. The minimum requirements for printed wiring board performance verification to the QPL/QML product assurance level shall satisfy the guidelines of [appendix B](#).

4.3 Qualification inspection. Qualification is possible by two different methods based on the product assurance level used, QPL (see 4.3.1) or QPL/QML (see 4.3.2).

4.3.1 QPL. Qualification inspection for the QPL product assurance level shall be performed at a laboratory acceptable to the Government (hereafter referred to as a "certified suitable laboratory", see [A.6.6](#) and [C.5](#)) on qualification test specimens produced with material, equipment, and procedures that will be used in subsequent production. The requirements concerning the qualification test specimens, number of specimens to be tested, and the test routines they shall be subjected to, and the extent of qualification shall be as specified in [appendix A](#).

4.3.2 QPL/QML. The minimum requirements for qualification to the QPL/QML product assurance level shall be as specified in [appendix B](#).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Flexible and rigid-flex printed wiring boards are intended primarily for use in electronic and electrical equipment to eliminate high density hand wiring, where space is limited and where compact packaging is desirable.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, revision letter (with any amendment number when applicable), and date of this specification.
- b. Issue of DoDISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see [2.2](#)).
- c. Packaging requirements (see [5.1](#)).
- d. Appropriate type (see [1.2.1](#)) and flexibility class (see [1.2.2](#)).
- e. Title, number, revision letter (with any engineering change proposal or notice of revision number when applicable), and date of the applicable master drawing (see [3.1.1](#)).

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6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in [Qualified Products List \(QPL\) No. 50884](#) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center Columbus, ATTN: DSCC-VQE, P.O. Box 3990, Columbus, Ohio 43218-3990, or by email 5998.Qualifications@dla.mil, or at Universal Resource Locator (URL) <http://www.dsccl.dla.mil/programs/qmlqpl>. Application procedures should conform to the guidelines of SD-6, "Provisions Governing Qualification" (see 6.3.3).

6.3.1 Transference of qualification. Manufacturers currently qualified to MIL-P-50884D amendment 1 will have their qualification transferred to this document. The expiration date of their current qualification will not be changed. Qualifications in process (before the date of this document) will be performed to the requirements MIL-P-50884D amendment 1. New applications for qualification (after the date of this document) should be performed to the requirements of this revision.

6.3.2 Retention of qualification. Printed wiring boards verified and certified to MIL-P-50884C (with any amendment) or to any product assurance level contained herein will retain qualification to this document.

6.3.2.1 Discussion. MIL-P-50884C (unamended) certification program was not governed by the policies and procedures of the Defense Standardization Program as defined by DoD 4120.3-M and therefore does not exist within the QPL program of MIL-P-50884C with Amendment 1 and beyond. For additional information concerning this issue, see MIL-P-50884C, paragraph 60.1.

6.3.3 "Provisions Governing Qualification". Copies of SD-6, "Provisions Governing Qualification", may be downloaded at URL <http://assistdocs.com/search> or obtained upon application to Document Automation and Production Services (DAPS), Building 4D (DPM-DODSSP), 700 Robbins Avenue, Philadelphia, PA 19111-5094.

6.4 Terms and definitions.

6.4.1 Design standard. A document that establishes the baseline parameters (default values), standard practices and guidelines for the design of printed wiring boards. Within this document, the term "design standard" is used to describe those documents that contains the design, construction, material, and test coupon requirements and guidelines used to produce panels of flexible printed wiring boards.

6.4.2 Printed wiring board types. The printed wiring board types should be as specified in IPC-2223 or MIL-STD-2118.

6.4.2.1 Type 1. Type 1 flexible printed wiring boards have only one conductive layer (single sided conductor pattern) with coverlayer and no plating in the component holes. In addition, the design may contain shields or stiffeners. Type 1 flexible printed wiring boards are usually designed for [class B](#) (continuous flex) applications.

6.4.2.2 Type 2. Type 2 flexible printed wiring boards are printed wiring boards with conductor patterns on both sides of the printed board (double sided). In addition, the design of the printed wiring board may require the following: (1) that the holes through the base material be plated through to connect the conductor patterns on both sides together, (2) with or without shields, and (3) with or without stiffeners. Type 2 flexible printed wiring boards are usually designed for [class B](#) (continuous flex) applications.

6.4.2.3 Type 3. Type 3 flexible printed wiring boards are multilayered (with three or more conductor layers) with plated-through holes. Type 3 printed wiring boards are usually designed for [class A](#) (flex to install) applications.

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6.4.2.4 Type 4. Type 4 flex-rigid printed wiring boards are multilayered boards containing plated-through holes with rigid sections connected by flexible sections. Type 4 printed wiring boards are usually only designed to be used in class A (flex to install) applications.

6.4.2.5 Type 5. Type 5 printed wiring boards are multilayer bonded rigid and/or flexible printed wiring board combinations without plated-through holes.

6.4.3 Product assurance. The method of complying with the two different levels of this document using either the QPL method (implemented by amendment 1 to MIL-P-50884C) or the new method QPL/QML (introduced by MIL-P-50884D).

6.4.3.1 QML. A list of manufacturers, by name and plant address, who have met the certification and qualification requirements stated in MIL-PRF-31032. A QML focuses on qualifying an envelope of materials and processes rather than individual products or designs. That envelope is qualified by carefully selecting representative worst case test vehicles or representative samples from production that contain all potential combinations of materials and processes that may be subsequently used during production. A QML is normally appropriate for items of supply that have very rapid technological advancement or a myriad of variations or custom designs that make individual product qualifications impractical or excessively expensive.

6.4.3.2 QPL. A QPL focuses on qualifying individual products or families of products. A QPL will normally be appropriate for items of supply that are stable and will be continually available for extended period of time.

6.4.3.3 QPL/QML. A transitional program that allows a manufacturer that is certified and qualified to the QML program of MIL-PRF-31032 to fabricate, test, and supply products to this revision of this document.

6.4.4 Acquiring activity. The organizational element of the Government which contracts for articles, supplies, or services may authorize a contractor or subcontractor to be its agent. When this organizational element of the Government has given specific written authorization to a contractor or subcontractor to serve as agent, the agent will not have the authority to grant waivers, deviations, or exceptions to this specification unless specific written authorization to do so has also been given by the Government organization, which is the preparing activity or qualifying activity. In the absence of a specific acquiring activity, the acquiring activity will be an organization within the supplier's company that is independent of the group responsible for device design, process development, or screening, or may be an independent organization outside the supplier's company.

6.5 Compliant printed wiring boards. For a printed wiring board to be compliant with this document, it has to be produced by a manufacturer qualified for listing on QPL No. 50884 or reciprocal listing as described in appendix B, and come from a lot which was subjected to and passed all inspection of product for delivery verifications using the applicable product assurance program.

6.6 Supersession.

6.6.1 Superseded types and classes. Superseded types and classes are listed below:

- a. Type A of MIL-P-50884B (the ability to withstand only one solder operation without degradation) was not superseded and therefore does not apply or exist in newer revisions.
- b. Type B of MIL-P-50884B (the ability to withstand five solder and unsoldering operation without degradation) was superseded by all printed wiring board types of MIL-P-50884C and beyond.
- c. Class 1 of MIL-P-50884B was superseded by types 1, 2, and 5 of MIL-P-50884C and beyond.
- d. Class 2 of MIL-P-50884B was superseded by types 3 and 4 of MIL-P-50884C and beyond.

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6.6.2 Design, construction and verification. Design, construction, and verification supersession information is included in [appendix D](#) of this document.

6.6.3 Reference to superseded specifications. All the requirements of this document can be interchangeable with those documents identified as MIL-P-50884. Therefore, existing documents (master drawings or OEM documents) referencing MIL-P-50884 need not be revised, updated, or changed to make reference to MIL-P-50884 in order for this document to be used.

6.6.4 Diagrams and figures. Most diagrams and figures that were in previous revisions of MIL-P-50884 have been eliminated from this document. See [appendix A](#) for guidance concerning diagrams and figures.

6.7 Design standards. This document contains requirements and guidelines for the testing of printed wiring boards that were designed to and or make use of test coupons conforming to IPC-2221. See [appendix D](#) for additional guidance regarding the verification of panels using different design standards.

6.8 Environmentally preferable materials. Environmentally preferable materials should be used to the maximum extent possible to meet the requirements, and promotes economically advantageous life cycle costs. The chart below lists the Environmental Protection Agency's (EPA) top 17 hazardous materials targeted for major usage reduction. If any of these hazardous materials are required, it is recommended that it be used only when other materials cannot meet performance requirements.

| | | |
|------------------------|------------------------|-------------------------|
| Benzene | Dichloromethane | Tetrachloroethylene |
| Cadmium and compounds | Lead and compounds | Toluene |
| Carbon Tetrachloride | Mercury and compounds | 1,1,1 – Trichloroethane |
| Chloroform | Methyl Ethyl Ketone | Trichloroethylene |
| Chromium and compounds | Methyl Isobutyl Ketone | Xylenes |
| Cyanide and compounds | Nickel and compounds | |

6.9 Subject term (key word) listing.

Design standard
Master drawing
Qualified Manufacturer List (QML)
Qualified Product List (QPL)
Test coupon
Verification Conformance Inspection

6.10 Amendment notations. The margins of this specification are marked with a vertical lines to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

APPENDIX A

PRODUCT ASSURANCE (QUALIFICATION AND VERIFICATION) REQUIREMENTS
FOR QUALIFIED PRODUCTS LIST PROGRAMS

A.1. SCOPE

A.1.1 Scope. This appendix contains the requirements and procedures for manufacturers using the traditional Qualified Products List (QPL) method of product assurance (qualification and verification inspection) for printed wiring boards covered by this specification. The process for extending and retaining qualification is also herein. This appendix is a mandatory part of this specification for non-QML manufacturers. The information contained herein is intended for compliance.

A.2. APPLICABLE DOCUMENTS

A.2.1 General. The documents listed in this section are specified in sections A.3 and A.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections A.3 and A.4 of this specification, whether or not they are listed.

A.2.1.1 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

- J-STD-003 – Solderability Tests for Printed Boards.
- IPC-2221 – Printed Board Design, Generic Standard for.
- IPC-2223 – Flexible Printed Boards, Sectional Design Standard for.
- IPC-A-600 – Acceptability of Printed Boards.
- IPC-TM-650 – Test Methods Manual.
- IPC-100041 – Master Drawing for Single Sided Printed Boards.
- IPC-100042 – Master Drawing for Double Sided Printed Boards.
- IPC-100043 – Master Drawing for 10 Layer Multilayer Printed Boards.
- IPC-100044 – Master Drawing for 4 Layer Multilayer Printed Boards.

(Application for copies should be addressed to the Association Connecting Electronics Industries (IPC), 3000 Lakeside Drive, Suite 309 S, Bannockburn, IL 60015-1249 or <http://www.ipc.org>.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

A.2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

APPENDIX A

A.3. REQUIREMENTS

A.3.1 General. The performance requirements contained in this section, although sometimes determined by examination of sampled printed wiring boards or test coupons, apply to all deliverable printed wiring boards.

A.3.1.1 Master drawing (see [A.6.2.1.d](#)). Printed wiring boards delivered under this specification shall be of the material, design, and construction specified on the applicable master drawing. For the purposes of this appendix, when the term "specified" is used without additional reference to a specific location or document, the intended reference shall be to the applicable master drawing. If individual design details are not specified on the applicable master drawing, then the baseline design parameters shall be as detailed in the design standard that was used to design the printed wiring board (see [A.3.3](#)).

A.3.2 Qualification. Printed wiring boards furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable QPL at the time of award of contract (see [A.4.5](#) and [A.6.3](#)). In addition, the manufacturer shall certify that the product assurance requirements of [A.4.5.5.2](#) have been met and are being maintained.

A.3.3 Design (see [A.6.2.1.e](#)). Printed wiring boards shall be of the design as specified. Unless otherwise specified (see [A.3.1.1](#)), if individual design details are not specified on the applicable master drawing, then the baseline design parameters to be used for acceptability of finished product requirements shall be as detailed in the design standard that was used to design the printed wiring board. If no design standard is specified on the master drawing or the appropriate design standard cannot be determined, then the default design shall be performance class 3 of IPC-2221 and IPC-2223.

A.3.3.1 Test coupons. Test coupon design, quantity, and placement, shall be in accordance with IPC-2221 and IPC-2223. NOTE: Test coupons shall be as specified in the applicable design standard and shall reflect worst case design conditions of the printed board(s) they represent.

A.3.4 Material. The printed wiring boards shall be constructed of material as specified (see [A.3.1.1](#)). When a definite material is not specified (see [A.3.1.1](#)), a material shall be used that will enable the printed wiring board to meet the performance requirements of this specification. Acceptance or approval of any material shall not be construed as a guaranty of the acceptance of the finished printed wiring board.

A.3.4.1 Tin finishes. Unless otherwise specified (see [A.3.1.1](#)), the use of pure tin, as an underplate or final finish, is prohibited both internally and externally. Tin content of printed wiring board finishes or solders shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass (see [A.6.11](#)).

A.3.5 Visual and dimensional requirements. The finished printed wiring board shall meet the dimensional (such as cutouts, overall thickness, periphery, etc.) requirements specified (see [A.3.1.1](#)) and in [A.3.5.1](#) through [A.3.5.9](#). [IPC-A-600](#) contains figures, illustrations, and photographs that can aid in the visualization of externally observable accept/reject conditions of printed wiring board test specimens. If a condition is not addressed herein or specified on the master drawing, it shall comply with the class 3 criteria of [IPC-A-600](#).

APPENDIX A

A.3.5.1 Base materials (flexible and rigid).

A.3.5.1.1 Edges of flexible sections. Defects such as burrs, nicks, tears, or delamination, along the trimmed edges of flexible sections of printed wiring boards shall be acceptable provided the penetration does not reduce the edge spacing by more than 50 percent of the edge spacing specified (see A.3.1.1). Discoloration or resin recession along the trimmed edges of the flexible sections following the surface solderability test is acceptable providing the discoloration or resin recession dimension does not exceed the thickness of the adhesive material in the bonding area (when applicable) or reduce the edge spacing below the requirements of the master drawing.

A.3.5.1.2 Edges of rigid sections (types 4 and 5). Defects such as burrs, nicks, and haloing along the edges of rigid sections of printed wiring boards shall be acceptable provided the penetration does not reduce the edge spacing by more than .10 inch (0.25 mm) or 50 percent of the edge spacing specified (see A.3.1.1), whichever is less.

A.3.5.1.3 Surface imperfections. Surface imperfections (such as scratches, pits, dents, and weave texture) shall be acceptable providing the imperfection meets the following:

- a. The base material reinforcement material (woven or non-woven fiber) is not cut, disturbed, or exposed.
- b. The imperfection does not bridge between conductors (weave texture may bridge conductors).
- c. The dielectric spacing between the imperfection and conductors does not reduce conductor spacing below the specified minimum requirements (see A.3.1.1).

A.3.5.1.4 Subsurface imperfections. Subsurface imperfections (such as blistering, haloing, and delamination) shall be acceptable providing the imperfection meets the following:

- a. The imperfection is translucent.
- b. The imperfection does not bridge more than 25 percent of the distance between conductors or plated-through holes. No more than two percent of the printed wiring board area on each side shall be affected.
- c. The imperfection does not reduce conductor spacing between adjacent conductors below the minimum requirements specified (see A.3.1.1).
- d. The imperfection does not propagate as a result of testing (such as rework simulation, thermal stress, or thermal shock).

A.3.5.1.4.1 Foreign inclusions. Foreign inclusions shall be permitted when they meet the following:

- a. The inclusion is trapped within the flexible portion of the printed board.
- b. The inclusion is located at least .010 inch (0.25 mm) from the nearest conductor.
- c. The inclusion does not reduce the spacing between conductors below the minimum conductor spacing specified (see A.3.1.1).
- d. The inclusions longest dimension is no greater than .032 inch (0.81 mm) in circuitry areas. Inclusions in non-circuitry areas have no maximum dimension requirement.

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A.3.5.1.4.2 Subsurface spots. Subsurface spots shall be permitted when they meet any of the following:

- a. The spots are translucent.
- b. The spots are known to be weave texture other than delamination or disbonding.
- c. The spots are isolated white spots that are at least .010 inch (0.25 mm) from the nearest conductor or that do not propagate as a result of any soldering operation (gelation particles are acceptable regardless of location).

A.3.5.1.4.3 Adhesive voids (for metal clad flexible base materials only). Adhesive voids that are no greater than .020 inch (0.51 mm) or 25 percent of spacing shall be acceptable.

A.3.5.2 Conductor pattern.

A.3.5.2.1 Annular ring, external. The minimum external annular ring shall be as specified (see A.3.1.1). If not specified, the minimum external annular ring shall be .002 inch (0.051 mm) for plated through holes and .006 inch (0.152 mm) for unsupported holes. Unless otherwise specified, the external annular ring may have, in isolated areas, a 20 percent reduction of the minimum external annular ring specified (see A.3.1.1), due to defects such as pits, dents, nicks, pinholes and extruded adhesive onto the land. Unless otherwise specified, plated holes identified as vias can have a maximum of 90 degrees of hole breakout if the breakout does not occur at the conductor to land intersection.

A.3.5.2.2 Conductor spacing. The conductor spacing shall be as specified (see A.3.1.1). The minimum edge spacing (the spacing between the edge of the printed wiring board and conductors) shall be as specified (see A.3.1.1).

A.3.5.2.3 Conductor width. The conductor width(s) shall be as specified (see A.3.1.1).

A.3.5.2.3.1 Conductor pattern imperfections. The conductor pattern shall contain no cracks, splits or tears. Unless otherwise specified (see A.3.1.1), any combination of edge roughness, nicks, pinholes, cuts or scratches exposing the base material shall not reduce each conductor width more than 20 percent of its minimum specified width. There shall be no occurrence of the 20 percent reductions greater than .50 inch (12.70 mm) or 10 percent of a conductor length, whichever is less.

A.3.5.2.4 Conductor finish coverage. The conductor finish plating or coating shall completely cover the basis metal of the conductive pattern. Complete conductor coverage by solder does not apply to the vertical conductor edges. There shall be no evidence of any lifting or separation of conductor finish plating or coating from the surface of the conductive pattern. There shall be no whiskers of solder or plating on the surface of the conductive pattern. For designs using solder resist over bare conductors, it shall be acceptable to have up to .010 inch (0.25 mm) of exposed base metal at the interface between the solder resist and the basis metal conductor finish. For design requiring unfused tin-lead plating as a final conductor finish coverage, the thickness shall be as specified (see A.3.1.1 and A.3.3).

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A.3.5.3 Coverlayer. Unless otherwise specified, the coverlayer requirements specified in A.3.5.3.1 through A.3.5.3.5 shall apply.

A.3.5.3.1 Coverage. Coverlayer coverage imperfections (such as blisters, pits, skips, and voids) shall be acceptable providing the imperfection complies with the following:

- a. The coverlayer imperfection shall not expose isolated conductors whose spacing is less than the electrical spacing required for the voltage range and environmental condition specified in the applicable design standard.
- b. In areas containing parallel conductors, the coverlayer imperfection shall not expose isolated conductors whose spacing is less than .020 inch (0.5 mm) unless one of the conductors is a test point or other feature area which is purposely left uncoated for subsequent operations.
- c. The exposed conductor shall not be bare copper.
- d. The coverlayer imperfection does not expose plated holes or via holes that are to be tented or filled by coverlayer.
- e. Blisters in the coverlayer shall not exceed the following: Two per side, maximum size .010 inch (0.25 mm) in longest dimension, does not reduce electrical spacing between conductors by more than 25 percent.
- f. Pits and voids in non-conductor areas shall be acceptable provided they have adherent edges and do not exhibit lifting or blisters in excess of that allowed in A.3.5.3.1.e.

A.3.5.3.2 Delamination. There shall be no coverlayer delamination along the outer edges of the coverlayer (see A.3.5.1.1). Coverlayer delamination shall be acceptable providing the following conditions are met:

- a. At random locations away from conductors if each delamination is no larger than .01 square inch (6.45 square mm) and is not within .040 inch (1.0 mm) of the printed wiring board edge or access hole edge. The total number of the above delaminations shall not exceed three in any 1 square inch (645 square mm) of coverlayer surface area.
- b. Along conductor edges, the total delamination does not exceed either .02 inch (0.51 mm) in width or 20 percent of the spacing between adjacent conductors, whichever is smaller.
- c. When design requires coverage to the edge of flexible sections; chipping, delamination, lifting, or separation of the coverlayer along the edge of flexible sections shall not penetrate more than .05 inch (1.3 mm) or 50 percent of the distance to the closest conductor, whichever is less.

A.3.5.3.2.1 Wrinkles or creases. Wrinkles or creases in the coverlayer shall be acceptable provided the requirements of A.3.5.3.2 are met.

A.3.5.3.2.2 Class B only. After exposure to the flexibility endurance test (see A.3.7.4.3 and A.4.8.4.3), there shall be no propagation of any coverlayer separation or delamination in the continuous flex area for class B designs.

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A.3.5.3.3 Registration. The coverlayer shall be registered to the land or terminal patterns in such a manner as to meet the requirements specified (see A.3.1.1). If a clearance is specified, no encroachment of the coverlayer on the land is allowed, except at the conductor attachment. If no registration requirements are specified, the following shall apply:

- a. For plated-through holes and vias, the following shall apply:
 - 1) Coverlayer misregistration onto plated-through component hole lands (plated-through holes to which solder connections are to be made) shall not reduce the external annular ring below the specified minimum requirements. The requirements of A.3.5.3.1a and A.3.5.3.1b shall also be met.
 - 2) Coverlayer shall not encroach into plated-through hole barrels or onto lands of unplated holes to which solder connections will be made.
 - 3) Unless specified to be solder filled, coverlayer is permitted in plated holes or vias in which no lead is to be soldered.
- b. For surface mount lands with no plated-through holes, the following shall apply:
 - 1) For lands with a pitch of .050 inch (1.27 mm) or greater, coverlayer encroachment is on one side of land only and does not exceed .002 inch (0.050 mm).
 - 2) For lands with a pitch less than .050 inch (1.27 mm), coverlayer encroachment shall not exceed .001 inch (0.025 mm). The encroachment can occur on adjacent sides, but not on opposite sides of the land.
- c. For ball grid array lands, the following shall apply:
 - 1) If the BGA land is coverlayer defined, allowable misregistration of the coverlayer causes breakout of the land of not more than 90 degrees.
 - 2) If the BGA land is copper defined, the coverlayer shall not encroach onto the land. Coverlayer on the land-to-via connecting conductor shall be acceptable.
 - 3) If the BGA land is connected to a via and a coverlayer dam is specified, the dam shall remain in place and be continuous over the conductor to the via (no cracked, peeling, or missing coverlayer).
- d. Edge-board contacts and test points which are intended for assembly testing shall be free of coverlayer unless a partial coverage allowance is specified.
- e. Coverlayer shall not encroach into plated-through hole barrels or onto other surface features such as connector fingers, test points, or lands of unplated holes to which solder connections will be made.

A.3.5.3.4 Thickness. The coverlayer thickness shall be as specified (see A.3.1.1).

A.3.5.3.5 Coverlayer cure. The cured coverlayer coating shall not exhibit tackiness and blistering or delamination shall not be in excess of that allowed in A.3.5.3.1 or A.3.5.3.3.

A.3.5.4 Hole pattern accuracy. The accuracy of the hole pattern (size and location) on the printed wiring board shall be as specified (see A.3.1.1).

A.3.5.5 Lifted lands. There shall be no lifted lands on the deliverable printed wiring board.

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A.3.5.6 Registration, external (method I). Misregistration shall not reduce the minimum external annular ring below its specified limits (see A.3.1.1).

A.3.5.7 Solder resist (when applicable). Unless otherwise specified, the solder resist requirements specified in A.3.5.7.1 through A.3.5.7.4 shall apply.

A.3.5.7.1 Coverage. Solder resist coverage imperfections (such as blisters, skips, and voids) shall be acceptable providing the imperfection meets all of the following:

- a. The solder resist imperfection shall not expose two adjacent conductors whose spacing is less than the electrical spacing required for the voltage range and environmental condition specified in the applicable design standard.
- b. In areas containing parallel conductors, the solder resist imperfection shall not expose two isolated conductors whose spacing is less than 0.5 mm (.020 inch) unless one of the conductors is a test point or other feature area which is purposely left uncoated for subsequent operations.
- c. The exposed conductor shall not be bare copper.
- d. The solder resist imperfection does not expose tented via holes.

A.3.5.7.2 Discoloration. Discoloration of metallic surfaces under the cured solder resist is acceptable.

A.3.5.7.3 Registration. The solder resist shall be registered to the land or terminal patterns in such a manner as to meet the requirements specified (see A.3.1.1). If no requirements are specified, the following apply:

- a. Unless otherwise specified, solder resist shall not encroach onto surface mount lands.
- b. Solder resist misregistration onto plated-through component hole lands (plated-through holes to which solder connections are to be made) shall not reduce the external annular ring below the specified minimum requirements.
- c. Solder resist shall not encroach into plated-through hole barrels or onto other surface features (such as connector fingers or lands of unplated holes) to which solder connections will be made.
- d. Solder resist is permitted in plated-through vias or holes in which no lead is to be soldered.
- e. Test points which are intended for assembly testing shall be free of solder resist unless a partial coverage allowance is specified.

A.3.5.7.4 Thickness. The solder resist thickness shall be as specified (see A.3.1.1).

A.3.5.8 Stiffener. Complete bonding of the stiffener to the flexible portion of the printed wiring board is not required (see A.6.9).

A.3.5.8.1 Stiffener access hole registration. Stiffener access hole registration shall be such that the size or diameter of the access hole shall not reduce the component land area or minimum annular ring below the limits specified (see A.3.5.2.1).

A.3.5.9 Wicking. Wicking of plating or solder extending .010 inch (0.25 mm) into the base material shall be acceptable provided it does not reduce the conductor spacing below the minimum clearance spacing requirements specified (see A.3.1.1).

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A.3.6 Plated hole requirements. When examined by microsection, the plated holes of the microsectioned test specimen (which includes plated-through holes, blind vias, buried vias, low aspect ratio blind vias, and microvias) shall meet the requirements of A.3.6.1 through A.3.6.14. If not specified in A.3.1.1 or herein, the requirements of A.3.3 shall be met. IPC-A-600 contains figures, illustrations, and photographs that can aid in the visualization of internally observable accept/reject conditions of microsectioned test specimens. If a condition is not addressed herein or specified on the master drawing, it shall comply with the class 3 criteria of IPC-A-600.

A.3.6.1 Annular ring, internal. The minimum annular ring for functional internal lands on types 3 and 4 printed wiring boards shall be as specified (see A.3.1.1). If not specified on the master drawing, the minimum internal annular ring shall not be less than .002 inch (0.051 mm).

A.3.6.2 Conductor thickness. The conductor thickness shall be as specified (see A.3.1.1). When a copper foil weight requirement is specified, a reduction in thickness up to 10 percent below the minimum allowable foil thickness specified by the applicable material specification shall be considered acceptable in order to accommodate a processing allowance for cleaning either by chemical or mechanical means.

A.3.6.3 Dielectric layer thickness. The minimum dielectric thickness separating the conductor layers of the printed wiring boards shall be as specified (see A.3.1.1). If not specified on the master drawing, the minimum dielectric spacing for rigid base materials shall be .0035 inch (0.089 mm) and for flexible base materials .0015 inch (0.038 mm).

A.3.6.3.1 Thermal planes. The minimum lateral spacing between adjacent conductive surfaces (nonfunctional pads) or plated-through hole and the thermal plane shall be as specified (see A.3.1.1). Radial cracks, wicking, or voids in the hole-fill insulation material shall not reduce by 75 percent the specified lateral spacing between adjacent conductive surfaces.

A.3.6.3.2 Coverlayer thickness. Unless otherwise specified (see A.3.1.1), the thickness of the coverlayer shall not be measured.

A.3.6.4 Delamination. Printed wiring boards shall have no delaminations in excess of that allowed in A.3.5.1.4.

A.3.6.5 Etchback or smear removal.

A.3.6.5.1 Etchback (when specified, see A.3.1.1). When specified (see A.3.1.1), printed wiring boards shall be etched back for the lateral removal of resin and reinforcement material (woven glass or other media) from the internal conductors prior to plating. The etchback shall be effective on at least the top or bottom (horizontal) surface of each internal conductor. Negative etchback is not acceptable when etchback is specified (see A.3.1.1).

A.3.6.5.1.1 Etchback limits. Unless otherwise specified (see A.3.1.1), etchback shall not exceed .003 inch (0.08 mm) or be less than .0001 inch (0.0025 mm) with .0005 inch (.013 mm) being a preferred depth when measured at the internal copper contact area protrusion.

A.3.6.5.2 Smear removal (hole cleaning). When etchback is not specified (see A.3.1.1), the vertical faces of the internal conductors of the plated-through hole shall be cleaned to be free of resin smear. Lateral removal of base material from the hole wall shall not exceed .001 inch (0.03 mm). When etchback is not specified (see A.3.1.1), a negative etchback of .0005 inch (0.013 mm) maximum shall be acceptable.

A.3.6.6 Base material voids.

A.3.6.6.1 As received condition of rigid base materials. Laminate voids with the longest dimension of .003 inch (0.08 mm) or less shall be acceptable.

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A.3.6.6.2 After rework simulation, thermal shock or thermal stress testing (see figure 1). Laminate voids are not evaluated in zone A. Laminate voids in zone B with the longest dimension of .003 inch (0.08 mm) or less shall be acceptable provided the conductor spacing is not reduced below the minimum dielectric spacing requirements, laterally or vertically, as specified (see A.3.1.1).

A.3.6.6.3 Adhesive voids (for metal clad flexible base materials only). Adhesive voids that are no greater than .020 inch (0.51 mm) shall be acceptable. Multiple adhesive voids in the same plane between adjacent plated holes shall not have a combined length which exceeds .020 inch (0.51 mm).

A.3.6.7 Lifted lands.

A.3.6.7.1 As received condition. There shall be no lifted lands on the as received microsectioned test specimen. When inspected in accordance with A.4.8.2 and lifted lands are present, the lot shall be 100 percent visually inspected in accordance with A.4.8.1 for separation of the lands from the base material.

A.3.6.7.2 After rework simulation, thermal stress or thermal shock testing. After undergoing rework simulation, thermal stress, or thermal shock testing (see A.3.7.4.6, A.3.7.4.10, and A.3.7.6.2), the maximum allowed distance from the base material surface to the bottom of the edge of the land or pad shall be no greater than the total land thickness. The total land thickness is equal to the combined thickness of the metal foil and copper plating on that land.

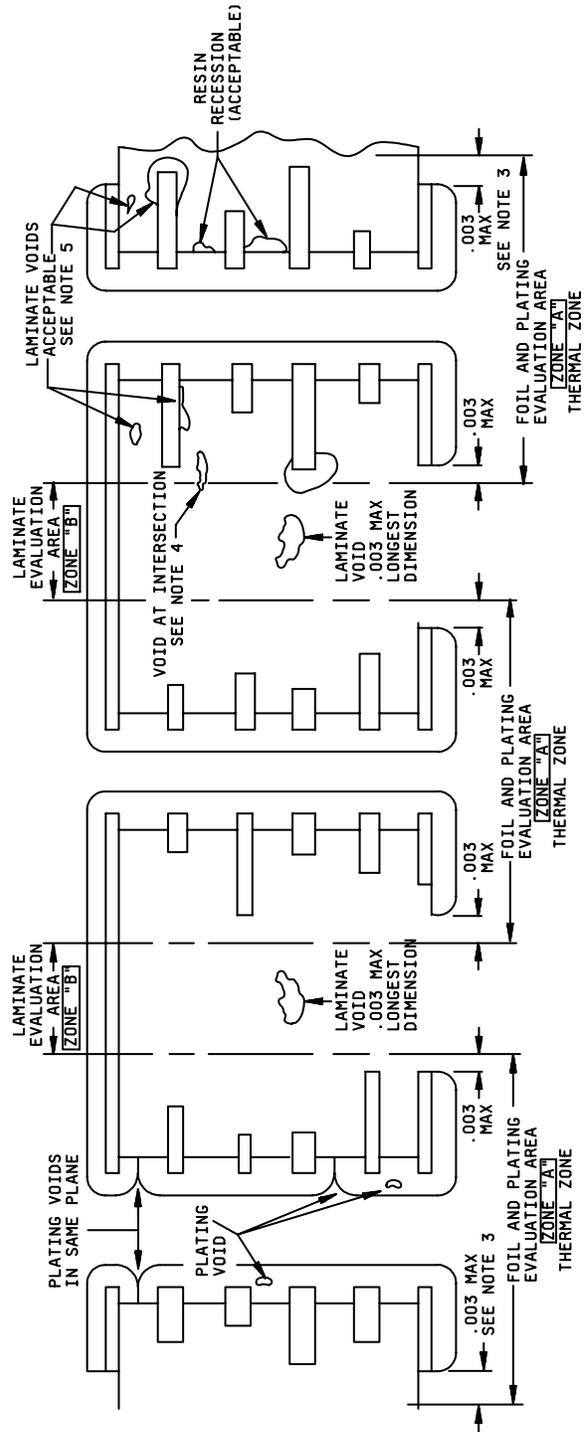
A.3.6.8 Plating and coating properties.

A.3.6.8.1 Conductor finish thickness (when applicable). Unless otherwise specified on the master drawing (see A.3.1.1), the conductor finish plating or coating thickness shall be as specified in table I. (Also see A.3.5.2.4).

TABLE I. Conductor plating and finish thickness.

| Material | Thickness, in inches (mm) | |
|--|------------------------------|------------------------------|
| Gold (electroplated) for edge-board contacts and areas not to be soldered | .00005 (0.0013 mm) minimum | |
| Gold (electroplated) for areas to be soldered | .000018 (0.00046 mm) maximum | |
| Gold (electroplated) for areas to be wire bonded, ultrasonic | .000002 (0.00005 mm) minimum | |
| Gold (electroplated) for areas to be wire bonded, thermosonic | .00003 (0.0008 mm) minimum | |
| Nickel (electroplated) for edge-board contacts | .0001 (0.0025 mm) minimum | |
| Nickel (electroplated) as a barrier to prevent formation of copper-tin compounds | .00005 (0.0013 mm) minimum | |
| Organic solderability preservative (OSP) | Solderable | |
| Immersion silver | Solderable | |
| Electrodeposited tin-lead, fused or solder coat | Coverage and solderable | |
| Electrodeposited tin-lead, unfused | .0003 (0.008 mm) minimum | |
| Solder coat over base copper | Coverage and solderable | |
| ENIG | Electroless nickel | .00012 (0.003 mm) minimum |
| | Immersion gold | .000002 (0.00005 mm) minimum |

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NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Typically beyond land edge most radially extended.
4. Void at intersection of zone A and zone B. Laminate voids greater than .003 (0.08 mm) that extend into zone B are rejectable.
5. Laminate voids are not evaluated in zone A. Laminate voids greater than .003 (0.08 mm) that extend into zone B are rejectable.

FIGURE 1. Typical plated-through hole cross section after thermal stress or rework simulation.

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A.3.6.8.2 Copper plating thickness (when applicable). Unless otherwise specified on the master drawing (see A.3.1.1), copper plating thickness (on the surface, in plated-through holes, in blind and buried vias) shall be as specified in table I-1. Unless otherwise specified (see A.3.1.1), copper plating thickness applies to the hole wall, the surface land, and the knee of the plated hole. Unless otherwise specified (see A.3.1.1), a 20 percent reduction of the specified copper plating thickness shall be acceptable. Any 20 percent thickness reduction shall be non-continuous (isolated; not more than 10 percent of the composite board thickness). Any copper plating less than 80 percent of the specified thickness shall be treated as a void.

TABLE I-1. Copper plating thickness, in inches (mm).

| | Type 2 | Type 3 | Type 4 | Type 3 & 4 |
|-------------------------|-------------------------------------|------------------|------------------|------------------|
| | Through holes | | | |
| Overall board thickness | ≤ .008 (0.2 mm) | >.008 (0.2 mm) | >.008 (0.2 mm) | >.030 (0.76 mm) |
| Minimum average | .0005 (0.013 mm) | .001 (0.025 mm) | .001 (0.025 mm) | .0014 (0.035 mm) |
| Minimum thin area | .0004 (0.010 mm) | .0008 (0.020 mm) | .0008 (0.020 mm) | .0012 (0.030 mm) |
| | Blind vias | | | |
| Minimum average | | .0006 (0.015 mm) | .0006 (0.015 mm) | .0006 (0.015 mm) |
| Minimum thin area | | .0005 (0.013 mm) | .0005 (0.013 mm) | .0005 (0.013 mm) |
| | Blind microvias | | | |
| Minimum average | | .0005 (0.013 mm) | .0005 (0.013 mm) | .0005 (0.013 mm) |
| Minimum thin area | | .0004 (0.010 mm) | .0004 (0.010 mm) | .0004 (0.010 mm) |
| | Buried vias cores (single layer) | | | |
| Minimum average | | .0006 (0.015 mm) | .0006 (0.015 mm) | .0006 (0.015 mm) |
| Minimum thin area | | .0005 (0.013 mm) | .0005 (0.013 mm) | .0005 (0.013 mm) |
| | Buried vias (greater than 2 layers) | | | |
| Minimum average | | .001 (0.025 mm) | .001 (0.025 mm) | .001 (0.025 mm) |
| Minimum thin area | | .0008 (0.020 mm) | .0008 (0.020 mm) | .0008 (0.020 mm) |

A.3.6.8.2.1 Copper plating voids. The copper plating in the plated-through holes shall not exhibit any void in excess of the following:

- a. There shall be no more than one plating void per panel, regardless of length or size.
- b. There shall be no plating void in excess of 5 percent of the total printed wiring board thickness.
- c. There shall be no plating voids evident at the interface of an internal conductive layer and plated hole wall.

A.3.6.8.2.2 Plating separations (see A.6.4.3). Except for along the vertical edge of the external copper foil, there shall be no separations or contamination between the hole wall conductive interfaces. Conductive interface separations along the vertical edge of the external copper foil shall be acceptable.

A.3.6.9 Hole wall deficiencies. Nodules, plating folds, or plated glass fibers that project into the copper plating shall be acceptable provided that the hole diameter and the hole wall copper thickness are not reduced below their specified limits (see A.3.1.1).

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A.3.6.10 Metallic cracks. There shall be no cracks in the internal layer conductive foils, platings, or coatings. Cracks in outer layer metal foil shall be acceptable if they do not propagate into the plated copper. Cracks shall not be acceptable in the copper plating.

A.3.6.11 Nail-heading. Nail-heading of conductors shall not exceed 1.5 times the copper foil thickness.

A.3.6.12 Resin recession.

A.3.6.12.1 As received condition. Resin recession at the outer surface of the plated-through hole barrel wall shall be permitted provided the maximum depth as measured from the barrel wall does not exceed .003 inch (0.08 mm) and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated.

A.3.6.12.2 After rework simulation, thermal shock or thermal stress testing. Resin recession at the outer surface of the plated-through hole barrel shall be permitted and is not cause for rejection.

A.3.6.13 Wicking. Wicking of copper plating extending .003 inch (0.08 mm) into the base material shall be acceptable provided it does not reduce the conductor spacing below the minimum clearance spacing requirements specified (see A.3.1.1).

A.3.6.14 Undercutting. Undercutting at each edge of the conductors shall not exceed the total thickness of the copper foil and plated copper.

A.3.7 Inspection requirements. The detailed requirements contained in this section, although determined by examination of sample printed wiring boards or test coupons, apply to all deliverable printed wiring boards.

A.3.7.1 Acceptability (of printed wiring boards). When examined as specified in A.4.8.1, the printed wiring boards shall be in accordance with the acceptance requirements specified in A.3.1.1 (master drawing), A.3.4 (material), A.3.5 (visual and dimensional), A.3.8 (marking), A.3.10 (repair) and A.3.11 (workmanship), as applicable.

A.3.7.2 Acceptability (of microsectioned test specimens). When printed wiring board test specimens (finished printed wiring boards, supporting test coupons, or qualification test specimens) are microsectioned and examined as specified in A.4.8.2, the requirements specified in A.3.6 shall be met.

A.3.7.2.1 As received. After meeting the requirements of A.3.8 and A.3.11 when inspected in accordance with A.4.8.1, the as received printed wiring board test specimen shall be microsectioned and inspected in accordance with A.4.8.2 and shall meet the requirements of A.3.6.

A.3.7.2.2 Registration, internal.

A.3.7.2.2.1 By microsection (method II). Unless otherwise specified (see A.3.1.1), when inspected as specified in A.4.8.2.2, the layer-to-layer pattern misregistration shall not reduce the minimum annular ring below its specified (see A.3.1.1) limits.

A.3.7.2.2.2 Optional internal registration by registration test coupons. Registration test coupons may have been designed into the printed wiring board by the design activity, or may be added to the panel by the manufacturer to enhance testability (see A.4.8.2.2.2 and appendix D). To be usable for acceptance purposes, registration test coupons shall relate the actual grid location of each circuitry layer to all other circuitry layers and to the hole pattern accuracy required (see A.3.5.4) in each printed wiring board.

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A.3.7.3 Chemical requirements.

A.3.7.3.1 Cleanliness. When printed wiring boards are tested in accordance with [A.4.8.3.1](#), the levels of cleanliness shall be in accordance with the requirements of A.3.7.3.1.1 or A.3.7.3.1.2, as applicable.

A.3.7.3.1.1 Prior to the application of solder resist (see [A.6.5](#)). Unless otherwise specified, prior to the application of solder resist, the level of ionic contamination shall not exceed 10.06 micrograms/square inch (1.56 micrograms/square centimeter). The sodium chloride salt equivalent ionic contamination test equipment specified in [A.6.5.2](#) may be used in lieu of the method specified in [A.4.8.3.1](#). When printed wiring boards are tested using the sodium chloride salt equivalent ionic contamination test equipment specified in [A.6.5.2](#), the final value shall be less than equivalents of sodium chloride specified for the printed wiring board surface area tested.

A.3.7.3.1.2 Completed printed wiring boards (when specified, see [A.3.1.1](#) and [A.6.2.2.g](#)). The levels of cleanliness for completed printed wiring boards shall be as specified.

A.3.7.3.2 Resistance to solvents (marking inks or paints). After marking is tested in accordance with [A.4.8.3.2](#), any specified markings which are missing in whole or in part, faded, smeared, or shifted (dislodged) to the extent that they cannot be readily identified shall constitute failure.

A.3.7.4 Physical requirements.

A.3.7.4.1 Bow and twist (stiffener sections). When tested as specified in [A.4.8.4.1](#), the maximum allowable bow and twist for rigid or stiffener sections of the printed wiring board shall be 0.75 percent for designs that use surface mount components and 1.5 percent for all other designs, unless otherwise specified (see [A.3.1.1](#)).

A.3.7.4.2 Conductor edge outgrowth.

A.3.7.4.2.1 Solder covered conductors. When the printed wiring board test specimen is examined as specified in [A.4.8.1](#), there shall be no outgrowth of the solder coating on the conductor edges.

A.3.7.4.2.2 Conductors covered with metals other than solder. After undergoing the test as specified in [A.4.8.4.2](#), the printed wiring board test specimen shall be examined as specified in [A.4.8.1](#) and the maximum permissible outgrowth on conductors shall be .001 inch (0.03 mm).

A.3.7.4.3 Flexibility endurance (class B only). When tested as specified in [A.4.8.4.3](#), printed wiring board test specimen shall be capable of withstanding the specified conditions of A.3.7.4.3.1 or [A.3.7.4.3.2](#), as applicable, without any evidence of damage, degradation or rejectable delamination. After the test, the requirements specified in [A.3.5.3.2](#), [A.3.7.5.1](#) and [A.3.7.5.2](#) shall be met.

A.3.7.4.3.1 Qualification and periodic testing. Printed wiring board test specimen shall be capable of withstanding 100,000 cycles without any evidence of damage, degradation or rejectable delamination. The following details and exceptions shall apply:

- a. The printed wiring board test specimens shall be in accordance with [table II](#) or [VI](#), as applicable.
- b. Number of printed wiring board test specimens to be tested: One.
- c. Number of flex cycles: 100,000 cycles.
- d. Mandrel size (when applicable): The mandrel size for types 1 and 2 shall be 12 times the sum of the total ply thickness reduced to the nearest .125 inch (3.18 mm). The mandrel size for types 3, 4, and 5 shall be 24 times the sum of the total ply thickness reduced to the nearest .125 inch (3.18 mm). The mandrel shall not be less than .125 inch (3.18 mm).

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A.3.7.4.3.2 User specified (see A.3.1.1 and A.6.2.2). The number of flexing cycles, flexing rate, and points of application of the flexing, travel of loop (if other than one inch (25.4 mm) minimum), and diameter of mandrel (when applicable) shall be specified on the master drawing. If no parameters are specified on the master drawing, use the qualification and lot acceptance test default values of A.3.7.4.3.1.

A.3.7.4.4 Folding flexibility (class A only). When tested as specified in A.4.8.4.4, printed wiring board test specimen shall be capable of withstanding the specified conditions of A.3.7.4.4.1 or A.3.7.4.4.2, as applicable, without any evidence of damage, degradation or rejectable delamination. After the test, the electrical requirements specified in A.3.7.5.1 and A.3.7.5.2 shall be met.

A.3.7.4.4.1 Qualification and periodic testing. Two printed wiring board test specimens shall be tested. The number of fold cycles shall be 25 cycles in both directions. The point of application shall be the center of the test specimen, orthogonal to the longest length. The mandrel size for types 1 and 2 shall be 12 times the sum of the total ply thickness reduced to the nearest .125 inch (3.18 mm). The mandrel size for types 3, 4, and 5 shall be 24 times the sum of the total ply thickness reduced to the nearest .125 (3.18 mm). The mandrel shall not be less than .125 inch (3.18 mm).

A.3.7.4.4.2 User specified (see A.3.1.1 and A.6.2.2). The folding flexibility test parameters shall be as specified on the master drawing. The minimum parameters specified on the master drawing shall be as follows:

- a. Direction of bend.
- b. Degree of bend.
- c. Number of fold cycles.
- d. Diameter of mandrel.
- e. Points of application.

A.3.7.4.5 Plating adhesion. When tested as specified in A.4.8.4.5, there shall be no plating particles or conductor patterns removed from the printed wiring board test specimen except for outgrowth.

A.3.7.4.6 Rework simulation. Rework simulation is not applicable for printed wiring board designs that do not use any plated through-holes for component attachment.

A.3.7.4.6.1 Types 1 and 5 with unsupported holes (bond strength). After undergoing the test specified in A.4.8.4.6.1, the unsupported land shall withstand 5 pounds (2.27 Kg) pull or 500 lb/in (3.4 MPa), whichever is less.

A.3.7.4.6.2 Types 2, 3 and 4 with plated-through holes. After undergoing the test specified in A.4.8.4.6.2, the type 2, 3 or 4 printed wiring board test specimens shall meet the following requirements:

- a. External visual and dimensional inspection: When inspected as specified in A.4.8.1, there shall be no evidence of blistering or delamination in excess of that allowed in A.3.5.
- b. Internal visual and dimensional inspection: The printed wiring board test specimen is microsectioned and inspected in accordance with A.4.8.2, the requirements specified in A.3.6 through A.3.6.14 shall be met.

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A.3.7.4.7 Solderability. Solderability testing is applicable only on printed wiring board designs that require soldering during circuit card assembly processes. Printed wiring board designs that use compliant pin technology only for component attachment do not require solderability testing. Printed wiring board designs that use surface mount components only shall be tested for surface solderability as specified in A.3.7.4.7.2.

A.3.7.4.7.1 Hole (plated through hole) solderability. After undergoing the test specified in A.4.8.4.7.1, the printed wiring board test specimen shall conform to the accept/reject criterion (good wetting, pinholes, dewetting, non-wetting, etc.) specified in J-STD-003 class 3 or [appendix E](#), as applicable.

A.3.7.4.7.2 Surface (or surface mount land) solderability. After undergoing the test specified in A.4.8.4.7.2, the printed wiring board test specimen shall conform to the accept/reject criterion (good wetting, pinholes, dewetting, non-wetting, etc.) specified in J-STD-003 class 3 or [appendix E](#), as applicable.

A.3.7.4.8 Solder resist cure and adhesion. When tested as specified in A.4.8.4.8, the cured solder resist coating shall not exhibit tackiness, blistering, or delamination and the maximum percentage of cured solder resist lifted from the surface of the base material, conductors, and lands of the coated printed wiring board test specimen shall be in accordance with the following:

- a. Bare copper or base material: Maximum percentage of lifting 0 percent.
- b. Gold or nickel plating: Maximum percentage of lifting 5 percent.
- c. Tin-lead plating or solder coating: Maximum percentage of lifting 10 percent.

A.3.7.4.9 Surface peel strength (types 3 and 4 foil laminated printed wiring boards). When tested as specified in A.4.8.4.9, the surface conductor shall withstand a minimum peel strength greater than or equal to the "after thermal stress" values for the corresponding copper foil type, profile and weight specified by the base material specification. Unless otherwise specified (see A.3.1.1), the peel strength values for base material thicknesses over .0197 inch (0.050 mm) specified by the base material specification shall be used. This requirement is only applicable to foil laminated types 3 and 4 printed wiring boards that have surface conductors or surface mount lands. Printed wiring boards with no external circuitry (external terminal land or pads only) do not require peel strength testing.

A.3.7.4.10 Thermal stress.

A.3.7.4.10.1 Types 1 and 5. After undergoing the test specified in A.4.8.4.10, the printed wiring board test specimen shall be inspected in accordance with A.4.8.1 and shall not exhibit any cracking or separation of plating and conductors, blistering or delamination shall not exceed the limits allowed in A.3.5.1.3 and lands shall not lift in excess of that allowed in A.3.5.5.

A.3.7.4.10.2 Types 2, 3 and 4. After undergoing the test specified in A.4.8.4.10, the printed wiring board test specimen shall be examined in accordance with A.4.8.1 and shall exhibit no blistering or delamination in excess of that allowed in A.3.5.1.3. After meeting the visual and dimensional requirements of A.3.5, the printed wiring board test specimen shall be microsectioned and inspected in accordance with A.4.8.2 and shall meet the requirements of A.3.6 through A.3.6.14.

A.3.7.4.11 Coverlayer adhesion. When tested as specified in A.4.8.4.11, the maximum percentage of cured coverlayer lifted from the conductors, lands, or surface of the printed wiring board test specimen shall be in accordance with the following:

- a. Bare copper or base material: Maximum percentage of lifting 0 percent.
- b. Gold or nickel plating: Maximum percentage of lifting 5 percent.
- c. Tin-lead plating or solder coating (melting metals): Maximum percentage of lifting 10 percent.

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A.3.7.5 Electrical requirements.

A.3.7.5.1 Circuit continuity. The circuit continuity test shall be in accordance with A.4.8.5.1. For qualification inspection there shall be no open circuits whose resistance exceeds 5 ohms. For production testing, there shall be no open circuit whose resistance exceeds 10 ohms. For referee purposes, 0.5 ohm maximum per inch of circuit length shall apply.

A.3.7.5.2 Circuit shorts. When tested as specified in A.4.8.5.2, the resistance between mutually isolated conductors shall be greater than 10 megohms.

A.3.7.5.3 Dielectric withstanding voltage (DWV). When inspected as specified in A.4.8.5.3, there shall be no flashover, sparkover, or breakdown.

A.3.7.5.4 Heat sinking planes. When metal core printed wiring boards are inspected as specified in A.4.8.5.2, the dielectric material used to insulate the heat-sinking plane from circuitry and plated through holes shall provide an insulation resistance greater than 2 megohm. There shall be no flashover, sparkover, or dielectric breakdown.

A.3.7.6 Environmental requirements.

A.3.7.6.1 Moisture and insulation resistance (MIR). When tested as specified in A.4.8.6.1, the printed wiring board test specimen shall have a minimum of 500 megohms of resistance between conductors. After the test, the printed wiring board test specimen shall be inspected in accordance with A.4.8.1 and the specimen shall not exhibit blistering, measing, or delamination in excess of that allowed in A.3.5.1.3.

A.3.7.6.2 Thermal shock. While undergoing the test specified in A.4.8.6.2, a resistance change of 10 percent or more between the first and last high temperature measurements shall be considered a reject. After the test, the printed wiring board test specimens shall meet the following requirements:

- a. External visual and dimensional inspection (all types): When inspected as specified in A.4.8.1, there shall be no evidence of plating cracks, blistering, or delamination in excess of that allowed in A.3.5.1.3.
- b. Internal visual and dimensional inspection (types 3 and 4): When the printed wiring board test specimen is microsectioned and inspected in accordance with A.4.8.2, the requirements specified in A.3.6 shall be met.

A.3.8 Marking. Unless otherwise specified (see A.6.2), each production printed wiring board, each qualification test specimen, and each set of quality conformance test circuit strips (as opposed to each individual test coupon) shall be marked as specified (see A.3.1.1) and herein. As a minimum, each production printed wiring board, qualification test specimen, or quality conformance test circuit strip shall reference the printed wiring board manufacturers' CAGE (Commercial and Government Entity), lot date, and printed wiring board traceability code. The marking shall be produced by the same process used in producing the conductive pattern; or by the use of a nonconductive, fungistatic ink or paint applied to the printed wiring board or to a label which is applied to the printed wiring board; or by mechanical pencil marking on a metallic area provided for marking purposes may also be used. All marking shall be able to withstand solder fluxes, cleaning solutions, and molten solder encountered in the manufacture of printed wiring boards, shall remain legible after all tests, and in no manner affect printed wiring board performance.

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A.3.9 Traceability. Unless otherwise specified, traceability shall be available for review by the qualifying or contracting activity for a minimum of 3 years after delivery of the printed wiring boards. Lost or inadequate supporting data, test coupons, and microsection mounts may result in loss of qualification.

A.3.9.1 Quality conformance test circuitry (QCTC) and test coupons. Each quality conformance test circuitry shall be identifiable with those corresponding production printed wiring boards produced on the same panel that also produced the QCTC. All individual test coupons separated from its QCTC or qualification test specimen shall have its traceability maintained back to the QCTC or qualification test specimen from which the test coupons were separated.

A.3.9.2 Printed board materials. Traceability shall be such that for each printed wiring board, all printed board materials specified or used shall be traceable to a material production lot, inspection lot, or other specified grouping.

A.3.10 Repair. When inspected in accordance with [A.4.8.1](#), printed wiring boards shall not reveal any evidence of repair.

A.3.11 Workmanship. Printed wiring boards shall be processed in such a manner as to be uniform in quality and shall be free of defects in excess of those allowed in this appendix that could affect life or serviceability.

A.4. VERIFICATION

A.4.1 Classification of inspections. The inspections requirements specified herein are classified as follows:

- a. Qualification inspection (see [A.4.5](#)).
- b. Inspection of product for delivery (see [A.4.6](#)).
- c. Periodic conformance inspection (see [A.4.7](#)).

A.4.2 Test and measuring equipment. Measuring and test equipment of sufficient accuracy, quality, and quantity to permit performance of the required inspection shall be established and maintained by the manufacturer. The establishment and maintenance of a calibration system to control the accuracy of the measuring and test equipment shall be in accordance with section [C.5](#) of [appendix C](#), or equivalent.

A.4.3 Inspection conditions. Unless otherwise specified in the applicable test method or procedure, inspections and tests may be performed at ambient conditions.

A.4.4 Printed wiring board performance verification. Printed wiring board performance verification shall consist of inspections on the production printed wiring boards and the QCTC or test coupons referenced in tables herein for in-process, groups A, B, and C inspections. Selection of test coupons for testing shall be in accordance with the applicable inspection table. Each production printed wiring board or panel of printed wiring boards shall include sufficient test coupons to complete the applicable verification requirements specified. The design of test coupons shall be as specified on the applicable master drawing (see [A.3.1.1](#)). The minimum number of test coupons on the production panel and the requirements for positioning the test coupons on the panel shall be in accordance with the requirements of the applicable design standard (see [A.3.1.1](#) and [appendix D](#)).

A.4.5 Qualification inspection (see [A.6.3](#)). Qualification inspection shall be performed at the manufacturing location and a laboratory acceptable to the Government on sample qualification test specimens produced with equipment and procedures normally used in production.

A.4.5.1 Qualification eligibility. The fabrication of the qualification test vehicles may begin before authorization to test is granted, however before the start of qualification testing, the manufacturer shall receive authorization from the qualifying activity.

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A.4.5.2 Samples.

A.4.5.2.1 Qualification test specimens. Qualification test specimens shall conform to the following for the type of printed wiring boards for which qualification is sought:

- a. Type 1: The qualification test specimens for type 1 shall meet the requirements specified on [DSCC Form 19W](#) and the hole locations and conductor patterns of master drawing [IPC-100041](#).
- b. Type 2: The qualification test specimens for type 2 shall meet the requirements specified on [DSCC Form 19W](#) and the hole locations and conductor patterns of master drawing [IPC-100042](#).
- c. Types 3 and 4: The qualification test specimens for types 3 and 4 shall meet the requirements specified on [DSCC Form 19W](#) and the hole locations and conductor patterns of master drawing [IPC-100043](#). In addition, samples conforming to A.4.5.2.1.e shall be supplied for [class B](#) flexibility class coverage.
- d. Type 5: The qualification test specimens for type 5 shall meet the requirements specified on [DSCC Form 19W](#) and the hole locations and conductor patterns of master drawing [IPC-100044](#).
- e. Class B: When qualifying for types 3 or 4 (normally [class A](#)), one type 1 or type 2 qualification test specimen shall also be submitted at the same time.

If design defaults are not listed on [DSCC Form 19W](#), then the values specified in [IPC-2221](#) shall apply. See modification to the requirements of [IPC-100041](#), [IPC-100042](#), [IPC-100043](#), and [IPC-100044](#) specified in A.4.5.2.1.1.

A.4.5.2.1.1 Modifications to qualification test specimens. All portions of zones A, B, C (except for the external conductor traces on test coupon E-5), and D of the test pattern are now required for qualification testing. Zone D shall be used only in the manufacturer test routine detailed in [A.4.5.3.1](#). Other changes to the design or requirements of the qualification test specimens are detailed on the authorization to test form, [DSCC Form 19W](#), available from the qualifying activity. Requests for other modifications to the qualification test specimens shall be made prior to, or at the time of, the request for qualification testing.

A.4.5.2.2 Sample size. For types 1, 2, and 5, a sample of at least four qualification test specimens shall be produced by the manufacturer. For types 3 and 4, a sample of at least four qualification test specimens, plus one type 1 or 2 qualification test specimen shall be produced by the manufacturer. Unless otherwise specified on the qualifying activity approved authorization, the qualification test specimens shall be serialized and comply with the identification marking requirements of [A.3.8](#).

A.4.5.3 Inspection routines. Qualification inspection shall consist of the tests and inspections specified below. The following details shall apply:

- a. At least four qualification test specimens (zones A, B, C, and D) shall be tested by the manufacturer in accordance with [A.4.5.3.1](#).
- b. Two of the partial qualification test specimens (zones A, B, and C) that passed the tests specified in [A.4.5.3.1](#) shall then be destructively tested at a certified suitable laboratory (see [A.6.6](#)) in accordance with [A.4.5.3.2](#).
- c. The two remaining partial qualification test specimens not subjected to destructive testing at a certified suitable laboratory shall be retained as reference samples by the manufacturer for a period of 12 months.

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A.4.5.3.1 Manufacturer test routine (MTR). The manufacturer shall perform the inspections specified in the MTR column of [table II](#). Non-destructive inspections shall be performed on zones A, B, and C on all of the completed qualification test specimens in the lot. Destructive testing and microsection inspections shall be performed on test coupons from zone D. Further details concerning test coupons selection can be found in the application for qualification available from the qualifying activity.

A.4.5.3.2 Certified suitable laboratory test routine (CTR). The certified suitable laboratory shall subject two of the partial qualification test specimens (zones A, B, and C) to the inspections specified in the CTR column of [table II](#). The order of the inspections and tests is optional; however, the cleanliness test shall be performed first and the DWV test shall be performed after MIR inspection.

A.4.5.3.3 Contract services. Manufacturers wanting to use an external subcontracted service for production of printed wiring board shall first qualify using their own equipment/processes internal to their facility. Once qualified internally, a manufacturer may qualify using the subcontracted service. This additional subcontracted qualification will not be listed separately on the QPL. The subcontract service shall not be extended to another external subcontracted service or manufacturer.

NOTE: For the purposes of this appendix, the internal equipment/process condition applies only to those processes used to manufacture the qualification test specimen. When applying for qualification of sub-contracted services, the process and the company performing the sub-contracted service shall be identified. If the manufacturer has no internal capability to perform a certain production step (either used during qualification or only used during production) this shall be identified on the application for authorization to test. If the sub-contracted service is changed, the manufacturer shall requalify.

A.4.5.3.4 Qualification rejection. Qualification approval will not be granted if any of the qualification test specimens tested in accordance with [table II](#) fail to meet the specified requirements.

A.4.5.4 Extent of qualification.

A.4.5.4.1 Printed wiring board type. Qualification of a particular printed wiring board type shall be extended to cover all conductor patterns of that same printed wiring board type produced.

- a. Qualification of type 4 printed wiring boards shall be extended to cover all other types (5, 3, 2, and 1).
- b. Qualification of type 3 printed wiring boards shall be extended to cover types 1 and 2 printed wiring boards.
- c. Qualification of type 2 printed wiring boards shall be extended to cover type 1 printed wiring boards.
- d. Qualification of type 5 printed wiring boards shall be extended to cover type 1 printed wiring boards.
- e. Qualification of any type shall be extended to cover the approved type or types with a stiffener or solder resist.

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TABLE II. Qualification inspection.

| Inspection | Requirement paragraph | Method paragraph | Test specimen <u>1/</u> | | Notes |
|------------------------------------|-----------------------|------------------|-------------------------|-------------------|--------------|
| | | | MTR | CTR | |
| <u>Visual and dimensional:</u> | | | | | |
| Acceptability | A.3.7.1 | A.4.8.1 | PWB | PWB | <u>2/</u> |
| <u>Microsection:</u> | | | | | |
| As received | A.3.7.2.1 | A.4.8.2 | AB-12 | A-3 | |
| Registration (method II) | A.3.7.2.2 | A.4.8.2.2 | <u>3/</u> | <u>3/</u> | |
| <u>Chemical:</u> | | | | | |
| Cleanliness | A.3.7.3.1 | A.4.8.3.1 | PWB | PWB | |
| Resistance to solvents | A.3.7.3.2 | A.4.8.3.2 | <u>4/ 5/</u> | <u>4/</u> | |
| <u>Physical:</u> | | | | | |
| Bow and twist | A.3.7.4.1 | A.4.8.4.1 | PWB | PWB | <u>2/ 6/</u> |
| Flexibility endurance | A.3.7.4.3 | A.4.8.4.3 | | H-1 | <u>7/</u> |
| Folding flexibility | A.3.7.4.4 | A.4.8.4.4 | | H-2 | |
| Plating adhesion | A.3.7.4.5 | A.4.8.4.5 | J-1 & J-2 | C-1, C-4, and C-5 | |
| Rework simulation | A.3.7.4.6 | A.4.8.4.6 | | B-2 | |
| Solderability | | | | | |
| Hole | A.3.7.4.7.1 | A.4.8.4.7.1 | AB-10 | A-4 and B-4 | <u>8/</u> |
| Surface | A.3.7.4.7.2 | A.4.8.4.7.2 | AB-7 | D-2 and D-6 | <u>9/</u> |
| Thermal stress | A.3.7.4.10 | A.4.8.4.10 | AB-8 and AB-13 | A-1 and B-6 | <u>10/</u> |
| Surface peel strength | A.3.7.4.9 | A.4.8.4.9 | | P | <u>11/</u> |
| <u>Electrical:</u> | | | | | |
| Circuit continuity | A.3.7.5.1 | A.4.8.5.1 | H-1, -2, and -3 | D-3 | <u>12/</u> |
| Circuit shorts | A.3.7.5.2 | A.4.8.5.2 | H-1, -2, and -3 | E-3 | |
| Dielectric withstanding voltage | A.3.7.5.3 | A.4.8.5.3 | | E-1 | <u>13/</u> |
| <u>Environmental:</u> | | | | | |
| Moisture and insulation resistance | A.3.7.6.1 | A.4.8.6.1 | | E-1 | <u>13/</u> |
| Thermal shock | A.3.7.6.2 | A.4.8.6.2 | | D-3 | |

- 1/ See A.4.5.2.1 for qualification test specimen description. MTR designates manufacturer's test routine and CTR designates the certified test laboratories test routine. For column MTR, when a test coupon is referenced (e.g. AB-10), only one of the two coupons (9 of 18 available holes) shall be inspected, whereas for column CTR, when an individual test coupon designation is referenced (e.g. D-3) means inspect the specified test coupon. See qualification test specimen master drawing for test coupon design.
- 2/ The reference "PWB" in a column means inspect all features, holes, and patterns in zones A, B, and C of a qualification test specimen with the exception that conductor spacing and width on test coupon E-5 shall not be evaluated in zone C.
- 3/ Type 3 and 4 only. See A.4.8.2.2 for registration sample units and microsectioning details. Test coupons AB-8 and AB-13 (column MTR) or A-1 and B-6 (column CTR) can be used to meet the diagonal corner requirement.
- 4/ The minimum number of samples shall be at least one sample for each solution specified by the applicable test method (i.e., one sample for each solution required).
- 5/ Required only if the manufacturer has the capability to perform this test during group A inspection (see A.4.8.3.2.1).
- 6/ Bow and twist shall be evaluated on rigidized section or stiffener portions only.

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TABLE II. Qualification inspection – Continued.

- 7/ Flexibility endurance shall be performed on a type 1 specimen.
- 8/ Test coupons AB-10 (36 holes from four specimens) shall be used for the MTR routine; test coupons A-4 and B-4 (36 holes from two specimens) shall be used for the CTR routine.
- 9/ Type 1 and type 5 only.
- 10/ Use coupon closest to the corner on MTR routine. One of the test coupons shall be microsectioned in the qualification test specimen's length direction and the other shall be microsectioned along the qualification test specimen's width direction.
- 11/ Peel strength testing is only required for qualification when the manufacturer uses foil lamination on the outer layers. See [A.4.8.4.9.1](#) for test coupon design.
- 12/ When circuit continuity verification is performed manually, the current shall not be in excess of 1.5 amperes and the time of application shall not exceed 30 seconds.
- 13/ The DWV test shall be performed after the MIR test.

A.4.5.4.2 Classes. Qualification to flexibility [class B](#) shall be extended to cover flexibility [class A](#).

A.4.5.4.3 Base material types.

A.4.5.4.3.1 Flexible base material types. Qualification of any type of flexible base material type shall be extended to cover all flexible base material types. Qualification with a metal cladding adhesion method (adhesive/adhesiveless) shall be as follows:

- a. Adhesive family include all base materials that rely/use an adhesive to hold the metal to both sides of the dielectric. Note "cast" materials are considered to be in the adhesiveless family.
- b. Adhesiveless family includes all base materials that use other techniques (such as chemically deposited or vapor deposition) to adhere the basis metal to both sides of the dielectric.

A.4.5.4.3.2 Rigid base material types. Qualification with a rigid base laminate material shall be as follows:

- a. Qualification with thermosetting resin (see IPC-T-50 and [A.6.4.6.1](#)) base material types shall be extended to cover all other types of thermosetting resin base materials.
- b. Qualification with thermoplastic resin (see IPC-T-50 and [A.6.4.6.2](#)) base material types shall be extended to cover all other types of thermoplastic resin base materials.

A.4.5.4.4 Stiffeners and solder resist. Qualification of any printed wiring board type shall be extended to cover the approved type with a stiffener or solder resist.

A.4.5.4.5 Mass lamination (see [A.6.4.4.1](#)). Qualification of a contract lamination (four conductor layers) shall be extended to cover a contract lamination of three conductor layers. Qualification of a contract lamination (ten conductor layers) shall be extended to cover a contract lamination of three or more conductor layers. NOTE: Qualification test specimens for four layer contract lamination shall meet the requirements specified in [A.4.5.2.1.d](#). Qualification test specimens for ten layer contract lamination shall meet the requirements specified in [A.4.5.2.1.c](#).

A.4.5.4.6 Processes.

A.4.5.4.6.1 Etchback. Qualification using etchback shall be extended to cover non-etchback.

A.4.5.4.6.2 Process changes. Any changes to a manufacturers qualified base material type, equipment, or processes shall be reviewed by the qualifying activity for determination if partial or full requalification is necessary.

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A.4.5.5 Retention of qualification. To retain qualification, the manufacturer shall make available to the qualifying activity data concerning production of qualified product at 12 month intervals. The qualifying activity shall establish the initial reporting date. The retention of qualification data shall consist of:

- a. A summary of the results of the tests performed for inspection of product delivery (in-process and group A) indicating as a minimum the number of lots that have passed and the number of lots that have failed. The results of tests of all reworked lots shall be identified and accounted for.
- b. A summary of the results of tests performed for groups B and C inspection performed and completed during the 12 month period.
- c. The actual test data for group A, B, or C or all shall be supplied to the qualifying activity upon request.
- d. The extent of qualification specified in [A.4.5.4](#) shall apply.
- e. Group B is performed each month, only for those months in which production occurred.
- f. To retain qualification, the manufacturer shall requalify every 36 months from the date of initial qualification.
- g. In the event that no production occurred during the 12 month period, the manufacturer shall either requalify or certify that it still has the capabilities and facilities necessary to produce and test the qualified product.

Failure to communicate with the qualifying activity within 60 days after the end of the 12 month period may result in loss of qualification. In addition, the manufacturer shall immediately notify the qualifying activity at any time during the 12 month period that the inspection data indicates failure of the qualified product to meet the performance requirements of this appendix.

A.4.5.5.1 Requalification (see [A.6.3.2](#)). Qualifications expire 36 months from the date of initial qualification. In order to maintain a QPL listing, manufacturers shall complete requalification before the end of its current 36 month qualification.

A.4.5.5.2 Product assurance information. The manufacturer shall make available to qualifying activity an approved quality manual or procedures that as a minimum addresses the following information:

- a. In-process and group A verification procedures.
- b. Test coupon quantity, design, placement and usage procedures.
- c. The definition of complexity used to select samples for group B verification testing.

A.4.6 Inspection of product for delivery. Inspection of product for delivery shall consist of in-process and group A inspection. Except as specified in [A.4.7.1.4](#), delivery of printed wiring boards which have passed in-process and group A inspection shall not be delayed pending the results of the periodic inspection. Anomalies or defects noted on sample printed wiring boards or test coupons (or both) defined herein shall be recorded and the proper corrective action shall be initiated. Manufacturers that are qualified to use subcontract services are still responsible for in-process and group A inspections and shall be subject to loss of qualification if the results of in-process and group A inspections indicate failure of the product to meet the applicable requirements.

A.4.6.1 In-process inspection. Each inspection lot of printed wiring boards or panels, as applicable shall be inspected in accordance with [table III](#), as applicable. When permanent solder resist is specified (see [A.3.1.1](#)), the in-process inspections specified in subgroups 1, 2 and 3 of [table III](#) shall be performed prior to solder resist application. Prior to lamination of type 3 or 4 printed wiring boards, the in-process inspections specified in subgroup 2 of [table III](#) shall be performed.

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A.4.6.1.1 Inspection lot.

A.4.6.1.1.1 Subgroup 1. An inspection lot shall correspond to each production lot or each change of shift of work force, whichever occurs first. Production lots may be grouped based on same materials, same type or types of interfacial connections and terminations, and same processing requirements.

A.4.6.1.1.2 Subgroups 2 and 3. An inspection lot shall consist of the number of printed wiring boards fabricated from the same materials, using the same processing procedures, produced under the same conditions within a maximum period of 1 month and offered for inspection at one time.

A.4.6.1.2 Sample size. The number of printed wiring boards or panels to be selected from each inspection lot shall be in accordance with [table III](#).

A.4.6.1.3 Rejected lots. If an inspection lot is rejected as a result of a failure to pass the subgroup 1 tests specified, the manufacturer shall withdraw the lot, take corrective action in connection with the cleaning materials and procedures, reclean the lot prior to application of permanent solder resist coating, and resubmit the lot for inspection. Printed wiring boards are not acceptable if the permanent solder resist coating has been applied to a contaminated surface. If an inspection lot is rejected for subgroup 2 or 3 tests, the manufacturer may screen (100 percent inspection) out the defective units (printed wiring boards or panels). Defective printed wiring boards shall not be shipped.

A.4.6.1.4 Materials inspection. Materials inspection shall consist of certification supported by verifying data that the materials used in fabricating the printed wiring boards are in accordance with the applicable referenced specifications or requirements specified (see [A.3.1.1](#)), prior to such fabrication. Unless otherwise specified (see [A.3.1.1](#)), verifying data need not be submitted to the qualifying activity or acquiring activity, but shall be made available upon request.

TABLE III. In-process inspection.

| Inspection | Requirement paragraph | Method paragraph | Sample size ^{1/} | Notes |
|----------------------|--|--|--|-----------------------------|
| Subgroup 1 | | | | |
| Material Cleanliness | A.3.4 A.3.7.3.1 | A.4.8.1 A.4.8.3.1 | See A.4.6.1.4 Plan BN or TL | ^{2/} |
| Subgroup 2 | | | | |
| Conductor spacing | A.3.5.2.2 | A.4.8.1 | Plan BH | ^{2/} ^{3/} |
| Conductor width | A.3.5.2.3 | A.4.8.1 | Plan BH | ^{2/} ^{3/} |
| Subgroup 3 | | | | |
| Plating adhesion | A.3.7.4.5 | A.4.8.4.5 | Plan BH | ^{2/} ^{4/} |

^{1/} See [appendix C, table VIII](#) for C = 0 sampling plans.

^{2/} Performed prior to solder resist application.

^{3/} Performed prior to lamination on each production lot.

^{4/} A non-reflowed test coupon prior to reflow may be required (see [A.6.2](#)).

A.4.6.2 Group A inspection. Group A inspection shall consist of the inspections specified in [table IV](#). The qualified manufacturer shall be responsible for completion of all group A inspections and shall be subject to loss of qualification for failure not to complete or to have completed all group A test and inspections.

APPENDIX A

A.4.6.2.1 Inspection lot. A group A inspection lot shall consist of the number of printed wiring boards fabricated from the same materials, using the same processing procedures, produced under the same conditions within a maximum period of 1 month and offered for inspection at one time.

A.4.6.2.2 Sampling procedures. Statistical sampling and inspection shall be in accordance with [appendix C](#). For 100 percent inspection, all rejected units (printed wiring boards or panels of printed wiring boards) shall not be supplied on the contract. The following details on panel/test coupon sampling shall apply:

- a. As received (see [A.3.7.2.1](#)):
 - (1) Types 1, 2, and 5: The number of test coupons to be microsectioned shall be based on a statistical sample of panels in the lot in accordance with [appendix C, table VIII](#), series L.
 - (2) Types 3 and 4: One test coupon "A" per panel shall be microsectioned and inspected (see A.4.6.2.2d). The orientation of the cross section shall be orthogonal to the "thermal stress" microsection.
- b. Solderability (see [A.3.7.4.7](#)):
 - (1) For Sequential Electrochemical Reduction Analysis (SERA), samples shall be selected in accordance with [appendix E](#).
 - (2) For J-STD-003 class 3: When using test coupon "S", the number of samples to be tested shall be based on a statistical sample of the number of panels in the lot in accordance with [appendix C, table VIII](#), series L. When using test coupon "A", the number of samples to be tested shall be based on the same statistical sample of test coupon "S", but a multiple of 4 shall be applied to the resulting sample size.
- c. Thermal stress (see [A.3.7.4.10](#)):
 - (1) Types 1, 2 and 5: The number of test coupons to be microsectioned shall be based on a statistical sample of panels in the lot in accordance with [appendix C, table VIII](#), series L.
 - (2) Types 3 and 4: A minimum of one B test coupon per panel shall be microsectioned and inspected. Additional B test coupons shall be microsectioned based on a statistical sample of panels in the lot in accordance with [appendix C, table VIII](#), series J. For designs with blind or buried vias, at least one additional test coupon "B" sample shall be thermal stressed in accordance with [A.4.8.4.10](#) and inspected to the requirements of [A.3.7.2](#) for each additional copper plating process used. See [A.6.12](#) for additional guidance.
- d. Registration (method II, types 3 or 4 only): When method II is to be used, registration shall be evaluated using any combination of two microsectioned test specimens taken from diagonal corners of the panel. Both test coupons shall have been microsectioned in the vertical plane with one test coupon representing the panel's length (X) direction and the other representing the panel's width (Y) direction. Test coupons from the 'as received' (see [A.3.7.2.1](#)), 'thermal stress' (see [A.3.7.4.10](#)) or when available, 'hole solderability' (see [A.3.7.4.7.1](#)) verifications may be used.

Note concerning the types 3 and 4 "as received" and "thermal stress" microsections. A minimum of two test coupons (one A and one B) per panel shall be microsectioned. One of the test coupon shall be microsectioned in the panel's length direction and the other shall be microsectioned along the panel's width direction. One of the test coupons shall represent the "as received" condition and the other the after "thermal stress" condition.

A.4.6.2.3 Rejected lots. If an inspection lot is rejected, the manufacturer may rework it to correct the defects and resubmit the lot for reinspection, or screen out the defective units (if possible). Resubmitted lots shall be inspected using tightened inspection (see [appendix C](#)). Such lots (reworked or screened) shall be clearly identified as reinspected lots. Products which have failed any group A inspection and have not been reworked and have not passed reinspection (as specified in this appendix) may not be delivered as compliant printed wiring boards.

APPENDIX A

A.4.6.2.4 Disposition of sample units. Sample printed wiring boards which have passed all of group A inspection may be delivered if the inspection lot is accepted.

TABLE IV. Group A inspection.

| Inspection | Requirement paragraph | Method paragraph | Test specimen ^{1/} | | | | | Sample plans ^{2/} |
|--|------------------------|----------------------|-----------------------------|------------------|-----------|------------|-----------|--|
| | | | T1 | T2 | T3 | T4 | T5 | |
| <u>Visual and dimensional</u> | | | | | | | | |
| Acceptability Registration (method I) | A.3.7.1 A.3.5.6 | A.4.8.1 A.4.8.1.2 | PWB <u>5/</u> | PWB <u>5/</u> | PWB | PWB | PWB | Plan BH <u>3/</u> <u>4/</u> Plan TJ see <u>6/</u> |
| <u>Microsection</u> | | | | | | | | |
| As received Registration (method II) | A.3.7.2.1 A.3.7.2.2 | A.4.8.2 A.4.8.2.2 | | B | B | A A - B | | See <u>6/</u> See <u>6/</u> and <u>7/</u> |
| <u>Chemical</u> | | | | | | | | |
| Resistance to solvents | A.3.7.3.2 | A.4.8.3.2 | <u>8/</u> | <u>8/</u> | <u>8/</u> | <u>8/</u> | <u>8/</u> | See <u>8/</u> |
| <u>Physical</u> | | | | | | | | |
| Bow and twist | A.3.7.4.1 | A.4.8.4.1 | PWB | PWB | PWB | PWB | PWB | Plan BH <u>9/</u> |
| Conductor edge outgrowth | A.3.7.4.2 | A.4.8.4.2 | PWB | PWB | PWB | PWB | PWB | Plan BH |
| Plating adhesion | A.3.7.4.5 | A.4.8.4.5 | <u>10/</u> | C | C | C | C | Plan BH/TJ <u>3/</u> <u>7/</u> |
| Solderability | | | | | | | | |
| Hole | A.3.7.4.7.1 | A.4.8.4.7.1 | | A - S | A - S | A - S | | See <u>6/</u> <u>11/</u> <u>12/</u> |
| Surface | A.3.7.4.7.2 | A.4.8.4.7.2 | <u>10/</u> | C | C | C | | Plan BH/TJ <u>6/</u> <u>10/</u> |
| Solder resist cure and adhesion | A.3.7.4.8 | A.4.8.4.8 | | | G | G | G | Plan TJ |
| Thermal stress | A.3.7.4.10 | A.4.8.4.10 | | B | B | B | | See <u>6/</u> |
| <u>Electrical</u> | | | | | | | | |
| Circuit continuity | A.3.7.5.1 | A.4.8.5.1 | X | | PWB | PWB | | 100 percent <u>13/</u> |
| Circuit shorts | A.3.7.5.2 | A.4.8.5.2 | X | | PWB | PWB | | 100 percent <u>13/</u> |

^{1/} T1 designates a type 1 design; T2 designates a type 2 design; T3 designates a types 3 design; T4 designates a type 4 design and T5 designates a type 5 design; PWB means inspect the entire production printed wiring board, whereas an individual test coupon designation means inspect the specified test coupon. See [appendix D](#) herein for test coupon identification (name) translation to the applicable design standard.

^{2/} See [appendix C, table VIII](#) for C = 0 sampling plans and [C.4.5](#) for examples.

^{3/} Some attributes may need to be inspected prior to lamination or solder resist application.

^{4/} The solder resist thickness test can be performed on either a test coupon at a sampling of TJ or production printed wiring board at a sampling of BH, manufacturer's option.

^{5/} Test coupon or production printed wiring board, manufacturer's option.

^{6/} See [A.4.6.2.2](#) for sample size and test specimen description.

^{7/} An optional method of verifying registration using test coupons (method III) is available. See [A.4.8.2.2.2](#) for details.

^{8/} See [A.4.8.3.2.1](#) for test specimen description and sample size.

^{9/} Rigidized sections or stiffener portions only.

^{10/} Test coupon "C" or production printed wiring board.

^{11/} For printed wiring boards using only surface mount lands for component attachment, the surface solderability test can be used in lieu of the hole solderability test.

^{12/} A or S test coupon, manufacturers option.

^{13/} Types 3 and 4 printed wiring boards only. Note: It is assumed that both continuity and circuit shorts can be visually verified for types 1, 2, and 5. If continuity and circuit shorts cannot be verified using visual inspection, then the production PWBs shall be tested using a sample size in accordance with [appendix C, table VIII](#), series H.

APPENDIX A

A.4.7 Periodic conformance inspection. Periodic conformance inspection shall consist of groups B and C inspection. Except where these inspections show noncompliance with the applicable requirements (see A.4.7.1.4 and A.4.7.2.4), delivery of printed wiring boards which have passed in-process and group A inspection shall not be delayed pending the results of these periodic inspections. Periodic inspections shall be performed at a certified suitable laboratory (see A.6.6).

A.4.7.1 Group B inspection. Group B inspection shall consist of the inspections specified in table V.

A.4.7.1.1 Inspection lot. The sample units (test coupons) shall be randomly selected from the most complex (see A.6.4.2) inspection lot that has passed all in-process and group A inspections during that production month (i.e., the group B reporting period). The most complex printed wiring boards shall be as determined by the manufacturer using its definition of complex (see A.6.4.2), subject to approval by the qualifying activity.

A.4.7.1.2 Sampling procedures. Samples for each extent of qualification base material type family (see A.4.5.4.3) produced during that reporting period shall be subjected to group B inspection. Because of the performance nature of this document, the design details of the test coupons will need to be supplied with the sample units (see A.6.8).

A.4.7.1.2.1 Sample unit selection. Unless otherwise specified in A.4.8.3.2 (resistance to solvents) or A.4.8.4.9 (surface peel strength), the following criteria shall be used in selecting samples for group B testing:

- a. The sample units shall be from the most complex (see A.6.4.2) printed wiring board design produced that calendar month that allow for each test to be performed.
- b. The sample units shall be randomly selected from panels which have passed group A inspection during that calendar month.
- c. The sample units can be either:
 - (1) Two sets of quality conformance test circuitry, or
 - (2) Two test coupons for each test to be performed.

A.4.7.1.3 Frequency. The frequency of selecting sample units and performing group B testing shall be on a monthly basis. The sample units shall be submitted for testing within 30 calendar days after the end of each reporting period.

A.4.7.1.4 Failures. If one or more sample units fail to pass group B inspection, the sample shall be considered to have failed. The qualifying activity shall be notified of any group B failure within 3 business days. Group B inspection shall be repeated on additional sample units (either all group B inspections or just the group B inspection which the original sample failed, at the option of the qualifying activity) from the next most complex (see A.6.4.2) inspection lot from the same month that the failure occurred. Group A testing and shipment of the product represented by the failed group B sample shall be discontinued.

A.4.7.1.4.1 Corrective actions. Corrective actions shall be taken on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions (materials, processes, etc.), and which are considered subject to the same failure.

APPENDIX A

A.4.7.1.4.2 Noncompliance. If the lot or lots directly represented by the group B failure have been shipped, the manufacturer shall notify the acquiring activity of the failure and shall recall the affected lot or lots for reinspection, if possible. All other lots represented by extension of qualification by the failed group B sample are considered noncompliant until a sample from the next most complex (see A.6.4.2) inspection lot passes group B inspection.

A.4.7.1.4.3 Reinstitution of group A inspection. After successful completion of group B reinspection, group A inspection of product represented by the group B failure may be reinstated.

A.4.7.1.5 Disposition of sample units. Test coupons which have been subjected to group B shall be retained as specified in A.3.9.

TABLE V. Group B inspection.

| Inspection | Requirement paragraph | Method paragraph | Test coupon by type ^{1/} | | Notes |
|------------------------------------|-----------------------|------------------|-----------------------------------|--------|-------|
| | | | Types 1, 2, 3, and 5 | Type 4 | |
| <u>Subgroup 1</u> | | | | | |
| Resistance to solvents | A.3.7.3.2 | A.4.8.3.2 | 2/ | 2/ | 2/ |
| Rework simulation | A.3.7.4.6 | A.4.8.4.6 | 3/ | 3/ | 3/ |
| Moisture and insulation resistance | A.3.7.6.1 | A.4.8.6.1 | E | E | |
| Dielectric withstanding voltage | A.3.7.5.3 | A.4.8.5.3 | E | E | 4/ |
| <u>Subgroup 2</u> | | | | | |
| Surface peel strength | A.3.7.4.9 | A.4.8.4.9 | | P | 5/ |

^{1/} See 1.2, A.3.1.1, and A.6.4.6 herein.

^{2/} See A.4.8.3.2.1 for test specimen description and number of samples required.

^{3/} The holes to be tested and inspected shall represent component holes used for through-hole mounting.

^{4/} Dielectric withstanding voltage shall be performed after the moisture and insulation resistance test on the same test coupon subjected to the moisture and insulation resistance test.

^{5/} Test coupon P is detailed in A.4.8.4.9.1.

A.4.7.2 Group C inspection. Group C inspection shall consist of the inspections specified in table VI for flexibility classes (A and B).

A.4.7.2.1 Inspection lot. The sample units (test coupons or production printed boards) shall be randomly selected from the inspection lot that have passed all in-process and group A inspections during that reporting period.

A.4.7.2.2 Sampling procedures. The selection of sample units and testing shall be on an annual basis. Samples for each flexibility class (see 1.2.2) and each extent of qualification grouping based on the flexible base material type (see A.4.5.4.3.1) produced during that reporting period shall be subjected to group C inspection. If no printed wiring boards were produced during the reporting period, then group C inspection does not need to be performed.

Example: If both flexibility class A and class B printed wiring boards were produced of adhesive flexible metal clad base material family and only class A printed wiring boards were produced using adhesiveless flexible metal clad base material family, then testing would be as follows:

- a. Adhesive family: Both class A and class B verification tests (folding flexibility and flex endurance) would need to be performed.
- b. Adhesiveless family: Only class A verification test (folding flexibility) would need to be performed.

APPENDIX A

A.4.7.2.2.1 Sample unit selection. Unless otherwise specified, the following criteria shall be used in selecting samples for group C testing:

- a. The sample units shall be for each class of product produced during that reporting period. Note: If only class A printed wiring boards were produced during the reporting period, then only class A needs to be tested.
- b. The sample units shall be randomly selected from panels which have passed in-process and group A inspection during that inspection period.
- c. The sample units can be either:
 - (1) Two test coupons or sets of quality conformance test circuitry, or
 - (2) Two printed wiring boards for each test to be performed.

A.4.7.2.3 Frequency. The frequency of group C testing shall be annually. The sample units shall be submitted for testing within 30 calendar days after the end of each reporting period.

TABLE VI. Group C inspection.

| Inspection | Requirement paragraph | Method paragraph | Test specimen <u>1/</u> |
|---------------------------------|-----------------------|------------------|-------------------------|
| Flexibility endurance (class B) | A.3.7.4.3 | A.4.8.4.3 | PWB or <u>2/</u> |
| Folding flexibility (class A) | A.3.7.4.4 | A.4.8.4.4 | PWB or <u>3/</u> |

1/ See 1.2, 6.4.2, and A.3.1.1 herein.

2/ A suitable single-sided portion of a type 3, 4, or 5 printed wiring board or the test specimen described in the applicable test method.

3/ A suitable portion of a production printed wiring board or the test specimens described in A.4.8.4.4.1.

A.4.7.2.4 Noncompliance. If one or more sample units fail to pass group C inspection, the manufacturer shall notify the qualifying activity of such failure within 3 business days. The manufacturer shall take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials, processes, etc., and which are considered subject to the same failure. If the lot or lots directly represented by the group C failure have been shipped, the manufacturer shall notify the acquiring activity of the failure and shall recall the affected lot or lots for reinspection, if possible. All other lots represented by extension of qualification by the failed group C sample are considered noncompliant until a sample passes group C inspection. Group A inspection and shipment of the product shall be discontinued until corrective action, acceptable to the qualifying activity, has been taken. After the corrective action has been taken, group C inspection shall be repeated on additional sample units (all inspections, or the inspection which the original sample failed, at the option of the qualifying activity). Group A inspection may be reinstated; however, final acceptance and shipment shall be withheld until the group C inspection, has shown that the corrective action was successful.

A.4.7.2.5 Disposition of sample units. Test specimens which have been subjected to group C shall be retained as specified in A.3.9.

A.4.8 Methods of inspection. The following verification test methods described herein are proven methods and shall be the referee method in case of dispute.

APPENDIX A

A.4.8.1 Acceptability inspection. The visual and dimensional features of the printed wiring board test specimen shall be inspected using either an optical apparatus or aid which provides a minimum magnification of 1.75X (3 diopters) or by using automated inspection techniques. Referee inspection of the printed wiring board test specimen features shall be accomplished at a magnification of 10X.

A.4.8.1.1 Annular ring, external (see [A.3.5.2.1](#)). The measurement of the annular ring on external layers is from the inside surface (within the hole) of the plated hole or unsupported hole to the outer edge of the annular ring on the surface of the printed wiring board. See [IPC-TM-650, method 2.2.1](#) for illustration.

A.4.8.1.2 Registration (method I) (types 1 and 2) (see [A.3.5.6](#)). Layer-to-layer registration of type 1 and type 2 printed wiring boards shall be satisfied if the outer layers meet the external annular ring (see [A.3.1.1](#) and [A.3.5.2.1](#)) and hole pattern accuracy (see [A.3.1.1](#) and [A.3.5.4](#)) requirements.

A.4.8.1.3 Solder resist thickness (see [A.3.5.7](#)). Solder resist thickness shall be inspected by any micrometer or by microsection in accordance with A.4.8.2.

A.4.8.2 Microsection inspection. Microsection inspections (to evaluate characteristics such as plated-through holes, plating thickness, or foil thickness) shall be accomplished by using the preparation and inspection methods specified below.

- a. Microsection preparation. Microsection preparation shall be accomplished by using methods in accordance with either test method numbers [2.1.1](#) or [2.1.1.2](#) of [IPC-TM-650](#). Automatic microsectioning techniques may be used in lieu of test methods 2.1.1 or 2.1.1.2 of [IPC-TM-650](#). The following details shall apply:
 - (1) Number of holes per specimen. A minimum of three plated holes cross sectioned vertically shall be made for each test specimen required. Each side of the three plated holes shall be viewed independently.
 - (2) Accuracy. All three plated holes of each test specimen shall be sectioned, ground, and polished to within ± 10 percent of the center of the drilled diameter of the hole.
 - (3) Pre microetch evaluations. The test specimens shall be evaluated for plating separations, superfluous copper, and wicking prior to microetching.
 - (4) When more than two test specimens are contained in a mount (coupon-stacking or gang mounting), the following shall apply:
 - (a) The test specimens shall not be in direct contact with any other test specimen in the mount. The recommended minimum distance between test specimens in a mount is .010 inch (0.025 mm).
 - (b) The traceability requirements of [A.3.9.1](#) shall apply.
- b. Microsection examination and inspection. Microsection examination and inspection shall be accomplished in accordance with test method number [2.2.5](#) of [IPC-TM-650](#) to evaluate characteristics such as dielectric spacing, etchback, plating thickness, foil thickness, etc., in plated holes. If more than three plated holes are on a test specimen, all holes shall be evaluated. The following details shall apply:
 - (1) Magnifications. Unless otherwise specified in test method number [2.2.5](#) of [IPC-TM-650](#), the test specimens shall be inspected at a magnification of 100X ± 5 percent. Referee inspections shall be accomplished at a magnification of 200X ± 5 percent.
 - (2) Evaluations. Pre and post microetch evaluations for the criteria of [A.3.6](#) shall be accomplished at magnifications specified above. The test specimens shall be evaluated for plating separations, superfluous copper, and wicking both prior and after to microetching.

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A.4.8.2.1 Plated-through hole inspection (see [A.3.6](#)). When inspected in accordance with [A.4.8.2](#), the following details shall apply:

- a. Annular ring (internal) (see [A.3.6.1](#)). This measurement shall apply to all internal lands for all three holes.
- b. Dielectric layer thickness (see [A.3.6.3](#)). The dielectric layer thickness shall be inspected between all conductor layers present in the test specimen.
- c. Plating and coating thickness (see [A.3.6.8](#)). Isolated thick or thin sections shall not be used for averaging. However, isolated areas of reduced copper thickness shall be measured for compliance with the requirements of [A.3.6.8](#).
- d. Copper plating voids (see [A.3.6.8.2.1](#)). Any plated-through hole in the microsection failing the plating void criteria A.3.6.8.2.1 subparagraphs a, b or c, shall be cause for the entire panel of printed wiring boards associated with the microsection to be rejected. The following details apply if a single plating void is found:
 - (1) Type 2: If the plating void does not exceed the conditions of [A.3.6.8.2.1](#), the entire lot (100 percent panel inspection) shall be microsectioned and inspected for voids. If a plating void is present on any panel, a referee microsection shall be performed using an A or B test coupon from the opposite corner of that panel. If the referee has no plating voids, that panel is acceptable, however, if a plating void is present in that microsection, that panel of printed wiring boards shall be rejected.
 - (2) Types 3 and 4: If the plating void does not exceed the conditions of [A.3.6.8.2.1](#), a referee microsection shall be performed using an A or B test coupon from the opposite corner of the panel. If the referee has no plating voids, the panel is acceptable, however, if a plating void is present in that microsection, that panel of printed wiring boards shall be rejected.
- e. Thermal planes (see [A.3.6.3.1](#)). The lateral dielectric spacing between the heat sinking planes and adjacent conducting surfaces (nonfunctional lands) or plated-through holes shall be measured at the closest point between these surfaces or the plated-through hole.

A.4.8.2.2 Registration. Layer-to-layer registration shall be determined by either evaluating microsectioned test coupons (method II, see A.4.8.2.2.1) or by evaluating of special registration coupons when provided (method III, see A.4.8.2.2.2).

A.4.8.2.2.1 Method II (by microsectioned sample units). Registration shall be evaluated using any combination of the 'as received' (see [A.3.7.2.1](#)) and or 'thermal stress' (see [A.3.7.4.10](#)) microsectioned test specimens taken from diagonal corners of the panel. Both test coupons shall have been microsectioned in the vertical plane with one test coupon representing the panel's length (X) direction and the other representing the panel's width (Y) direction.

A.4.8.2.2.2 Method III (optional) (by registration test coupons). Registration test coupons and techniques, when provided by the printed wiring board fabricator, shall be evaluated in accordance with methods approved by the qualifying activity and when applicable, the acquiring activity. Unapproved methods of measurement using registration test coupons shall be backed up by method II of [A.4.8.2.2.1](#) using the appropriate test coupons (see [table IV](#)) from the same panel. Two non-destructive methods for determining registration are available using the following test coupon designs:

- a. Test coupon F (etch factor not needed).
- b. Test coupon R (etch factor of each layer needed).

If other registration test coupon designs and requirements are provided as an element of the design documentation set, registration can be evaluated in accordance with the criteria specified on the applicable master drawing.

APPENDIX A

A.4.8.3 Chemical inspection.

A.4.8.3.1 Cleanliness (by resistivity of solvent extract) (see [A.3.7.3.1](#) and [A.6.5](#)). The printed wiring board shall be inspected for cleanliness in accordance with [IPC-TM-650, method 2.3.25](#).

A.4.8.3.2 Resistance to solvents (marking ink or paint) (see [A.3.7.3.2](#)). Marking ink or paint resistance to solvents shall be inspected in accordance with [IPC-TM-650, method 2.3.4](#). The following details apply:

- a. The marked portion of the test specimen shall be brushed.
- b. After the test, the test specimen shall be visually inspected in accordance with [A.4.8.1](#) for legibility of marking.

A.4.8.3.2.1 Sampling procedures and test specimens. The resistance to solvents test shall be performed either during group A (every lot) or during group B (monthly). The test specimens can be either production printed wiring boards or quality conformance test circuitry strip identification areas (see [appendix D](#)) containing ink or paint marking. The minimum number of samples shall be at least one sample for each solution specified by the applicable test method (i.e., one sample for each solution required).

A.4.8.4 Physical inspections.

A.4.8.4.1 Bow and twist (see [A.3.7.4.1](#)). The printed wiring board shall be inspected for bow and twist in accordance with [IPC-TM-650, method 2.4.22](#).

A.4.8.4.2 Conductor edge outgrowth (see [A.3.7.4.2](#)). The extent of outgrowth, on conductors covered with metals other than fused tin-lead or solder coating, shall be determined by measuring the conductor width before and after mechanically removing the overhang metal. If a referee test is required, cross-sectioning of the conductor shall be performed. The procedure for removing overhang metal, for this test, shall be as follows:

- a. Wet the printed wiring board test specimen in tap water at approximately room temperature.
- b. While wet, brush the printed wiring board test specimen with a brass wire brush to remove the overhang metal. Brush in the direction of the functional line, using moderate pressure.

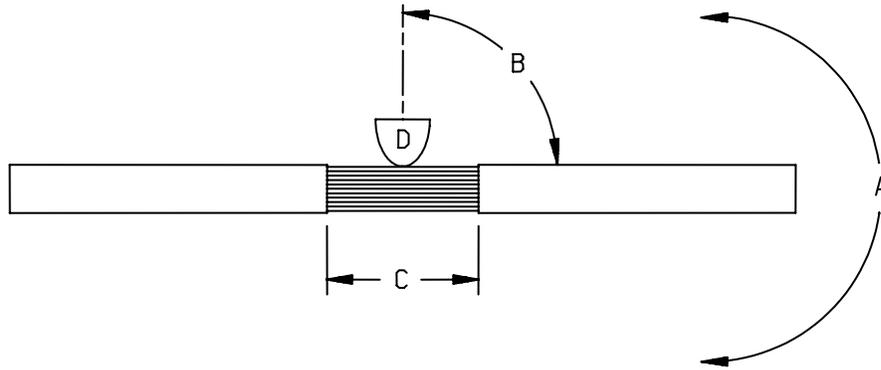
A.4.8.4.3 Flexibility endurance (see [A.3.7.4.3](#)). The flexibility endurance test shall be in accordance with [IPC-TM-650, method 2.4.3](#). The flexibility endurance test may also be performed using an alternate method specified in [A.6.7.1](#). The following exceptions to the test specimen shall apply: Test specimens can be either a single sided portion of production printed board or the test specimen specified in [IPC-TM-650, method 2.4.3](#).

A.4.8.4.4 Folding flexibility (see [A.3.7.4.4](#)) (see [A.6.4.10](#)). The folding flexibility test shall be performed by subjecting the test specimen to fold cycles as described below and as depicted on [figure 2](#). The specified number of fold cycles shall be performed with the mandrel placed in contact with the test specimen on one side and then again with the mandrel placed in contact with the test specimen on the opposite side. After completion of the specified number of fold cycles, both directions, the test specimen shall be tested for electrical defects in accordance with [A.3.7.5.1](#) and [A.3.7.5.2](#).

A.4.8.4.4.1 Test specimens. Folding flexibility shall be evaluated using any of the following designs:

- a. A multilayer rigid-flex portion of production printed board.
- b. Test coupon "H-1", "H-2", or "H-3" as defined in [IPC-100043](#) or [IPC-100044](#).
- c. Test coupon "X" specified in [IPC-2221](#).

APPENDIX A



NOTES:

- a. Direction of bend (detail A).
- b. Degree of bend (detail B).
- c. Points of application (detail C).
- d. Diameter of mandrel (detail D).

FIGURE 2. Folding flexibility.

A.4.8.4.5 Plating adhesion (see A.3.7.4.5). The printed wiring board test specimen shall be inspected in accordance with IPC-TM-650, method 2.4.1, with the following details and exceptions. When edge board contacts are part of the pattern, at least one pull shall be on the contacts. Fresh tape shall be used for each pull. If overhang metal breaks off (slivers) and adheres to the tape, it is evidence of outgrowth (see A.3.7.4.2), but not a plating adhesion failure (see A.3.7.4.5).

A.4.8.4.6 Rework simulation.

A.4.8.4.6.1 Unsupported hole (see A.3.7.4.6.1). The printed wiring board test specimen shall be inspected in accordance with IPC-TM-650, method 2.4.21 with the following details and exceptions: Three holes per test coupon shall be tested. Insert wires in holes in selected lands and solder to lands by machine or hand, as applicable. The insert wire lead shall have a diameter so that the diameter of the hole will be at a maximum of .020 inch (0.51 mm) greater than the diameter of the inserted wire lead. The wires shall not be clinched. It shall be considered a failure when a land around an unsupported hole is loosened.

A.4.8.4.6.2 Plated through hole (see A.3.7.4.6.2). Rework simulation of plated-through holes shall be tested in accordance with IPC-TM-650, method 2.4.36, except that the rework simulation shall be performed after stabilizing the test coupons at temperatures of 15 degrees Celsius to 35 degrees Celsius and relative humidity of 40 to 85 percent for a period of 24 hours.

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A.4.8.4.7 Solderability (see [A.3.7.4.7](#)). The default category of coating durability of **J-STD-003** is category 2. When required by the master drawing, accelerated conditioning for coating durability shall be in accordance with **J-STD-003**. For printed wiring boards using only surface mount components, the surface solderability test can be used in lieu of the hole solderability test. For mixed component designs (both surface mount and through hole attachment), unless otherwise specified, only the hole solderability test shall be performed.

A.4.8.4.7.1 Hole (plated-through hole) (see [A.3.7.4.7.1](#)). The printed wiring board test specimens shall be inspected in accordance with J-STD-003 class 3 or [appendix E](#).

A.4.8.4.7.2 Surface or surface mount land(see [A.3.7.4.7.2](#)). The printed wiring board test specimens shall be inspected in accordance with J-STD-003 class 3 or [appendix E](#).

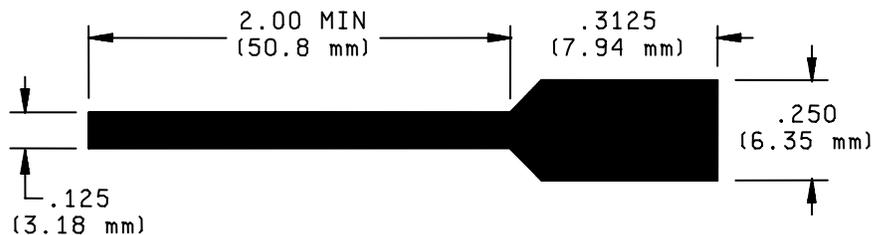
A.4.8.4.8 Solder resist cure and adhesion (see [A.3.7.4.8](#)). The permanency and adhesion of cured solder resist shall be determined in accordance with [IPC-TM-650, method 2.4.28.1](#).

A.4.8.4.9 Surface peel strength (type 4 using foil lamination) (see [A.3.7.4.9](#)). The peel strength shall be inspected in accordance with condition A of [IPC-TM-650, method 2.4.8](#), except that the after thermal stress condition and after exposure to processing chemicals tests shall not be performed. Plated tin-lead, solder coating or other plated metallic resist shall be chemically removed prior to test or shall be prevented from being deposited during manufacturing. The test specimen shall not be coated with any organic coating for test. All peel strength readings obtained shall meet the minimum requirement.

A.4.8.4.9.1 Test specimens. The test specimen shall consist of a conductor that provides a minimum test length of 2 inches (50.8 mm) and a conductor width of .125 inch (3.18 mm). NOTE: This test coupon is described in figure 2A or in [IPC-TM-650, section 5.8.3](#). At least one test coupon per foil laminated side shall be placed on the panel where space is available. Eight peel strength specimens shall be selected from two different production lots; four from each lot or 100 percent if the number of coupons available is less than four for a production lot. If only one foil laminated lot is submitted/passes group A inspection in a calendar month, then only the test coupon(s) from that lot shall be submitted.

A.4.8.4.10 Thermal stress (see [A.3.7.4.10](#)). The printed wiring board test specimen shall be inspected for thermal stress in accordance with [IPC-TM-650, method 2.6.8](#). The following details shall apply. Test specimens constructed of adhesiveless metal-clad flexible base materials shall be subjected to test condition A. Test specimens constructed of adhesive flexible metal-clad base materials shall be subjected to test condition B.

A.4.8.4.11 Coverlayer adhesion (see [A.3.7.4.11](#)). The adhesion and permanency of cured coverlayers shall be determined in accordance with [IPC-TM-650, method 2.4.28.1](#).



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A.4.8.5 Electrical inspection.

A.4.8.5.1 Circuit continuity (see [A.3.7.5.1](#)). A current shall be passed through each net by applying electrodes on the terminals at each end of the net. The current passed through the net shall not exceed those specified in the applicable design standard (see [A.3.1.1](#) and [appendix D](#)) for the smallest conductor in the circuit.

A.4.8.5.2 Circuit shorts (isolation resistance)(see [A.3.7.5.2](#)). A test voltage shall be applied between each net and all other nets that are adjacent to the net under test. The voltage shall be applied between nets of each layer and the electrically isolated net of each adjacent layer. For manual testing the voltage shall be 200 volts minimum and shall be applied for a minimum of 5 seconds. When automated test equipment is used, the minimum applied test voltage shall be as specified on the applicable master drawing. If a test voltage of the printed wiring board is not specified on the applicable master drawing, the test voltage shall be the maximum rated voltage of the net being tested. If no maximum rated voltage is specified, the minimum test voltage shall be 40 volts.

A.4.8.5.3 Dielectric withstanding voltage (see [A.3.7.5.3](#)). The printed wiring board test specimen shall be tested in accordance with [IPC-TM-650, method 2.5.7](#), test condition B. The following details and exceptions apply:

- a. Test specimen: The test specimen shall be as identified in [tables II or V](#).
- b. Magnitude of test voltage: Condition B (1,000 V dc +25 V dc, -0 V dc).
- c. Duration of application of test voltage: 30 seconds +3, -0 seconds.
- d. Points of application: The dielectric withstanding voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer.

A.4.8.6 Environmental inspection.

A.4.8.6.1 Moisture and insulation resistance (see [A.3.7.6.1](#)). The printed wiring board test specimen shall be tested in accordance with [IPC-TM-650, method 2.6.3](#), class 3, test specimen preparation method A. The initial and final resistance measurements shall be taken at 500 V dc, +25 V dc, -0 V dc).

A.4.8.6.2 Thermal shock (see [A.3.7.6.2](#)). The printed wiring board test specimen shall be tested in accordance with [IPC-TM-650, method 2.6.7.2](#), with the following exceptions:

- a. The printed wiring board test specimens shall be subjected to 100 temperature cycles in accordance with test condition D of [IPC-TM-650, method 2.6.7.2](#).
- b. Transfer time between chambers shall be less than 2 minutes. The thermal capacity of the test chambers used shall be such that the ambient temperature shall reach the specified temperature within 2 minutes after the test specimen has been transferred to the appropriate chamber.
- c. During the test, a resistance measurement shall be taken during the first and last high temperature cycle.

A.5. PACKAGING

A.5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see [A.6.2](#)). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the military service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

APPENDIX A

A.6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

A.6.1 Intended use. This appendix is intended to be used by manufacturers not certified to the QML printed board specification, MIL-PRF-31032. This appendix is not a duplicate or look-alike of any MIL-PRF-31032 specification sheet, and most of the historic performance and verification requirements are still contained in this appendix. However, many of the "enhanced" acceptance criteria or methods developed for MIL-PRF-31032 associated specifications have been added as the baseline or are available as an option.

A.6.2 Acquisition requirements.

A.6.2.1 Primary acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, revision letter (with any amendment number when applicable), and date of this specification.
- b. Packaging requirements (see [A.5.1](#)).
- c. Appropriate type (see [1.2.1](#)) and flexibility class (see [1.2.2](#)).
- d. Title, number, revision letter (with any engineering change proposal or notice of revision number when applicable), and date of the applicable master drawing (see [3.1.1](#)).
- e. Title, number, revision letter (with any notice number when applicable), and date of the applicable design standard (see [A.3.3](#)).
- f. Part identification (if applicable), and marking instructions including size, location and application method (see [A.3.1.1](#) and [A.3.8](#)).
- g. Whether microsectioned test specimens, samples or photographs are required to be delivered with the order.

A.6.2.2 Additional acquisition requirements. Acquisition documents should also specify the following data, if applicable:

- a. Verification Conformance Inspection option (if other than option 4) (see [appendix D](#)).
- b. Design related, if different than the applicable design standard (see [appendix D](#)).
 - (1) Minimum annular ring (external or internal) (see [A.3.1.1](#)), if different than the applicable design standard.
 - (2) Minimum conductor width (see [A.3.1.1](#)), if different than the applicable design standard.
 - (3) Minimum conductor spacing (see [A.3.1.1](#)), if different than the applicable design standard.
 - (4) Minimum dielectric thickness (see [A.3.1.1](#)), if different than the applicable design standard.
 - (5) Minimum edge spacing requirement (see [A.3.1.1](#)), if different than the applicable design standard.
 - (6) Copper plating thickness (see [A.3.1.1](#)), if different than the applicable design standard.
 - (7) Conductor finish plating (see [A.3.1.1](#)), if other than solder coating or tin-lead.

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- c. Conductor edge outgrowth or overhang, if applicable (see [A.3.7.4.2](#)).
- d. Circuit shorts (isolation resistance) requirements (see [A.3.7.5.2](#)).
- e. Surface (foil lamination) peel strength, if applicable (see [A.3.7.4.9](#)).
- f. Non-delivery of sample units which have not been subjected to electrical testing (continuity and circuit shorts tests) and have passed all other tests to groups A and B inspection.
- g. Cleanliness (organic) (see [A.3.7.3.1](#) and [A.6.5](#)).
- h. If special, or other identification, marking is required (see [A.3.8](#)).

A.6.3 Qualification. Although the qualification test specimen master drawings IPC-100041, IPC-100042, and IPC-100043 specified in [A.2.1.1](#) requires the use of flexible materials compliant to specific specification sheets in IPC-FC-231, IPC-FC-232, IPC-FC-233 and IPC-FC-241 (superseded by IPC-4202, IPC-4203, and IPC-4204), and rigid base materials compliant to MIL-P-13949 (now MIL-S-13949), manufacturer's now use the notes contained in [DSCC Form 19W](#) for base materials or by specifying the base material on the application for qualification. In addition, the holes and patterns of zone C (except for test coupon E-5) of the qualification master drawing are required to be present on the qualification test specimen and are required for qualification testing.

A.6.3.1 Transference of qualification. Manufacturers currently qualified to MIL-P-50884C will have their qualification transferred to this document. The expiration date of their current qualification will not be changed. Qualifications in process (before the date of this document) will be performed to the requirements MIL-P-50884D with amendment 1. New applications for qualification (after the date of this document) should be performed to the requirements of this amendment.

A.6.3.2 Qualification expiration and QPL-50884. Qualification listings within QPL-50884 for manufacturers qualified under this appendix (QPL product assurance level) includes the qualification expiration date as the last six digits of the test reference number. This date, formatted as (month/day/year), is the actual qualification expiration date for that listing. This date signifies that the company is no longer qualified (unless notified in writing by the qualifying activity) whether or not that individual listing has been removed the QPL. If the company has not requalified before the next issue of the QPL is published, then the listing will not be included on the QPL.

A.6.4 Terms and definitions.

A.6.4.1 Base material types. Qualification of a particular flexible base material types will be extended to cover all flexible base material types of that same family.

- a. Adhesiveless family includes all base materials that use other techniques to hold the basis metal to one or both sides of the dielectric.
- b. Adhesive family include all base materials that rely/use an adhesive to hold the metal to both sides of the dielectric. Note "cast" materials are considered adhesiveless.

A.6.4.2 Complex (as related to group B testing). Complexity of printed wiring boards will usually depend on the base materials used; dielectric layer thickness; overall printed wiring board thickness; number of conductor layers; conductor widths and spacings; intricacy of patterns; size, quantity, aspect ratio and positioning of plated holes; tolerancing of any or all of the above; the presence of internal thermal planes or heat sinks, and all combinations of the above with respect to their manufacturing difficulty, and their effects upon the consistent ability of the printed wiring boards to meet the requirements of the periodic testing, unless otherwise specified by the contracting activity.

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A.6.4.3 Conductive interfaces. The term conductive interfaces is used to describe the junction between the hole wall plating or coating and the surfaces of internal and external layers of metal foil. The interface between platings and coating (electroless copper, direct metallization copper and non-electroless electroless copper substitutes, etc., and electrolytic copper, whether panel or pattern plated), are also considered a conductive interface.

A.6.4.3.1 External conductive interfaces. An external conductive interface is considered to be the junction between the surface copper foil and the deposited or plated copper.

A.6.4.3.2 Internal conductive interfaces. An internal conductive interface is considered to be the junction between the internal layers (copper foil posts or internal layers) and the deposited or plated copper.

A.6.4.4 Contract service(s). Contract services are those services contracted or performed (or both) outside the qualified manufacturer's immediate facility, not to include verification testing including electrical function tests.

A.6.4.4.1 Mass lamination. Manufacturers requesting to use contract services lamination (mass lamination) must be qualified to type 4 of the same base material type requested. The qualification test specimens and sample size must be as specified in A.4.5.2.1. The qualification test specimens must be produced by the QPL manufacturer and the mass laminator and must be representative of the subsequent production process. Printed wiring board manufacturers using contract services are subject to the conditions of A.4.5.3.3.

A.6.4.5 Printed wiring board test specimen. The term printed wiring board test specimen is used to describe all of the following; production printed wiring boards, qualification test specimens, or test coupons.

A.6.4.6 Resin systems families.

A.6.4.6.1 Thermosetting resin. For the purposes of this document, the following base material types are classified as containing thermosetting resins: AF, BF, BI, GB, GC, GF, GH, GI, GM, QI, and SC.

A.6.4.6.2 Thermoplastic resin. For the purposes of this document, the following base material types are classified as containing thermoplastic resin: GR, GP, GT, GX, and GY.

A.6.4.7 Printed board thickness. The overall printed wiring board thickness includes metallic depositions, fusing, and solder resist. The overall thickness is measured across the printed wiring board extremities (thickest part), unless a critical area, such an edge card connector or card guide mounting location, is identified on the master drawing.

A.6.4.8 Quality-conformance test circuitry (QCTC). See IPC-T-50.

A.6.4.9 As received (microsection condition). As received means after tin-lead is reflowed or fused or after solder coating but prior to thermal stress, rework simulation, thermal shock or bond strength testing.

A.6.4.10 Fold cycle.

- a. A fold cycle is defined as taking one end of the specimen and folding it around a mandrel and then unfold back to the original starting position, traveling 180 degrees in one direction and 180 degrees in the opposite direction.
- b. A fold cycle may also be defined as folding (using opposite ends) the ends toward each other (fold the same direction) and then unfold back to the original starting position, with each end traveling 90 degrees in one direction and 90 degrees in the opposite direction.

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A.6.5 Cleanliness.

A.6.5.1 Flux removal. Selection of procedures for flux removal is at the manufacturer's discretion. A procedure should be chosen which will enable the printed wiring board fabricator to produce results enabling compliance with this document. Both polar and nonpolar solvents may be required to effect adequate flux removal.

A.6.5.2 Alternate methods and equipment. The following methods of determining the cleanliness of printed wiring boards have been shown to be equivalent to the sodium chloride equivalent ionic contamination test method:

- a. The Kenco Alloy and Chemical Company, Incorporated, "Omega Meter™, Model 200."
- b. Alpha Metals Incorporated, "Ionograph™."
- c. Zero Systems, Incorporated, "Zero Ion™, Model ZI-100."
- d. Westek, "ICOM 5000™."

Table VII list the equivalence factors for these methods in terms of micrograms equivalents of sodium chloride per unit area.

TABLE VII. Equivalence factors.

| Method | Equivalence factors | Equivalents of sodium chloride | | Related IPC-TM-650 test method |
|--------------------------------|---------------------|--------------------------------|--------------------------|--------------------------------|
| | | Micrograms per square inch | Micrograms per square cm | |
| Resistivity of solvent extract | 1.00 | 10.06 | 1.56 | 2.3.5 |
| Omega meter™ | 1.39 | 14.00 | 2.20 | 2.3.26 |
| Ionograph™ | 2.01 | 20.00 | 3.10 | 2.3.26.1 |
| Zero ion™ | 3.68 | 37.00 | 5.80 | N/A |
| ICOM 5000™ | 2.20 | 22.00 | 3.40 | N/A |

A.6.6 Certified suitable laboratories (acceptable to the Government). Government accepted test laboratories are those facilities that have demonstrated their ability to perform the verification test required by this document. Levels of acceptance include group A, group B, group C, and qualification testing.

A.6.7 Alternate test methods. Other test methods may be substituted for those specified herein provided it is demonstrated to and approved by the qualifying activity that such a substitution in no way relaxes the requirements of this specification.

A.6.7.1 Flexibility endurance (see A.4.8.4.3). The flexibility endurance test may be performed using the alternate test procedure detailed in IPC-TM-650, method 2.4.3.1.

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A.6.8 Group B sample critical design details. Past versions of this document contained default design details that were assumed to apply to all test coupons subjected to group B inspection, regardless of the master drawing design requirements. With the issuance of this document, the design details which were universally used to determine acceptance or failure of the group B samples, are no longer considered universally applicable to the group B test coupons. The printed wiring board design details (plating thickness, dielectric separation, external, and internal annular ring, etc.) or the default design standard that applies to the test coupons, should be submitted along with test coupons so that a proper group B evaluation of the design can be completed.

EXAMPLE: The master drawing of the most complex design selected for group B testing requires .003 inch (0.08 mm) of copper plating thickness, .006 inch (0.15 mm) of dielectric spacing, and .005 inch (0.13 mm) internal annular ring. These design details are considerably different than the baseline design parameters found in either IPC-2223 or IPC-2221. If on these same samples, the group B test laboratory found that the samples exhibited .002 inch (0.05 mm) of copper plating thickness, .005 inch (0.13 mm) of dielectric spacing and .004 inch (0.10 mm) internal annular ring, the test laboratory could not claim, state, or certify that the results of group B testing or the samples met the specification requirement.

A.6.9 Stiffener adhesion test and requirement. This document does not include the stiffener adhesion test or requirement contained in MIL-P-50884C. All stiffeners are viewed as a mechanical support and total bonding of the stiffener to the printed wiring board is not required for compliance with this document.

A.6.10 Figures and illustrations. This document contains very few figures or illustrations depicting acceptable or rejectable conditions as in previous revisions. The diagrams, figures, and illustrations (but not the accept/reject values) contained in IPC-A-600 should be used in visualizing many of the acceptable or rejectable conditions.

A.6.11 Tin finishes (see A.3.4.1). The use of alloys with tin content greater than 97 percent may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture, and can develop under typical operating conditions on products that use such materials. Tin whisker growth could adversely affect the operation of electronic equipment systems. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of 3 percent lead have shown to inhibit the growth of tin whiskers. For additional information on this matter refer to ASTM B545.

A.6.12 Vias. This specification includes provisions for verifying the performance of designs containing through vias, blind vias, buried vias, controlled depth drilled vias, laser drilled vias, low aspect ratio blind vias, microvias, semi-blind vias, semi-buried vias, and trepanned vias.

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APPENDIX A

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APPENDIX B

OPTIONAL PRODUCT ASSURANCE (QUALIFICATION AND VERIFICATION) REQUIREMENTS
FOR QUALIFIED MANUFACTURER LIST PROGRAMS

B.1. SCOPE

B.1.1 Scope. This appendix contains optional requirements concerning the QPL/QML product assurance level for printed wiring boards covered by this specification. The process for extending qualification is also outlined herein. This appendix is not a mandatory part of this specification. It can be used only by manufacturers certified or qualified for listing on QML-31032. The information contained herein is intended for guidance only.

B.2. APPLICABLE DOCUMENTS

B.2.1 General. The documents listed in this section are specified in sections B.3 and B.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections B.3 and B.4 of this specification, whether or not they are listed.

B.2.2 Government documents.

B.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-31032 – Printed Circuit Board/Printed Wiring Board, General Specification for.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

B.2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

B.3. REQUIREMENTS

B.3.1 Performance requirements. The performance requirements of the applicable MIL-PRF-31032 associated specification shall apply to all printed wiring boards procured to the QPL/QML product assurance level.

B.3.2 Accept/reject criteria. The accept/reject criteria of the applicable MIL-PRF-31032 associated specification shall apply to all printed wiring boards procured to the QPL/QML product assurance level.

B.3.3 QML brand. At the option of the manufacturer, the QML brand specified in MIL-PRF-31032 may be placed on printed wiring boards that comply with the product assurance requirements of this appendix.

APPENDIX B

B.4. VERIFICATION

B.4.1 Qualification inspection (reciprocal qualification from MIL-PRF-31032). A reciprocal qualification listing (i.e., from a technology qualified to a MIL-PRF-31032 associated specification) to this document will depend on the level of QML technology qualified. Unless otherwise detailed in MIL-PRF-31032 qualification test plan, following guidelines will apply:

- a. Printed board type (see [6.4.2](#), [A.4.5.4.1](#), and [D.3.6](#)). The extent of qualification for base materials types defined in [A.4.5.4](#) will apply. EXAMPLE: A type 2 qualification under a MIL-PRF-31032 associated specification will not justify a type 4 qualification listing to this document.
- b. Printed board material (see [A.4.5.4.3](#)). The extent of qualification for base materials types defined in [A.4.5.4](#) will apply. EXAMPLE: An adhesiveless flexible metal clad base material qualification under a MIL-PRF-31032 associated specification will justify an adhesiveless flexible metal clad base material qualification listing to this document.
- c. Complexity. The QPL/QML manufacturer can supply QPL compliant printed wiring boards greater than their qualified QML capability (similar to the traditional QPL product assurance level). Printed board designs verified using the QPL/QML option shall flow through the conversion of customer requirements element of the approved Quality Management (QM) plan as described in MIL-PRF-31032, Appendix A. The Technical Review Board (TRB) shall evaluate designs exceeding their current QML-31032 qualification listing to determine if the add-on qualification provisions of MIL-PRF-31032 shall be used. Reasons for not using the add-on qualification provisions shall be documented in the periodic status reports.

B.4.1.1 Concurrent qualification. Manufacturers already qualified to the QPL level of this document will retain that listing after transitioning to the QPL/QML level. The 3 year expiration time will not apply to the QPL/QML product assurance level.

B.4.1.2 Retention (see [B.6.4](#)). The QML status report described in MIL-PRF-31032 will cover the QPL/QML retention requirements to this document.

B.4.2 QPL/QML product assurance. The product assurance requirements for the QPL/QML level of printed wiring board furnished under this specification shall be satisfied by certification to MIL-PRF-31032. All printed wiring boards manufactured and delivered in compliance with this appendix should be produced in accordance with the approved quality management plan.

B.4.3 Printed wiring board performance verification. Printed wiring board performance verification inspection shall consist of inspections on the production printed wiring boards and test coupons specified in the applicable MIL-PRF-31032 associated specification. The following details are applicable to the QPL/QML product assurance level:

- a. Lot conformance inspection (LCI) product acceptance testing should be based on the applicable verification flows (in-process and group A) offered by this document (see [A.4.4](#) and [appendix D](#)) or the routine from a similar technology described by a MIL-PRF-31032 specification sheet. The various verification flows should be based upon the design standard used to design the printed wiring boards and the available panel test coupons for the printed wiring boards.
- b. MIL-PRF-31032 periodic conformance inspection (PCI) program can be used in lieu of groups B and C inspection of this document.
- c. Test optimization is applicable to this appendix and can be applied to any verification flow detailed in this document.

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B.5. PACKAGING

B.5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the military service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

B.6. NOTES

B.6.1 Intended use. This appendix is intended to be used by manufacturers certified to MIL-PRF-31032 to reduce the complexity of maintaining multiple product/process and testing flows (both MIL-P-50884 or MIL-PRF-31032) within a the manufacturing and testing facility.

B.6.2 Application of the QPL/QML product assurance level to existing requirements.

B.6.2.1 Use of existing master drawings. The QPL/QML printed wiring board manufacturer can use pre-existing master drawing and production artwork without any modifications (existing production masters test coupons and requires no additional or new ones).

B.6.2.2 Form, fit, and function. The form, fit, and function of the printed wiring boards, whether the QPL/QML product assurance level or the QPL product assurance level is used, will be the same.

B.6.2.3 Certification. The printed wiring boards can be certified as being compliant to this document (MIL-P-50884).

B.6.3 Benefits of the QPL/QML product assurance level. Printed wiring boards produced by QML manufacturers using the provisions of this appendix in lieu of previous revisions would be compliant to this document (MIL-P-50884) when using the QPL/QML product assurance level with the added benefits as follows:

- a. The QPL/QML manufacturer can use pre-existing master drawing and production artwork without any modifications needed (can use existing production masters test coupons and requires no additional or new ones).
- b. The printed wiring boards, whether the QPL/QML option or the QPL option is used, will be the same.
- c. The level of quality will be the same or higher than the QPL product assurance level.
- d. When using the correct (for the design) verification test, the cost should be the same or less due to enhancements made to accept/reject criteria.
- e. Customers will be more confident that a QPL/QML manufacturer has demonstrated the capabilities to build its design dues to its QML certification and qualification rather the generic standardized qualification test vehicle of the QPL quality assurance level portion of this document.

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APPENDIX B

B.6.4 Retention issues. The manufacturer need only to keep the qualifying activity apprised of its total QML program, i.e., MIL-PRF-31032 QML and this document's QPL/QML product assurance level. This means that the manufacturer does not have to maintain two separate compliance programs, (i.e., no need for a QPL compliance program for this document and a QML program for MIL-PRF-31032).

B.6.5 Certificates of compliance issues. The manufacturer can certify QPL/QML printed wiring boards process under their MIL-PRF-31032 QML program as compliant to this document. The certificate of compliance should reference the QPL/QML product assurance level to differentiate the compliant product from printed wiring boards verified using the QPL product assurance level offered in this document.

B.6.6 Past specification revisions (see appendix D for more details). Printed wiring boards procured to this document meets and exceeds all quality and reliability requirements of previous revisions of MIL-P-50884.

APPENDIX C

C = 0 (ZERO DEFECT) SAMPLING

C.1. SCOPE

C.1.1 Scope. This appendix details the statistical sampling procedures to be used with the QPL product assurance level of this specification. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance.

C.2. APPLICABLE DOCUMENTS

C.2.1 General. The documents listed in this section are specified in sections C.3, C.4, and C.5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections C.3, C.4, and C.5 of this specification, whether or not they are listed.

C.2.1.1 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

NATIONAL CONFERENCE OF STANDARDS LABORATORIES

NCSL Z540-1 – Calibration Laboratories and Measuring and Test Equipment – General Requirements.

(Application for copies should be addressed to NCSL International, 2995 Wilderness Place, Suite 107, Boulder, CO 80301-5404 or at URL <http://www.ncsli.org>.)

C.2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

C.3. DEFINITIONS AND SYMBOLS

C.3.1 Definitions. The following definitions shall apply for all statistical sampling procedures:

- a. C = 0 sample plan: The C = 0 sample plans are defined as a combination of a test specimen usage identifier (see C.3.1.b below) and a sample size series (see C.3.1.c below). The resulting C = 0 sample plan will be a two character designator combination that identifies the sample size series that is to be with a type of test specimen for a particular verification (see C.4.5).
- b. Test specimen usage identifier (see C.4.5 for examples): The following usage modifiers are used to differentiate when a particular plan is to be used for a particular test specimen:
 - (1) The letter "B" will be used to signify that production printed boards are to be sampled.
 - (2) The letter "T" will be used to signify that test coupons are to be sampled based on the number of panels in the lot.
 - (3) An asterisk "*" will be used for either printed boards or test coupons.

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- c. Sample size series: The sample size series is defined as the following series of letters: A, D, F, H, J, L, and N that are listed in [table VIII](#) (see [C.4.5](#) for examples).
- d. Tightened inspection: Tightened inspection is defined as inspection performed using the next sample size value in the sample size series lower than that specified.
- e. Acceptance number (C): The acceptance number is defined as an integral number associated with the selected sample size which determines the maximum number of defectives permitted for that sample size.
- f. Rejection number (R): Rejection number is defined as one plus the acceptance number.

C.3.2 Symbols. The following symbols shall apply for all statistical sampling procedures:

- a. C: Acceptance number.
- b. R: Rejection number.

C.4. STATISTICAL SAMPLING PROCEDURES AND SAMPLE PLAN TABLE

C.4.1 General. Statistical sampling shall be conducted using the $C = 0$ method. The $C = 0$ method as specified herein is a sampling plan that provides a high degree of assurance that a lot having a proportion defective greater than the specified acceptance number ($C = 0$) will not be accepted. For all situations, the acceptance number (C) shall be equal to 0 ($C = 0$) and the rejection number (R) shall be 1 or greater ($R \geq 1$).

C.4.2 Acceptance and procedure.

C.4.2.1 Acceptance number ($C = 0$). Acceptance of inspection lots shall be based on an acceptance number of zero ($C = 0$).

C.4.2.2 Rejection number ($R \geq 1$). Failure of a sample unit for one or more tests of a subgroup shall be charged as a single failure. One or more sample rejects shall be cause for failure of the lot or subplot, as applicable. Any failure on any of the sample units shall constitute a failure of the entire inspection lot or subplot.

C.4.3 Tightened inspection (for reevaluation purposes). Tightened inspection shall be performed by sampling using double the sample size as specified in [table VIII](#) with zero failures allowed or 100 percent.

C.4.4 Sample size. The sample size for each subgroup shall be determined from [table VIII](#). If lot size is smaller than sample size, test all of the units. The manufacturer may, at their option, select a sample size greater than that required; however, the number of failures permitted shall not exceed the acceptance number.

C.4.5 $C = 0$ sample plan construction (selection and usage of the sample size series). The sample size series of [table VIII](#) to be used will be directed from the appropriate inspection table. The inspection table will specify the $C = 0$ sample plan (test specimen identifier and sample size series) or plans (test printed wiring board, test coupons, or either one) to use.

EXAMPLES: If an inspection table specified that "Plan BF or TL" be used when verifying test specimens, it is specifying that sample size series "F" of [table VIII](#) shall be used for selecting printed wiring boards and sample size series "L" shall be used for selecting test coupons. If the same inspection table specified that "Plan *H" be used (the asterisk "*" representing both printed wiring boards and test coupons), then sample size series "H" of [table VIII](#) shall be used for either printed wiring boards or test coupons.

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TABLE VIII. C = 0 (zero defect) sampling.

| Lot size | Sample size (number of test specimens to be inspected) ^{1/} | | | | | | |
|--------------|--|----------|----------|----------|----------|----------|----------|
| | Series A | Series D | Series F | Series H | Series J | Series L | Series N |
| 1 to 8 | All | All | All | 5 | 3 | 2 | 1 |
| 9 to 15 | All | All | 13 | 5 | 3 | 2 | 1 |
| 16 to 25 | All | All | 13 | 5 | 3 | 2 | 1 |
| 26 to 50 | All | 32 | 13 | 5 | 5 | 3 | 1 |
| 51 to 90 | 50 | 32 | 13 | 7 | 6 | 4 | 2 |
| 91 to 150 | 50 | 32 | 13 | 11 | 7 | 5 | 2 |
| 151 to 280 | 50 | 32 | 20 | 13 | 10 | 6 | 2 |
| 281 to 500 | 50 | 48 | 29 | 16 | 11 | 7 | 3 |
| 501 to 1,200 | 75 | 73 | 34 | 19 | 15 | 8 | 4 |
| 201 to 3,200 | 116 | 73 | 42 | 23 | 18 | 9 | 5 |

^{1/} If lot size is smaller than sample size test all of the units.

C.5. TEST EQUIPMENT AND INSPECTION FACILITIES

C.5.1 Calibration. All tests and measurements for process control, qualification testing, lot conformance inspection or periodic conformance inspection shall be made with capable instruments whose accuracy has been verified. Calibration of measurement and test equipment and test standards that control the accuracy of inspection and test equipment and facilities shall be in accordance with [NCSL Z540-1](#), or equivalent.

C.5.2 Inspection facilities. The inspection facility used to perform qualification testing and periodic conformance inspection shall be approved by the qualifying activity for the performance of the tests and inspection requirements of compliant printed wiring boards.

C.5.3 Acquiring activity or manufacturer imposed tests. Acquiring activity or manufacturer imposed tests shall be in accordance with the requirements specified in the master drawing. If any additional imposed tests detect a problem, the manufacturer shall submit all panels/printed wiring boards in the lot to those tests to eliminate rejects and shall take steps to determine and eliminate the cause of failure.

C.5.4 Test method alternatives. Alternate test methods are allowed provided that it is demonstrated to the qualifying activity that such alternatives in no way relax the requirements of the test method referenced by this specification (see [appendix B](#)).

C.5.5 Procedure in case of test equipment malfunction or operator error. When it has been established that a improper test is due to test equipment malfunction or operator error, the inspection facility shall document the results of its investigations and corrective actions, if required, and shall make this information available to the qualifying activity and the acquiring activity, as applicable.

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APPENDIX D

SUPERSESION, VERIFICATION CONFORMANCE INSPECTION OPTIONS,
AND USAGE OF PAST DESIGN STANDARDS

D.1. SCOPE

D.1.1 Scope. This appendix contains information and guidance concerning the supersession of legacy Department of Defense documents such as MIL-P-50884 revision C and MIL-STD-2118. This appendix is not a mandatory part of this specification. The information contained herein is intended for guidance only.

D.2. APPLICABLE DOCUMENTS

D.2.1 General. The documents listed in this section are specified in sections D.3 and D.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections D.3 and D.4 of this specification, whether or not they are listed.

D.2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

| | | |
|-----------|---|--|
| J-STD-003 | – | Solderability Tests for Printed Boards. |
| IPC-T-50 | – | Terms and Definitions for Interconnecting and Packaging Electronic Circuits. |
| IPC-D-249 | – | Design Standard for Flexible Single and Double-Sided Printed Boards. |
| IPC-D-275 | – | Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies. |
| IPC-2221 | – | Generic Standard for Printed Board Design. |
| IPC-2223 | – | Design Standard for Flexible Printed Boards, Sectional. |

(Application for copies should be addressed to the IPC - Association Connecting Electronics Industry, 3000 Lakeside Drive, Suite 309 S, Bannockburn, IL 60015-1249 or <http://www.ipc.org>.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

D.2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

D.3. DEFINITIONS

D.3.1 Design standard. A document that establishes the standard practices, guidelines, and default values for the design of printed wiring boards. Within this document, the term "design standard" is used to describe those documents that contain the design, construction, material, and test coupon requirements and guidelines.

D.3.2 Legacy designs or documents. See D.4.1.

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D.3.3 Supersession. The act of replacing a legacy document that no longer exists or is no longer supported with a currently supported document.

D.3.5 Quality conformance test circuitry. See IPC-T-50.

D.3.6 Printed wiring board types. The printed board types are defined in IPC-2223.

D.4. SUPERSESSION

D.4.1 Superseded specifications. [Appendix A](#) of this document includes the essential requirements of the previous revision and can be used to supersede the following specifications:

- a. MIL-P-50884C, dated 4 May 1984 with amendment 1, dated 19 August 1988.
- b. MIL-P-50884C, dated 4 May 1984 with amendment 2, dated 22 June 1990.
- c. MIL-P-50884C, dated 4 May 1984 with amendment 3, dated 13 December 1991.
- d. MIL-P-50884C, dated 4 May 1984 with amendment 4, dated 9 April 1993.
- e. MIL-P-50884C, dated 4 May 1984 with amendment 5, dated 27 November 1998.

D.4.1.1 Reference to superseded specifications. All the requirements of this document (MIL-P-50884D) can be interchangeable with those of MIL-P-50884. Therefore, existing procurement documents (master drawings or OEM documents) referencing MIL-P-50884 need not be revised, updated, or changed to make reference to MIL-P-50884 in order for this document to be used.

D.4.1.2 Revisions. Printed wiring boards tested to this document generally would meet or exceed the performance requirements of past revisions. However, due to various changes in acceptability and evaluation criteria, testing procedures and test coupon sampling, an exact duplication of a previous revision cannot be claimed or made in all areas of concern. Manufacturers should not pick-and-choose or mix acceptability requirements and test procedures from one revision of MIL-P-50884 to another. Compliance should be either to MIL-P-50884B, MIL-P-50884C (with a specific amendment, if applicable), or this document entirely, unless the manufacturer documents a direct correlation between the revisions (with any amendments, if applicable) under consideration.

D.4.2 Superseded guidelines and standards. The following design standards have been superseded by IPC-2221 and IPC-2223 for all types and classes of printed wiring boards:

MIL-STD-2118, dated 4 May 1984.
MIL-P-50884B (appendix), dated 19 January 1976.
MIL-P-50884A, dated 5 June 1972.

D.4.2.1 Retooling. Printed wiring boards that were designed using superseded Department of Defense design standards do not require conversion to IPC-2221/IPC-2223.

D.4.2.2 Superseded types. Before MIL-P-50884C, only single and double sided printed wiring boards were covered in MIL-P-50884. The obsolete type A requirements in MIL-P-50884B (flexible printed wiring that is capable of withstanding at least one solder operation without terminal degradation) did not carry over to MIL-P-50884C. However, the type B requirements in MIL-P-50884B (flexible printed wiring that is capable of withstanding at least five solder and unsolder operations without terminal area degradation, i.e., rework simulation) was carried over to and extended to all printed wiring board designs in MIL-P-50884C.

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D.4.3 Testing.

D.4.3.1 Group A testing. Group A testing should be performed to the specific revision, and amendment if applicable, called out by the acquisition documents. For example, if printed wiring boards are produced to MIL-P-50884C with amendment 1, MIL-P-50884C with amendment 3 and MIL-P-50884D, a manufacturer would be expected to perform group A testing, for the applicable lot, to the requirements of the revision specified. In those three different revisions (C w/amendment 1, C w/amendment 3, and D) a requirement for an acceptability criteria or test procedure may be the same or it might be significantly different. Retention of qualification summaries for group A should list the lots produced, grouped by revision and amendment.

D.4.3.2 Group B samples and testing. Samples to be selected for group B testing should be based on the most complex compliant printed wiring boards produced that month. For example, if printed wiring boards are produced to MIL-P-50884C, MIL-P-50884C with amendment 4 and MIL-P-50884D during a given month, and the most complex printed wiring boards produced that month were in the lot ordered to MIL-P-50884C with amendment 4, then that should be the lot from which the group B sample should be selected. The samples should be tested in accordance with MIL-P-50884C with amendment 4. If during that same month, printed wiring boards were produced to MIL-P-50884B and MIL-P-50884C (unamended), group B tests to those specific revisions would also be required in order to be compliant to those revisions, unless specifically specified in the contract.

D.4.3.3 Group C samples and testing. Group C testing is for manufacturers of **class A** and **class B** printed wiring boards to verify that it is still capable of meeting the flexibility class performance requirements. Samples to be selected for group C testing, unlike group B inspection, are not based on the most complex compliant printed wiring boards produced that month or reporting period. The group C samples can be either production printed wiring boards or the appropriate test coupon.

D.4.4 Superseded test coupons. Before MIL-P-50884C, test coupons were only used for first article inspection and not required for production. The production panel test coupons were introduced within MIL-P-50884C and MIL-STD-2118 were for the supplier certification program concept. The production test coupons of MIL-P-50884C, described within MIL-STD-2118, should be used when already incorporated onto production tooling. New designs or jobs should use the test coupons specified in IPC-2221 and IPC-2223. Table IX contains a cross listing of the various test coupon designations that have been used in superseded design standards.

D.4.5. Test coupons, placement, quantity and usage. IPC-2221 contains a table that specifies for each production panel the test coupon placement, quantity (see note below) and usage (similar to IPC-D-275 and IPC-2221). However, MIL-STD-2118 did not provide a table that specifies for each production panel the test coupon placement, quantity, and usage.

NOTE: There needs to be a sufficient number of test coupons on the production panel in order to be able to perform group A and when necessary, group B inspection regardless of the number of test coupons specified by the design standard.

D.4.5.1 Intended use and intent of this appendix. This appendix can be used to understand the test coupons that were referenced in previous revisions of this document. These guidelines are intended for the re-identification and proper usage of test coupons within this document that are or were originally identified in various legacy Department of Defense printed wiring board design standards. This appendix is intended for use in conjunction with a manufacturer's verification conformance compliancy program.

D.4.5.2 Supporting documents. The documents in this section may be used as guidelines for the development of a verification conformance optimization program and are not mandatory for this specification.

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D.4.5.4 Test coupons, placement, quantity, and usage. IPC-2221 contains a table that specifies for each production panel the test coupon placement, quantity, and usage (as did IPC-D-275 and MIL-STD-275). However, MIL-STD-2118 did not contain a table that specifies for each production panel the test coupon placement, quantity, and usage. In the past, when attempting to be compliant with the group A table of MIL-P-50884C, it was confusing and/or difficult to determine how many test coupons were needed on the production panel, how many test coupons needed to be microsectioned, and what evaluations could be combined during group A inspection.

TABLE IX. Test coupon translation.

| Usage in this document | MIL-STD-2118 | IPC-D-249 | IPC-2221 <u>1/</u> | IPC-100041 |
|--|---------------|-----------|--------------------|------------|
| Hole solderability As received (microsection) | A | A | A | A |
| Thermal stress (microsection) Rework simulation | B | B | B | B |
| Plating adhesion | C | C | C | C |
| Interconnect resistance (continuity) | D | D | D | D |
| Insulation resistance | E | | E | E |
| Flexibility | F | H | H | H |
| Solder resist | I/G <u>2/</u> | G | G/T | G |
| Peel strength | <u>3/</u> | | P | |
| Solderability | | | S | |
| Registration | | | F | |

1/ H coupon was added to IPC-2221 with IPC-2221, Amendment 1.

2/ MIL-P-50884C, group A table reference test coupon "G" while MIL-STD-2118 displayed a test coupon "I" next to the solder resist test coupon figure.

3/ See IPC-TM-650 methods 5.8.3.

APPENDIX E

SEQUENTIAL ELECTROCHEMICAL REDUCTION ANALYSIS
SOLDERABILITY TEST

E.1. SCOPE

E.1.1 Scope. This test method describes the method and procedure used to evaluate oxidation levels on solderable surfaces. The type and quantity of oxides on copper, tin, and lead surfaces have a significant impact on solderability. The procedure involves using electrochemical reduction techniques to determine the type and quantity of oxide on plated-through holes, attachment lands, and printed wiring board surface conductors. The sequential electrochemical reduction analysis (SERA) solderability test method is offered as an alternative to other solderability test methods required by this document. This test method shall not be contractually imposed upon either the contractor or sub-contractor. This appendix is not a mandatory part of the specification. The information contained herein is intended for compliance only when volunteered as an alternative to the other solderability test methods detailed.

E.2. APPLICABLE DOCUMENTS

E.2.1 General. The documents listed in this section are specified in sections E.3, E.4, and E.5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections E.3, E.4, and E.5 of this specification, whether or not they are listed.

E.2.2 Government documents.

E.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those-cited in the solicitation or contract.

FEDERAL SPECIFICATIONS

A-A-59282 – Chemicals, Analytical; General Specification for.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

E.2.2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

J-STD-004 – Requirements for Soldering Fluxes.

(Application for copies should be addressed to the IPC – Association Connecting Electronics Industry, 3000 Lakeside Drive, Suite 309 S, Bannockburn, IL 60015-1249 or <http://www.ipc.org>.)

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THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC. (IEEE)

IEEE-488 – IEEE Standard Digital Interface For Programmable Instrumentation.

(Copies of these documents are available online at <http://iee.org> or from the IEEE Operations Center, 445 Hoes Lane, Piscataway, New Jersey 08854-1331.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

E.2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

E.3. DEFINITIONS

E.3.1 Sequential Electrochemical Reduction Analysis (SERA). A chronopotentiometric reduction method for assessing tin-lead finish solderability.

E.4. TESTING

E.4.1 Apparatus (see figure 3).

E.4.1.1 Reservoir (see detail A). The reservoir shall be a container constructed of a nonmetallic, nonreactive material with a minimum volume of 500 ml. The reservoir shall have an inlet/outlet port, test head chamber port, and a saturated calomel electrode (SCE) reference electrode port. The inlet/outlet port shall be connected to a vacuum trap tube. The inlet/outlet port shall incorporate a diffuser to aid in the effectiveness of the inert gas purging. Polypropylene tubing may be used for connection tubing. All connection fittings shall be of a nonreactive material. The reservoir shall have the capability of maintaining a positive pressure environment. The reservoir shall be emptied and rinsed with deionized water for every 16 hours of testing.

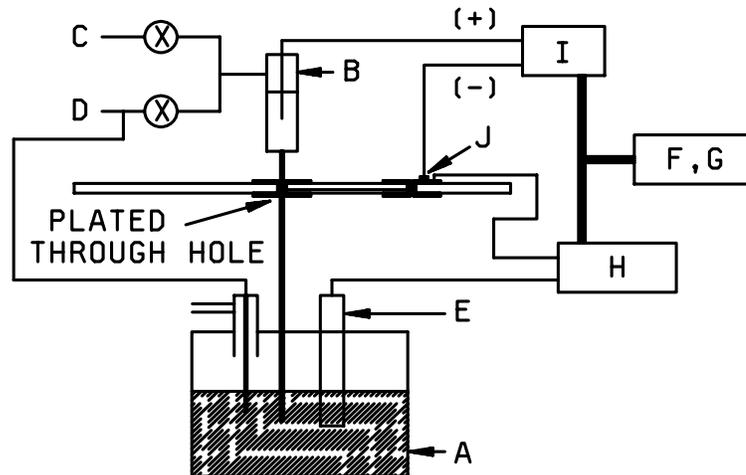


FIGURE 3. Schematic of SERA plated through hole apparatus.

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E.4.1.2 Test head (see [detail B](#)). The test head shall be constructed of a nonmetallic, nonreactive material. The test head shall have ports to allow inert gas purging and intake/expulsion of borate buffer solution. The test head shall have either an optical or mechanical means of aligning the test head chamber over the test plated-through hole. The test head shall use Vitron or equivalent o-rings for the test head to test surface interface seals. These o-rings shall be replaced after every 8 hours of testing unless integrity of the o-rings can be documented for extended periods. The test head shall have the capability of maintaining a positive pressure environment.

E.4.1.3 Vacuum pump (see [detail C](#)). A vacuum pump shall be used to draw buffer solution into and out of the test head compartment. The vacuum pump shall be able to draw minimum vacuum of 5 inches of Hg (16.9 kPa).

E.4.1.4 Gas regulator (see [detail D](#)). An in-line gas regulator shall be used to monitor the flow of the inert purging gas. The gas regulator shall be able to measure a minimum of 1 cubic foot per hour (0.02832 cubic meters per hour) at standard temperature and pressure.

E.4.1.5 SCE reference electrode (see [detail E](#)). The reference electrode shall be a SCE reference-electrode with a temperature range of -5 degrees Celsius to +60 degrees Celsius and a Ph range of 0-14. The SCE reference electrode shall be stored in such a manner as to prevent drying out (either in a saturated KCl solution or in accordance with the manufacturer's instructions). The SCE reference electrode shall be calibrated in accordance with the manufacturer's instructions once every 30 days.

E.4.1.6 Computer (see [detail F](#)). The computer shall be equivalent to or better than a MS-DOS compatible, 80286-12MHz, with 512 Kbyte of internal memory and floppy and hard disk drives.

E.4.1.7 IEEE-488 interface card (see [detail G](#)). An IEEE-488 interface card is required for data acquisition between the computer, the digital multimeter, and the programmable current source.

E.4.1.8 Digital multimeter (see [detail H](#)). A digital multimeter is required to measure the voltage changes during the SERA reduction. The digital multimeter shall have the following characteristics:

- a. A measurable voltage range of 0 V to -2.0 V.
- b. A voltage measurement tolerance of ± 5 mV.
- c. Voltage measurement root-mean-square noise level should not exceed 10 Mv.
- d. Input impedance should be greater than 1 G-Ohm.

E.4.1.9 Programmable current source (see [detail I](#)). A programmable current source is required to apply a constant current during the SERA reduction. The programmable current source shall have the following minimum characteristics:

- a. The applied current should be variable in 0.1 microamp steps between 1.0 microamps and 10 microamps.
- b. The applied current should remain constant within ± 5 percent.

E.4.1.10 Printed wiring board (PWB) contact pin (see [detail J](#)). A contact pin is required to complete the electrical circuit with the test plated-through hole. The PWB contact pin shall not exert a force of greater than .5 pounds (0.23 Kg) nor alter the plated-through hole form, fit, or function.

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E.4.2 Materials.

E.4.2.1 Borate buffer solution. The SERA test requires the use of a borate buffer solution. This solution uses reagent grade boric acid, sodium borate ($\text{Na}_2\text{B}_4\text{O}_7 \cdot 10 \text{H}_2\text{O}$), and deionized water. The recipe is 6.18 grams/liter boric acid and 9.55 grams/liter of sodium borate. The Ph of the borate buffer solution shall range in the range of 8.3 to 8.4. Adjustments to the buffer Ph shall be made using either boric acid or sodium borate additions.

E.4.2.2 Inert gas. An inert gas is required to purge oxygen from the system. Either argon or ultra high purity (99.998 percent) dry nitrogen shall be used.

E.4.2.3 Deionized water. Deionized water comprises a portion of the borate buffer solution and shall be used to rinse the test plated-through hole after completion of the SERA analysis. The deionized water shall be 1 Megohm conductivity or better.

E.4.2.4 Isopropyl alcohol. Isopropyl alcohol is used to rinse the test plated-through hole after the completion of the SERA analysis. Reagent grade isopropyl alcohol, in accordance with A-A-59282, shall be used.

E.4.2.5 Potassium chloride solution (KCl). The SCE reference electrode may be stored in a saturated KCl solution. This solution uses reagent grade potassium chloride, in accordance with A-A-59282, in a saturated solution form.

E.5. PROCEDURES

E.5.1 General. The test procedure shall be performed on three plated-through holes randomly chosen on the printed wiring board or representative test coupon. The SERA test shall be performed just prior to packaging for storage or shipment or immediately upon removal from the manufacturer's protective package. During handling, care shall be exercised to prevent the surfaces being tested from being abraded or contaminated by grease, perspirants, abnormal atmosphere, etc. The test procedure consists of the following operations:

- a. Proper preparation of SERA system (see E.5.2).
- b. Application of test method (see E.5.3).
- c. Evaluation of test data (see E.5.4).
- d. Proper post test preparation of SERA system (see E.5.5).

E.5.2 Preparation of SERA systems.

- a. Initiate inert gas flow into system and allow a minimum of 10 minutes to elapse prior to testing.
- b. Turn on digital multimeter and programmable current source and allow a minimum of 10 minutes to elapse prior to testing.
- c. Remove reference electrode port and rinse with deionized water. Replace reference electrode port and add sufficient quantity of borate buffer solution to immerse the SCE reference electrode a minimum of 1 inch (25.4 mm).
- d. Remove SCE reference electrode from storage container. Rinse with deionized water, wipe with clean soft cloth, and place into reference electrode port. Attach system electrical connections in accordance with figure 3.
- e. Remove and replace test head o-ring seals as required (see E.4.1.2).
- f. Close SERA test head together thus seating o-rings together on a representative sample plated-through hole and perform vacuum check on system. No visible air bubbles shall be detected in the test head chamber which would indicate improper sealing.

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E.5.3 Application of test method.

- a. The test operator shall record the specimen lot date code and manufacturer for each individual printed wiring board. An individual printed wiring board reference chart for the test plated-through holes and PWB contact pin locations shall be maintained for each test specimen configuration.
- b. Insert test specimen onto SERA test head and allow a minimum of 4 seconds for inert gas purging of the test head. Ensure inert gas bubbling is occurring in the reservoir tube.
- c. Attach PWB contact pin.
- d. Attach electrical source leads.
- e. Draw borate buffer solution into test head chamber a minimum of 75 percent of chamber height. Visually monitor test head chamber for leaks.
- f. Partially flush test head chamber to 50 percent height to dislodge any gas bubbles which could be trapped in test hole.
- g. Input computer data for test specimen and test hole identification. Set current density at 30 μ amp per centimeter squared (plated-through hole area shall be calculated as specified in E.5.3.1), test duration at a minimum of 400 seconds, the number of open circuit samples to be measured, and the number of systems measurements at one reading per second. The minimum test duration may be reduced provided complete plated-through hole reduction has been achieved.
- h. Perform SERA test to test duration completion.
- i. Remove electrical source leads.
- j. Remove PWB contact clamp.
- k. Flush borate buffer solution from test hole.
- l. Remove test specimen from SERA test head.
- m. Rinse test plated-through hole with deionized water saturated cotton swab for a minimum of 3 seconds, then rinse test plated-through hole with isopropyl alcohol saturated cotton swab for a minimum of 3 seconds. Allow test plated-through hole to air dry. The rinsing operations may be conducted for all test holes as a one time operation provided the rinsing operation is completed within 10 minutes of completion of the last test hole on that individual printed wiring board specimen. Other documented rinsing operations may be used provided their effectiveness is as good as or better than the cotton swab rinse process.

E.5.3.1 Plated-through hole area calculation. The area of plated-through holes shall be determined using:

$$\text{Area} = (2)(\pi)(R1)(H) + [(2)(\pi)(R2^2) - (2)(\pi)(R1^2)]$$

where

- H = Printed wiring specimen thickness.
R1 = Plated-through hole radius.
R2 = O-ring internal radius.

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An example of the calculation is as follows:

H = See table X for the values for H.
R1 = Plated-through hole radius = .018 inches nominal (0.046 cm).
R2 = O-ring internal radius = 0.075 cm.

$$\begin{aligned} \text{Area} &= (2)(\pi)(0.046)(H) + [(2)(\pi)(0.075)^2 - (2)(\pi)(0.046)^2] \\ &= (0.22890)(H) + [0.03534 - 0.013295] \\ &= 0.2890 \text{ cm (H cm)} + [0.022045 \text{ cm}^2] \end{aligned}$$

TABLE X. SERA plated-through hole example calculation data.

| Printed wiring board thickness (inches) | H (centimeters) | Area (centimeters ²) |
|--|--------------------|-------------------------------------|
| .020 | 0.0508 | 0.0367 |
| .030 | 0.0762 | 0.0441 |
| .040 | 0.1016 | 0.0514 |
| .050 | 0.1270 | 0.0587 |
| .060 | 0.1524 | 0.0661 |
| .070 | 0.1778 | 0.0734 |
| .080 | 0.2032 | 0.0808 |
| .090 | 0.2286 | 0.0881 |
| .100 | 0.2540 | 0.0955 |
| .110 | 0.2794 | 0.1028 |

E.5.4 Evaluation of test data. The change in reduction voltage shall be plotted versus the charge density (current density against time). This SERA curve generated shall be differentiated and then incorporate the following moving window average, curve smoothing function:

$$V(n) = \text{SUM } [V(n-5) \text{ through } V(n+5)] / 11$$

The following eight SERA parameters shall be calculated from the differentiated and smoothed SERA curve using the following threshold limits listed below. Figure 4 illustrates these parameters and threshold limits on an example SERA curve.

1. Voc = The final open circuit voltage measured for the SERA differentiated/smoothed curve.
2. Q1 = The area under the curve defined by: Nmin1 threshold value (defined constant value).
3. V2 = The voltage on the differentiated/smoothed curve defined by: (Nmin3 + Nmin1 threshold values) / 2.
4. Q2 = The area under the curve defined by: Nmin3 threshold value – Nmin 1 threshold value.
5. V3 = The voltage on the differentiated/smoothed curve defined by: (Nmin5 + Nmin3 threshold value)/2.
6. Q3 = The area under the curve defined by: Nmin5 threshold value – Nmin3 threshold value.

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7. Vf = Most negative reduction voltage measured for the SERA differentiated/smoothed curve.
8. Qt = Total reduction charge (summation of Q1 + Q2 + Q3) for the SERA differentiated/smoothed curve.

Threshold constraints:

- a. Constant = First point on curve for measured voltage before applying current.
- b. Nmin1 = First point on curve where measured voltage < -0.85 volts.
- c. Nmin3 = Minimum calculated dVoltage between N1 and N2.
N1 = First point between Nmin1 and N2 where calculated Dvoltage < -0.003 volts.
N2 = Last point on curve where measured voltage < -1.3 volts.
- d. Nmin5 = Last point on curve where calculated Dvoltage < -1.3 volts.

Unless otherwise agreed upon by the printed wiring board fabricator and user, the SERA parameter for V2 shall meet the minimum acceptable value listed in table XI. The other seven SERA parameters shall be within the ranges listed in table XII for a ROM0 or ROM1 flux in accordance with J-STD-004. The printed wiring board soldering performance in the manufacturing process will be directly related to the specific flux used in the soldering process. It is the printed wiring board users responsibility to document the critical SERA parameter levels for other specific flux systems.

TABLE XI. Minimum acceptable V2 value.

| SERA parameter | Minimum acceptable value |
|----------------|--|
| V2 | Equal to or more positive than -1.07 V |

TABLE XII. SERA values for ROM0 or ROM1 flux in accordance with J-STD-004.

| SERA parameter | Minimum acceptable value |
|----------------|-------------------------------------|
| Voc | -0.461 to -0.613 V |
| Q1 | 0.0 to +1.312 mC/cm ² |
| Q2 | 0.0 to +3.823 mC/cm ² |
| Q3 | 0.0 to +3.299 mC/cm ² |
| V3 | -1.29 to -1.412 V |
| Vf | -1.365 to -1.466 V |
| Qt | +2.005 to +5.985 mC/cm ² |

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E.5.5 Proper post test preparation of SERA system.

- a. Shut off inert gas flow into system.
- b. Shut off digital multimeter and programmable current source.
- c. Remove SCE reference electrode, rinse with deionized water and wipe clean with clean soft cloth. Place SCE reference electrode in storage container.
- d. Remove reference electrode port and dump out borate buffer solution. Rinse inner and outer surfaces of reference electrode port with deionized water. Replace reference electrode port into system.
- e. Remove o-rings and dispose of as required (see E.4.1.2). Rinse test head o-ring seal with deionized water and wipe dry with clean soft cloth.
- f. Empty reservoir of borate buffer solution, rinse with deionized water, and refill with buffer solution as required (see E.4.1.1).

E.6. NOTES

E.6.1 Note. The equipment described herein is a result of a United States Army MANTECH Program investment. SERA is a scientific means of measuring solderability of circuit boards and components. The technology is based upon measurements of the type and quantity of oxides using SERA method. Rockwell International at Thousand Oaks, CA is the patent holder, and the United States Army MANTECH Program was successful in developing, proving, commercializing, and standardizing the equipment and processes. Round robin tests by a government-industry team were successfully completed in the standardization effort. The United States Army has a perpetual royalty free license and the equipment is currently on a number of weapons production lines. The technical point of contact for future inquiries should be directed to the sole source supplier:

ECI Technology
1 Madison Street
East Rutherford, NJ 07073

Phone: (973) 773-8686
Facsimile: (973) 773-8797
Electronic mail: ecitechnology@eci.com
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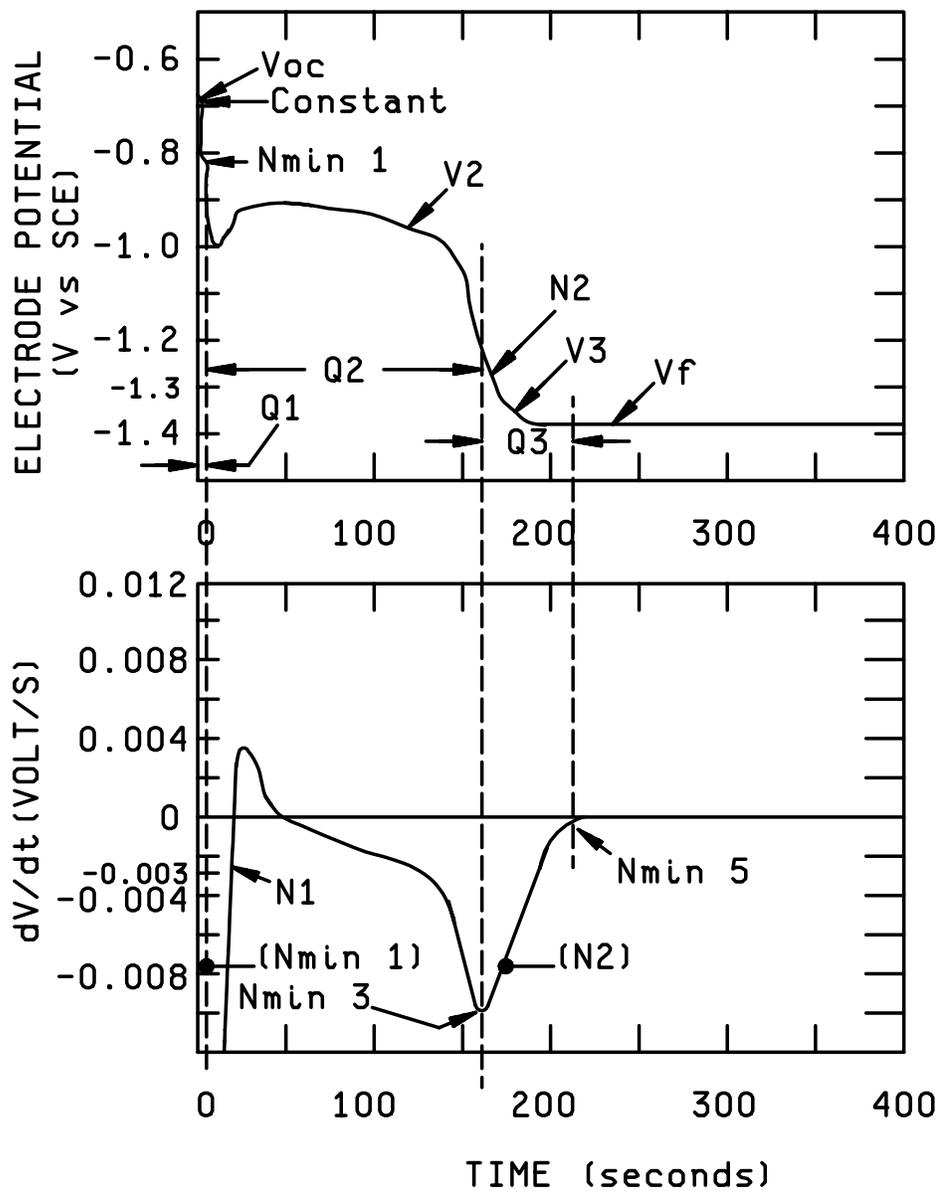


FIGURE 4. Example SERA differentiated/smoothed curve.

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w/AMENDMENT 2

Custodians:
Army – CR
Navy – EC
Air Force – 11
DLA – CC

Preparing activity:
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Army – AR, MI
Navy – AS, MC, OS, SH, TD
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