

The documentation and process conversion measures necessary to comply with this revision shall be completed by 26 November 2016.

INCH-POUND

MIL-PRF-19500/732E
26 August 2016
SUPERSEDING
MIL-PRF-19500/732D
8 October 2014

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT RADIATION HARDENED,
P-CHANNEL, SILICON, THROUGH-HOLE AND SURFACE MOUNT,
TYPES 2N7519 AND 2N7520, QUALITY LEVELS JANTXV AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for a P-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance (JANTXV and JANS) are provided for each device type as specified in [MIL-PRF-19500](#), with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}) for use in particular power-switching applications. See 6.7 for JANHC and JANKC die versions. Provisions for radiation hardness assurance (RHA) to two radiation levels ("R" and "F") are provided for JANTXV and JANS product assurance levels.

* 1.2 Package outlines. The device package outlines are as follows: TO-257AA (T3) in accordance with [figure 1](#), SMD 5 TO-276AA (U3 or ceramic lid U3C) in accordance with [figure 2](#), and a modified (tabless) TO-257AA in accordance with [figure 3](#), for all encapsulated device types. The dimensions and topography for JANHC and JANKC unencapsulated die are as listed in slash sheet [MIL-PRF-19500/741](#).

* 1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Type	P _T (1) T _C = +25°C	P _T T _A = +25°C	R _{θJC} (2)	V _{DS}	V _{DG}	V _{GS}	I _{D1} (3) (4) T _C = +25°C	I _{D2} (3) (4) T _C = +100°C	I _S	I _{DM} (5)	T _J and T _{STG}
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A(pk)	°C
2N7519U3, 2N7519U3C	75	1.56	1.67	-30	-30	±20	-22	-18	-22	-88	-55 to
2N7520U3, 2N7520U3C	75	1.56	1.67	-60	-60	±20	-21	-13.3	-21	-84	+150
2N7519T3, D5	75	1.56	1.67	-30	-30	±20	-20	-18	-20	-80	
2N7520T3, D5	75	1.56	1.67	-60	-60	±20	-20	-13	-20	-80	

- (1) Derate linearly 0.6 W/°C for $T_C > +25^\circ\text{C}$.
- (2) See [figure 4](#), thermal impedance curves.
- (3) The following formula derives the maximum theoretical I_D specs. I_D is limited by package and device construction to 20 A for TO-257AA (T3, D5) and to 22 A for TO-276AA:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

- (4) See [figure 5](#), maximum drain current graph.
- (5) $I_{DM} = 4 \times I_{D1}$ as defined in note (3).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

AMSC N/A

FSC 5961



* 1.4 Primary electrical characteristics at T_c = +25°C.

Type	Min V _{(BR)DSS} V _{GS} = 0 I _D = 1.0 mA dc	V _{GS} (TH)1 V _{DS} ≥ V _{GS} I _D = 1.0 mA dc		Max I _{DSS1} V _{GS} = 0 V _{DS} = 80 percent of rated V _{DS}	Max r _{DS(on)} (1) V _{GS} = 12 V dc		EAS at I _{D1}	I _{AS}
					T _J = +25°C at I _{D2}	T _J = +150°C at I _{D2}		
	V dc	V dc		μA dc	ohm	ohm	mJ	A
		Min	Max					
2N7519U3, 2N7519U3C	-30	-2.0	-4.0	-10	0.070	0.091	152	-22
2N7520U3, 2N7520U3C	-60	-2.0	-4.0	-10	0.085	0.170	110	-21
2N7519T3, D5	-30	-2.0	-4.0	-10	0.072	0.094	200	-20
2N7520T3, D5	-60	-2.0	-4.0	-10	0.087	0.180	134	-20

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANTXV" and "JANS".

1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "R" and "F".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7519" and "7520".

* 1.5.4 Suffix symbols. The following suffix symbols are incorporated in the PIN for this specification sheet:

T3	Indicates a through-hole mount package similar to a TO-257AA (see figure 1).
U3	Indicates a 3 pad surface mount package similar to a TO-276AA (SMD-0.5) (see figure 2).
U3C	Indicates a 3 pad ceramic lid surface mount package similar to a TO-276AA (SMD-0.5) (see figure 2).
D5	Indicates a through hole mount package similar to a tabless TO-257AA (see figure 3)

* 1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <http://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as specified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

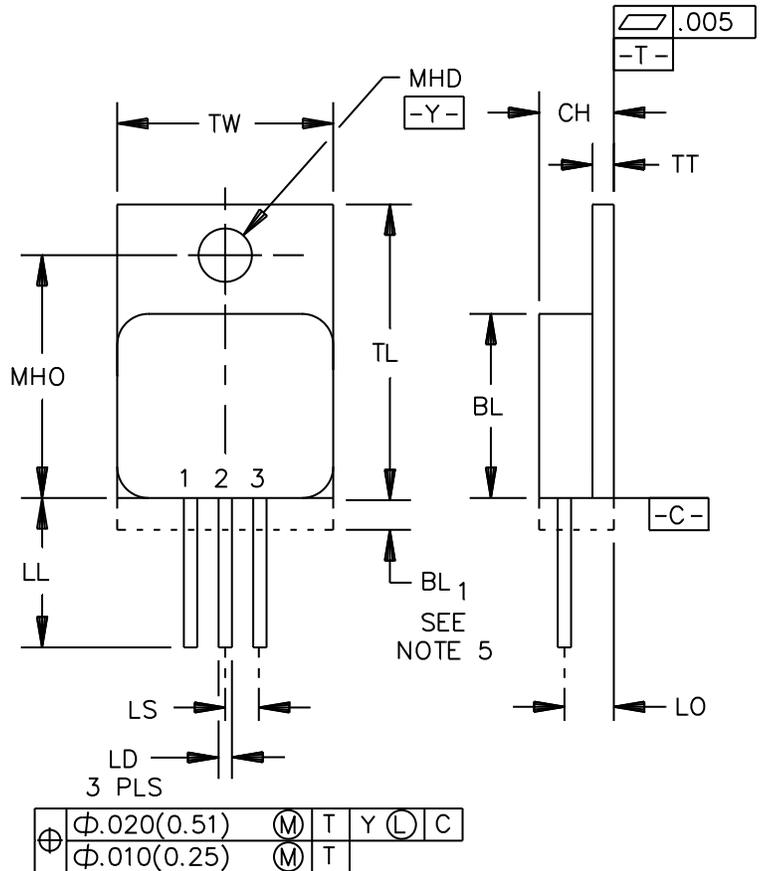
3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

* 3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and on [figures 1](#) (T3, TO-257AA), [2](#) (U3, surface mount TO-276AA), and [3](#) (D5, tabless TO-257AA) herein.

3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Pin-out. The pin-out of the device shall be as shown on [figure 1](#) and [figure 2](#).

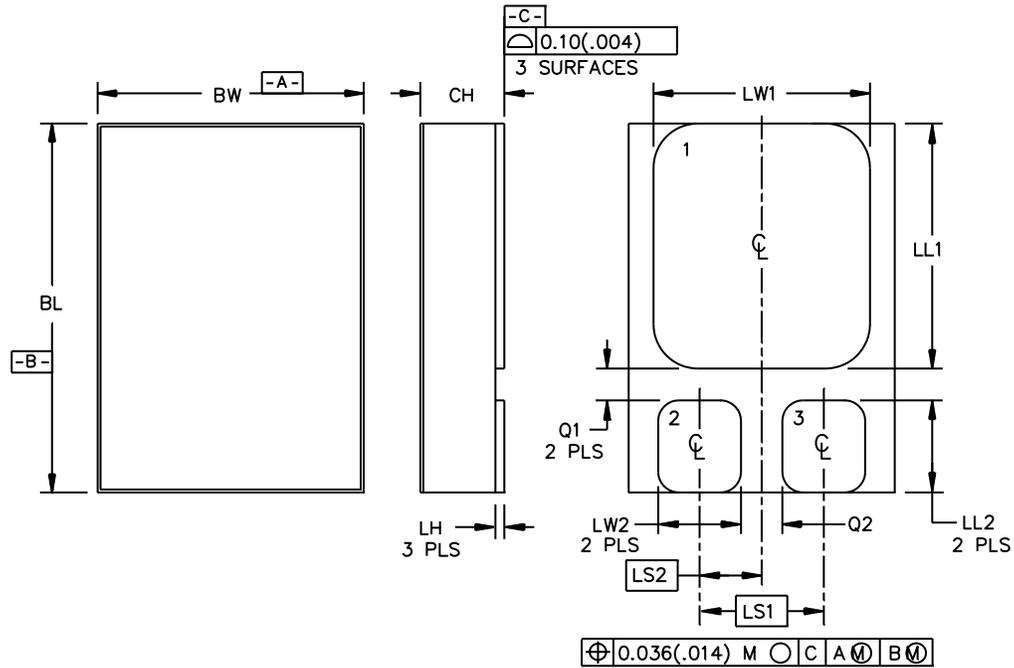
Dimensions				
Ltr	Inches		Millimeters	
	Min	Max	Min	Max
BL	.410	.430	10.41	10.92
BL ₁		.033		0.84
CH	.190	.200	4.83	5.08
LD	.025	.035	0.64	0.89
LL	.600	.650	15.24	16.51
LO	.120 BSC		3.05 BSC	
LS	.100 BSC		2.54 BSC	
MHD	.140	.150	3.56	3.81
MHO	.527	.537	13.39	13.64
TL	.645	.665	16.38	16.89
TT	.035	.045	0.89	1.14
TW	.410	.420	10.41	10.67
Term 1	Drain			
Term 2	Source			
Term 3	Gate			



NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. All terminals are isolated from the case.
3. This area is for the lead feed-thru eyelets (configuration is optional, but will not extend beyond this zone).
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions for TO-257AA (2N7519T3 and 2N7520T3).

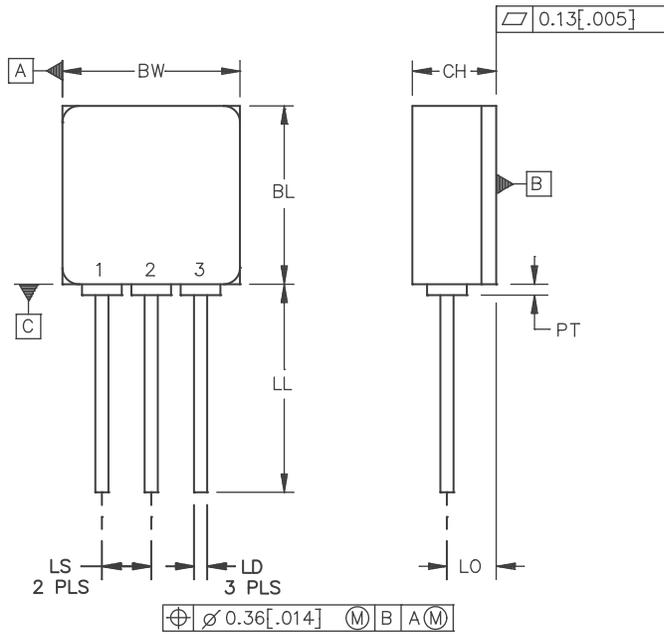


Ltr.	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.03	10.29
BW	.291	.301	7.39	7.64
CH (for U3)		.124		3.15
CH (for U3C)		.134		3.40
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.92	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.
3. Terminal 1 - Drain, Terminal 2 - Gate, Terminal 3 - Source.

FIGURE 2. Physical dimensions for SMD.5 TO-276AA (2N7519U3, 2N7519U3C, 2N7520U3, and 2N7520U3C).



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.410	.430	10.42	10.92	
BW	.410	.420	10.42	10.67	
CH	.190	.200	4.83	5.08	
LD	.025	.035	0.64	0.88	
LL	.500	.625	12.7	15.88	3
LO	.120 BSC		3.05 BSC		
LS	.100 BSC		2.54 BSC		
PT		.028		0.71	3
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Protrusion thickness (PT) of ceramic eyelets included in dimension LL.
4. All terminals are isolated from case.
5. In accordance with ASME Y14.5M, diameters are equivalent to $\varnothing x$ symbology.

* FIGURE 3. Physical dimensions for TO-257AA tabless package (2N7519D5 and 2N7520D5).

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics shall be as specified in [1.3](#), [1.4](#), and [table I](#) herein.

3.7 Workmanship. Transistors shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. See the design safe operation area figures herein. Electrical measurements (end-points) shall be in accordance with [table III](#) herein.

* 4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV level
(3)	Gate stress test (see 4.5.3)	Gate stress test (see 4.5.3)
(3)	Method 3470 of MIL-STD-750, E _{AS} (see 4.5.4)	Method 3470 of MIL-STD-750, E _{AS} (see 4.5.4)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.5.2)	Method 3161 of MIL-STD-750, thermal impedance (see 4.5.2)
(1) 9	Subgroup 2 of table I herein; I _{GSSF1} , I _{GSSR1} , I _{DSS1}	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein; I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(on)1} , V _{GS(TH)1} . Δ I _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. Δ I _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. Δ I _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein; I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(on)1} , V _{GS(TH)1}
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein; Δ I _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. Δ I _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. Δ I _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δ r _{DS(on)1} = ± 20 percent of initial value. Δ V _{GS(TH)1} = ±20 percent of initial value.	Subgroups 2 and 3 of table I herein; Δ I _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. Δ I _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. Δ I _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δ r _{DS(on)1} = ±20 percent of initial value. Δ V _{GS(TH)1} = ±20 percent of initial value.
17	For TO-257 and U3 packages: Method 1081 of MIL-STD-750 (see 4.5.5), Endpoints: Subgroup 2 of table I herein.	For TO-257 and U3 packages: Method 1081 of MIL-STD-750 (see 4.5.5), Endpoints: Subgroup 2 of table I herein.

- (1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
- * (2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, r_{DS(on)1}, and V_{GS(th)1} shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#), and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#) and [table I](#) herein. End-point electrical measurements shall be in accordance with [table I](#), subgroup 2 herein

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of [MIL-PRF-19500](#), and herein.

4.4.2.1 Quality level JANS (table E-VIA of [MIL-PRF-19500](#)).

<u>Subgroup</u>	<u>Method</u>	<u>Inspection</u>
B3	1051	Test condition G, 100 cycles.
B3	2077	Scanning electron microscope (SEM) qualification may be performed anytime prior to lot formation.
B4	1042	Condition D. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5	1042	Test condition B, $V_{GS} = \text{rated}$; $T_A = +175^{\circ}\text{C}$; $t = 24$ hours.
B5	1042	Test condition A, $V_{DS} = \text{rated}$; $T_A = +175^{\circ}\text{C}$; $t = 120$ hours.
B5	2037	Bond strength, test condition D.

4.4.2.2 Quality level JANTXV (table E-VIB of [MIL-PRF-19500](#)).

<u>Subgroup</u>	<u>Method</u>	<u>Inspection</u>
B2	1051	Test condition G, 25 cycles. (45 total, including 20 cycles performed in screening).
B3	1042	Test condition D. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5 and B6		Not applicable.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and herein.

<u>Subgroup</u>	<u>Method</u>	<u>Inspection</u>
C2	2036	Test condition A, weight = 10 lbs (4.54 Kg), $t = 10$ s (applicable to TO-257AA only).
C5	3161	See 4.5.2 , $R_{\theta JC(\text{max})} = 1.67^{\circ}\text{C/W}$.
C6	1042	Test condition D. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse response measurements. The conditions for pulse response measurement shall be as specified in section 4 of MIL-STD-750.

* 4.5.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with test method 3161 of MIL-STD-750 using the guidelines in that test method for determining I_M , I_H , t_H , t_{sw} , (and V_H where appropriate). See table III, subgroup 4 herein.

4.5.3 Gate stress test. Apply $V_{GS} = -24$ V minimum for $t = 250$ μ s minimum.

4.5.4 Single pulse avalanche energy (E_{AS}).

- a. Peak current (I_{AS}) $I_{AS(max)}$.
- b. Peak gate voltage (V_{GS}) 12 V.
- c. Gate to source resistor (R_{GS}) $25\Omega \leq R_{GS} \leq 200\Omega$.
- d. Initial case temperature (T_C) $+25^\circ\text{C}$, $+10^\circ\text{C}$, -5°C .
- e. Inductance (L) $\left[\frac{2E_{AS}}{(I_{DI})^2} \right] \left[\frac{(V_{BR} - V_{DD})}{V_{BR}} \right] \text{mH}$ minimum.
- f. Number of pulses to be applied 1 pulse minimum.
- g. Supply voltage (V_{DD}) 25 V.

4.5.5 Dielectric withstanding voltage.

- a. Magnitude of test voltage 800 V dc (TO-257), 600 V dc (U3).
- b. Duration of application of test voltage 15 seconds (min).
- c. Points of application of test voltage All leads to case (bunch connection).
- d. Method of connection Mechanical.
- e. Kilovolt-ampere rating of high voltage source 1,200 V/1.0 mA (min).
- f. Maximum leakage current 1.0 mA.
- g. Voltage ramp up time 500 V/second

*

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance 2/	3161	See 4.5.2	$Z_{\theta JC}$			$^{\circ}C/W$
Breakdown voltage, drain to source	3407	$V_{GS} = 0$ V dc, $I_D = -1$ mA dc, bias condition C	$V_{(BR)DSS}$			
2N7519U3, 2N7519T3 2N7519U3C, 2N7519D5				-30		V dc
2N7520U3, 2N7520T3 2N7520U3C, 2N7520D5				-60		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = -1$ mA dc	$V_{GS(TH)1}$	-2.0	-4.0	V dc
Gate reverse current	3411	$V_{GS} = +20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSF1}		+100	nA dc
Gate reverse current	3411	$V_{GS} = -20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSR1}		-100	nA dc
Drain current	3413	$V_{GS} = 0$ V dc, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS1}		-10	μA dc
Static drain to source on-state resistance	3421	$V_{GS} = -12$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)1}$			
2N7519U3, 2N7519U3C					0.070	Ω
2N7520U3, 2N7520U3C					0.085	Ω
2N7519T3, 2N7519D5					0.072	Ω
2N7520T3, 2N7520D5					0.087	Ω
Forward voltage	4011	Condition A, pulsed (see 4.5.1), $I_D = I_{D1}$, $V_{GS} = 0$ V dc	V_{SD}		-5.0	V
<u>Subgroup 3</u>						
High temperature operation:						
		$T_C = T_J = +125^{\circ}C$				
Gate reverse current	3411	$V_{GS} = -20$ V dc and $+20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSS2}		± 200	nA dc
Drain current	3413	$V_{GS} = 0$ V dc, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS2}		-25	μA dc

See footnotes at end of table.

*

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - Continued						
Static drain to source on-state resistance 2N7519U3, 2N7519U3C 2N7520U3, 2N7520U3C 2N7519T3, 2N7519D5 2N7520T3, 2N7520D5	3421	$V_{GS} = -12$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)3}$			
					0.084	Ω
					0.136	Ω
					0.086	Ω
					0.139	Ω
Gate to source voltage (threshold) Low temperature operation: Gate to source voltage (threshold)	3403 3403	$V_{DS} \geq V_{GS}$, $I_D = -1$ mA dc $T_C = T_J = -55^\circ\text{C}$ $V_{DS} \geq V_{GS}$, $I_b = -1$ mA dc	$V_{GS(TH)2}$ $V_{GS(TH)3}$	-1.0		V dc
					-5.0	V dc
<u>Subgroup 4</u>						
Forward transconductance 2N7519U3, 2N7519U3C, 2N7519T3, 2N7519D5 2N7520U3, 2N7520U3C, 2N7520T3, 2N7520D5	3475	$I_D = \text{rated } I_{D2}$, $V_{DD} = -15$ V (see 4.5.1)	gFS	12		S
Switching time test	3472	$I_D = \text{rated } I_{D1}$, $V_{GS} = -12$ V dc, $R_G = 7.5 \Omega$, $V_{DD} = 50$ percent of rated V_{DS}		10		S
Turn-on delay time			$t_{d(on)}$		25	ns
Rise-time 2N7519U3, 2N7519U3C, 2N7519T3, 2N7519D5 2N7520U3, 2N7520U3C, 2N7520T3, 2N7520D5			t_r		100	ns
Turn-off delay time 2N7519U3, 2N7519U3C, 2N7519T3, 2N7519D5 2N7520U3, 2N7520U3C, 2N7520T3, 2N7520D5			$t_{d(off)}$		65	ns
Fall time 2N7519U3, 2N7519U3C, 2N7519T3, 2N7519D5 2N7520U3, 2N7520U3C, 2N7520T3, 2N7520D5			t_f		50	ns
					75	ns
					70	ns
					50	ns

See footnotes at end of table.

*

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u> Safe operating area test (high voltage) Electrical measurements	3474	See figure 6 ; $t_p = 10$ ms, $V_{DS} = 80$ percent of rated V_{DS} See table I , subgroup 2 herein.				
<u>Subgroup 6</u> Not applicable						
<u>Subgroup 7</u> Gate charge	3471	Condition B	$Q_{G(on)}$		45	nC
2N7519U3, 2N7519U3C, 2N7519T3, 2N7519D5						
On-state gate charge			Q_{GS}		20	nC
2N7519U3, 2N7519U3C, 2N7519T3, 2N7519D5						
Gate to drain charge			Q_{GD}		18	nC
2N7520U3, 2N7520U3C, 2N7520T3, 2N7520D5						
Reverse recovery time	3473	$di/dt \leq 100A/\mu s$, $I_D = I_{D1}$ $V_{DD} \leq 30$ V $V_{DD} \leq 50$ V	t_{rr}		75	ns
2N7519U3, 2N7519U3C, 2N7519T3, 2N7519D5						
2N7520U3, 2N7520U3C, 2N7520T3, 2N7520D5					100	ns

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ This test required for the following end-point measurements only:

- Group B, subgroups 3 and 4 (JANS).
- Group B, subgroups 2 and 3 (JANTXV).
- Group C, subgroup 2 and 6.
- Group E, subgroup 1.

*

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/			Symbol	Pre-irradiation limits		Post-irradiation limits		Post-irradiation limits		Unit
	Method	Conditions		R, F		R		F		
				Min	Max	Min	Max	Min	Max	
<u>Subgroup 1</u>										
Not applicable										
<u>Subgroup 2</u>		$T_C = +25^\circ\text{C}$								
Steady-state total dose irradiation (V_{GS} bias) 4/	1019	$V_{GS} = -12\text{V}$ $V_{DS} = 0$								
Steady-state total dose irradiation (V_{DS} bias) 4/	1019	$V_{GS} = 0$ $V_{DS} = 80$ percent of rated V_{DS} (pre-irradiation)								
End-point electricals:										
Breakdown voltage, drain to source	3407	$V_{GS} = 0$ $I_D = -1$ mA bias condition C	$V_{(BR)DSS}$							
2N7519U3, 2N7519U3C, 2N7519T3, 2N7519D5				-30		-30		-30		V dc
2N7520U3, 2N7520U3C, 2N7520T3, 2N7520D5				-60		-60		-60		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	$V_{GS(th)1}$	-2.0	-4.0	-2.0	-4.0	-2.0	-5.0	V dc
Gate reverse current	3411	$V_{GS} = -20$ V $V_{DS} = 0$ bias condition C	I_{GSSR1}		-100		-100		-100	nA dc
Gate forward current	3411	$V_{GS} = 20$ V $V_{DS} = 0$ bias condition C	I_{GSSF1}		100		100		100	nA dc
Drain current	3413	$V_{GS} = 0$ bias condition C $V_{DS} = 80$ percent of rated V_{DS} (pre-irradiation)	I_{DSS1}		-10		-10		-10	μA dc

See footnotes at end of table.

*

TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Post-irradiation limits		Unit
	Method	Conditions		R, F		R		F		
				Min	Max	Min	Max	Min	Max	
Static drain to source on-state voltage	3405	$V_{GS} = -12$ V condition A pulsed (see 4.5.1) $I_D = I_{D2}$	$V_{DS(on)1}$							
2N7519U3 2N7519U3C					1.296		1.296		1.296	V dc
2N7520U3 2N7520U3C					1.157		1.157		1.157	V dc
2N7519T3 2N7519D5					1.296		1.296		1.296	V dc
2N7520T3 2N7520D5					1.131		1.131		1.131	V dc
* Forward voltage source to drain diode	4011	Condition A, $V_{GS} = 0$ $I_D = I_{D1}$	V_{SD}		-5.0		-5.0		-5.0	V dc

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package, or in any qualified package, that the manufacturer has data to correlate the performance to the designated package.

4/ Separate samples shall be pulled for each bias.

TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles	
Hermetic seal	1071	As applicable	
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	

1/ A separate sample for each test shall be pulled.

2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

3/ The sampling plan applies to each bias condition.

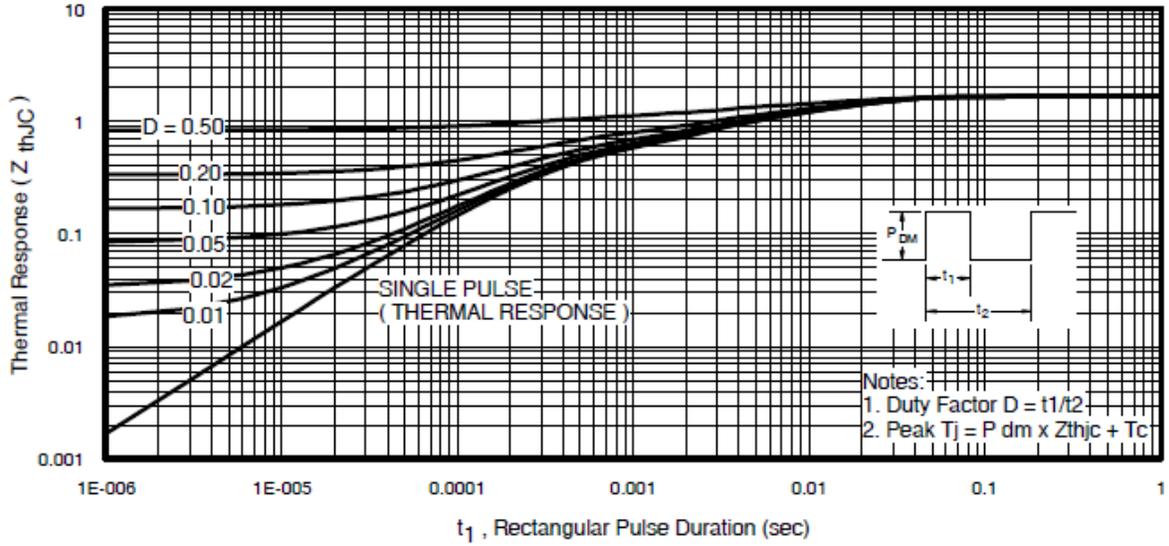
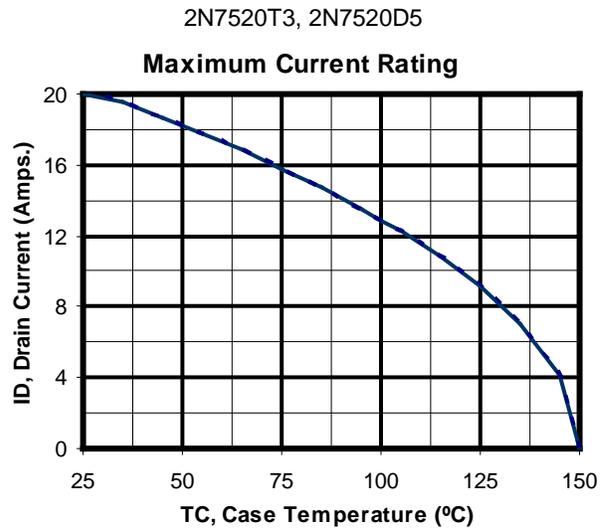
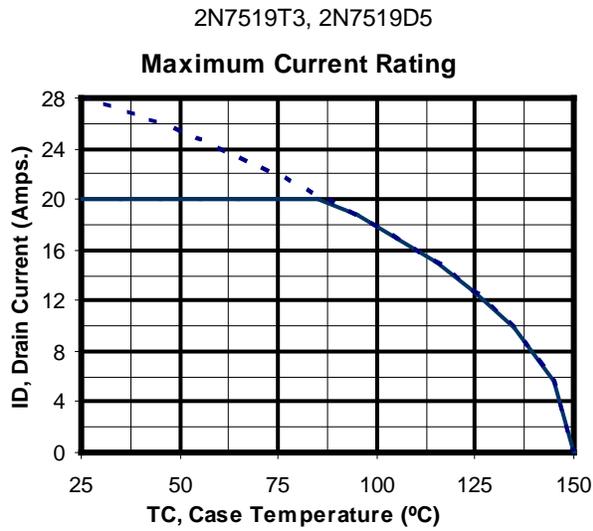
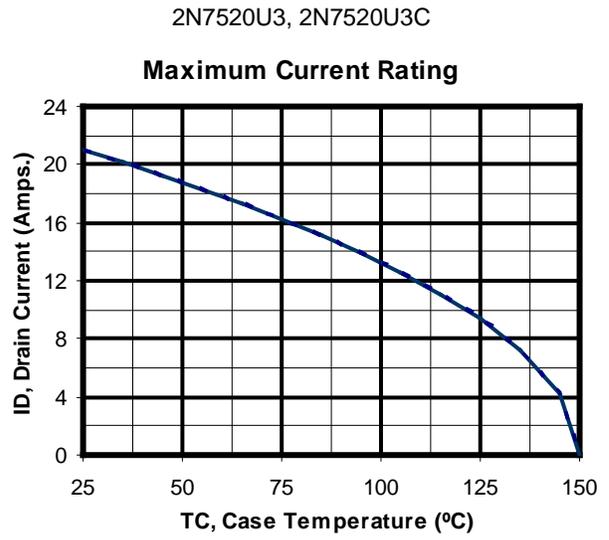
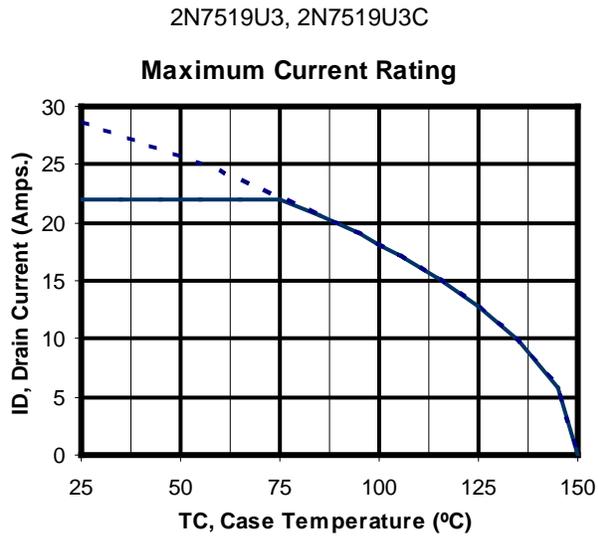
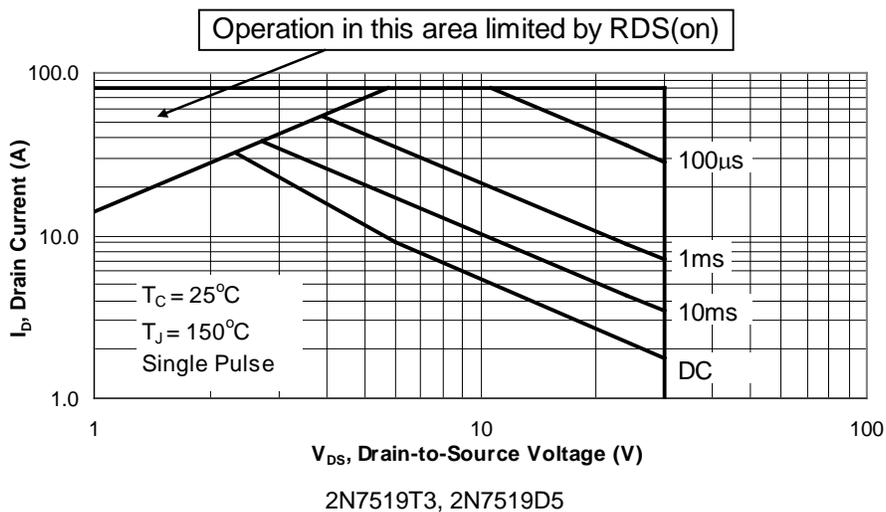
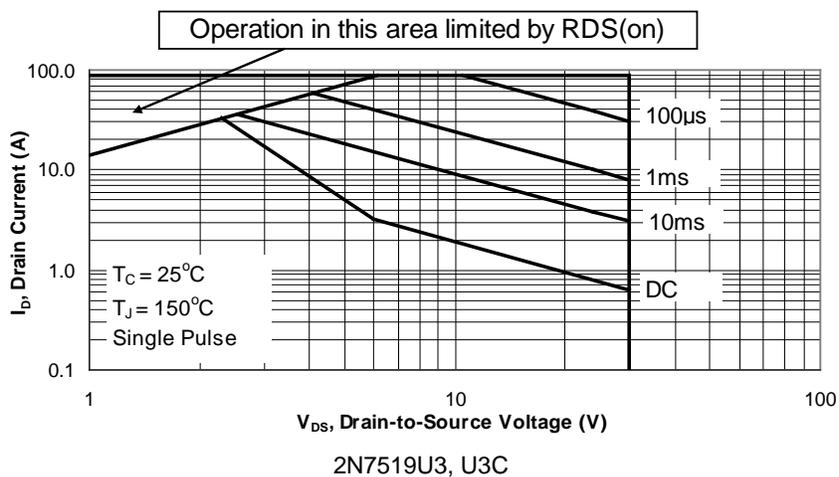


FIGURE 4. Thermal impedance curves.



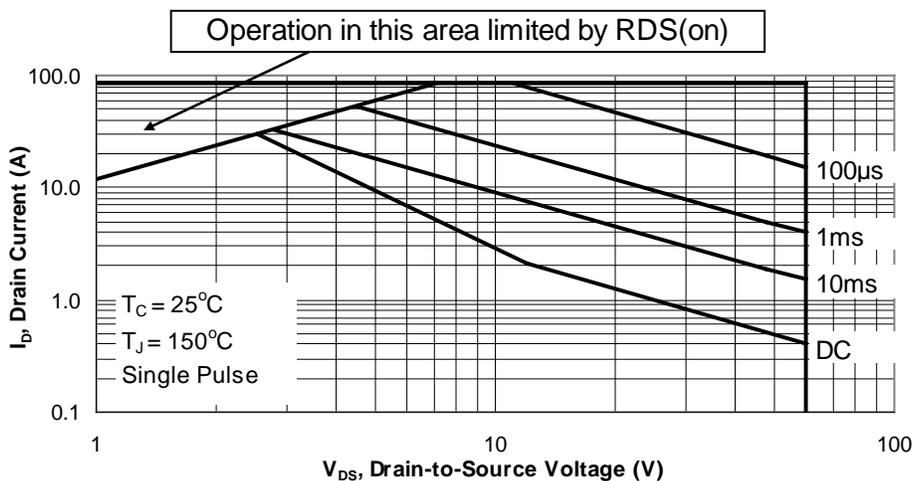
*

FIGURE 5. Maximum drain current versus case temperature graphs.

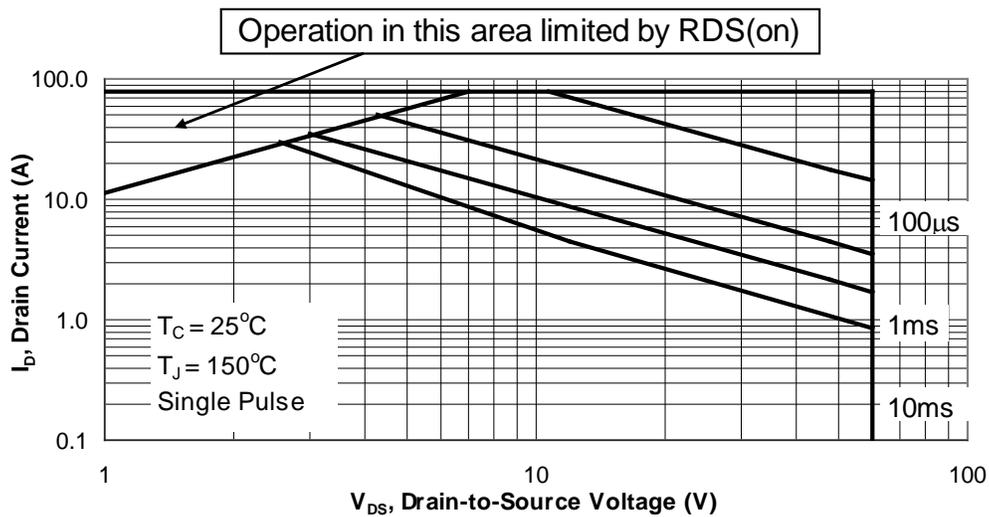


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FIGURE 6. Safe operating area graph.



2N7520U3 an U3C



2N7520T3, 2N7520D5

*

FIGURE 6. Safe operating area graph. - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

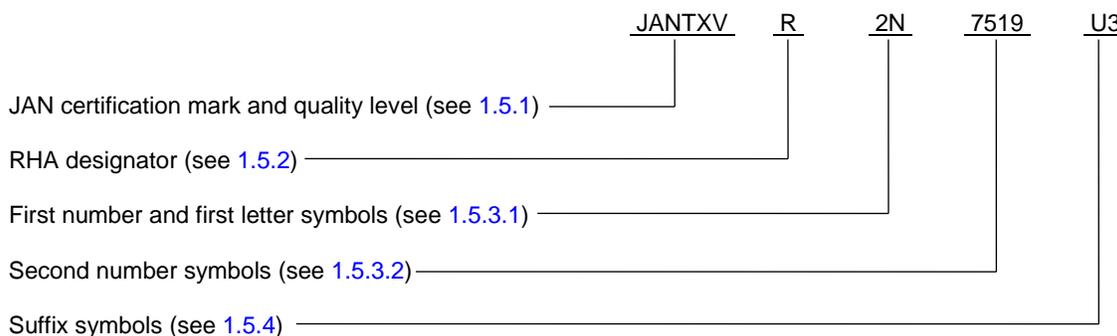
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see [3.4.1](#)).
- d. The complete Part or Identifying Number (PIN), see [1.5](#) and [6.4](#).
- e. For acquisition of RHA designated devices, [table II](#), subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.
- f. If specific SEE characterization conditions are desired (see section [6.8](#) and [table IV](#)), manufacturer's cage code should be specified in the contract or order.
- g. If SEE testing data is desired, it should be specified in the contract or order.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List ([QML 19500](#)) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



* 6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7519D5	JANTXV#2N7519D5	JANS2N7519D5	JANS#2N7519D5
JANTXV2N7519T3	JANTXV#2N7519T3	JANS2N7519T3	JANS#2N7519T3
JANTXV2N7519U3	JANTXV#2N7519U3	JANS2N7519U3	JANS#2N7519U3
JANTXV2N7519U3C	JANTXV#2N7519U3C	JANS2N7519U3C	JANS#2N7519U3C
JANTXV2N7520D5	JANTXV#2N7520D5	JANS2N7520D5	JANS#2N7520D5
JANTXV2N7520T3	JANTXV#2N7520T3	JANS2N7520T3	JANS#2N7520T3
JANTXV2N7520U3	JANTXV#2N7520U3	JANS2N7520U3	JANS#2N7520U3
JANTXV2N7520U3C	JANTXV#2N7520U3C	JANS2N7520U3C	JANS#2N7520U3C

(1) The number sign (#) represents one of two RHA designators available (R or F).

6.6 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types (military PIN)	Commercial PIN		
	TO-257AA	TO-276AA (SMD-0.5)	TO-276AA (SMD-0.5) with ceramic lid
2N7519U3		IRH NJ597Z30	
2N7520U3		IRH NJ597034	
2N7519T3	IRHYS597Z30CM		
2N7520T3	IRHYS597034CM		
2N7519U3C			IRH NJC597Z30
2N7520U3C			IRH NJC597034

* 6.7 JANHC and JANKC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet [MIL-PRF-19500/741](#).

6.8 Application data.

6.8.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see [table IV](#)) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

*

TABLE IV. Manufacturers characterization conditions.

Manufacturers CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of September 2009 and older)	SEE <u>1/</u>	1080	See MIL-STD-750 method 1080	3 devices
	Electrical measurements		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I , subgroup 2	
	SEE irradiation:		Fluence = $3E5 \pm 20$ percent ions/cm ² , flux = $2E3$ to $2E4$ ions/cm ² /sec, temperature = $25 \pm 5^\circ\text{C}$ Surface LET = $38 \text{ MeV}\cdot\text{cm}^2/\text{mg} \pm 5\%$, range = $35 \mu\text{m} \pm 7.5\%$, energy = $270 \text{ MeV} \pm 7.5\%$	
	2N7519D5, 2N7519U3, 2N7519U3C, and 2N7519T3		In situ bias conditions: $V_{DS} = -30 \text{ V}$ and $V_{GS} = 20 \text{ V}$, (nominal 3.42 MeV/nucleon at Texas A & M Cyclotron)	
	2N7520D5, 2N7520U3, 2N7520U3C, and 2N7520T3		In situ bias conditions: $V_{DS} = -60 \text{ V}$ and $V_{GS} = 20 \text{ V}$, (nominal 3.86 MeV/nucleon at Brookhaven National Lab Accelerator) Surface LET = $61 \text{ MeV}\cdot\text{cm}^2/\text{mg} \pm 5\%$, range = $31 \mu\text{m} \pm 10\%$, energy = $330 \text{ MeV} \pm 7.5\%$	
	2N7519D5, 2N7519U3, 2N7519U3C, and 2N7519T3		In situ bias conditions: $V_{DS} = -30 \text{ V}$ and $V_{GS} = 15 \text{ V}$, $V_{DS} = -25 \text{ V}$ and $V_{GS} = 20 \text{ V}$, (nominal 2.53 MeV/nucleon at Texas A & M Cyclotron)	
2N7520D5, 2N7520U3, 2N7520U3C, and 2N7520T3		In situ bias conditions: $V_{DS} = -60 \text{ V}$ and $V_{GS} = 10 \text{ V}$, $V_{DS} = -45 \text{ V}$ and $V_{GS} = 15 \text{ V}$, $V_{DS} = -25 \text{ V}$ and $V_{GS} = 20 \text{ V}$, (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator) Surface LET = $84 \text{ MeV}\cdot\text{cm}^2/\text{mg} \pm 5\%$, range = $28 \mu\text{m} \pm 7.5\%$, energy = $350 \text{ MeV} \pm 10\%$		

See footnotes at end of table.

*

TABLE IV. Manufacturers characterization conditions (continued).

Manufacturers CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of September 2009 and older)	SEE <u>1/</u>	1080	See MIL-STD-750 method 1080	3 devices
	Electrical measurements		I _{GSS1} and I _{DSS1} in accordance with table I , subgroup 2	
	SEE irradiation:		Fluence = 3E5 ±20 percent ions/cm ² , flux = 2E3 to 2E4 ions/cm ² /sec, temperature = 25 ±5°C	
	2N7519D5, 2N7519U3, 2N7519U3C, and 2N7519T3		Surface LET = 38 MeV-cm ² /mg ± 5%, range = 35 μm ±7.5%, energy = 270 MeV ±7.5%	
	2N7520D5, 2N7520U3, 2N7520U3C, and 2N7520T3 Electrical measurements		In situ bias conditions: V _{DS} = -30 V and V _{GS} = 10 V, V _{DS} = -25 V and V _{GS} = 15 V, (nominal 1.74 MeV/nucleon at Texas A & M Cyclotron)	
			In situ bias conditions: V _{DS} = -60 V and V _{GS} = 10 V, (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator)	
			I _{GSS1} and I _{DSS1} in accordance with table I , subgroup 2	
<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;"> Upon qualification, all manufacturers will provide the verification test conditions to be added to this table. </div>				

1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with [table I](#), subgroup 2, may be performed at the manufacturer's option.

* 6.9 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

6.10 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC
(Project 5961-2016-074)

Review activity:
Army- MI
Air Force - 99

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