METRIC

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MILITARY HANDBOOK

ELECTROSTATIC DISCHARGE CONTROL HANDBOOK FOR PROTECTION OF ELECTRICAL AND ELECTRONIC PARTS, ASSEMBLIES AND EQUIPMENT (EXCLUDING ELECTRICALLY INITIATED EXPLOSIVE DEVICES) (METRIC)

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FOREWORD

1. This military handbook is approved for use by all Departments and Agencies of the Department of Defense.

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Naval Sea Systems Command, SEA 91Q22, 2531 Jefferson Davis Highway, Arlington, Virginia 22242-5160, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

3. This handbook provides guidance, not mandatory requirements, for the establishment and implementation of an Electrostatic Discharge (ESD) Control Program in accordance with the requirements of MIL-STD-1686. This document is applicable to the protection of electrical and electronic parts, assemblies and equipment from damage due to ESD. It does not provide information for the protection of electrically initiated explosive devices.

4. Various segments of industry are aware of the damage static electricity can impose on metal oxide semiconductor (MOS) parts. The sensitivity of other parts to electrostatic discharge damage has also become evident through use, testing, and failure analysis. Trends in technology utilizing new materials, processes and design techniques, including increased packaging densities result in some parts being more susceptible to ESD.

5. Electrical and electronic parts which have been determined to be ESD sensitive (ESDS) include: microelectronic discrete and integrated semiconductor devices; thick and thin film resistors, chips and hybrid devices; and piezoelectric crystals. Subassemblies, assemblies and equipment containing these parts are also ESDS.

6. Materials which are prime generators of electrostatic voltages include, but are not limited to, common plastics such as polyethylene, vinyls, foam, polyurethane, synthetic textiles, fiberglass, glass, rubber, and other commonly used materials. Damaging electrostatic voltage levels are commonly generated by contact and subsequent separation of these materials by industrial processes and personnel movement.

7. Intense pressure has existed, and continues to exist, for a "cook book" approach to ESD control program implementation. Simplistic approaches to a complex technical subject such as electrostatic discharge control program design and implementation are neither desirable, cost effective nor feasible. A single "cook book" ESD control program cannot be mandated or prepared which is applicable for all situations. An "idealized" ESD control program may represent overkill for most applications. In contrast, a less rigorous

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program may not offer sufficient or adequate protection in all situations. Therefore, an ESD control program must be custom-tailored to meet the specific requirements of the preparer for their specific product in its unique manufacturing facility and expected environments. The ESD control program plan (data item description (DID) DI-RELI-80669A) is developed to establish efficient and cost effective ESD controls and procedures. The ESD control program plan provides the opportunity to tailor the technical approach for implementation of ESD controls in a meaningful and cost effective manner.

8. The protection of ESDS parts, subassemblies, assemblies and equipment will be provided through the implementation of cost effective ESD controls. The lack of implementation of ESD controls and procedures throughout the equipment life-time has resulted in increased repair costs, equipment downtime, and reduced mission readiness.

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1. SCOPE

1.1 Scope. This handbook provides guidance for developing, implementing and monitoring an ESD control program in accordance with the requirements of MIL-STD-1686. Information is provided in 6.1 that cross references the various revisions of MIL-HDBK-263 to the appropriate revision of MIL-STD-1686. This handbook is not applicable to electrically initiated explosive devices. The specific guidance provided is supplemented by the technical data contained in the appendices. Table I provides a cross-reference listing of MIL-STD-1686 requirements, MIL-HDBK-263 guidance, and MIL-HDBK-263 supplementary technical data.

TABLE I. Cross-reference table.

MIL-STD-1686B Requirement section	MIL-HDBK-263B Guidance section	MIL-HDBK-263B Supplementary technical data appendix
1.3	1.2	--
1.3.1	1.2.1, 1.3	--
1.3.1.1	1.3	--
4.1	4.1	--
4.2	1.3.2, 5.1, 5.5	--
5.1	5.1	--
5.1.1	5.1	--
5.2	5.2	B, D
5.2.1.1	5.2.1	B, D
5.2.1.2	5.2.2	D
5.3	5.3	E
5.3.1	5.3.1	E
5.3.2	5.3.2	E
5.4	5.4	F, G, H, I

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TABLE I. Cross-reference table - Continued.

MIL-STD-1686B Requirement section	MIL-HDBK-263B Guidance section	MIL-HDBK-263B Supplementary technical data appendix
5.5	5.5	H
5.5.1	5.5	H
5.6	5.6	I
5.7	5.7	J
5.8	5.8	--
5.8.1	5.8	--
5.8.2	5.8.1	--
5.8.3	5.8.2	--
5.8.3.1	5.8.3	--
5.9	5.9	--
5.9.1	5.9	--
5.9.2	5.9	--
5.10	5.10	I
5.11	5.11	H, K
5.11.1	5.11	H, K
5.11.2	5.11	H, K
5.12	5.12	H, K
5.12.1	5.12	E, F
5.12.2	5.12	E, F
5.13	5.13	B, C

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1.2 Application of MIL-STD-1686. The application of MIL-STD-1686 requirements will result in continuous ESD controls throughout the life-time of ESD susceptible parts, assemblies, and equipment. For this reason, MIL-STD-1686 requirements will be applied to Government and contractor activities including subcontractors, suppliers, and vendors. The term "contractor" in MIL-STD-1686 will be replaced with "Government activity" as appropriate when the requirements are applied to the Government.

1.2.1 MIL-STD-1686 application considerations. Effective application of MIL-STD-1686 requirements mandates careful consideration of the technical and cost impacts associated with each acquisition type. Proper application of MIL-STD-1686 requirements must address three considerations: tailoring, mission critical or essential equipment, and reacquisition requirements. Each of these considerations is related. Tailoring of MIL-STD-1686 is directly related to the work efforts to be performed. As an example, an acquisition that is initiated for new design hardware items should incorporate all elements required by MIL-STD-1686 (see table I of MIL-STD-1686). In contrast to this, reacquisition of hardware items not previously subject to an ESD control program should delete the MIL-STD-1686 requirement for design protection. Redesign of hardware for reacquisitions is generally not cost effective. This also applies in the case of Government acquisition of non-developmental items (NDI) or commercial off-the-shelf (COTS) electronic equipment. In these cases, redesign of NDI or COTS electronic equipment to conform to MIL-STD-1686 design hardening requirements (if invoked) would negate the cost benefits of NDI/COTS acquisition. Closely related to these topics is the inclusion of class 3 parts, assemblies, and equipment in the ESD control program. This aspect of ESD control is solely at the discretion of the acquiring activity and should be invoked only for equipment designated by the acquiring activity as mission critical or essential.

1.3 Tailoring of MIL-STD-1686. MIL-STD-1686, as discussed above, is applied to both Government and contractors to ensure ESD controls are continuously provided throughout the life-time of ESD susceptible parts, assemblies, and equipment. When MIL-STD-1686 is contractually invoked the initial step that should be performed by the contractor is a contract review to determine if any part of the acquisition has been designated as mission critical or essential equipment by the acquiring activity. If this has been done, MIL-STD-1686, 1.3.1.1 requires that the ESD control program encompasses not only Class 1 and Class 2 parts, assemblies and equipment but be expanded to also include Class 3 items. This is a first step in the tailoring of MIL-STD-1686.

1.3.1 Contractual review. The second step performed by the contractor in tailoring MIL-STD-1686 should be the completion of a review to determine the exact ESD control program requirements invoked in the contract. MIL-STD-1686, 1.3.1 states "The contractor shall tailor the ESD control program for the acquisition by selecting the applicable functions and elements of Table I." This requirement does not preclude or limit Government tailoring or

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modification of MIL-STD-1686 for a specific acquisition. Contractor review of the contractual document is critical to determining contractual requirements, compliance with contractual requirements and tailoring of MIL-STD-1686 by the contractor. Tailoring of MIL-STD-1686 must always be accomplished in accordance with the contractual requirements.

1.3.2 Deliverable data requirements. The review of the contract or purchase order will also provide a determination of Government Data Requirements (see MIL-STD-1686, 6.2) for the acquisition. When the contract or purchase order requires that an Electrostatic Discharge Control Program Plan be developed and delivered, MIL-STD-1686, 1.3.1 requires that tailoring rationale and data be included in the Plan. Contractor tailoring of MIL-STD-1686 is subject to approval by the acquiring activity and is normally accomplished by formal Government acceptance or rejection of the plan.

1.3.3 Tailoring flow chart. To facilitate the understanding of the MIL-STD-1686 tailoring process Figure 1 graphically depicts the process as discussed above and in MIL-STD-1686, 1.3.1. The reference numbers in the Figure 1 flow chart blocks are the MIL-STD-1686 requirements paragraphs and are included for ready reference. Figure 1 cannot, and does not take precedence over contractual, delivery order or MIL-STD-1686 requirements.

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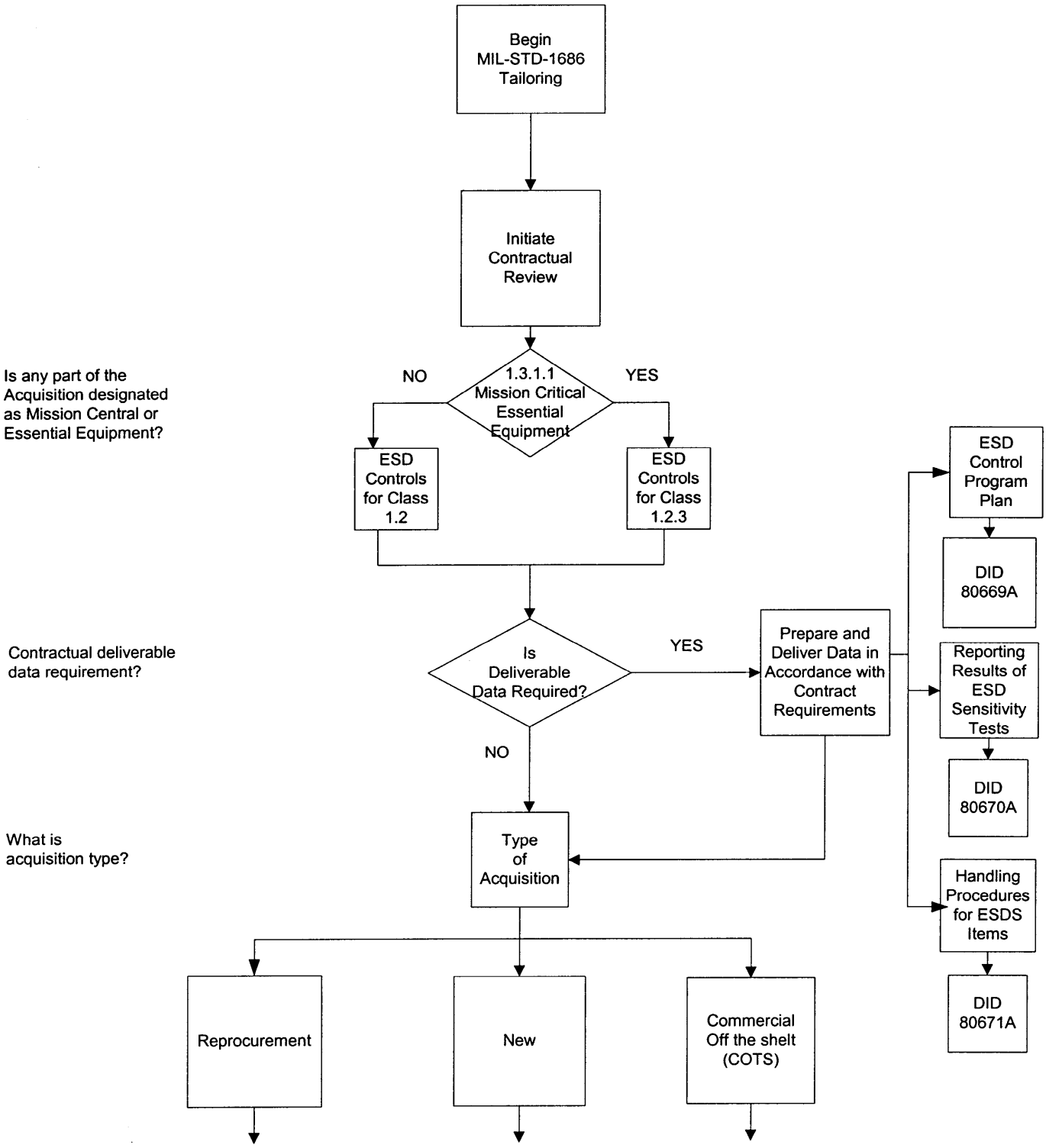

FIGURE 1. MIL-STD-1686 tailoring.

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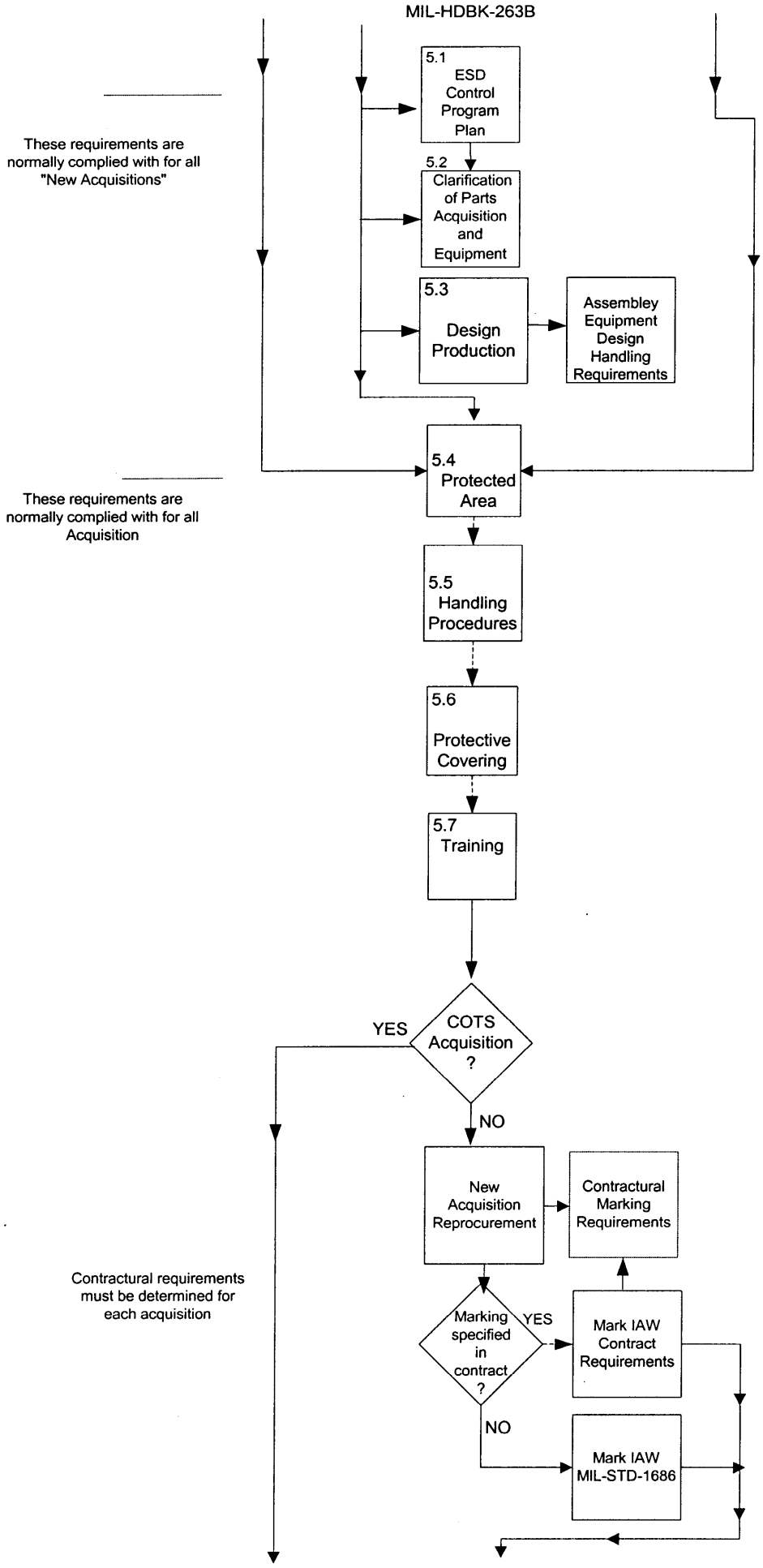

FIGURE 1. MIL-STD-1686 tailoring - Continued.

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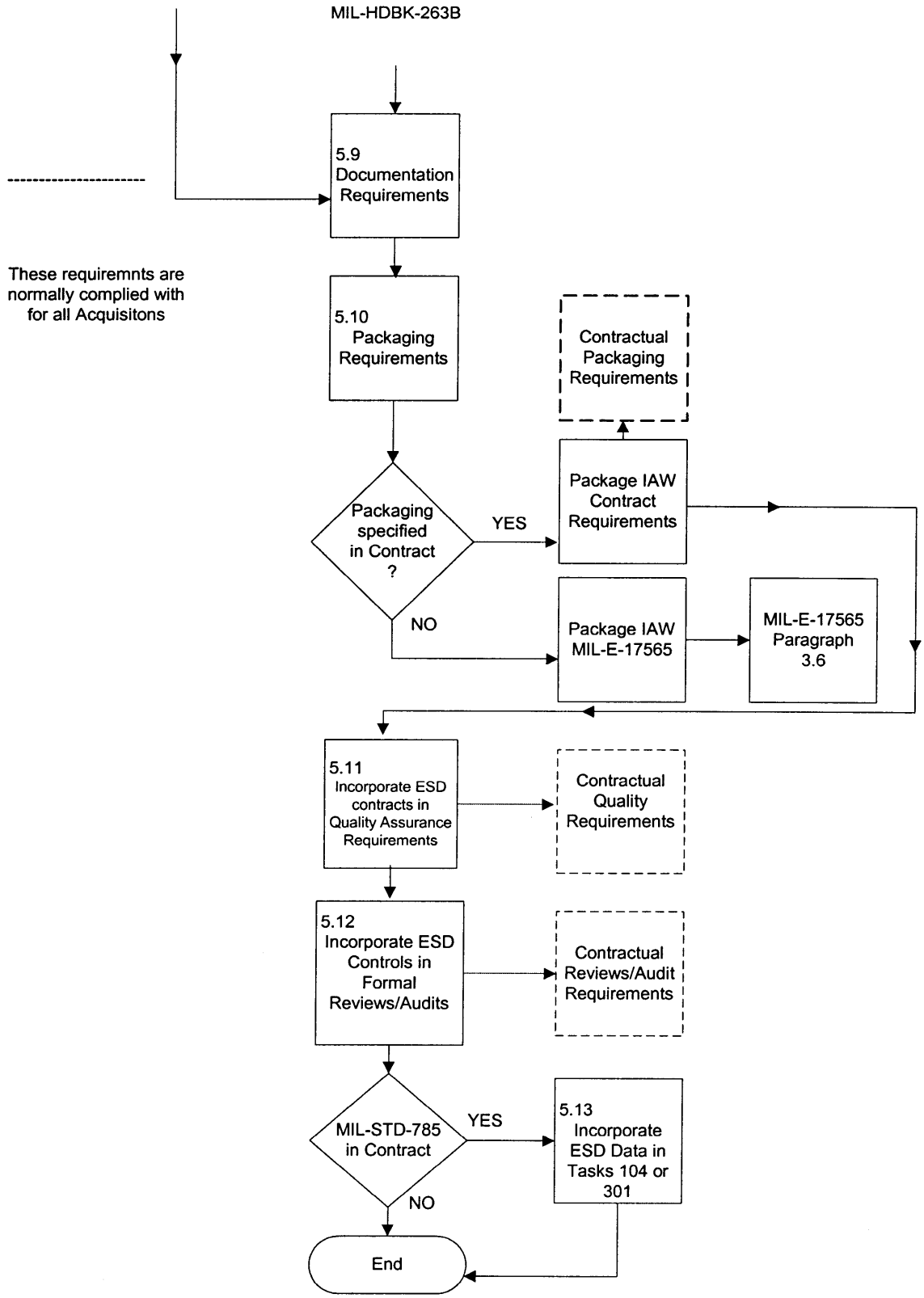

FIGURE 1. MIL-STD-1686 tailoring - Continued.

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2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, handbooks, and bulletins. The following specifications, standards, handbooks, and bulletins form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

MILITARY

MIL-E-17555	-	Electronic and Electrical Equipment, Accessories, and Provisioned Items (Repair Parts): Packaging of.
MIL-S-19500	-	Semiconductor Devices, General Specification for.
MIL-T-31000	-	Technical Data Packages, General Specification for.
MIL-M-38510	-	Microcircuits, General Specification for.
MIL-H-38534	-	Hybrid Microcircuits, General Specification for.
MIL-I-38535	-	Integrated Circuits (Microcircuits) Manufacturing, General Specification for.
MIL-T-47500	-	Technical Data Packages.

STANDARDS

MILITARY

DOD-STD-100	-	Engineering Drawing Practices.
MIL-STD-454	-	Standard General Requirements for Electronic Equipment.
MIL-STD-750	-	Test Methods for Semiconductor Devices.
MIL-STD-785	-	Reliability Program for Systems and Equipment Development and Production.
MIL-STD-883	-	Test Methods and Procedures for Microelectronics.
MIL-STD-1521	-	Technical Reviews and Audits for Systems, Equipments, and Computer Programs.
MIL-STD-1686	-	Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices). (Metric)

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MIL-STD-2073-1 - DOD Materiel Procedures for Development and Application of Packaging Requirements.
MIL-STD-2073-2 - Packaging Requirement Codes.

BULLETINS

MILITARY
MIL-BUL-103 - List of Standardized Military Drawings (SMDs)

(Unless otherwise indicated, copies of federal and military specifications, standards, handbooks, and bulletins are available from the Standardization Documents Order Desk, Bldg. 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

ELECTRONIC INDUSTRIES ASSOCIATION STANDARD
RS-471 - Symbol and Label for Electrostatic Sensitive Devices.

(Application for copies should be addressed to the Electronic Industries Association, Engineering Department, 2001 Eye Street, NW, Washington, DC 20006.)

RELIABILITY ANALYSIS CENTER (RAC)
VZAP-91- Electrostatic Discharge Susceptibility Data 1991

(Application for copies should be addressed to the Reliability Analysis Center, P.O. Box 4700, Rome, NY 13440-8200.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. DEFINITIONS

3.1 Definitions. The following definitions apply to MIL-STD-1686 requirements and MIL-HDBK-263 guidance.

3.2 Accelerated life testing. A test under which test conditions are more severe than specified operating conditions.

3.3 Antistatic property. This term refers to the reduction of triboelectric charge generation. Antistatic materials minimize the generation of static charges. This property is not dependent upon material resistivity.

3.4 Assembly. A number of parts or subassemblies or any combination thereof joined together to perform a specific function and capable of disassembly.

3.5 Avalanche breakdown. A breakdown caused by the cumulative multiplication of charge carriers through field-induced impact ionization.

3.6 Bulk breakdown. An energy dependent failure mechanism where changes in parameters result from metallization alloying or impurity diffusion due to localized high temperatures.

3.7 Catastrophic failure. A failure resulting in the permanent loss of a critical function.

3.8 Charge. The product of capacitance times voltage. Q (charge) = C (capacitance) x V (voltage).

3.9 Charged device model. A model characterizing a particular ESD failure mechanism in which an item isolated from ground is charged and is subsequently discharged causing a short duration discharge pulse.

3.10 Classification of ESDS parts, assemblies and equipment. Classification of ESDS parts, assemblies, and equipment that are susceptible to ESD voltages as defined by MIL-STD-1686. ESDS susceptibility voltages are classified as:

Class 1: Susceptible to damage from ESD voltages greater than 0 to 1,999 volts.

Class 2: Susceptible to damage from ESD voltages of 2,000 to 3,999 volts.

Class 3: Susceptible to damage from ESD voltages of 4,000 to 15,999 volts.

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NOTE: For the purpose of MIL-STD-1686, parts, assemblies and equipment susceptible to ESD voltages of 16,000 volts or higher are considered non-ESD sensitive.

3.11 Classification testing. The testing procedures used to determine the ESD susceptibility class of parts. This procedure is described in MIL-STD-1686, appendix A.

3.12 Conductive material. For the purpose of ESD protection, material with the following characteristics:

Surface conductive type:	Materials with a surface resistivity less than 10^5 ohms per square.
Volume conductive type:	Materials with a volume resistivity less than 10^4 ohm-centimeter.

3.13 Corona discharge. A luminous discharge due to ionization of the air around a conductor.

3.14 Decay time. The time required for a voltage to be reduced to a given percentage of the initial voltage.

3.15 Device. An individual part such as a microcircuit or semiconductor device.

3.16 Dielectric breakdown. The failure of a dielectric material due to excessive voltage.

3.17 Dissipative material. For the purpose of ESD protection, material with the following characteristics:

Surface conductive type:	Materials with a surface resistivity equal to or greater than 10^5 but less than 10^{12} ohms per square.
Volume conductive type:	Materials with a volume resistivity equal to or greater than 10^4 but less than 10^{11} ohm-cm.

3.18 Earth ground. That portion of an electrical circuit that is at zero potential with respect to earth. (See ground.)

3.19 Electric field. The region surrounding an electrically charged object in which another electrical charge will experience force. Commonly referred to as an electrostatic field.

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3.20 Electrical and electronic part. A part such as a microcircuit, discrete semiconductor, resistor, capacitor, or piezoelectric crystal.

3.21 Electrostatic charge. Electrical charge at rest. The negative or positive charge present on the material or item surface. (See charge.)

3.22 Electrostatic discharge (ESD). A transfer of electrostatic charge between objects at different potentials caused by direct contact or induced by an electrostatic field.

3.23 Electrostatic discharge sensitive (ESDS). The relative tendency of a device's performance to be affected or damaged by an ESD event.

3.24 Electrostatic field. A voltage gradient between electrostatically charged surfaces. (See electric field.)

3.25 Electrostatic shield. A barrier or enclosure that prevents or attenuates the penetration of an electric field.

3.26 Electrostatics. That class of phenomena which is recognized by the presence of electrical charges, either stationary or moving, and the interactions of these charges, this interaction being solely by reason of the charges themselves and their position and not by reason of their motion. (Ref: Electrostatics and Its Applications, A.D. Moore, Editor.)

3.27 Equipment. An assembly or any combination of parts, subassemblies and assemblies mounted together, normally capable of independent operation in a variety of situations.

3.28 ESD protected area. An area which is constructed and equipped with the necessary ESD protective materials, equipment, and procedures to limit ESD voltages below the sensitivity level of ESDS items handled therein.

3.29 ESD protective handling. Handling material and equipment in a manner to prevent damage from ESD.

3.30 ESD protective material. Material with one or more of the following properties: limits the generation of electrostatic charge; dissipates electrostatic charge; or provides shielding from electric fields. For the purpose of this handbook, ESD protective materials are classified as conductive or dissipative.

3.31 ESD protective packaging. Packaging with ESD protective materials to prevent ESD damage to ESDS items.

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3.32 ESD sensitivity (ESDS) classification. Classification of the sensitivity of electronic parts, assemblies, and equipment based on their susceptibility to damage from electrostatic discharge.

3.33 Field induced model. A model characterizing an electrically floating device which is subjected to an electrostatic field and then is contacted to an object causing an ESD.

3.34 Ground. A mass such as the earth, or a ship or vehicle hull, capable of supplying or accepting electrical charge.

3.35 Handled or handling. Actions during which items are hand manipulated or machine processed.

3.36 Hard ground. A connection directly to earth ground.

3.37 Human body model. A standardized test model, characterized by the use of a 1,500 ohm resistor and a 100 picofarad capacitor.

3.38 Induction. The process by which an electrical charge establishes a charge in a nearby object without physical contact.

3.39 Input protection. A protective network at the input pins of an item to prevent electrical damage.

3.40 Insulative material. For the purpose of ESD protection, materials not defined as conductive or dissipative are considered to be insulative.

3.41 LRU. Line or lowest replaceable unit (electrical/electronic assembly or subassembly).

3.42 Part. One piece, or two or more pieces joined together which are not normally subject to disassembly without destruction of designed use. Parts, components, and devices are synonymous.

3.43 Protected area. See ESD protected area.

3.44 Protective handling. The special handling that is given to ESDS items in order to prevent ESD damage.

3.45 Protective packaging. Packaging with ESD protective materials to prevent electrostatic damage to ESDS items.

3.46 Protective storage. Storage of ESDS items while enclosed in ESD protective covering or packaging.

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3.47 Resistivity. A measure of the resistance of a material to electric current either through its volume or on its surface. Surface resistivity is the ratio of direct current (dc) voltage to the current that passes across the surface of a material. The unit measurement for surface resistivity (ρs) is ohms per square. Volume resistivity is the ratio of dc voltage per unit of thickness applied across two electrodes in contact with a specimen to the amount of current per unit area passing through the material. The unit of measurement for volume resistivity (ρv) is ohm-centimeter.

3.48 Soft ground. A connection to ground through a resistance sufficient to limit current flow to safe levels for personnel.

3.49 SRU. System or shop replaceable unit (electrical/electronic subassemblies-usually a part of an LRU).

3.50 Static shielding materials. Material that attenuates an ESD.

3.51 Subassembly. Two or more parts which form a portion of an assembly or a unit replaceable as a whole, but having a part or parts which are individually replaceable.

3.52 Tailoring. As used herein, tailoring is the process by which individual requirements for a comprehensive ESD control program are evaluated to determine the extent to which they are applicable for a specific acquisition.

3.53 Technical data. As used herein, technical data means recorded information (regardless of the form or the method of the recording) of a scientific or technical nature used in a specific acquisition.

3.54 Technical data package (TDP). A TDP consists of a technical description of an item adequate for supporting an acquisition strategy, design, production, engineering, and logistic support. The TDP includes all applicable technical data such as drawings, associated lists, specifications, standards, performance requirements, quality assurance provisions, packaging and handling details.

3.55 Triboelectric effect. The generation of electrostatic charge on an object by rubbing or other type of contact.

4. GENERAL REQUIREMENTS OF MIL-STD-1686

4.1 General. The primary objective of ESD control program implementation is to provide continuous ESD protection. Life-time electrostatic control and protection entails implementation of ESD control program requirements (see ESD control program requirements table of MIL-STD-1686) during design, production, inspection, test, storage, shipment, installation, maintenance and repair functions. MIL-STD-1686 requirements, as tailored by the contractor (see MIL-

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STD-1686, 1.3.1) and approved by the acquiring activity will define the ESD control program requirements for specific programs or products. Table I provides a cross-reference listing between the requirements sections of MIL-STD-1686, the guidance sections of MIL-HDBK-263, and the supplementary technical data appendices of MIL-HDBK-263.

5. DETAILED REQUIREMENTS OF MIL-STD-1686

5.1 ESD control program plan. The ESD control program plan provides the data required in accordance with MIL-STD-1686 and Data Item Description (DID) DI-RELI-80669A when required by the contract or purchase order (see MIL-STD-1686, 6.2). The approved ESD control program plan is the basis for comprehensive ESD controls and program implementation. The plan describes the scope of the ESD control program; describes the tasks, activities, and procedures necessary to protect ESD sensitive items; identifies organizations responsible for the tasks and activities; and lists directive or guidance documents used in the ESD control program. The plan also describes ESD control requirements imposed on subcontractors and suppliers by prime contractors. The final element of the plan is a listing of the specific ESD protective tools, materials, and equipment used in the ESD control program. The major element in a properly structured technically effective ESD control program plan is the assessment of the ESD susceptibility of the parts and their required protection levels. The selection of specific ESD control procedures or materials is at the option of the plan preparer. MIL-STD-1686 does not mandate or preclude the use of any appropriate procedures or materials.

5.2 Classification of ESDS parts, assemblies and equipment. ESDS parts, assemblies, and equipment are classified as class 1, 2, or 3 in accordance with MIL-STD-1686. MIL-STD-1686 requires that the ESD control program normally encompass only class 1 and 2 parts, assemblies and equipment. For mission critical or essential equipment, as designated by the contracting activity, class 3 parts, assemblies and equipment shall be included in the ESD control program in accordance with MIL-STD-1686. Classes 1, 2, and 3 of MIL-STD-1686 may be optionally subdivided to more selectively classify ESDS parts, assemblies and equipment. Subclassification voltage ranges are discretionary, but they must correlate to the sensitivity classification voltages in accordance with MIL-STD-1686.

5.2.1 Part classification. The sequence for parts ESD sensitivity classification in accordance with MIL-STD-1686 is predicated upon the requirement to eliminate duplicative non-cost effective testing where feasible. MIL-STD-883 Method 3015, commonly referred to as the Human Body Model (HBM), is the military ESD test method for microelectronics (microcircuits) and is referenced in MIL-M-38510, MIL-H-38534, MIL-I-38535, MIL-BUL-103, and MIL-STD-1686. MIL-STD-750 Method 1020 is the military HBM ESD test method for semiconductor (discrete) devices. These documents provide a coordinated requirement for ESD

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testing. ESD sensitivity data contained in the MIL-M-38510 Qualified Products List (QPL), the MIL-H-38534/MIL-I-38535 Qualified Manufacturer Listing (QML), or the Reliability Analysis Center ESD sensitive item list (ESDSIL) will provide the definitive microcircuit classification data required for ESD control program implementation. In those cases where classification testing is not cost effective, parts may be classified in accordance with MIL-STD-1686, appendix B. Where definitive test data is required for parts not included in the appropriate QPL/QML, Military Bulletin, or VZAP-91, MIL-STD-1686 appendix A is used. It should be noted that when the Reliability Analysis Center's VZAP-91 data base is used for classification, the test circuit should be in conformance with the MIL-STD-1686 appendix A test circuit or a comparable test method approved by the contracting activity. MIL-STD-1686 provides another cost effective classification method when ESD sensitivity levels are specified in applicable military part specifications. When parts ESD sensitivity testing is performed in accordance with MIL-STD-1686, classification test data should be as specified.

5.2.2 Assembly and equipment classification. Assembly and equipment ESD sensitivity classification are in accordance with the most sensitive class of part used in the assembly or equipment. When assemblies or equipment incorporate protective circuitry to meet the design protection requirements of MIL-STD-1686, the assembly or equipment is classified at the design hardened voltage protection level (see 5.3 below for additional guidance). Classification of assemblies or equipment incorporating protective methods to meet the MIL-STD-1686 2,000 or 4,000 volt design hardening requirement must be based upon approved and justified analytical techniques or actual test.

5.3 Design protection. MIL-STD-1686 design protection requirements for assemblies (2,000 volts) and equipment (4,000 volts) specifically relate to the protection (design hardening) at the points of external connection to the assembly or equipment (inputs, outputs and interface connection points). Since it is not possible to provide universal definitions of the terms "assembly" or "equipment," guidance should be obtained from the acquiring activity to define these terms for a specific acquisition.

5.3.1 Protection of parts and assemblies. When class 1 parts must be used, MIL-STD-1686 requires design protection to reduce the ESD sensitivity of the assembly external connection points to greater than 2,000 volts. Assemblies utilizing protective circuitry to meet the 2,000 volt assembly requirement of MIL-STD-1686 may still contain parts sensitive to damage at voltage levels less than 2,000 volts. In these cases, the assembly would be classified as 2,000 volts (class 2). Part level classification, of the parts used in the assembly, will be indicative of the part's actual classification.

5.3.2 Protection of equipment. Equipment meeting the design hardening requirement (4,000 volts) of MIL-STD-1686 at the points of external connection to the equipment (inputs, outputs and interface connection points) may still

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contain assemblies and parts sensitive to damage at voltages less than 4,000 volts. In these cases, the equipment would be classified as 4,000 volts (class 3). Part level classification, of the parts used in the equipment, will be indicative of the part's actual classification.

5.4 Protected areas. An ESD protected area consists of the materials, equipment, and procedures required to control or minimize electrostatic charges (static voltage levels). The fundamental ESD protected area concept is to limit static voltage levels below the damage threshold of the most sensitive ESDS parts, assemblies and equipment handled therein. Considerations in the design of ESD protected areas are the requirements for adequate grounding procedures, personnel electrical safety, and the development of handling procedures (see 5.5). ESD protected areas are required when handling ESDS parts, assemblies and equipment outside of their ESD protective covering or packaging. When ESDS parts, assemblies and equipment must be handled outside of protected areas without protective covering or packaging, detailed ESD protective handling procedures are required.

5.4.1 Related design factors. Related to the design of protected areas are factors such as minimizing static charges generated by personnel clothing, hair, and movement; the need to designate and clearly identify protected areas; and the essential requirement to address personnel safety requirements.

5.5 Handling procedures. Complementing ESD protected area requirements are the requirements for detailed handling procedure for ESDS parts, assemblies and equipment in accordance with MIL-STD-1686. Technically adequate handling procedures are directly related to the level of protection provided by the protected area. Handling procedures must be comprehensive and address the entire range of potential situations and physical locations where ESDS items will be handled. Practically, the handling procedures must address the concept of handling in both fully protected areas and unprotected areas. The detail required in the handling procedures increases as the level of protection provided by the protected area decreases. Documented handling procedures may be required by the contract or purchase order (see MIL-STD-1686, 6.2) and are prepared in accordance with DID DI-RELI-80671A when required.

5.6 Protective covering. The MIL-STD-1686 protective covering requirement is closely linked to, and complements the requirements for protected areas and handling procedures. ESDS sensitive parts, assemblies and equipment require continuous ESD controls and protection. This consists of the ESD controls and protection provided by the protected area requirement or the requirement for protective covering when not being worked on or handled outside of protective areas. Selected ESD protective covering consists of the materials (tote boxes, containers, bags, pouches, rails, or boxes) that provide adequate levels of ESD protection based upon the sensitivity of the parts, assemblies

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and equipment in accordance with MIL-STD-1686 section 5.2. Selected protective covering materials may be the same materials required for packaging or preparation for delivery, supplementary reusable materials, or one time use materials.

5.7 Training. Recurrent ESD training for personnel is an integral and critical part of an ESD control program. Recurrent ESD training includes initial and follow-on training required to reinforce program requirements and modification based upon lessons-learned. New evolutionary concepts and correction of deficiencies identified during reviews and audits should also be part of the training process. The training requirements are developed in conjunction with the handling procedures for ESDS parts, assemblies and equipment required by MIL-STD-1686.

5.8 Marking of hardware. The MIL-STD-1686 requirement for marking of hardware pertains to those ESDS parts, assemblies and equipment which have not been marked in accordance with an applicable (otherwise specified) military specification or standard. If there is an applicable specification or standard, the item of hardware (part, assembly or equipment) should be marked in accordance with the requirements of that specification or standard. However, if no applicable specification or standard applies, and no other marking requirements have been specified, marking shall be in accordance with MIL-STD-1686, 5.8, marking of hardware. MIL-STD-1686 specifies that ESDS parts shall be marked with the EIA RS-471 symbol.

5.8.1 ESDS assemblies. MIL-STD-1686, 5.8.2 requires that assemblies be marked with the EIA RS-471 symbol. The location of the symbol must be in a position readily visible to personnel when the assembly is incorporated in its next higher assembly. The exact location is left to the discretion of the contractor. Additional options have been provided for those instances where the physical size or orientation of the assembly precludes compliance with this MIL-STD-1686 requirement, including the option of developing alternative marking procedures.

5.8.2 Equipment. MIL-STD-1686 states the requirement for marking of equipment containing ESDS parts and assemblies. This section also requires the use of the EIA RS-471 symbol. In addition, the caution statement shown in MIL-STD-1686 shall be placed adjacent to the symbol. The exact location of the symbol and caution statement is left to the discretion of the contractor but the location must meet the basic equipment marking requirement as specified in MIL-STD-1686.

5.8.3 External equipment terminals. MIL-STD-1686 contains the requirement for the marking of external equipment terminals connected internally to ESDS parts and assemblies within the equipment. The EIA RS-471 symbol must be used, and it must be located adjacent to the external terminals.

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5.9 Documentation. Deliverable documentation, as discussed in MIL-STD-1686 refers to deliverable documentation required by the contract, delivery order, or purchase order invoking MIL-STD-1686. This deliverable documentation is specified in the contract data requirements list (CDRL), DD Form 1423. In the case of drawings prepared in accordance with DOD-STD-100 or Technical Data Packages in accordance with MIL-T-31000, or MIL-T-47500, as applicable, ESD requirements and symbol locations shall be specified or referenced. Examples of deliverable documentation include, but are not limited to, technical data packages, technical manuals, provisioning technical documentation, logistics support analysis data, and drawings. MIL-STD-1686 requires that deliverable documentation identify class 1, 2, and, when specified mission critical or essential class 3 parts, assemblies, equipment, and the connectors, test points, and terminals connected to ESDS parts and assemblies collectively as ESDS. This means that the exact classification (that is, class 1, 2, or 3) is not required; however, exact classification data may be used by the contractor if desired. A collective identification of parts, assemblies, equipment, connectors, test points, and terminals as ESDS is required. MIL-STD-1686 also requires that the deliverable documentation include or refer to documented ESD protective procedures. MIL-STD-1686 allows the contractor the option of identifying ESDS parts, assemblies, or equipment collectively as ESDS, or the use of exact classifications (class 1, 2 and, when required, class 3) in nondeliverable documentation used for ESD control program implementation. Additionally, nondeliverable documentation may optionally include or refer to documented ESD protective procedures.

5.10 Packaging. Normally contracts and delivery or purchase orders specify exact packaging requirements using MIL-STD-2073 packaging requirement codes (PRCs). When packaging requirements are not otherwise specified, ESD protective packaging shall be as specified in MIL-E-17555 in accordance with MIL-STD-1686. MIL-STD-1686 contains the additional requirement that ESD protective caps shall be used on equipment external connectors connected to ESDS parts and assemblies within the equipment. The MIL-STD-1686 requirement for protective caps complements and is in consonance with MIL-STD-454, requirement 10 for the protection of unmated connectors with metal or plastic caps during maintenance, storage and shipment.

5.11 Quality assurance requirements. The quality assurance requirements of MIL-STD-1686 indicate the importance of incorporating ESD control program requirements in Total Quality Management and quality assurance efforts, including those performed at subcontractors, suppliers, and vendors. Quality assurance evaluates conformance with MIL-STD-1686 requirements and the approved ESD control program plan.

5.12 Formal reviews and audits. Scheduled design, program reviews, and audits, such as those required by MIL-STD-1521, shall be used to assess compliance with MIL-STD-1686 and the approved ESD control program plan. These reviews will assess the information required in MIL-STD-1686 to determine the

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acceptability of design decisions, ESD controls, procedures and program progress.

5.13 Failure analysis. In accordance with MIL-STD-1686, the intent of failure analysis is to consider all causes of failures. A comprehensive failure analysis program will include ESD failure mechanisms as part of the analysis process. When failures have been attributed to ESD, this data should be used as a basis for assessing the effectiveness of the ESD control program and the determination of corrective action requirements.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. This document provides guidance information to assist the user in designing and implementing an ESD control program in accordance with MIL-STD-1686B requirements. The supplementary technical data provided in appendices A through L is provided as information only for reference. Due to the nature of the changes in MIL-STD-1686B this handbook is intended for use only with MIL-STD-1686B. For those contracts incorporating DOD-STD-1686 of 2 May 1980, the companion document is DOD-HDBK-263 of 2 May 1980. For those contracts incorporating MIL-STD-1686A of 8 August 1988, the companion document is MIL-HDBK-263A of 22 February 1991.

6.2 Issue of DODISS. When this handbook is used in acquisition, the applicable issue of the DODISS must be cited in the solicitation (see 2.1.1, and 2.2).

6.3 Subject term (key word) listing.

Electrostatic protection
Electrostatic discharge sensitive (ESDS)
ESD control program
Metal oxide semiconductors
Semiconductor devices
Static electricity
Triboelectric effect

6.4 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:
Army - ER
Navy - SH
Air Force - 17

Preparing activity:
Navy - SH
(Project RELI-0067)

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Review Activities:
Army - AT, CR, MI, AR, GL, SM
Navy - AS, EC, OS, SA
Air Force - 11, 15, 19, 99

User Activities:
Navy - MC
Air Force - 69
NASA/NPPO

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APPENDICES

INTRODUCTION

The supplementary technical information contained in these appendices is intended to provide a convenient source of technical information for related subjects. This technical information is not, and cannot be, totally comprehensive or complete for all subjects.

The information contained in the appendices purposely does not permit a simplistic approach to ESD control program implementation. Meaningful ESD controls can only be implemented based upon a knowledge based approach:

(a) Knowledge of the susceptibility levels of parts, assemblies, and equipment
(b) Knowledge of the cost and technical tradeoffs of specific control techniques, materials, and processes
(c) Knowledge of ESD control program requirements

MIL-STD-1686 contains ESD control program requirements. MIL-STD-1686 does not mandate or preclude the use of any specific ESD control materials, techniques, or processes. The selection, or exclusion, of any specific material, technique, or process is at the option of the ESD control program contractor. The corollary to this is that the contractor is required to demonstrate a knowledge of the products (and their ESD susceptibility levels) requiring protection and design technically meaningful and cost effective controls.

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APPENDIX A

STATIC ELECTRICITY

10. SCOPE

10.1 Scope. This appendix provides an overview of the nature and sources of static electricity. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. INTRODUCTION

30.1 General. Electrostatics (static electricity) and the associated phenomena are extremely complex physical events. A principle textbook on electrostatics is "Electrostatics and Its Applications" edited by A.D. Moore. The introduction to this textbook defines electrostatics as "... that class of phenomena which is recognized by the presence of electrical charges, either stationary or moving, and the interaction of these charges, this interaction being solely by reason of the charges themselves and their position and not by reason of their motion." Electrical charge is the fundamental physical problem causing damage to ESD sensitive parts, assemblies, and equipment.

30.2 Nature of static electricity. Static electricity is electrical charge at rest. There are two events for a body that can result in electrical charge:

(a) electrons can move or migrate within a body resulting in polarization; this can occur even when a single body has a net overall charge of zero.
(b) the transfer of electrons from one body to another (conductive charging) resulting in a net positive or negative charge.

The movement or transfer of electrons is due to the interaction of charged bodies, or charged and uncharged bodies. The magnitude of the charge is primarily dependent on the size, shape, composition and electrical properties of the substances which make up the bodies. Some substances readily give up electrons while others tend to accumulate electrons. A body with an excess of electrons is charged negatively; a body with an electron deficit is charged positively. When two substances of any type are contacted or rubbed together, one substance gains electrons and the other loses electrons. This results in each substance becoming charged. When the two materials are subsequently separated, the net positive or negative charge on each substance can be measured. These charges are equal, of opposite polarity, and in the case of

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non-conductors tend to remain in the localized area of contact. Charges on a conductor are rapidly distributed over its surface and the surfaces of other conductive objects which it contacts.

30.2.1 Electrostatic fields. An electrostatic field or lines of force are present around a charged body. Conductive, dissipative and insulative bodies that enter this field will be polarized by induction (that is, without contacting the charged body). In a conductive or dissipative body, electrons closest to the more negative part of the field are repelled, leaving that area relatively positively charged. These electrons are attracted to the more positive part of the field creating negatively and positively charged areas. The net charge on the body will remain zero. If a conductive polarized body is subsequently grounded, electrons will flow to or from the polarized surface near the ground and upon removal of the ground the body retains a net charge due to the excess or deficit of electrons. In a non-conductive body electrons are less mobile, but dipoles tend to align with the field creating apparent surface charges. A non-conductor cannot be inductively charged.

30.2.2 Capacitance-voltage relationship. The capacitance of a charged body relative to another body or ground also has an effect on the electrostatic voltage. When capacitance is reduced for a given charge (Q), there is an inverse linear increase in voltage based on the relationship $Q = CV$, where C is the capacitance and V is the voltage. As the capacitance is continually decreased the voltage will increase until a discharge occurs via an arc. For example, when common polyethylene bags are rubbed, the charge potential may be only a few hundred volts while in contact with a work surface. However, when the same bag is picked up by an operator, the charge potential may be several thousand volts due to the decrease in capacitance. It should also be noted that the energy (E) stored in a capacitor is expressed by the relationship $E = 1/2CV^2$.

30.3 Triboelectric series. The generation of static electricity caused by contacting or rubbing two substances is called the triboelectric effect. A triboelectric series is a list of substances in an order of positive to negative charging as a result of the triboelectric effect. A substance higher on the list is positively charged (loses electrons) when contacted with a substance lower on the list (which gains electrons). The order of ranking in a triboelectric series is not always a constant or repetitive. Furthermore, the degree of separation of two substances in the triboelectric series does not necessarily indicate the magnitude of the charges created by triboelectric effect. Order in the series and magnitude of the charges are dependent upon the properties of the substance, but these properties are modified by factors such as purity, ambient conditions, pressure of contact, speed of rubbing or separation, and the contact area over which the rubbing occurs. A sample triboelectric series is provided in table II. In addition to the rubbing of two different substances, substantial electrostatic charges can also be generated triboelectrically when two pieces of the same material, especially

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common plastic in intimate contact, are separated as occurs when separating the sides of a plastic bag.

30.4 Prime sources of static electricity. Typical prime charge sources commonly encountered in a facility are listed in table III. These prime sources are essentially insulators and are typically synthetic materials. Electrostatic voltage levels generated with these insulators can be extremely high since they are not readily distributed over the entire surface of the substance or conducted to another contacting substance. The conductivity of some insulative materials is increased by absorption of moisture under high humidity conditions onto the otherwise insulating surface, creating a slightly conductive sweat layer which tends to dissipate static charges over the material surface. The generation of 15,000 volts from common plastics in a typical facility is not unusual. Table IV shows typical electrostatic voltages generated in a facility. These electrostatic voltage levels are indicative of the relative charge (Q) on the object in accordance with the relationship $Q = CV$ (see 30.2.2).

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TABLE II. Sample triboelectric series. 1/

Positive	Human hands
+	Rabbit fur
	Glass
	Mica
	Human hair
	Nylon
	Wool
	Fur
	Lead
	Silk
	Aluminum
	Paper
	Cotton
	Steel
	Wood
	Amber
	Sealing wax
	Hard rubber
	Nickel, copper
	Brass, silver
	Gold, platinum
	Sulfur
	Acetate rayon
	Polyester
	Celluloid
	Orlon®
	Polyurethane
	Polyethylene
	Polypropylene
	PVC (vinyl)
	KEL F®
Negative	Silicon
-	Teflon®

1/ This list is an example only. The precise order of materials in any triboelectric series is dependent upon many variable factors. Any example triboelectric series may not be repeatable. It should also be noted that charge magnitude is not a function of separation on this list.

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TABLE III. Typical prime charge sources.

Object or process	Material or activity
Work surfaces	Waxed, painted or varnished surfaces Common vinyl or plastics
Floors	Sealed concrete Waxed, finished wood Common vinyl tile or sheeting
Clothes	Common clean room smocks Common synthetic personnel garments Non-conductive shoes Virgin cotton 1/
Chairs	Finished wood Vinyl Fiberglass
Packaging and handling	Common plastic - bags, wraps, envelopes Common bubble pack, foam Common plastic trays, plastic tote boxes, vials, parts bins
Assembly, cleaning, test and repair areas	Spray cleaners Common plastic solder suckers Solder irons with ungrounded tips Brushes (synthetic bristles) Cleaning or drying by fluid or evaporation Temperature chambers Cryogenic sprays Heat guns and blowers Sand blasting Electrostatic copiers Cathode ray tubes

1/ Virgin cotton can be a static source at low relative humidities such as below 30 percent.

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TABLE IV. Typical electrostatic voltages. 1/

Means of static generation	Electrostatic voltages	
	10 to 20 percent relative humidity	65 to 90 percent relative humidity
Walking across carpet	35,000	1,500
Walking over vinyl floor	12,000	250
Worker at bench	6,000	100
Vinyl envelopes for work instructions	7,000	600
Common poly bag picked up from bench	20,000	1,200
Work chair padded with polyurethane foam	18,000	1,500

1/ Caution should be exercised when attempting to correlate the above, or actual measured voltages with the potential to damage ESDS items. See 30.1 through 30.2.2.

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APPENDIX B

SUSCEPTIBILITY TO ESD

10. SCOPE

10.1 Scope. The susceptibility of assemblies and equipment to ESD is directly related to the susceptibility of the parts used in the assembly and equipment. This appendix provides technical data related to the susceptibility of parts, assemblies, and equipment; types of ESD failures; ESDS part types; ESD related failure mechanisms; and part constituents susceptible to ESD. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. SUSCEPTIBILITY OF PARTS, ASSEMBLIES AND EQUIPMENT

30.1 Susceptibility of parts. Numerous parts are susceptible to damage when an ESD event occurs or when these parts are exposed to electrostatic fields. ESDS parts can be destroyed by an ESD event regardless of their electrical and ground connections. A ground connection is not required to destroy an ESDS part. Parts having pins connected to ground and their voltage and signal sources can be damaged by ESD even when installed in their parent assemblies and equipment. ESDS parts are listed by part type in appendix B of MIL-STD-1686. This part sensitivity data is based upon the results of MIL-STD-1686 appendix A testing, which is referred to as Human Body Model (HBM) ESD testing.

30.2 Susceptibility of assemblies and equipment. Assemblies and equipment containing ESDS parts are often as sensitive as the most sensitive ESDS part they contain. Incorporation of protective circuitry in assemblies and equipment provides varying degrees of protection from ESD applied to their terminals. Such assemblies and equipment are still vulnerable from induced ESD caused by strong electrostatic fields or by direct part, assembly or equipment contact with a charged object.

40. TYPES OF ESD FAILURE

40.1 Intermittent, upset, and hard failures. ESD can cause intermittent or upset (transient) failures as well as hard failures. Intermittent or upset failures can occur on certain types of parts such as large scale integration (LSI) memories. Such failures occur when equipment is in operation and is usually characterized by a loss of information or temporary distortion of its functions. No apparent hardware damage occurs and proper operation resumes

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automatically after the ESD exposure or in the case of some digital equipment, after re-entry of the information by resequencing the equipment.

40.1.1 Upset failures. Upset can be the result of the electrical noise associated with an ESD spark in the vicinity of the equipment. The electrical noise may enter electronic equipment by either conduction or radiation. In the near field of an ESD, capacitive or inductive coupling, depending on the impedances of the ESD source and the receiver, is dominant. In the far field, electromagnetic field coupling exists.

Equipment operation is upset if the ESD-induced voltage, and/or currents exceed the signal levels in the electronic circuit. In high impedance circuits the signals are voltage levels, thus capacitive coupling will dominate and ESD-induced voltage will be the major problem. In low impedance circuits the signals are current based, thus inductive coupling will dominate and the ESD-induced currents will cause the problem.

Since the voltages and currents necessary to cause damage are one to two orders of magnitude greater than those required to cause upset, damage is more likely when there is conductive coupling--that is, the ESD spark must be directly coupled to the circuit. Radiated coupling will normally cause only upset.

40.1.2 Hard failures. While upset failures occur when the equipment is operating, catastrophic (hard) failures can occur any time. Catastrophic ESD failures can be the result of electrical overstress of electronic parts caused by an ESD such as: a discharge from a person or object, an electrostatic field, or a high voltage spark discharge. Some catastrophic failures may not occur until after exposure to multiple ESD events. Marginally damaged ESDS parts, which require operating stress and time to cause further degradation, may ultimately experience catastrophic failure. Only certain part types seem to be susceptible to this latent failure process. There are some types of catastrophic ESD failures which could be mistaken for upset failures. For example, an ESD could result in aluminum shorting through a SiO_2 dielectric layer. Subsequent high currents flowing through the short, however, could vaporize the aluminum and open the short. This failure may be confused with upset failure if it occurs during equipment operation, but the damage due to the ESD would be a latent defect that will probably reduce the operating life of the part.

40.1.3 Susceptible parts. Parts that are susceptible to ESD upset are any logic family that requires small energies to switch states or small changes of voltage in high impedance lines. Examples of families that are sensitive would be NMOS, PMOS, CMOS and low power TTL. Linear circuits with high impedance, and high gain inputs would also be highly susceptible along with RF amplifiers and other RF parts at the equipment level. Proper design for RFI immunity can protect these parts from damage due to ESD high voltage spark

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discharge. To protect parts sensitive to ESD high voltage spark discharge at the equipment level requires: good RFI/EMC design, buffering of busses, proper termination of busses, shielding of bus conductors and the avoidance of penetrations of the equipment cabinet that lead to sensitive parts.

50. FAILURE MECHANISMS

50.1 Typical failure mechanisms. ESD related failure mechanisms typically include:

(a) thermal secondary breakdown
(b) metallization melt
(c) dielectric breakdown
(d) gaseous arc discharge
(e) surface breakdown
(f) bulk breakdown.

The failure mechanisms of (a), (b), and (f) are energy dependent, while failure mechanisms (c), (d), and (e) are voltage dependent. All the above failure mechanisms are applicable to microelectronic and semiconductor devices. Failure mechanisms (b) or (d) have been evident in film resistors; failure mechanism (f), in piezoelectric crystals. Besides these catastrophic failure mechanisms unencapsulated chips and LSI MOS integrated circuits have exhibited temporary failure due to failure mechanism (d) from positive charges deposited on the chip as a by-product of gaseous arc discharge within the package between the lid and the substrate.

50.1.1 Thermal secondary breakdown. Thermal secondary breakdown is also known as second breakdown. Since thermal time constants of semiconductor materials are generally large compared with transient times associated with ESD pulses, there is little diffusion of heat from the area of power dissipation and large temperature gradients can form in the parts. Localized junction temperatures can approach material melt temperatures, usually resulting in development of hot spots and subsequent junction shorts due to melting. This phenomenon is termed thermal secondary breakdown. For junction melting to occur in bipolar (p-n) junctions, sufficient power must be dissipated in the junction. In the reverse bias condition, most of the applied power is absorbed in the immediate junction area with minimal power loss in the body of the part. In the forward bias condition, the junction exhibits lower resistance. Even though a greater current flows, a greater percentage of the power is dissipated in the body of the part. Thus more power is generally required for junction failure in the forward bias condition. For most transistors, the emitter-base junction degrades with lower current values than collector-base junctions. This is because the emitter-base junction normally has smaller dimensions than any of the other junctions in the circuit. For reversed polarity signals, only a very small microampere current flows until the voltage exceeds the breakdown voltage of the junction.

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At breakdown, the current increases and results in junction heating due to the nucleation of hot spots and current concentrations. At the point of second breakdown, the current increases rapidly due to a decrease in resistivity and a melt channel forms that destroys the junction. This junction failure mode is a power dependent process.

50.1.2 Metallization melt. Failures can also occur when ESD transients increase part temperature sufficiently to melt metal or fuse bond wires. Theoretical models exist which allow computation of currents causing failure for various materials as a function of area and current duration. Such models are based on the assumption of uniform area of the interconnection material. In practice, it is difficult to maintain a uniform area; the resultant non-uniform area can result in localized current crowding and subsequent hot spots in the metallization. This type of failure could occur where the metal strips have reduced cross-sections as they cross oxide steps. Normally, due to shunting of the currents by the junction, this failure requires an order of magnitude larger power level at higher frequencies than is required for junction damage at lower frequencies. Below 200 to 500 megahertz the junction capacitance still presents a high impedance to currents, shunting them around the junction.

50.1.3 Dielectric breakdown. When a potential difference is applied across a dielectric region in excess of the region's inherent breakdown characteristics, a puncture of the dielectric occurs. This form of failure is due to voltage rather than energy, and could result in either total or limited degradation of the part depending on the pulse energy. For example, the part may heal from a voltage puncture if the energy in the pulse is insufficient to cause fusing of the electrode material in the puncture. It will, however, usually exhibit lower breakdown voltage or increased leakage current after such an event, but not catastrophic part failure. This type of failure could result in a latent defect resulting in catastrophic failure with continued use. The breakdown voltage of an insulating layer is a function of the pulse rise time since time is required for avalanching of the insulating material.

50.1.4 Gaseous arc discharge. For parts with closely spaced unpassivated thin electrodes, gaseous arc discharge can cause degraded performance. The arc discharge condition causes vaporization and metal movement which is generally away from the space between the electrodes. The melting and fusing does not move the thin metal into the interelectrode regions. In melting and fusing, the metal pulls together and flows or opens along the electrode lines. There can be fine metal globules in the gap region, but not in sufficient numbers to cause bridging. Shorting is not considered a major problem with unpassivated thin metal electrodes. On a surface acoustic wave (SAW) band pass filter device with thin metal of approximately 4,000 angstroms (Å) and 3.0 micrometers (μm) electrode spacing operational degradation was experienced from ESD.

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When employing thicker metallization such as 13,500 Å, this gaseous arc discharge in an arc gap at typically 50 μm can be used for protection to dissipate incoming high voltage spikes.

For LSI and memory ICs with passivation/active junction interfaces susceptible to inversion, gaseous arc discharge from inside the package can cause positive ions to be deposited on the chip and cause failure from surface inversion. This has been reported to occur especially on parts with non-conducting lids. A special case of this is ultraviolet (UV) EPROMs with quartz lids where failures can be annealed by neutralizing the positive charge with ultraviolet light through the quartz lid.

50.1.5 Surface breakdown. For perpendicular junctions the surface breakdown is explained as a localized avalanche multiplication process caused by narrowing of the junction space charge layer at the surface. Since surface breakdown depends on numerous variables, such as geometry, doping level, lattice discontinuities, or unclean gradients, the transient power which can be dissipated during surface breakdown is generally unpredictable. The destruction mechanism of surface breakdown results in a high leakage path around the junction, thus nullifying the junction action. This effect, as well as most voltage sensitive effects like dielectric breakdown, is dependent upon the rise time of the pulse and usually occurs when the voltage threshold for surface breakdown is exceeded before thermal failure can occur. Another mode of surface failure is the occurrence of an arc around the insulating material which is similar to metallization gaseous discharge. In this case, the discharge is between metallization and semiconductor regions.

50.1.6 Bulk breakdown. Bulk breakdown results from changes in junction parameters due to high local temperatures within the junction area. Such high temperatures result in metallization alloying or impurity diffusion resulting in drastic changes in junction parameters. The usual result is the formation of a resistance path across the junction. This effect is usually preceded by thermal secondary breakdown.

50.2 Part constituents susceptible to ESD. Different parts are susceptible to ESD in various degrees. These variations are due to different part designs and different constituents that go into making the part. Table V is a summary of constituents that are incorporated into various parts which are sensitive to ESD. Table V also lists the part types in which some of these constituents are found and the associated failure processes involved.

50.2.1 MOS structures. A MOS structure is a conductor and a semiconductor substrate separated by a thin dielectric. Thus the acronym MOS for metal-oxide semiconductor is derived. A more general acronym for this structure is MIS for metal-insulator-semiconductor. Dual dielectric systems such as MNOS (metal-nitride-oxide-semiconductor) are included in this susceptible constituent classification.

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50.2.1.1 Part types. Integrated circuit MOS technologies are NMOS (N-channel MOS), PMOS (P-channel MOS) and CMOS (Complementary MOS). Variations on these technologies include metal gate, silicon gate and silicon on sapphire MOS structures. Differences in the susceptibility of these MOS technologies are dependent on the oxide or oxide-nitride gate dielectric breakdown levels and the input protection circuitry connected to the external connections. The breakdown of the gate dielectric is mostly dependent on its thickness. Typically this has been 1,100 Å and with a dielectric strength ranging from $1x10^6$ volts per centimeter (V/cm) to $1x10^7$ V/cm. This results in breakdown levels between 80 and 100 volts. Newer technology variations, however, like

TABLE V. Part constituents susceptible to ESD.

Part constituent	Part type	Failure mechanism	Failure indicator
MOS structures	MOS FET (Discretes) MOS ICs Semiconductors with metallization cross-overs Digital ICs (Bi-polar and MOS) Linear ICs (Bi-polar and MOS) MOS capacitors Hybrids Linear ICs	Dielectric breakdown from excess voltage	Short (high leakage)

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TABLE V. Part constituents susceptible to ESD - Continued.

Part constituent	Part type	Failure mechanism	Failure indicator
Semiconductor junctions	Diodes (PN, PIN, Schottky) Transistors, bi-polar Junction field effect Transistors Thyristors Bi-polar ICs, digital and linear Input protection circuits on: Discrete MOS FETs MOS ICs	Microdiffusion from microplasma-secondary breakdown from excess energy or heat Current filament growth by silicon and aluminum diffusion (electro-migration)	Short circuit (no diode or transistor action)
Film resistors	Hybrid ICs: Thick film resistors Thin film resistors Monolithic IC-thin film resistors Encapsulated film resistors	Dielectric breakdown, voltage dependent-creation of new current paths (for thick film only) Joule heating-energy dependent-destruction of minute current paths (others)	Resistance shift
Metallization strips	Hybrid ICs Monolithic ICs Multiple finger overlay transistors	Joule heating-energy dependent metallization burnout	Open

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TABLE V. Part constituents susceptible to ESD - Continued.

Part constituent	Part type	Failure mechanism	Failure indicator
Field effect structures and non-conductive lids	LSI and memory ICs employing nonconductive quartz or ceramic package lids especially ultraviolet EPROMS	Surface inversion or gate threshold voltage shifts from ions deposited on surface from ESD (charge injection into dielectric material)	Operational degradation
Piezo-electric crystals	Crystal oscillators Surface acoustic wave devices	Crystal fracture from mechanical forces when excessive voltage is applied	Operational degradation
Closely spaced electrodes	Thin metal unpassivated, unprotected semiconductors microcircuits and surface acoustic wave devices	Arc discharge melting and fusing of electrode metal	Operational degradation

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VMOS (vertical groove MOS) which has a higher field intensity at the end of the groove and HMOS (high density MOS) which has thinner gate dielectric, have much lower breakdowns (25 to 80V) and therefore require more care in the design of the input protection circuitry.

Certain bipolar linear integrated circuit operational amplifiers incorporate capacitors on their monolithic chip. These capacitors are MOS structures and are susceptible to dielectric breakdown from ESD. Those operational amplifiers such as the 741 whose capacitors do not have apparent direct contact to external pins are less vulnerable than parts such as the HA2520 whose capacitors are placed directly across an external pin combination. Hybrid microcircuits can incorporate a chip capacitor which is a MOS structure with a dielectric vulnerable to ESD. MOS chip capacitors should not be used in hybrids since other chip capacitors are available which are not considered sensitive to ESD.

Many monolithic integrated circuits have metallization runs which cross-over active semiconductor regions or low resistivity semiconductor regions with field oxide between them serving as the insulator. These are sometimes referred to as parasitic MOS transistors. Typically, the field oxide is 15,000 Å thick with breakdown levels around 1,000 volts, but when the oxide is etched away for diffusion, subsequent growth of oxide before metallization may be less than 3,000 Å. In this case, breakdown could occur at 100 volts because of field intensification at the bottom corners of the metallization step and weak dielectric strength at the thin-thick oxide interface. When external pins are directly connected to such metallization runs, susceptibility to ESD occurs.

50.2.1.2 Failure mechanisms. ESD can damage the oxide in MOS structures because their breakdown voltage is low in comparison to voltage levels encountered with ESD. Breakdown of the oxide insulator results in permanent damage as opposed to breakdown of a semiconductor which may be reversible. For very short duration over-voltages, some lattice damage might occur such that subsequent breakdown and therefore avalanche occurs at a lower value than the initial breakdown.

50.2.1.3 Failure indicators. As the dielectric punch-through occurs the metallization will flow through the dielectric to create a short. However, in some instances where there is particularly thin metallization such as 4,000 Å, or there is sufficient energy passed through the short, the metal will be vaporized and the short will clear but leave a cratered hole in the dielectric. Degraded performance may result but not a catastrophic failure. There is conjecture that the short in some circumstances might reappear or performance might continue to degrade.

50.2.2 Semiconductor junctions. Included in this constituent classification are p-n junctions, p-i-n junctions and Schottky barrier junctions. Their

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sensitivity to ESD depends on geometry, size, resistivity, impurities, junction capacitance, thermal impedance, reverse leakage current and reverse breakdown voltage. The energy required to damage a junction in the forward biased direction is generally ten times that required in the reversed bias direction. Junctions with high breakdown voltage of greater than 100 volts and low leakage currents of less than 1 nanoampere are generally more susceptible to ESD than junctions of comparable size with low breakdown, such as a 30 volt breakdown with leakage greater than 1 microampere.

50.2.2.1 Part types. The emitter-base junctions in bipolar transistors, whether integrated circuit or a discrete transistor, are usually more susceptible to ESD damage than collector-base or collector-emitter junctions. This is primarily due to size and geometry where the emitter side wall experiences large energy densities during reverse biased ESD. Because of larger areas the collector-base and collector-emitter do not experience the same energy densities, although with the collector-base and collector-emitter it is possible to laterally forward bias the base-emitter in which case current crowding at the emitter side wall will occur.

Junction field effect transistors which have high impedance gates are particularly sensitive to ESD. They have extremely low gate to drain and gate to source leakage on the order of less than 1 nanoampere and relatively high breakdown voltage of greater than 50 volts. Therefore the gate to drain and gate to source are usually the most sensitive ESD paths.

Schottky barrier junctions, such as the 1N5711 diode and TTL Schottky integrated circuits, are particularly sensitive to ESD because they have very thin junctions and the presence of metal which may be carried through the junction.

Not all diodes, transistors and thyristors contain semiconductor junctions that are considered sensitive to ESD. Some transient suppressor diodes, zener diodes, power rectifiers, power transistors and power thyristors have been found to be insensitive to ESD. Semiconductor junctions as sensitive ESD constituents are found not only in diodes, transistors, and bipolar integrated circuits but also in MOS as parasitic diodes and input protection clamps, although the input parts protection junctions are meant to provide protection from ESD damage, the size of the protective junctions are limited due to cost and performance tradeoffs. Thus ESD pulses of sufficient energy can damage the input protection junctions.

50.2.2.2 Failure mechanisms. The temperature coefficient of extrinsic semiconductors is positive. That is, the higher the temperature, the higher the resistance. This prevents current crowding and hot spots from forming at low temperatures. However, in the reverse biased mode all the energy is being dissipated by the relatively large voltage drop across the relatively narrow depletion width of the junction. Due to geometry effects, local resistance

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variations, and crystal defects, perfectly uniform current distribution does not occur across the junction. As an ESD occurs across the junction the temperature at the depletion region increases quickly and the extrinsic semiconducting material becomes an intrinsic semiconducting material, causing a sharp decrease in resistance, resulting in thermal secondary breakdown.

The more rapid the discharge, the more uniform the increase in temperature and therefore current across the junction. This means that for short duration discharges of less than 10 nanoseconds the resultant filament short is wide compared to longer duration discharges. It is possible for hot spots to develop but not grow completely across the junction such that at low bias voltages they do not cause a failure condition. However, during operation at certain bias conditions, locally high current densities may exist with a corresponding large increase in temperature at the previously formed hot spot locations. Thus, growth of a filament short may continue or silicon and metallization may diffuse through the junction via the electromigration process at temperatures greater than 200°C. The low leakage high breakdown JFET and Schottky barrier junctions seem to be particularly susceptible to this failure process. It is this same failure process that requires the breakdown test on JFETs be performed as a leakage test rather than by putting the junction into breakdown. With low leakage junctions, highly localized currents can occur during junction reverse breakdown. With Schottky barrier junctions, metallization is immediately available to migrate through the junction at localized hot spots.

50.2.2.3 Failure indicators. As the current filament develops across a semiconductor junction it is analogous to putting a short across the junction. High leakage current will be the failure indicator description.

50.2.3 Film resistors. Resistor material adhering to an insulating substrate comes under the ESDS constituent classification of film resistor. The degree of sensitivity will depend on the ingredients and formulation of the resistor material and size-power considerations.

50.2.3.1 Part types. Hybrid microcircuits frequently contain either thin film resistors or thick film resistors. Hybrid designs which cannot tolerate large changes in resistance, such as precision voltage regulators, are sensitive to ESD. Thick film resistors consist of a conductive metal oxide as the resistive element, a metal additive to improve electrical performance, and a glass frit to provide a support matrix, adhesion to the substrate, and resistivity control. Such parts are particularly sensitive to ESD. Since the change in resistance is almost always negative for thick films, electric discharge has been considered as a possible trimming method when conventional trimming overshoots the desired resistance tolerance. It has also been found that the thick film resistance changes are heavily dependent on voltage rather than energy.

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Thin film resistors, on the other hand, are more energy dependent and do not have changes greater than five percent in resistance until the energy of the discharge is sufficient to cause film rupture. In addition to hybrid microcircuits, some monolithic integrated circuits may also contain encapsulated thin film resistors, such as polysilicon resistors, as part of an input protection circuit.

Discrete encapsulated resistors which contain the film resistor structure are also sensitive to ESD. Carbon film, metal oxide, and metal film resistors are somewhat sensitive to ESD, especially at low tolerance and low wattage ratings. A frequent problem occurring with resistors is with the 0.05 watt metal film, part RNC50, specified at 0.1 percent tolerance. Putting these parts in a polyethylene bag and rubbing them on another bag is sufficient to shift the tolerance of these resistors.

50.2.3.2 Failure mechanisms. The ESD failure mechanisms of film resistors are not well defined. This is partly the result of not knowing the ingredients and formulations of the resistor material which are often held proprietary by the manufacturer.

For thick film resistors, the failure mechanism has been modeled as the creation of new shunt paths in a matrix of series-parallel resistors and infinitesimal capacitors isolating metallic islands. With the application of high electric fields the dielectric breakdown of the glass frit or other isolating dielectric material is exceeded and the ensuing rupture welds metallic particles together in a conducting path known as metallization melt. Since this model involves a dielectric breakdown process it is mostly voltage dependent.

It appears that the ESD behavior of resistive materials is very much a function of the number of parallel current paths, or the number of capacitive couplings between parallel paths in the film structure. The nature of the glass used in the material also appears to be quite important, both because it influences the distribution of the resistive elements and because it can act itself as a resistive element. Thus, the behavior of different thick film resistor paths to ESD can vary greatly. ESD sensitivity testing, therefore, should be specified for critical tolerance thick film resistors. For thin film resistors and encapsulated metal film, metal oxide and carbon film resistors, the failure mechanism is primarily a thermal, energy dependent process modeled as the destruction of minute shunt paths. This mechanism is associated with an increasing resistance. At a lower ESD voltage, there is some small negative resistance shift of the thin film and metal film type resistor which appears to be voltage dependent. This negative shift is usually not more than 5 percent and is typically less than 1 percent before changing to positive shifts as ESD voltage increases.

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50.2.3.3 Failure indicators. Some thin film resistors, such as deposited tantalum nitride on SiO_2 substrates, may be so small and power limited that human body model (see Appendix D) ESD voltages greater than 5,000 volts can melt the resistor open. In most cases, a shift in resistance will be the failure indicator. Thus for circuit designs tolerant of large resistance changes, the failure may not be critical. Generally, after exposure to an ESD, the stability of the resistor is reduced and the degree of instability is directly related to the level of ESD. Temperature coefficient changes have been known to result from such ESD exposure.

For thick film resistors, the resistance shift is negative. The resistance change can easily exceed 50 percent with some thick film pastes. Some exceptions to this may occur, especially at low resistance values.

For thin film, metal film, metal oxide and carbon film at lower ESD levels, small negative resistance shifts of less than five percent can be experienced. At higher ESD levels, large positive shifts greater than ten percent can be experienced, depending on the power rating.

50.2.3.4 Metallization strips. Relatively narrow thin metallizations on a substrate, such as SiO_2, which carries current between terminals without any other energy absorbing element in the path, are susceptible to ESD. These metallizations may consist primarily of aluminum or gold but can also be multi-layered. The failure mechanism is burnout from joule heating. This type of constituent is often used in monolithic integrated circuits, hybrid microcircuits and multiple finger overlay transistor construction found in switching and high frequency transistors. Joule heating is most likely to occur when: (1) the ESD source has very low contact resistance, resulting in high currents over short time constants; and (2) a low resistance large area diode is connected by the metallization path between the two terminals, resulting in large currents due to the low voltage drop in the diode forward biased direction. Increasing the width or thickness of the strip will decrease ESD sensitivity. The use of glassivation and thinner SiO_2 regions between the strip and the silicon also reduces ESD sensitivity. The failure indicator from this failure mode is open.

50.2.4 Passivated field effect structures with nonconductive lids. Various NMOS and PMOS integrated circuit designs have been found to fail from very localized high concentrations of positively charged ions on the outer passivated surface of the die. NMOS designs fail from excessive leakage currents from field inversion between N+ junctions such as thick field parasitic transistors, intermediate field parasitic transistors, EPROM transistors and normal select transistors. PMOS designs such as the floating gate, EPROM or depletion type field effect transistors fail when the negative charge on the floating gate is overcompensated by positive charge clusters on the outer surface of the die. This causes the part to turn off, giving an erroneous unprogrammed indication. The effective field from the positively

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charged ions needed to create this inversion has been found to exceed 85 volts per meter. Hermetic packages which have recorded this failure mode have nonconductive lids made from nontransparent ceramic, transparent sapphire and transparent borosilicate glass. These failures can be prevented by grounding the bottom surface of the lid over the die or by instituting preventive measures to avoid electrostatic charging of the nonconductive lid.

50.2.4.1 Part types. This failure mechanism is most common with NMOS and PMOS UV EPROMs having transparent lids. NMOS static RAMS in a ceramic package, however, have also been reported to fail from this ESD failure mechanism. Unless testing shows otherwise, LSI integrated circuits with nonconductive lids could conceivably have field effect structures which are susceptible to failure from undesirable field inversion or gate threshold voltage shifting.

50.2.4.2 Failure mechanisms. This failure mechanism involves positively charged ion clusters deposited on the die as a result of air breakdown in the air gap between the die surface and the bottom of the package lid. Charging of the bottom of the lid can be induced by several means, one of which is by freeze spraying the package with canned coolant. The positive charging rate of the freeze spray impinging on the top of the lid depends on the flow rate of the coolant from the can. At low flow rates the charging is negative and does not induce failure; at high flow rates sufficient positive charging can occur to induce failure. The localized air breakdown in the air gap of the package causes ionized streamers to form from the die to the lid. The positive charge on the bottom of the lid drives the positive charge in the streamer toward the die surface and attracts the negative charge toward the lid. This results in very localized clusters of positive ions on the die surface. Because of the nature of the air breakdown for certain package internal ambients, this charge is probably identical in type to the very large ions that can be experimentally created by positive corona discharge in air.

These localized positive charges also cause the formation of inversion layer leakage paths between N+ diffusions and shift the gate threshold voltage on PMOS depletion type transistors. The formation of leakage paths and the gate threshold shifts gives rise to isolated circuit failures.

This failure mechanism is recoverable by neutralizing the positive charge on the outer surface of the die. On UV EPROMs with transparent lids, recovery is nondestructive when 2,537 Å ultraviolet light with a minimum photon energy of 4.3 electron volts (eV) is applied to the chip for as short as 3 to 5 seconds.

50.2.4.3 Failure indicators. The failure indicators for this failure mode come under the general classification of operational degradation. This operational degradation will take the form of a functional failure. In the case of NMOS UV EPROMs, certain programmed bits appear unprogrammed and certain unprogrammed bits appear programmed. In one group of failure indicators, bit

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failures have been organized in columns where programmed bits appeared unprogrammed. In another group of failure indicators, bit failures were organized in rows where unprogrammed bits appeared programmed. The failure indicators for PMOS UV EPROMs are random single bit failures throughout the memory. The failure indicators for an NMOS static RAM have been reported as random bits stuck in a "1" or "0" logic state with an adjacent cell also stuck but in the opposite logic state.

50.2.5 Piezoelectric crystals. Part types such as quartz crystal oscillators and surface acoustic wave (SAW) devices can fail from ESD resulting in operational degradation. Electrical parameters of piezoelectric crystals contained within these parts are damaged by excessive driving current. The piezoelectric effect from high voltages causes mechanical stress and movement to be generated in the crystal plate. When the voltage is excessive, mechanical forces cause motion in excess of the elastic limit of the crystal and crystal fracture occurs. The fracture may occur as a lifted platelet as has been experienced in lithium niobate SAW delay lines. Such fractures, when occurring in sufficient number, will cause enough change to the operating electrical characteristics to cause failure.

50.2.6 Closely spaced electrodes. When employing thick metallization such as 13,500 Å, gaseous arc discharge in an arc gap 50 μm wide can be used as a protection device to dissipate incoming high voltage spikes. For parts with closely spaced unpassivated thin electrodes, however, gaseous arc discharge can cause degraded performance. Parts that employ thin closely spaced electrodes include surface acoustic wave (SAW) devices. Other parts, such as high frequency multiple finger transistors and new technology such as very large scale integration (VLSI) and very high speed integration (VHSI), could also be degraded to failure from arc discharge between metallization runs. The arc discharge causes vaporization and metal movement generally away from the space between the electrodes. The melting and fusing do not move the thin metal into the interelectrode regions but the metal pulls together and flows or opens along the electrode lines. There can be fine metal globules in the gap region but not in sufficient numbers to cause bridging. Shorting is not considered a major problem with unpassivated thin metal electrodes. ESD failures have been experienced on surface acoustic wave (SAW) band pass filters with thin metal of 4,000 Å and electrode spacing of 3.0 μm.

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APPENDIX C

CASE HISTORIES OF EOS/ESD FAILURES IN MILITARY ELECTRONICS

10. SCOPE

10.1 Scope. This appendix provides selected case histories of EOS/ESD failures from military electronics analyzed by the Department of Defense (DOD) Field Failure Return Program (FFRP). This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. INTRODUCTION

30.1 General. Both military contractors and the Government lack useful field reliability data. Field failures are typically discarded during the maintenance process, and there is no established means to track and capture meaningful piece part field data that is supported by detailed failure analysis. Rome Laboratory and the Reliability Analysis Center (RAC), a DOD Information Analysis Center (IAC) have operated the DOD Field Failure Return Program (FFRP) since August of 1987 to remedy this situation. The program is designed to provide feedback to industry and identify the root causes of field failure so that corrective actions can be implemented. This appendix reviews some case studies from the program where failures were the result of electrical overstress (EOS) or electrostatic discharge (ESD) and presents the relative percentage of removals caused by EOS and ESD events.

40. SUMMARY OF RESULTS

40.1 Summary of results. Over 2000 part failures from over 24 different military systems have been collected and reviewed. Ninety-five percent of the parts analyzed were actual field failures from operating military equipment that had been operating in the field for two to ten years. Most of the failures have been from DOD equipment such as radars, electronic warfare pods and navigational equipment. The data represents a wide variety of part types (more than two hundred different part numbers) and usage environments. Over 80 detailed failure analyses have been performed. The results of these analyses are categorized as shown in Figure 2.

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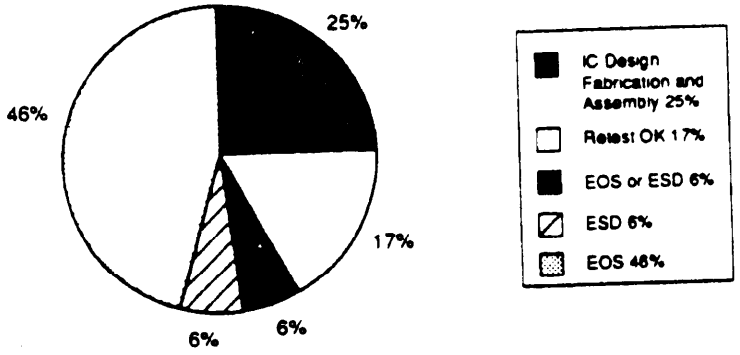

FIGURE 2. Failure Categories Based on Completed Failure Analysis.

As the pie chart in Figure 2 shows, 46% of the completed failure analysis (FA) reports identify EOS as the primary reason for the field removal. Two random samples of the 1650 field returns support this number. In one case four of nine parts delidded showed obvious EOS damage on the die surface and in another case nine of sixteen parts sampled were obviously EOS damaged. These failures are unique system application problems caused by poor system design or improper maintenance/operational procedures. In a few cases the evidence indicated ESD was the cause of failure (6%). Some of the field return data indicated that the damage was caused either by a powerful ESD event or an EOS event. These FA reports are categorized as "EOS or ESD" in Figure 2. Figure 2 also shows a substantial percentage of removals (17%) were functional when retested.

The IC Design Fabrication and Assembly category (25%) are parts with inherent flaws or latent defects manifested as field failures. The Retest OK category comprises the balance of the pie chart in Figure 2. Cracked solder joints, inaccurate diagnostics, and intermittents are some of the causes for these types of field removals.

The data in Figure 2 should be viewed with caution since true "field" data is difficult to neatly categorize and define. Figure 2 is a good first look at what is happening in the field, but much work remains, including increasing the population of parts analyzed, following up on corrective actions, and determining the field failure rate of the piece part involved. One should keep in mind that these part failures are mostly from avionic

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equipment where power quality is always a concern, so a large number of EOS failures are not surprising. Also, to duplicate and correctly identify an ESD event can be extremely costly and time consuming. There are several parts categorized as EOS that were suspected to be ESD but have not been confirmed.

50. SELECTED CASE HISTORIES

50.1 Selected case histories. The following case histories are used to illustrate the characteristics of EOS/ESD type field failures from operational military equipment.

50.1.1 ESD faults of monolithic dual n-channel JFETs. At an Air Force Air Logistic Center (ALC), suspected high failure rate parts are screened out of stock prior to use in the repair of avionic equipment. A sample of high failure rate parts suspected of being subjected to ESD were sent for failure analysis. The parts were monolithic dual n-channel JFETs (2N5197) and electrical testing agreed with the electrical data provided by the ALC. The parts arrived in approved ESD packages and ALC technicians took all necessary ESD precautions in the testing and handling of the device. The electrical data showed the gate to source breakdown voltage was practically zero, and the gate-to-source current was very high, which would indicate a gate oxide breakdown.

The gate-to-source short was barely visible with an optical microscope. The defect was not visible in the scanning electron microscope (SEM) prior to removal of the glassivation layer. Once this passivation was removed, the ruptured oxide above the junction punchthrough could be clearly seen. In all four parts analyzed, the short occurred at the very tip of the source metal run. This problem is still under investigation.

50.1.2 Digital to analog converter (DAC) failures caused by ESD. Five failed DACs were found to have shorted bit inputs on their CMOS analog multiplexer chips which were probably caused by electrostatic discharge. The hybrid failures were from a heads-up display in a fighter aircraft. There was no visible indication of any damage. The surface films were removed from the failed chips and extremely small gate oxide ruptures were found at the edges of source or drain diffusions only after SEM inspections.

A very effective technique for locating the failure sites in the SEM is to simply image the device using a low beam potential (about 2.5 KV) after removal of the gate metal. The surface of the gate and field oxides apparently charge to a positive potential while the substrate is grounded through the sample mount. This results in a voltage contrast type image. Open contact cuts and the oxide rupture sites are light because they are grounded through the substrate but good oxide areas are dark. Good gate oxides were also imaged this way, and they showed no bright spots. Energy dispersive X-ray analysis of two of the oxide rupture sites showed aluminum (alloyed gate

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metallization) in one case and magnesium (probably contamination from surface film etching) in another.

Some tests were done to try to simulate the cause of the failure using an ESD simulator. Similar damage sites were induced using a charged device model test. In this test, the device was charged to 500V through one bit input pin with all other pins floating and then discharged to ground through the same pin. It is thought that this test simulates a machine or materials related ESD event as opposed to a human body ESD event. The energy of the ESD pulse is stored in the parasitic capacitance of the overall device/pckage assembly to the outside world. The metal package of this hybrid is electrically floating (not connected to a device pin) and this may be related to this device's sensitivity. A charge build-up might occur between the case and internal circuit, which could then be discharged by grounding either the case or the circuit pins.

It is interesting to note that four of the five failures involved a corner pin, pin 1. The corner pins are thought to have a higher probability of receiving an ESD event from the environment because they most often touch first whenever the device is placed on a surface.

As a result of this failure analysis report, the packaging and handling procedures to improve ESD protection were reviewed, and a recommendation was made to electrically ground the metal case of the hybrid package.

50.1.3 EOS/ESD microprocessor faults. A microprocessor used in a Doppler radar of a strategic bomber was found to be failing in the field at a greater than 50% rate. At least half the time this radar was returned to depot, the microprocessor was found faulty and replaced. This microprocessor chip is considered a Class 1 device with a 0 to 1000V sensitivity. Nine of the nineteen parts collected for failure analysis showed visible damage at three different contact locations surrounding the bonding pad at the reset pin #5. An EOS/ESD event due to improper handling was suspected since pin #5 on the microprocessor is the only pin that is connected directly to an output pin on the circuit card. During routine maintenance of the radar set, this circuit card is removed and replaced frequently. This type of checkout is done on automatic test stations at the intermediate avionic shops in the field. Until recently the technicians in the field handled the circuit cards without taking proper ESD precautions.

In an attempt to recreate the conditions of failure, two good devices were subjected to repeated ESD pulsing using both the human body and charged device models. At the plus or minus 5000V (the limit of the equipment) level neither device showed any visible signs of damage. Both devices were then subjected to lower voltage levels for longer time periods. Visible damage was noticed when exposed to 60 volts for 5 seconds which was similar to what was

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seen in the field failure. However, there was not much damage at the other two sites.

Often it is difficult to tell the difference between a device that has been damaged by an electrical overstress versus an electrostatic discharge. This is especially true when analyzing field failures since the circumstances of failure are difficult to reproduce. In this case, it was probably a lower voltage (longer time) event because of the massive metal damage. However, there is some question about whether an ESD event much above 5000V could have caused this damage. A corrective action is under evaluation to modify the circuit card to prevent further damage from handling.

50.1.4 Bourns type 3269 cermet trim potentiometer. A 200 ± 10% Kohm Bourns type 3269 cermet trim potentiometer was being used in a low voltage, low current application. The resistance value of some potentiometers were quickly decreasing in value during use. Three good potentiometers and one confirmed failure were analyzed. The resistance value of the good devices were found to be within specification. The resistance of the bad device was a constant 164 Kohms.

The next step was to list all of the physical mechanisms that could cause the reduction in potentiometer resistance. Only two possible mechanisms could be found to explain the resistance shift. The first was contamination in the vicinity of the cermet resistive element which would allow for a parallel conduction path thus lowering the effective resistance. The second mechanism was an electrically induced breakdown of some of the glass binders in the cermet creating more conduction paths through the resistor thus reducing its value. Both mechanisms were simulated and duplicated the reported resistance shift.

The first mechanism investigated was that of a parallel conduction path. One of the good devices was mechanically decapsulated using a knife. The resistive element was measured before and after decapsulation with identical results. A salt (sodium chloride) solution was deposited on the resistive element and the resistance immediately dropped to levels below the specification limit. By adjusting the concentration of the solution and the moisture levels, it was possible to duplicate the 164 Kohm reading. The moisture level was controlled by the dampness of a piece of paper towel placed over the resistive element. Upon removal of the paper, the resistance would return to its original "as received" level.

Both the good element and the bad potentiometer were baked at 150°C for 10 minutes and returned to room temperature for resistance measurements. This cycle was repeated three times. In every case, the resistive elements returned to their prebake values. Based on this testing the contamination mechanism was ruled out.

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Before discussing the experiments on the second mechanism, the electrically induced breakdown of the glass binders, it would be well to review the basic electrical conduction mechanism of cermet (thick film) resistors. The resistors are a heterogeneous mixture of metal/metal oxide and lead silicate glass. Organic resins and solvents are added to the mixture to provide screen printing characteristics. The organic portions of the paste are removed by evaporation and oxidation during the drying and firing cycles. Typical firing temperatures are in the area of 800°C to 1000°C. After the firing, only the glass and metal mixture remains. The metal/metal oxide parts are joined to form a continuous three-dimensional network of chain segments within the glass binder. Conduction is through a tunneling barrier method. If a voltage is supplied across the resistor sufficient to break down some of the thin glass binder material between conductive particles, then more conduction can occur as a result of the decreased resistance. In the early days of cermet resistors this was intentionally done (a practice called "voltage bumping") to adjust resistors to lower values. The process resulted in stable resistors, but it was hard to predict the amount of voltage shift. The literature also contains information on ESD caused resistance shifts in cermet resistors.

An experiment was run on a good resistor and a bad resistor applying a series of 20 KV spikes to the resistors. The ESD pulses were applied using an ESD simulator. This system discharges a 100 pf capacitor through a 1,500 ohm series resistor. Both the literature and the theory of conduction in cermet resistors would lead to the fact that continual pulsing of the resistor with the same electrical pulses should result in decreasing resistance until an asymptotic level is reached. With a larger capacitor the level would probably be reached sooner. This is because the glass breakdown limit level is controlled by the voltage whereas the damage by each pulse is more a function of the energy in that pulse.

Both the good and bad units were pulsed in steps of 10 pulses between each resistance measurement. The good resistor took 80 pulses to reach an asymptotic level while the failed resistor only required 40 pulses. The good resistor had a 17% shift in resistance whereas the failed resistor only shifted 9.5%. This lends strong credence to the voltage spike theory. The failed resistor had been partially broken down so that both the resistance shift and the number of pulses required to reach an asymptote was about half of that for a good resistor.

The Bourns cermet model 3269 trim potentiometer was most likely damaged by a high voltage transient. This is supported by the following facts:

1. The failure occurred suddenly.

2. The resistance values remained stable at each level before and after pulsing.

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3. The induced damage to the failed part by voltage pulsing was only half of that for the good part (indicating previous voltage damage).

50.1.5 Conclusions. The previously presented case studies represent only a few selected examples of failure analysis of components in which the suspected cause was EOS or ESD. They were selected to provide information on the different types of failures seen in military systems and also to provide examples of the methodologies required to identify the root causes of failure.

The following conclusions can be drawn from these failure analyses; 1. Many field removals are a result of EOS or ESD, and 2. It is often difficult to distinguish between EOS and ESD failures.

Corrective actions such as, modification of the part or system design, selection of a less sensitive new part, addition of a protection network, or implementation of ESD safeguard measures are often effective solutions to problems in military hardware. Additionally, identification of EOS/ESD failures and corrective action can be extremely cost effective since recurring failures can often be avoided.

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APPENDIX D

ESD TESTING

10. SCOPE

10.1 Scope. This appendix addresses ESD part testing, using the MIL-STD-883/MIL-STD-750 human body model test circuit as referenced by MIL-STD-1686. For informational purposes additional types of ESD testing such as the charged device model, field induced model, machine model, and charged chip model are discussed. Assembly and equipment level testing methodologies are also discussed. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

20.1 Government documents.

20.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

MILITARY

MIL-S-19500 - Semiconductor Devices, General Specification for.
MIL-M-38510 - Microcircuits, General Specification for.
MIL-H-38534 - Hybrid Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-750 - Test Methods for Semiconductor Devices
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Bldg. 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

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20.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

INTERNATIONAL ELECTROTECHNICAL COMMISSION (IEC)
801-2 - Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment, Part 2: Electrostatic Discharge Requirements.

(Application for copies should be addressed to the American National Standard Institute, 1430 Broadway, New York, NY 10018.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

30. ESD TEST MODELS

30.1 Human body model (HBM). People are prime sources of ESD damage, therefore the test circuit used in MIL-STD-1686, by reference to MIL-STD-883/MIL-STD-750, is based upon a human body model. Electrostatic charges generated by contact or rubbing materials (such as clothing) are readily transmitted to a person's conductive sweat layer causing that person to be charged. When a charged person handles or comes in close proximity to an ESDS part, the part may be damaged by direct discharge or by an electrostatic field. The ESD from a person can be reasonably simulated for test purposes by means of the MIL-STD-883 Method 3015 and MIL-STD-750 Method 1020 test circuit. These test circuits are also referenced in MIL-M-38510, MIL-H-38534/MIL-I-38535, MIL-S-19500 and have been widely used in the military and industry for ESD testing. The selected values for human body model capacitance (100 picofarads (pF)) and resistance (1,500 ohms) are not based upon a worst case model. Selection criteria for these values are discussed below.

Human capacitance may be as high as several thousand pF, but is typically 50 to 250 pF. A study performed on human capacitance indicated that approximately 80 percent of the population tested had a capacitance of 100 pF or less. The variation in human capacitance is due to factors such as variations in the amount and type of clothing and shoes worn by personnel, and differences in floor materials.

Human resistance can range from 100 to 100,000 ohms, but is typically between 1,000 and 5,000 ohms. The variation in human resistance is due to factors such as the amount of moisture, salt and oils at the skin surface, skin

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contact area, and pressure. A value of 1,500 ohms provides a reasonable lower human resistance value. For energy sensitive parts, an increase in human body model capacitance to greater than 100 pF could result in damage to ESDS parts at voltage levels below those shown in MIL-STD-1686 appendix B. For instance, energy sensitive parts damaged at 400 volts using the 100 pF, 1,500 ohm human model would be damaged by slightly less than 300 volts had a 250 pF, 1,500 ohm model been used. Therefore, a part not considered as ESDS could actually be ESDS under more stringent human body model conditions. For predominately voltage sensitive ESDS parts, a variation in the capacitance value in the test circuit will cause little effect on the sensitivity. A decrease in the test circuit resistance will increase the voltage and energy delivered to the part and, therefore, the voltage level which causes damage decreases. The human body model of 100 pF, 1,500 ohms is considered to be a reasonable test circuit for standardizing the ESD sensitivity of parts.

Some ESDS parts are voltage sensitive while others are energy sensitive. In general, voltage sensitive parts fail due to dielectric breakdown of insulating layers or junctions. That is, the pulse shape, duration and energy can produce damage levels resulting in part thermal breakdown when the voltage level is below that needed to cause dielectric breakdown. The pulse is defined by the test circuit, the part resistance and capacitance (R-C) characteristics, the R-C time constant of the test circuit and the voltage at the capacitor. Thus, for a given test circuit with a fixed R-C (such as the MIL-STD-883 method 3015 test circuit) and a part with a given R-C, the voltage of the capacitor determines the shape of the pulse. Therefore, ESD sensitivity can be expressed as a voltage for both voltage and energy sensitive items for the given test circuit and part.

30.2 Charged device model (CDM). This model considers the case of a device that is charged on its lead frame or other conductive paths, and then quickly discharged to ground through one pin. In this case, charges residing on the metal parts of the die and package flow through the die and create failures of junctions, dielectrics and devices that are part of the discharge path. Device lead frames and packages can be charged triboelectrically just as the human body is charged. The voltage and the energy in such a device will depend on the position and orientation of the charged device with respect to ground.

The CDM sensitivity of a given device may be package dependent. Early experimental data indicates the same integrated circuit chip in a dual-in-line package (DIP) may be more susceptible to CDM damage when placed in a small outline package (SOP) or a pin grid array (PGA) package.

Experimental results indicate that the CDM discharge current is fast and oscillatory in nature, having both positive and negative polarities during the discharge, with risetimes measured in hundreds of picoseconds. By comparison, the HBM discharge has a typical rise time of 10-20 nanoseconds (ns) and

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durations measured in hundreds of nanoseconds. The equivalent circuit that gives responses similar to a CDM discharge characteristic is effectively a series LCR resonant circuit. The inductance (L) represents the package lead frame inductance which can vary between 1 and 20 nanohenry (Nh), depending upon the type of package used. The CR portion is actually composed of several small capacitors in parallel, each in series with a resistor. Two equivalent circuit representations for this model are commonly used. One applies solely to bipolar devices and the other to MOS type devices.

Figure 3 is the equivalent circuit representation for bipolar devices. The model includes the device capacitance, inductance and resistance and some path contact resistance. Depending on its capacitance and the voltage it is charged up to, the device can store substantial amounts of energy to be released on contact with ground with average powers per pulse ranging from several hundred to several thousand watts. Such powers are sufficient to degrade device parameters or melt silicon, similar to the human body model case.

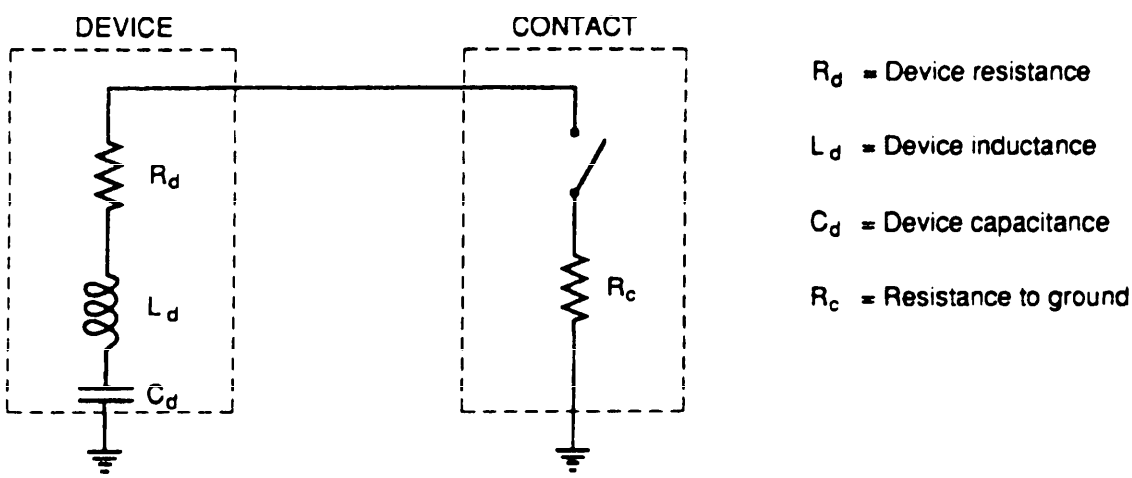

FIGURE 3. Equivalent circuit - bipolar devices.

The CDM MOS equivalent circuit is shown on figure 4. This model depicts multiple paths in the device with their own lumped elements. When one pin is grounded, each path on a device responds with its own characteristic discharge trace, and this leads to a potential difference between paths. If two such paths with significant differences in their discharge characteristics should cross or lie near each other, potentials exceeding the dielectric strength of the insulation between paths may occur with subsequent dielectric breakdown. In this model the charge is generated triboelectrically and resides on the

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conductors of the device and package. The capacitance of a device is a variable, depending on device size, construction, and orientation to ground. Since the potential and stored energy vary inversely with device capacitance, given that the charge is constant, a reorientation of the device can either increase or decrease the device potential and energy.

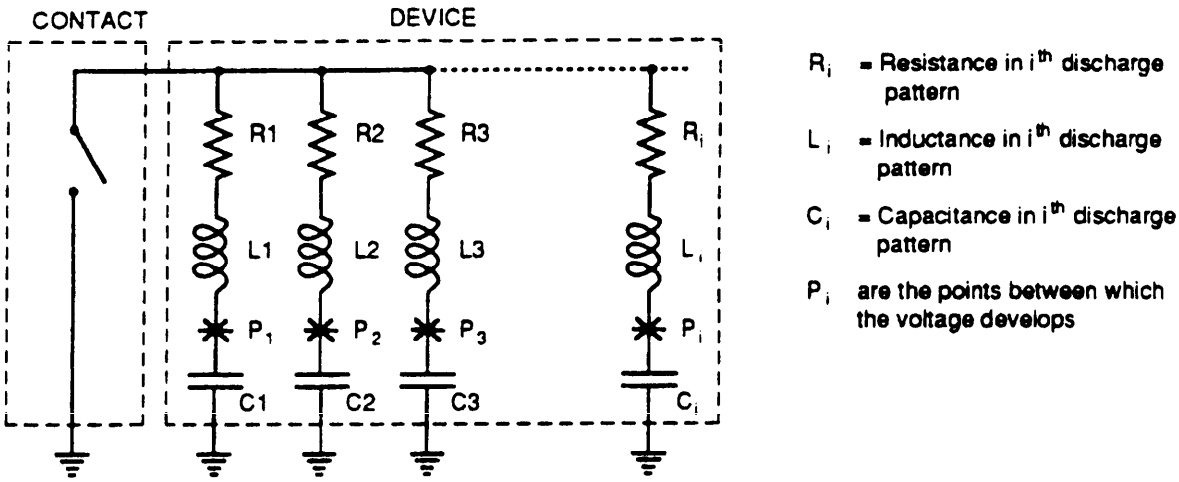

FIGURE 4. Equivalent circuit - MOS devices.

When devices on microcircuits are charged and inadvertently grounded, the energy in the discharge pulse is the sum of the energy stored on the device and on some of its connecting paths. The greater the energy the more potential for damage. Circuit boards with devices whose leads are routed directly to the terminals or edge of the boards are particularly susceptible to ESD damage during assembly and troubleshooting. These paths should be protected either by incorporating suitable path circuitry to shunt or reduce the discharge pulse power, or by using suitable ohmic edge board finger protectors to safely bleed the charge during handling.

In the case of HBM discharges, studies have revealed that damage is associated with metal penetration of junctions. This damage can be observed even when protective structures turn-on or function as designed. For CDM discharges, the current rise time is fast with an oscillatory waveform and protective structures may not have adequate time to function. Thus, CDM discharge can often be recognized because the damage occurs in the oxide (gate and field) areas. To ensure a high level of protection against the CDM discharge, it is necessary to have a large capacitance, with a small series resistance directly on the bond pad of the chip.

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Gate oxides that fail in the charged device test are always near a pad, and either the gate or drain connection may lead to the pad. Analysis of charged oxide device test failures has led to some general design principles for avoiding oxide damage. Some design strategies are aimed directly at limiting the voltage across vulnerable gates. Most others indirectly limit the gate voltage through layout and voltage clamping of power and ground buses. As most of the package charge flows through these buses, there is the distinct possibility of excessive voltage excursions, which threaten thin gate oxides.

30.3 Field induced model. All devices will experience charge separation and discharge if placed in an electrostatic field and grounded. The field induced model simulates a situation in which a device is contacted to a ground source while in the presence of an electrostatic field, resulting in a high amplitude, short duration ESD transient. Figure 5 illustrates this concept using a dual in-line package (DIP) device. First, an uncharged device is placed in an electrostatic field causing a charge separation in accordance with electromagnetic field principals. If the device is then contacted to ground (or any body of sufficiently large capacitance), the resulting charge redistribution results in an ESD. Additionally, the device now has a net charge and, if it is removed from the electrostatic field, it is susceptible to damage from a charged device type of discharge. This illustration also assumes zero resistance to ground upon discharge.

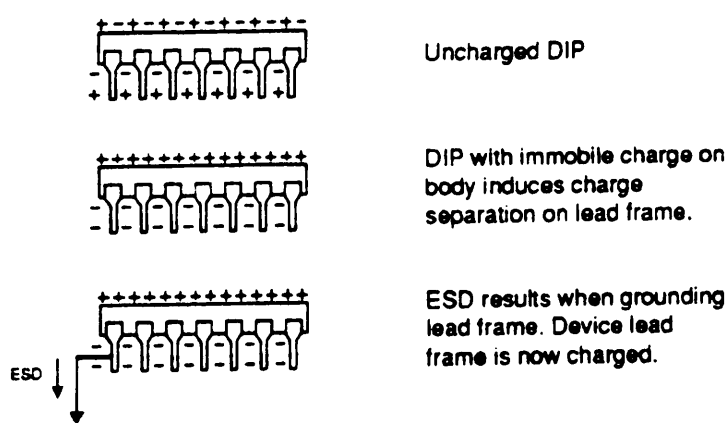

FIGURE 5. Charge induced on device.

30.4 Machine model. A variation of the HBM is the 200 Pf, zero-ohm machine model originated in Japan. This model represents the discharge occurring from the charged cables of a device or board tester. Test results using this model vary widely because series inductance is not specified. Some testers have

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series inductance values of 150 millihenry (mH) or more, which limits current rise time.

30.5 Charged chip model. The charged chip model (CCM) represents the ESD damage that may occur in the chip pick up operation of the framed carrier process. The bare chip, divided to each of the devices on the isolation film, is picked up by the metallic collet. At this time, an ESD may occur between the chip and collet, because the electrical potential of the chip is high as a result of the electrostatic charges on the film. The discharge current, having a very fast rise time, flows into the chip through the collet. This transient high voltage is applied to the gate oxide film before the diode connect substrate to the gate oxides can respond and results in damage to the chip.

40. TYPES OF ESD TESTING

40.1 General. Testing methods are described in the following paragraphs. The test circuits of MIL-STD-883 Method 3015 and MIL-STD-750 Method 1020, as required by MIL-STD-1686, are applicable to ESD classification testing of parts, assemblies and equipment. Part failure is defined as the inability of a part to meet one or more of the electrical parameters of the part specification. When an electrical parameter has not been specified, a change of 10 percent or more of the parameter after testing voltage is applied should be considered a failure. However, any measurable change in a part electrical parameter, due to an ESD, could be an indication of part damage. In addition, ESD testing is considered to be destructive. Therefore, parts subjected to ESD testing shall not be used in deliverable hardware.

40.2 Latent defect testing. The susceptibility of ESDS parts to latent defects can be evaluated by methods such as the following. One method is a form of accelerated testing where ESDS parts are pulsed approximately 25 percent below their known voltage sensitivity levels with multiple discharges until failure occurs. Some ESDS parts are weakened by successive discharges and this weakened condition reduces part life. The use of multiple discharge testing is realistic since parts can be exposed to ESD pulses many times during their life, for example, during production, packaging, transportation, receipt inspection, kitting, assembly, and test. Another method is to subject a sample of parts to single or multiple discharges below their ESD voltage and energy sensitivity levels. Parts exhibiting performance characteristics within specification limits are then put on life test with a control sample not subjected to the ESD pulsing. It should be noted that use of elevated temperature to achieve accelerated life testing may result in healing of dielectric punctures caused by an ESD. Statistical evaluation of the lives of the two samples can be used to determine the effects of ESD latent defect failure mechanisms on part life. Another approach to the evaluation of latent defects can be based upon analysis of failures and historical trends where such data is available.

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Damage due to discharge testing as provided above can be accumulative for some part types. Furthermore, an excessive repetition rate of discharges could build up hot spots in the part and cause an acceleration of the failure effects. Discharges should, therefore, be time spaced to allow for cooling within the part.

40.3 ESD spark testing. Most parts which are sensitive to ESD are also sensitive to other electromagnetic effects. Electromagnetic pulse (EMP) caused by ESD discharge in the form of a spark can cause part failure and cause equipment such as computers to upset. ESD spark testing can be performed by discharging the ESD in the form of a spark across a spark gap sized for the ESD test voltage. Another method is to bring the high voltage test lead of the test circuit close to the case or electrical terminal of an ESDS item, while it is operating.

40.4 Lot sample testing. Another consideration for ESD testing is to perform testing on lot samples of parts used in large quantities. Variations in lots from the same manufacturer, variations in fabrication techniques for specific date codes and variations between manufacturers, often result in differences in ESD sensitivity for the same part type. Lot ESD testing of parts on a sample basis could be used as a quality control check on purchased parts.

40.5 Assembly and equipment testing. The use of part testing procedures for an assembly and an equipment may be prohibitive in terms of costs. In such cases, classification techniques for assembly and equipment should be based on: (1) conservatively, the most ESDS part contained in that assembly; or (2) detailed circuit analysis of the voltage protection afforded by the ESD protective circuitry incorporated in that assembly or equipment. The MIL-STD-1686 Appendix C assembly and equipment test method is an adaptation of the MIL-STD-883 method 3015 HBM ESD test. MIL-STD-1686 Appendix C ESD testing applies only to assembly and equipment inputs, outputs, and interface connection points. This test method is used to determine compliance with MIL-STD-1686 design protection requirements. MIL-STD-1686 Appendix C testing is a destructive test and tested items shall not be used as deliverable hardware.

40.5.1 Assembly test method. Assembly testing is performed using a method and test circuit equivalent to that in MIL-STD-883 Method 3015. The following exceptions to the Method 3015 test apply: calibration and testing is required for 2,000 volts only; and the current waveform verification shall be accomplished at the output of the test apparatus (that is at the point of connection between the test apparatus and the assembly under test). A single assembly of each type shall be tested for ESD design protection at 2,000 volts using the following procedure. Prior to testing, the functionality of the assembly shall be characterized to verify it meets all applicable performance requirements. Each input, output, and interface connection point of the assembly shall then be pulsed with three positive and three negative pulses at a voltage level of 2,000 volts. Each connection point of the assembly shall

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be individually and sequentially connected to terminal A of the test apparatus. The assembly ground or common should be connected to terminal B of the test apparatus. Upon completion of testing, assembly functionality shall be retested. Assemblies not meeting all applicable performance requirements, subsequent to testing, shall be classified as failed assemblies.

40.5.2 Equipment test method. Equipment testing is performed using a method and test circuit equivalent to that in MIL-STD-883 Method 3015. The following exceptions to the Method 3015 test apply: calibration and testing is required for 4,000 volts only; and the current waveform verification shall be accomplished at the output of the test apparatus (that is at the point of connection between the test apparatus and the equipment under test). Each equipment type shall be tested for ESD design protection at 4,000 volts using the following procedure. Prior to testing, the functionality of the equipment shall be characterized to verify it meets all applicable performance requirements. Each input, output, and interface connection point of the equipment shall then be pulsed with three positive and three negative pulses at a voltage level of 4,000 volts. Each connection point of the equipment shall be individually and sequentially connected to terminal A of the test apparatus. The equipment ground or common should be connected to terminal B of the test apparatus. Upon completion of testing, equipment functionality shall be retested. Equipment not meeting all applicable performance requirements, subsequent to testing, shall be classified as failed equipment.

40.5.3 Other test methods. There are other test methods available. One example is the International Electrotechnical Commission (IEC) Publication 801-2. It should be noted that the ESD test generator specified in this procedure uses a capacitance value of 150 pF and a discharge resistor value of 150 ohms.

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APPENDIX E

DESIGN OF PROTECTION NETWORKS

10. SCOPE

10.1 Scope. This appendix provides information for the design of protection networks. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

20.1 Government documents.

20.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Bldg. 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

30. INTRODUCTION

30.1 General. Various protection networks have been developed to protect sensitive electronic parts. These circuit protection networks provide limited protection against ESD. Many of the protection networks designed into MOS devices reduce the susceptibility to ESD to a maximum of 800 volts. MIL-M-38510 VZAP test voltages for CMOS, for example, vary from 150 to 800 volts. Protection circuitry of some devices is improving and protection to 4,000 volts appears to be achievable for some MOS devices. However, electrostatic potentials of tens of thousands of volts can be generated in uncontrolled environments.

30.1.1 Degree of protection afforded. The protection afforded by specific protection circuitry is limited to a maximum voltage and a minimum pulse width. ESDs beyond these limits can subject the part's constituents to damage, or the protection circuitry constituents themselves, which are also

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often made of moderately or marginally sensitive ESDS parts may be damaged. Damage to the protection circuitry constituents could result in degradation in part performance or make the ESDS part more susceptible to subsequent ESDs. The degradation, for example, could be a change in speed characteristics of the ESDS part or an increase in leakage current of the ESDS part. Multiple ESDs, at voltages below the single pulse ESD sensitivity voltage or energy level can also weaken or cause failure of the part or protection circuitry constituents. Loss of protective circuitry may not be apparent after an ESD.

In summary, protection networks reduce but do not eliminate the susceptibility of a part to ESD. This reduction in ESD sensitivity, however, results in a lower incidence of ESD part failure.

The sensitivity of the same type of ESDS part can vary from manufacturer to manufacturer and from lot to lot by the same manufacturer. Similarly, the design and the effectiveness of protection circuitry also varies from manufacturer to manufacturer.

30.2 Protection network elements. The protection elements and their design parameters have to be optimized via an iterative procedure. The chosen design should be implemented, tested to failure, and the failure mode determined. Then a redesign to strengthen the failed structures can be undertaken, and the entire procedure repeated until the desired level of protection has been achieved. The optimization process starts with the analysis of established ESD protection elements, and design of ESD protection networks. The protection elements include diodes, resistors, contacts, metallization, three-layer devices (n-p-n or p-n-p), and four-layer devices (p-n-p-n) which are discussed below.

30.2.1 Diodes. Almost all "on chip" input protection networks employ some form of p-n junction. The factors that affect the characteristics of actual p-n junctions during ESD transients include high electric fields, high current densities, high temperature, and nonuniform current flow (second breakdown modes of operation), which will lead to significant deviation from the low voltage/low current diode characteristics. Consequently, the location of the p-n junction in a protection network is very important. It is imperative that circuit designers know the magnitudes of voltages and currents to be protected against. Furthermore, a clear understanding of the constraints on the breakdown voltage, input capacitance, area constraints, and the effects that an avalanching junction can have on nearby elements is required.

Recent advances in input protection circuit design for advanced CMOS processes include new process-tolerant circuitry based on a lateral silicon controlled rectifier (LSCR). The low-impedance, forward-conducting state provides design stability for a wide range of process variations. The LSCR device is very effective for various CMOS processes ranging from 2 μm abrupt junctions to 1 μm lightly doped drain (LDD) junctions with silicided diffusions. This

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protection circuit can be designed into very-large-scale integration (VLSI) devices with CMOS processes. Latchup susceptibility of this device is not a problem since no direct connection is made to the positive power supply. Caution should be observed to prevent interaction between adjacent input pins. This can be achieved by employing preventive guard rings. The output ESD protection techniques for advanced CMOS processes include: (1) effective design and layout of CMOS buffers to achieve good ESD protection and (2), a new buried diffusion structure that is immune to ESD performance degradation with silicided processes. Because of the suppression of silicidation at the drain junction and the forming of an abrupt junction at the source/drain, this device has an excellent ESD performance for both human body and machine models.

30.2.2 Resistors. Resistors have been used in ESD protection networks for many years, and when properly employed, they can enhance the input protection capability of certain networks. Two major classes of resistors are the diffused and the polycrystalline silicon (poly) types. Studies have shown that protection networks employing poly resistors connected directly to the input bond pad were more susceptible than networks that used diffused resistors. Thus, if resistors are required as part of an ESD protection network, only the diffused type should be considered. Also, the layout of the resistor should avoid 90° turns or any other geometry that could result in non-uniform current and electric field distributions.

30.2.3 Three-layer devices (n-p-n or p-n-p). Three-layer structures are found in all integrated circuit technologies. As a result, the connections to these layers and the spacing between them can have a significant effect on the ESD susceptibility levels of input/output structures. These devices can be formed as a result of source/drain diffusions or when cross-unders and diffused resistors are placed close to each other. Since these parasitic bipolar transistor actions can be triggered by the avalanche breakdown voltage, it is desirable to have control over this voltage. One common way is to lay out parts of the drain junction as a spherical junction, or tailor its breakdown voltage by ion implantation. Also, punch-through and MOS transistor action can act as a trigger for parasitic bipolar action if these modes are controlled in such a way as to initiate significant impact ionization currents.

30.2.4 Four-layer devices (p-n-p-n). Probably one of the most important protection elements, as far as bulk CMOS and bipolar technologies are concerned, is the two-terminal four-layer device (p-n-p-n). In the discrete form, these devices are called thyristors or semiconductor controlled rectifiers (SCRs). In bulk CMOS or bipolar technologies, these four-layer structures are almost unavoidable. However, parasitic SCRs can be extremely effective in protecting against damage caused by ESD transients. With proper optimization of the parameters controlling the SCRs (the direct current

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trigger voltage, holding current, and so forth), superior ESD protection networks can be realized.

To avoid the high field and/or current crowding regions associated with the p-n junctions, a novel on-chip ESD protection device using a static induction transistor principle is used. This method allows the sinking of discharge current directly from the pad to the substrate by implementing a vertical static induction transistor underneath each landing pad. This design avoids lateral flow of discharge current on the chip surface, and removes any reverse-biased junction along the discharge path. In addition, this saves chip area by being implemented under the contact pads, and offers the advantage of high speed and good thermal stability by virtue of being a majority-carrier device.

30.2.5 Contacts. Contacts between aluminum metallization and diffused regions play an important role in determining the ESD susceptibility levels of input structures. ESD hardness can be improved by allowing adequate metal-to-diffusion edge spacing; employing poly tabs for aluminum-poly-silicon contacts; the use of large circular contacts to avoid non-uniform current flow; and if process conditions allow, the use of deep diffusion junctions.

30.2.6 Metallization. A number of studies have shown that the dominant parameters for aluminum metallization failure during transient voltage conditions are the current density and the duration of the voltage pulse. For example, 90 degree turns cause nonuniform current distribution within the turn. Therefore, it is advantageous to avoid 90 degree turns in protection network metallization. Also, metallization at oxide steps may be much thinner than at other locations. Therefore, the widths of metal lines used in ESD protection networks should take into account this reduction in metallization thickness.

30.3 Design considerations for ESD protection networks. Protection network elements must always provide the lowest impedance path to ground for ESD transients, regardless of the pins receiving the transient, so that integral structures are never provoked into carrying the transient currents. The following are some general guidelines to implement protection networks.

(a) The network should defend against threats to all pin combinations.
(b) The network should defend against both polarities of the applied ESD transient.
(c) The design must be insensitive to slight misalignment and process variations.
(d) Use diffused resistors instead of poly resistors.
(e) Use poly tabs between metal-diffusion contacts.
(f) Avoid thin oxides on protection network elements.
(g) Allow adequate contact-to-diffusion edge spacing.

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30.4 Design precautions. Various design techniques have been employed in reducing the susceptibility of parts and assemblies to ESD. Diffused resistors and limiting resistors provide some protection, but are limited in the amount of voltage they can handle. Zener diodes require greater than 5 nanoseconds to switch and may not be fast enough to protect a MOS gate. Furthermore, zener diode schemes, diffused resistors and limiting resistors reduce the performance characteristics of the part which in many instances are the primary considerations for which that part was designed.

30.4.1 Part and hybrid design considerations. Some design rules to reduce ESD sensitivity for parts and hybrids are as follows:

(a) MOS protection circuitry improvement techniques are: increasing diode size; using diodes of both polarities; adding series resistors; and utilizing a distributed network effect;
(b) Avoid cross-unders beneath metal leads connected to external pins; otherwise treat the part as electrostatic sensitive. Also, since cross-unders are diffused during the N+ (emitter) diffusion process, the oxide over the diffusion will be thinner, causing this area to have a lower dielectric breakdown. If a deep N diffusion step is used in the fabrication process, deep N diffusions, rather than N+ diffusions, should be used for cross-unders;
(c) MOS protection circuits should be examined to see if the layout permits the protection diodes to be defective or blown without causing the circuit to be inoperative;
(d) Distance between any contact edge and the junction should be 70 microns or greater on bipolar parts;
(e) Linear IC capacitors should be paralleled by a p-n junction with sufficiently low breakdown voltage;
(f) For bipolar parts avoid designs permitting a high transient energy density to exist in a p-n junction depletion region during ESD events. Use series resistance to limit ESD current or use parallel elements to divert current from critical elements. The addition of clamp diodes between a vulnerable lead and one or more power supply leads can improve ESD resistance by keeping critical junctions out of reverse breakdown. If a junction cannot be kept out of reverse breakdown, physically enlarging the junction will make it more ESD resistant by reducing the initial transient energy density in inverse proportion to its area;
(g) The protection of a transistor from ESD can be improved by increasing the emitter perimeter adjacent to the base contact. This lowers transient energy density in the critical emitter sidewall. Enlarging the emitter diffusion area also helps in some pulse configurations;

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(h) As an alternative to using clamping diodes, which consume chip area and can cause unwanted parasitic effects, a "phantom emitter" transistor can be used to improve ESD resistance. The phantom transistor incorporates a second emitter diffusion shorted to the base contact. This creates a deliberate separation of the base contact from the normal emitter without interfering with normal transistor operation. The second emitter provides a lower break-down path BV_{CEO} between the buried collector and the base contact;

(i) Avoid pin layouts which put the critical ESD paths on corner pins which are prone to ESD;

(j) Avoid metallization cross-overs where possible. These cross-over areas are typically separated by thin dielectric layers. Cross-overs often impose a number of metallurgical requirements which are frequently incompatible. For example, once the first metallization layer (Al) is deposited, the circuit cannot be subsequently heated in excess of 550°C because the eutectic point of the Al-Si system is 575°C. Thus, the dielectric layer (SiO_2) should be deposited by a low temperature process such as pyrolytic deposition. This layer is prone to breakdown from ESD for two reasons:

(1) A low temperature growth of SiO_2 generally is not uniform in thickness and not free from pin holes;
(2) The dielectric layer is thin and thus the breakdown voltage is very low;

(k) Avoid parasitic MOS capacitors whenever possible. Microcircuits with metallization crossing over low resistance active regions, that is, V_{CC} over N+ guard rings are moderately sensitive to ESD. Such constructions include microcircuits with metallization paths over N+ guard rings. N+ guard rings are used in the N-type epitaxial islands to inhibit possible inversion of the N-type semiconductor to a P-type semiconductor, and to reduce the leakage current. Since the final oxide layer over the N+ guard ring is relatively thin, parasitic MOS capacitors of relatively low breakdown voltage are created when a metallization path passes over this ring. These MOS capacitor structures are ESDS as indicated in appendix B of MIL-STD-1686;

(l) Caution is advised in the use of microcircuits and hybrids containing dielectrically isolated bipolar parts which are generally moderately sensitive to ESD. Failure occurs due to breakdown of the thin dielectric layers between these small geometry bipolar parts from an ESD;

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(m) The input protection network should be near the bond pad. In other words, bussing the electrostatic pulse around the chip should be avoided;
(n) Avoid metal to diffusion contacts. A short polysilicon strap of adequate width should be used to connect the aluminum to the diffused resistor;
(o) During the design of an electrostatic protection network consideration must be given to the entire path of the pulse.

30.4.2 Assembly design considerations. Procedures are as follows:

(a) Latchup in CMOS, with the exception of analog switches, can be avoided by limiting output current. One solution is to isolate each output from its cable line with a resistor, and clamp the lines to V_{DD} and V_{SS} with two high speed switching diodes. The use of long input cables poses the possibility of noise pickup. In such cases filter networks should be used;
(b) Additional protection can be obtained for on-chip protected or unprotected MOS by adding external series resistors to each input;
(c) Where practicable, an RC network consisting of a relatively large value resistor and a capacitor of at least 100 pF should be used for sensitive inputs on bipolar parts to reduce effects from ESD. However, if circuit performance dictates, two parallel diodes clamping to a half volt in either polarity can be used to shunt the input to ground. This reduces disturbances to the input characteristics;
(d) Leads of class 1 parts mounted on PWBs should not be connected directly to connector terminals without ESD protection. Assembly designs containing ESDS items should be reviewed for incorporation of protective circuitry;
(e) Systems incorporating keyboards, control panels, manual controls, or key locks should be designed to dissipate personnel static charges directly to chassis ground, bypassing ESDS parts.

30.4.3 Product design recommendations for ESD hardening. Different design recommendations apply for each failure mechanism.

(a) Direct Contact. Reduce the probability of direct contact by careful product design. Internal sensitive devices should be buffered with "robust" devices, high voltage clamping circuits, and/or filters before routing their signals to external parts or connectors. Where sensitive leads at connectors must be available to the outside world, they should be recessed and difficult or impractical to contact manually.

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(b) Indirect Contact. An effective method is to provide for sufficient insulation or physical spacing between the outside world and any internal conductive parts or circuit traces which could lead directly, or indirectly, to an ESDS device. Insulation methods include installation of non-conductive films or tapes, sealing enclosure cracks or screw holes, and providing conductive guard traces or shields to divert the discharge energy from sensitive devices.

(c) Conducted or Radiated Noise. Careful choice of logic thresholds, shielding, low impedance circuitry, good ground system design, and meticulous circuit layout are some of the ways to minimize conducted or radiated noise problems. A conductive metallic barrier will tend to shield the circuits from radiated noise, especially if it completely encloses the circuits. But conductive coupling may occur due to secondary arcs from the shield to the circuits. To prevent this, the shield itself must be separated from the circuits. An insulating enclosure will not prevent radiated ESD noise from coupling to the circuits. Some enclosure designs utilize an insulating enclosure and within this, a metallic shield.

Compromising the integrity of most enclosures, for example, are holes, outlets for air and conductive items penetrating the barrier, such as screws, which allow ESD noise to pass through or around the barrier. These should be located well away from circuits. The noise through a hole is minimized by using several small holes instead of a single large one. Another approach is to make the depth of the hole at least five times its diameter, which greatly attenuates radiated ESD noise.

PCB design plays an important role in developing system immunity to ESD. The traces on a PCB are antennas for ESD-generated fields. Those connected to high impedance devices are antennas for electric fields, while those in low-impedance circuit loops are antennas for magnetic fields. To minimize the coupling to these antennas, line lengths must be kept as short as possible and loop areas must be kept as small as possible. Lines longer than a few centimeters and loop areas larger than a few centimeters square can receive significant ESD noise.

As the largest antennas within most systems, cables are particularly prone to having large voltages and/or currents induced in them by radiated ESD noise. But, cables can indirectly help prevent conductive coupling by providing a low-impedance path along which the charge may leave the system. The cable shield, the largest-diameter conductor in the cable, should be used as the ground path and be directly connected to a metal chassis.

Cables should be kept as short as possible, and each circuit line in the cable should be located physically close to its return line. In a ribbon

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cable, for example, every signal line should have a ground line located next to it. The actions taken to reduce loop areas also minimize common-mode coupling.

Cable design sometimes utilizes the filtering concepts used in circuit design. Some cable connectors have built-in shunt capacitors or clamping suppressors, and others incorporate series ferrite inductive leads.

Often overlooked, firmware and software ESD solutions are powerful methods for reducing the severity of transient upsets such as system lockup.

(d) Induced Charge. A shield is recommended around the sensitive devices and their input leads to minimize induced charge effects of electrostatic fields. Low impedance circuitry and other noise reduction methods are also often effective for induced charges.

30.4.4 ESDS part protection networks. Manufacturers have incorporated protection circuitry on most MOS devices (see figure 6). The purpose of these protection networks is to reduce the voltage across the gate oxide below the dielectric breakdown voltage without interfering with part electrical performance. Differences in fabrication processes, design philosophies and circuitry have resulted in different gate protection networks.

30.4.5 Transient suppressors. Some transient suppressors, depending on the pulse width and shape, could reduce the voltage and energy flowing into an electrical circuit to levels sufficiently low to avoid damage to parts at the assembly levels.

Two types of transient suppressors are commercially available. One is the metal oxide varistor; the other is a silicon p-n junction avalanche diode. Both rely on a nonlinear relationship between voltage and current such that at low voltages the current is extremely small, while at voltages above some "clamping" voltage the current increases rapidly. Both depend on the large voltage drop through the source impedance to reduce the voltage peak across the terminals of the device. The clamping voltage depends on the doping density in the p-n junction, and on the thickness (the number of grain boundaries) in the varistor. The junction area or volume (varistor) determine how much energy the suppressor can safely absorb during the transient. A highly desirable characteristic of these devices is the ability to respond in less than a nanosecond, as contrasted with the much slower response of air gaps and gas tube arrestors.

Suppressors include tin, zinc or bismuth oxide voltage-dependent resistors (VDRs), often referred to as metal oxide varistors, silicon voltage limiters, R-C networks and selenium stacks. Prior to making an ultimate judgment on any given type of suppressor, a final analysis should consider voltage levels to

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be encountered, response time of the suppressor, peak current, leakage current, energy absorption, operating temperature range, life, size, cost, and the voltage protection level desired.

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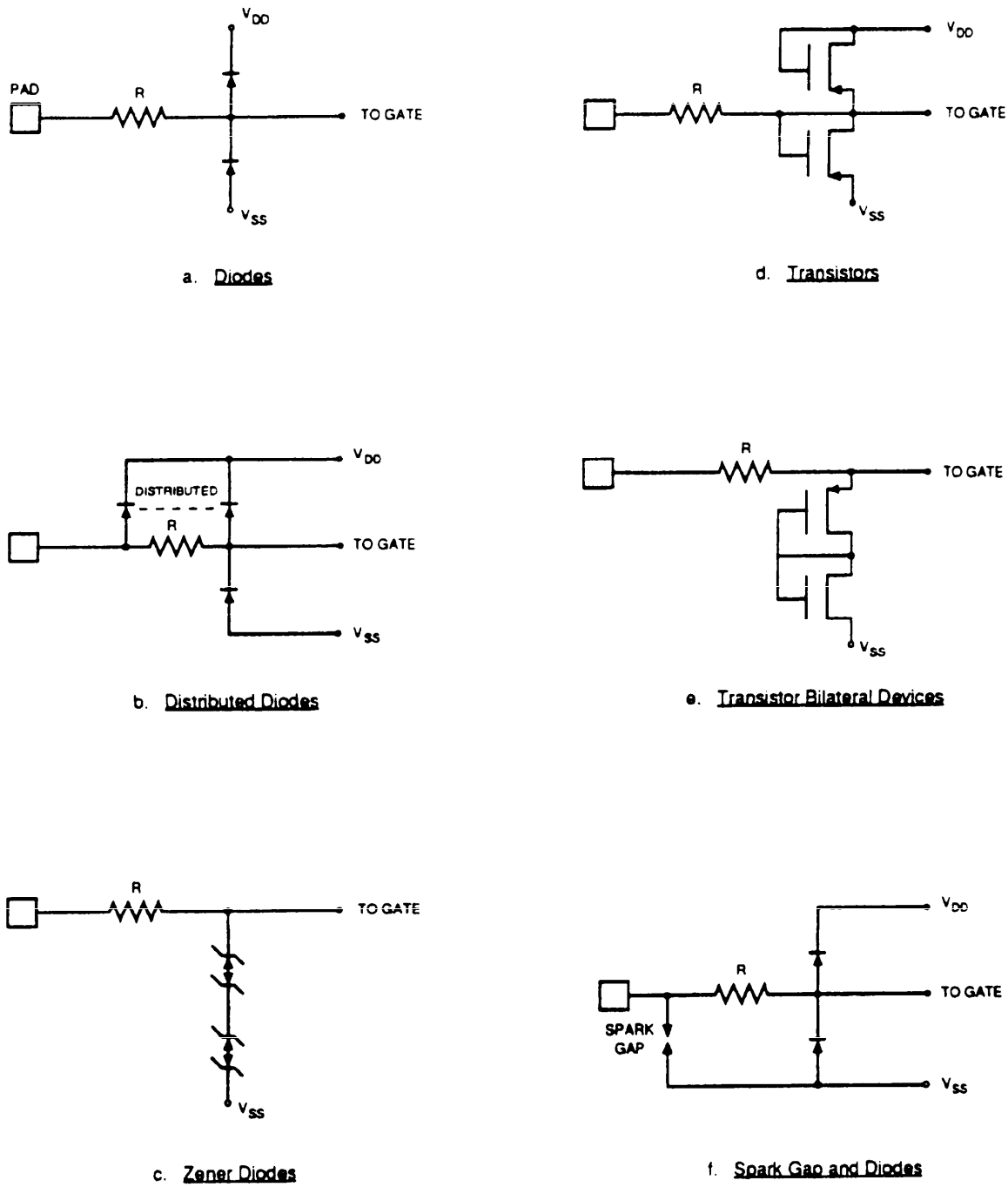

FIGURE 6. Gate protection networks.

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30.5 Experimental studies. Results of some experimental studies on ESD protection networks are as follows:

(a) The most effective circuits for input protection for NMOS contains either a field oxide device or a diffusion diode/resistor. The field oxide device was found superior due to enhanced parasitic bipolar operation. An ideal diffusion diode/resistor was determined to be a large diffused diode to improve the power to area ratio and provide maximum heat dissipation followed by a long straight resistor.

(b) The ESD mean failure voltage of NMOS output buffers is a critical function of the buffer layout. Failure voltage exhibits an approximately exponential variation with source/drain window to gate spacing at small spacings and saturates above a critical spacing value. The number and distribution of source/drain contact windows are also important. Failure voltage generally increases with physical size of output transistors.

(c) Recently a new novel ESD protection device, Double Implant Field Inversion Device in Well (DIFIDW), with deep junctions and uniformly thick gate oxide designed for scaled CMOS VLSI high pin count chips has been developed.

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APPENDIX F

PROTECTED AREAS

10. SCOPE

10.1 Scope. This appendix provides information on the concept, requirements, and operation of ESD protected areas. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

20.1 Government documents.

20.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

MILITARY

MIL-W-87893 - Workstation, Electrostatic Discharge (ESD) Control.

STANDARDS

MILITARY

MIL-STD-454 - Standard General Requirements for Electronic equipment.

HANDBOOKS

MILITARY

MIL-HDBK-419 - Grounding, Bonding, and Shielding for Electronic Equipments and Facilities Basic Theory.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Bldg. 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

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20.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

NATIONAL FIRE PROTECTION ASSOCIATION (NFPA)
70 - National Electrical Code.

(Application for copies should be addressed to the National Fire Protection Association, One Batterymarch Park, P.O. Box 9101, Quincy, MA 02269-9101.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

30. INTRODUCTION

30.1 Introduction. An ESD protected area consists of the tools, materials and equipment required to control or minimize static voltage levels. Complementing the requirement for protected areas are the associated handling procedures to be used in the protected area. The protected area can be a permanent designated area in a manufacturing, maintenance, or rework facility or a temporary area located immediately adjacent to equipment regardless of its physical location.

30.1.1 General concepts. The ESD protected area concept requires careful consideration of two elements. The first of these is to maintain personnel (electrical) safety at all times. This element is directly related to the types of materials (conductive or dissipative) selected for use in the protected area and the exact grounding procedures selected for use. The second element is related to the primary purpose of the protected area - the requirement to provide a technically adequate level of protection for ESDS items handled in the protected area. The objective of the protected area is to maintain the lowest possible electrostatic field intensity and voltages in the protected area.

The sophistication of the design of a protected area is directly related to the work processes performed, its location, and the environmental or physical limitations. For example, during field maintenance a protected area could consist of a temporary area free from static generating materials and equipped with a personnel wrist ground strap, portable protective work mat, and appropriate protective covering or packaging materials. A protective area in a manufacturing facility could include humidity controls, a comprehensive ESD

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protective work bench constructed of protective materials and grounded appropriately, utilization of local or room air ionization, and conductive flooring with the associated heel grounders or conductive footwear.

The design of the protected area is directly impacted by the susceptibility of the item and the complexity of the handling procedures used in the protected area. As the protected area becomes more comprehensive, the handling procedures used in the protected area become less complex. Less comprehensive protected areas require handling procedures of increased complexity to ensure the desired levels of protection are provided. The relationship between the level of protection provided by the protected area and the protection provided by the handling procedures themselves entails a constant tradeoff between these two elements. Protected areas, may for simplicity, be designed to provide an equal level of protection for all ESDS items throughout a facility. This standardized approach requires that the level of protection selected be adequate to protect all items handled in a given facility. Alternatively, protected areas may be designed throughout a facility to provide the level of protection required only for those ESDS items handled at specific work locations. The first approach, that of standardized protective areas and handling procedures for a given facility may be the most desirable from the viewpoint of personnel training, program implementation and surveillance, and cost effectivity.

ESD protective materials and equipment are discussed in appendix I. The design and selection of materials for use in a protected area is at the option of the organization implementing an ESD control program. The information provided in this appendix and appendix I does not mandate or preclude the use of any specific materials or techniques. The materials or techniques selected should be technically adequate and cost effective.

30.1.2 Elements of a protected area. The protected area is the focal point for effective ESD controls. It should be noted that the protected area concept is intended for use only when ESDS parts, assemblies, and equipment are handled outside of their protective covering or packaging. ESDS material that is properly protected by technically adequate protective covering or packaging requires no unique handling or storage procedures as long as the protective covering or packaging integrity is maintained. Protected area concepts consist of various complementary elements which include:

(a) Grounding considerations
(b) Safety and grounding requirements
(c) Tools, materials and equipment
(d) Operating procedures

Each of these elements is discussed below.

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40. GROUNDING CONSIDERATIONS

40.1 General. ESD protective materials and equipment that are to be grounded should be attached to the earth electrode subsystem of the facility (see MIL-HDBK-419) or attached to a ground constructed and tested in accordance with NFPA 70. Grounding on military platforms such as shipboard, aircraft or other vehicles shall be in accordance with the applicable military requirements, standards, or specifications.

50. SAFETY AND GROUNDING REQUIREMENTS

50.1 Personnel safety. Of prime importance are personnel safety requirements. The safety requirements of MIL-STD-454, Requirement 1 should be considered in the construction of ESD protected areas to reduce the chance of electrical shock to personnel. Maximum current levels in ESD protected areas should be limited to the perception level as shown in MIL-STD-454, requirement 1.

50.2 Ground potential of electrical equipment and power tools. The design and construction of the ESD protected area and ESD grounded work benches should ensure that all external parts, surfaces, and shields in electronic test equipment and power tools are at a common ground potential at all times during normal operation. The design should include consideration of potential ground faults and hazardous voltage levels which may exist in the protected area. Tools and test equipment on grounded work benches with metal or other conductive coverings can shunt the protective resistance in the work bench ground cable if allowed to contact the work surface. As an added precaution for personnel safety ground fault circuit interrupters (GFCI) can be used with electrical equipment. The GFCI senses leakage current from faulty equipment and interrupts the circuit almost instantaneously when these currents reach a potentially hazardous level. CAUTION MUST BE OBSERVED IN EMPLOYING PARALLEL PATHS TO GROUND THAT COULD REDUCE EQUIVALENT RESISTANCE OF PERSONS TO GROUND TO UNSAFE LEVELS. Personnel movements in conjunction with wrist straps, table tops and floor mats could result in such parallel paths.

50.3 Ground potential of protected areas. Grounded work bench surfaces constructed of metallic materials such as stainless steel require careful design and evaluation in the context of personnel electrical safety.

50.4 Alternative grounding procedures. There are many alternative grounding techniques that may be suitable for use in providing ESD protection. Selected grounding techniques must provide personnel safety at all times and be in accordance with the National Electrical Code and all other applicable requirements.

50.5 Grounding tradeoffs. The exact grounding methods selected for use in a given facility involve a series of technical tradeoffs predicated upon the

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exact materials selected for use and their relationship to the organizations' ESD handling procedures. The methodology and techniques selected must not compromise personnel safety. The use, or non-use of current limiting resistors in grounding circuitry is intimately related to the material selected for ESD protective work surfaces (which can range from metallic conductors such as stainless steel to dissipative material with surface resistivities of up to 10^{12} ohms per square). Other factors which are unique to each organization and facility, include the exact type of work performed in each protected area, that is, electrical test, mechanical assembly, and so forth, and the potential voltage sources that may be present in the protected area. The use, or non-use of devices such as GFCIs also requires careful consideration. Each of these elements preclude the design of a protected area which would be universally acceptable to all users.

60. TOOLS, MATERIALS AND EQUIPMENT

60.1 General. The tools, materials and equipment selected for use in a protected area can range from the minimum such as ESD protective work bench surfaces and personnel wrist straps, to more complex configurations that include air ionization, protective flooring, and continuous monitoring of wrist strap integrity and static voltage generation. The items selected are at the option of the protected area designer, however, care should be exercised during the design, construction and use of the protected area to exclude prime charge sources (see Appendix A, Table III). Figure 7 illustrates an ESD work bench. In addition, the protected area should be identified by precautionary signs; for example, ESD PROTECTED AREA. Figure 8 is an example of an ESD protected area sign and figure 9 is a typical certification/reinspection label. Information on ESD protective materials and equipment is contained in Appendix I.

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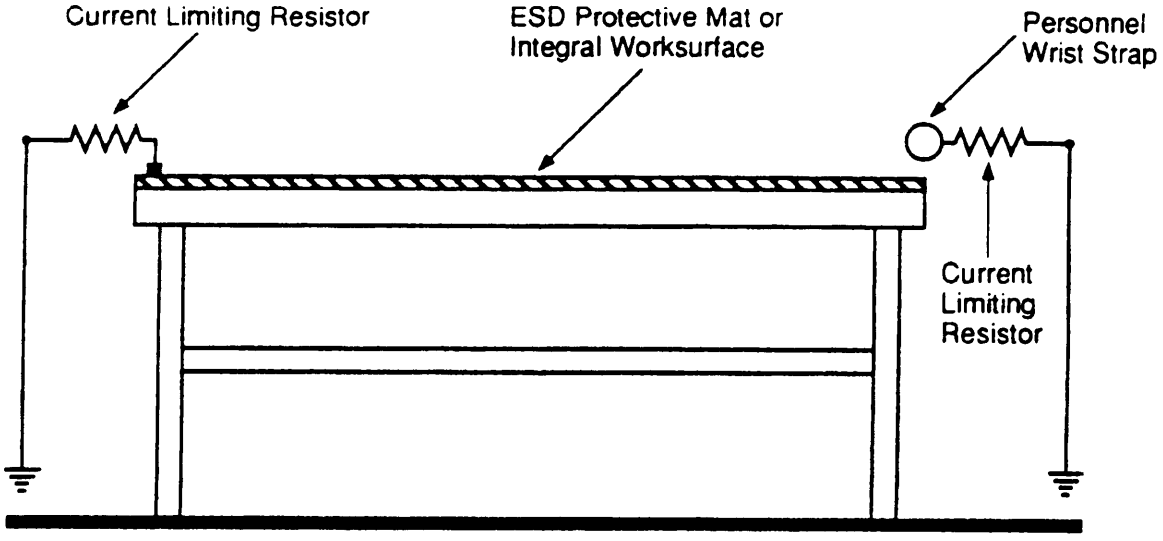

Note: ESD protective mat current limiting resistor optional

FIGURE 7. ESD protective work bench.

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CAUTION

ESD PROTECTED AREA

**USE ELECTROSTATIC
DISCHARGE PROTECTIVE
HANDLING PROCEDURES**

FIGURE 8. ESD protected area caution sign.

Certification Date: _____

By: _____

Reinspection due: _____

FIGURE 9. ESD protected area certification/reinspection label.

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60.2 Military specifications. MIL-W-87893(30) has been prepared by the Department of the Air Force principally for Air Force use. This specification covers specific resistance values, static decay values, and general construction requirements for static control workstations and their components.

70. OPERATING PROCEDURES

70.1 General. Access to ESD protected areas should be limited to personnel who are properly trained (see appendix J). General guidelines and sample operating procedures for use during handling of ESDS items may be found in appendix H.

80. CERTIFICATION/VERIFICATION AND MONITORING OF PROTECTED AREAS

80.1 Certification/verification and monitoring. Certification and monitoring should be performed at the time of installation for permanent protected areas and periodically thereafter. Certification takes place to ensure the protective area is installed as designed. Verification or periodic monitoring ensures the continuous integrity of the protective area.

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APPENDIX G

STATIC ELECTRICITY IN AN INTEGRATED CIRCUIT FABRICATION CLEAN ROOM

10. SCOPE

10.1 Scope. This appendix provides information on the problems of static electricity in an integrated circuit fabrication clean room. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. INTRODUCTION

30.1 General. In an effort to reduce particle related "random" defects, integrated circuit wafer fabrication is now performed in clean rooms, typically class 100 (that is, a maximum of 100 particles per cubic foot) or lower. These clean rooms include: filtered air pumped in to provide laminar flow across all work stations, the extensive use of synthetic materials such as polypropylene and nylon, and the requirement that all workers be covered head to toe in synthetic, lint-free smocks. All of these characteristics reduce the risk of particulate contamination, but greatly magnify the risk of the generation of static electricity.

30.2 Fabrication process considerations. Many steps in the wafer fabrication process require the use of harsh chemicals such as hydrochloric or hydrofluoric acid. The prevalence of these corrosive agents has discouraged the use of metals on the wafer fabrication line. Thus, the environment encountered by a wafer in process is composed almost completely of static-generating materials. Further, the requirements for low particle generation also dictate that all surfaces be as smooth as possible and cleaned frequently. Again, this is the worst possible situation for prevention of static generation. Generally, the finer the finish on two materials lying against each other the greater the electrostatic charge generated upon separation. In environments which require less-stringent cleanliness, often-handled implements and containers build up a layer of conductive oil from the skin of the workers. This works to suppress static generation. Solder suckers used in electronic board repair are a good example of this effect: while a new one might generate up to 50,000 volts of static electricity when used, a well-used implement will generate less than 1,000 volts. Unfortunately, wafer fabrication areas also prevent this static-limiting effect by frequent cleaning of all work surfaces and implements. Guidelines which minimize operator contact with anything that

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will contact a wafer also limit this effect. Operator contact is minimized by the use of plastic gloves and tweezers or other detachable handles.

30.3 Humidity considerations. One of the traditional simple cures for static problems is to control the relative humidity of an area to 40 percent relative humidity or greater. When the relative humidity is high, a thin conductive layer of water will be absorbed on the surface of most plastics (hygroscopic). This again helps to prevent static generation. Unfortunately, this too is prohibited in most wafer processing facilities. Some photoresists are very sensitive to moisture, in that the same thin layer of water which prevents static buildup also affects the adhesion of the photoresist. Thus, areas producing fine-geometry devices generally require a low relative humidity. Additionally, many of the processes in the production of a semiconductor wafer require high-temperature bakes. This tends to dry wafer and carrier surfaces even further. Also, any high-velocity fluid such as deionized water or air (in the case of vacuum pickup) can cause a charge buildup.

Thus, one can easily see that semiconductor fabrication lines have all the conditions necessary for high electrostatic voltage generation. Consider for example, an employee in a nylon coat shuffling across a clean floor in his plastic-soled booties: this employee can easily generate 7,000 to 8,000 volts of static electricity on his body. A fiberglass wafer carrier sliding across a polypropylene tabletop can easily generate 10,000 volts of static. An electrostatic survey of several wafer fabrication lines has revealed the following electrostatic potentials found on several common articles;

Wafers	5 kv
Wafer Carriers	35 kv
Plexiglass Covers Over Air Bearing Tract	8 kv
Tabletop	10 kv
Storage Cabinet	30 kv
Smocks	10 kv
Quartz Ware	1.5 kv

The areas found to contain the highest electrostatic voltages are typically those associated with areas which involved high temperature operations. The high temperatures apparently baked out the moisture layer on these surfaces, thus making them extremely static-generative. Wafer carriers which hold wafers during a dehydration bake are the best example of this effect.

Among the most dangerous areas usually encountered are those associated with visual inspections and electrical parameter recordings. These areas combine the worst-case conditions of individual wafer handling, high static charges, and ungrounded conductors in static fields which are brought into close contact with the wafer.

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40. ESD SUSCEPTIBILITY OF WAFERS

40.1 General. From the preceding discussion one can clearly see that semiconductor wafers are subjected to electrostatic charge throughout the fabrication process. Now consider what effect this charge will have on the wafer. A finished semiconductor, whether bipolar or MOS, is composed of various layers of conductors separated by layers of dielectrics. Generally, the process begins with a substrate of silicon and progresses with dielectric layers of silicon dioxide (SiO_2) and conductive layers of aluminum and/or polysilicon. Silicon dioxide has a breakdown voltage of about ten MV/cm or less depending on the characteristics of the layer. If a 10,000 Å thick layer of SiO_2 were used as a dielectric between conducting layers, a potential of only 1,000 volts would be sufficient to destroy this dielectric. MOS devices or erasable PROMs employing thin oxides of 200 Å to 1,000 Å can expect potentials as low as 30 volts to be destructive.

40.2 Worker induced problems. Consider also the effect the current induced by this electrostatic field may have on a conductive layer in the semiconductor. As was previously noted, a clean-room worker may easily develop 7,000 volts. If he now picks up his metal tweezers and grasps a wafer, the charge on his body will be conducted by the sweat layer of his skin through a low resistance path to the tweezers to the first conductor encountered on the wafer.

Packaged semiconductors have been known to be static-sensitive for some time. To prevent damage due to ESD, chip designers generally add input protection to the bond pads on the chip. These input protection networks provide a safe short to the substrate (generally ground) so that the chip will not be damaged by either the high voltage or high currents associated with the discharge. This technique has proven highly successful for limiting the susceptibility of packaged semiconductors to ESD. However, input protection networks provide very little protection for wafers since the ESD source can discharge directly through highly susceptible internal nodes of the die, thus bypassing the protection circuitry.

Contributing to the difficulty in identifying the magnitude of the wafer ESD problem is the fact that a certain number of non-functional die are expected and accepted without failure analysis being performed to verify the cause of failure. Additionally, normal good practice in handling wafers is to touch them when necessary on the periphery of the chip, thus limiting the chance of contamination or degradation (from an ESD) on internal devices. Since many of the devices on the outer edge of the chip are expected to be losses due to geometric considerations, it is an inherently difficult task to quantify the ESD problem in wafer yields.

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50. IMPLICATIONS OF THE PRESENCE OF STATIC CHARGES

50.1 General. In addition to the increased susceptibility to catastrophic failure of die in wafer form, there are also many secondary effects of the presence of static charges and particulate contamination. A discussion of these effects follows.

50.2 Particulate contamination. Particles can be filtered out of the air quite effectively; however, this does not eliminate them from the environment of the semiconductor wafer. Particles are also generated at nearly every stage of fabrication. People are probably the biggest source: lint from clothing, hair or dead skin flakes. Broken wafers are another source. Anytime one surface is scraped against another, some particles may be generated. Quartz wafer boats sliding into quartz tubes, wafers transferred from one carrier to another or plastic boxes opening or closing all may produce particles. Even the air filters themselves may shed fibers.

50.2.1 Charging of particles. Particles cannot be totally eliminated from the wafer fabrication process. There is, however, one particle-related effect which is often ignored. Most airborne particles are electrostatically charged. This charge may be generated when the particle is originally scraped off its parent material, or it may pick up a charge as it is blown across a surface.

Since the particle is mobile while floating in the air and highly charged, it will now react to any electrostatic field it finds itself in. Any statically charged surface can provide this field. The higher the electrostatic voltage the stronger the field. Charged particles will be repelled by a similarly charged surface but attracted by an oppositely charged surface. If either the particle or the surface is an insulator, the particle will not be neutralized upon collision and will thus adhere to the surface.

Either a wafer or a mask may act as such a charged surface. Since most particles found in semiconductor fabrication areas are nonconductors and large areas of a semiconductor's surface are covered by an oxide during most of the fabrication steps, particles attracted by the electrostatic field of a charged wafer or mask tend to become attached. This electrostatic force of attraction is considerable compared to force which may be applied to these tiny particles by a stream of compressed air or nitrogen. Even deionized water may not remove some of these particles. Normal tap water would be conductive enough to neutralize the static charge, however, deionized water is effectively an insulator.

60. FABRICATION PROCESSES AFFECTED BY STATIC CHARGES

60.1 Photolithography. The photolithography process used to produce semiconductors is inherently particle-sensitive. A particle on either the wafer

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or the mask during the exposure step on any level can cause a defect in the pattern. Depending on the size and location of the particle, this can cause either an initially defective die or a reliability failure later in the life of the part. As device geometries shrink, the size of particles which must be controlled also decreases. Additionally, consider the effect of 30 particles on the surface of a wafer which has 600 die per wafer, compared to the effect of these same 30 particles on a wafer which has only 300 larger die per wafer. If all 30 particles caused a defective die, the yield loss on the 600 die wafer would be only 5 percent, while that on the 300 die wafer would be 10 percent. Thus, the larger the die size, the greater the effect of particles.

60.2 Epitaxial growth. Electrostatically induced particles on the surface of the wafer can also have adverse effects during the epitaxial growth process. The effects can be a deviation in the rate of formation of steps, the formation of imperfect nuclei, and dislocations in the crystal structure. It will be more pronounced for a given size of contaminant as device geometries shrink further.

60.3 Oxide formation. Statically charged particles can also cause severe problems in gate oxidation steps in MOS and EPROM devices. Current technology is producing gate oxides of only a few hundred angstroms. Any charge on or near a wafer will attract and attach unwanted particles and it is obvious these particles can have detrimental effects on both device yield and long-term reliability. Since 50 Å particles are sufficient to cause gate oxide defects, the filtering of these particles is essential. Unfortunately, particles this small can pass through most filters and are below the detection threshold of most particle detectors. Therefore, even Class 10 clean rooms may contain a high density of 50 to 100 Å particles. Oxide is an amorphous form of glass consisting of a random network of silicon and oxygen atoms. Any particulate contaminant can disrupt this random structure such that crystalline regions will form. This crystalline structure is inherently more dense than the amorphous glass and the interface boundaries between them can be porous to impurities during subsequent processing steps. It also should be noted that devices with flawed gate oxides from particulate contaminates are more susceptible to failure from electrical transients.

There are certain fabrication processes at which the devices are susceptible to catastrophic damage from an ESD. Consider the following: in MOS wafer fabrication there is a step in which a thin layer of oxide is grown on the entire wafer surface on top of which is a layer of polysilicon which is later defined by photolithography and etched. Before the polysilicon is etched, it is in actuality forming a large capacitor between itself and the silicon substrate. At this stage, the oxide is very susceptible to ESD due to its large contact area. However, once the polysilicon is defined to form the gate, source and drain, the capacitance is much reduced along with the possibility of damage.

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APPENDIX H

GENERAL GUIDELINES AND SAMPLE OPERATING PROCEDURES FOR HANDLING ESDS PARTS, ASSEMBLIES AND EQUIPMENT

10. SCOPE

10.1 Scope. This appendix presents general guidelines and sample operating procedures for handling electrostatic discharge sensitive (ESDS) items. These guidelines are representative information only and require tailoring, by the addition and deletion of various elements, for the implementation of effective ESD controls in any given organization or facility. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. GENERAL GUIDELINES

30.1 Protective handling of ESDS items. Proper handling of ESDS items will significantly decrease the probability of ESD damage. The following general guidelines are applicable to the handling of ESDS items:

(a) Handling of ESDS items without ESD protective covering or packaging should be performed in ESD protected areas;
(b) Personnel handling ESDS items should be trained in ESD precautionary procedures, tested for competency and certified. Untrained personnel should not be allowed to handle ESDS items when the items are outside of the ESD protective covering or packaging;
(c) When not actively working with ESDS items, they should be protected by shunts such as bars, clips, or non-corrosive conductive foam or protective covering or packaging;
(d) Where personnel grounding straps cannot be used, personnel should ground themselves momentarily prior to removing ESDS items from their protective covering or packaging. When being handled out of their protective covering or packaging, ESDS items should be handled without touching ESDS parts or electrical runs;
(e) Test equipment probes should be momentarily grounded prior to contacting ESDS items;
(f) Electrically powered tools, test equipment and fixtures used in ESD protected areas should be properly grounded. Grounding of electrical test equipment should be via a grounded plug, not through the surface of the ESD protective work station;
(g) Power should not be applied to equipment while ESDS items are being removed or inserted. An exception to this is when equipment is

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specifically designed for assembly removal/replacement with the power on;

(h) Assure that all containers used in ESD protected areas are grounded before and during use, either directly or by contact with a properly grounded protective surface;

(i) Work instructions, test procedures, drawings and similar documents used in ESD protected areas should not be covered with or placed in common plastic sheeting or containers;

(j) Drawings for ESDS items should be marked with sensitive electronic device symbols, cautions, and reference handling procedures as applicable;

(k) Manufacturing, processing, assembly and inspection work instructions should identify ESDS items and require that such items be handled only by trained personnel and only in ESD protected areas when outside of their ESD protective covering or packaging;

(l) Personnel handling ESDS items should avoid physical activities which are static producing in the vicinity of ESDS items. Such activities include wiping feet and removing or putting on smocks;

(m) Personnel handling ESDS items should wear ESD protective clothing when appropriate. Such clothing should be periodically-monitored for proper performance. Common synthetic clothing should be regarded as a potential static hazard and handling precautions should be developed to prevent its contact with ESDS items. Gloves and finger cots, if used, should be made of ESD protective material;

(n) Neutralize charges on ESD protective covering or packaging by placing the covered or packaged item on an ESD protective surface prior to opening. Alternately, charges can be removed by grounded personnel touching the package;

(o) When testing ESDS items in test chambers precautionary techniques may be required to minimize the generation of electrostatic charges.

(p) When ESDS items are manually cleaned with brushes, only brushes with natural bristles should be used and ionized air should be directed over the cleaning area to dissipate any static charges. All automatic cleaning equipment should be grounded if practicable and leads and connectors of ESDS items should be shorted together during the cleaning operation. Conductive cleaning solvents should be used where practicable when cleaning ESDS items;

(q) Caution should be observed in using solvents such as acetone and alcohol or other cleaning agents for cleaning ESD protective materials. The use of such solvents can reduce the effectiveness of some ESD protective materials, especially those employing detergent type antistats which bleed to the surface to form a sweat layer with moisture in the air;

(r) Procedures for handling ESDS items should be developed and implemented. The detail of the procedures should be related to the sensitivity of the items being handled and the degree of control afforded by the protected areas.

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40. SAMPLE OPERATING PROCEDURES

40.1 Organizational elements affected by ESD controls. An effective ESD control program requires the coordination and integration of various organizational elements or functions within a facility and a system of checks and balances. Organizational elements affected generally include:

(a) Acquisition
(b) Design engineering
(c) Reliability engineering
(d) Quality assurance
(e) Manufacturing
(f) Test and maintenance
(g) Packaging and shipping

40.1.1 Functions. From a functional standpoint ESD operating procedures apply to:

(a) Design and drafting
(b) Inspection
(c) Test
(d) Manufacturing and processing
(e) Assembly
(f) Maintenance, repair and rework
(g) Packaging and marking
(h) Installation
(i) Transportation
(j) Failure analysis

50. OPERATING PROCEDURES

50.1 Sample operating procedures.

50.1.1 Acquisition. Procedures are as follows:

(a) Incorporate ESD control program requirements on all acquisitions related to design and handling of ESDS items;
(b) Work with quality assurance to ensure subcontractors and suppliers comply with ESD control program requirements;
(c) Maintain listing of supply sources of ESD protective equipment and materials.

50.1.2 Design engineering. Procedures are as follows:

(a) Identify all items recommended for use in the design that are ESDS and their susceptibility levels;

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(b) Select parts that offer the greatest immunity from ESD consistent with meeting performance requirements. For example, if MOS devices are used, select those which include maximum internal protection;
(c) Design protective circuitry into assemblies and equipment. Implement protective circuitry at the lowest practical level of assembly;
(d) Perform circuit analysis to determine whether assemblies containing ESDS parts are adequately protected;
(e) Ensure part and assembly drawings and other related engineering documentation include ESDS item identification;
(f) Ensure equipment and cabinet level drawings contain:

(1) The EIA RS-471 sensitive electronic device symbol if ESDS items are contained therein;
(2) Directions for labeling equipment cabinets containing ESDS items with the EIA RS-471 symbol and the following caution:

"CAUTION -- CONTAINS PARTS AND ASSEMBLIES
SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC
DISCHARGE (ESD)."

(g) Assist in failure analysis and implementation of corrective action;
(h) Present design considerations and conformance to ESD requirements at all design reviews.

50.1.3 Reliability. Procedures are as follows:

(a) Review parts list to identify ESDS items, determine ESDS sensitivity levels, maintain ESDS parts susceptibility data for use by design engineering;
(b) Perform ESD testing;
(c) Work with design to detect and classify possible ESD related failures or degraded performance;
(d) Analyze production and field information to detect possible ESD related failures or degraded performance;
(e) Be alert to part performance degradation due to ESD related latent failures;
(f) Ensure ESD design requirements are adequately implemented in the hardware design;
(g) Ensure failure analysis properly considers ESD failure modes.

50.1.4 Quality assurance. Procedures are as follows:

50.1.4.1 Quality control.

(a) Determine the requirements for the establishment of protected areas and grounded work benches. Certify protected areas and grounded

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work benches prior to their use and periodically thereafter. Document certification test procedures and data;

(b) Ensure the use of protective personnel clothing (when appropriate) and proper personnel grounding at all necessary points where ESDS items are handled outside their protective covering or packaging;

(c) Establish and conduct training programs to ensure all personnel handling ESDS items have received the necessary training and certification;

(d) Perform periodic audits to ensure the integrity of the ESD protected areas and ESD grounded work benches, personnel grounding facilities, grounding of tools and test equipment and the implementation of the handling, packaging and labeling procedures. Audits should be performed to assure that the ESD materials and equipment are maintaining their effectiveness;

(e) Verify that all technical data packages, drawings, and work instructions contain ESD markings, precautions and handling procedures as appropriate;

(f) Inspect ESDS items for proper ESD marking;

(g) Ensure acquisition documentation includes ESD program requirements as applicable;

(h) Perform audits and surveys of subcontractor and supplier ESD control programs;

(i) Perform ESD protective material evaluation.

50.1.4.2 Receiving inspection. Procedures are as follows:

(a) Be aware of all ESDS items to be delivered by vendors;

(b) Remove the unit package of an ESDS item from the shipping container. Do not open unit package. Examine the item for proper labeling and ESD protective packaging in accordance with applicable procedures or contractual requirements. Inspect as follows:

(1) ESDS marked packages - packages of ESDS items should be examined to verify conformance to the precautionary labelling and ESD protective packaging requirements of the contract;

(2) Non-ESDS marked packages - while the supplier is responsible for proper marking of packages containing ESDS items, the treatment of such items delivered without an ESDS marking should be governed as follows:

a. No ESDS marking, but in protective packaging - the packaging should be marked with proper markings and these ESDS items should be handled in accordance with the appropriate procedures. The supplier should be contacted to ensure proper marking of future shipments;

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b. No ESD marking, and no ESD protective packaging - the ESDS item should be rejected as defective and should not be accepted if resubmitted by the supplier.

(3) Open unit packaging and perform tests of ESDS items only in a protected area;
(4) Repackage tested ESDS items in ESD protective packaging material and ensure proper marking on the packaging.

50.1.4.3 In-process inspection and test. Procedures are as follows:

(a) Observe protective handling procedures;
(b) Open unit packaging of ESDS items only in protected areas;
(c) After examination and test, place ESDS assemblies in ESD protective covering or packaging materials.

50.1.4.4 Failure analysis laboratory. Procedures are as follows:

(a) Determine that all ESDS items received for failure analysis are properly packaged in ESD protective packaging material. If such items are not properly packaged, notify the sender of the item to prevent future unprotected failure analysis submittals;
(b) Perform failure analysis of ESDS items observing proper handling procedures.

50.1.5 Manufacturing.

50.1.5.1 Production and factory services. Procedures are as follows:

(a) Design and construct ESD protected areas;
(b) Work with quality assurance to implement and maintain protective procedures and measures;
(c) Investigate possible ESD related failure trends and problem areas occurring during production with reliability and quality assurance.

50.1.5.2 Material receiving area. Procedures are as follows:

(a) Observe protective handling for all ESDS items;
(b) Do not open packages containing ESDS items. Perform quantity counts of ESDS items to compare with contract quantities. If protective packaging is opaque or if counts cannot be verified without opening ESD protective packaging, quantity counts should be deferred to receiving inspection.

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50.1.5.3 Storeroom area. Procedures are as follows:

(a) Transport ESDS items to and from the stockroom area in ESD protective covering or packaging (items received by the storeroom without protective packaging should be referred to reliability);
(b) Do not open unit packages of ESDS items for count, issuance or kitting unless required. When required, opening of unit packaging of ESDS items should be performed in protected areas observing handling procedures. Repackage ESDS items in ESD protective covering or packaging;
(c) Ensure all packages and kits issued from the stockroom containing ESDS items are marked with the ESD sensitive symbol and precautions;
(d) Identify ESDS items on all kitting documentation.

50.1.5.4 Production, processing, assembly, repair and rework. Procedures are as follows:

(a) Observe protective handling procedures and perform operations only in ESD protected areas;
(b) Perform cleaning processes using conductive cleaning fluids or solvents;
(c) Upon completion of assembling and processing of the ESDS assembly, repackage in ESD protective covering or packaging material and ensure proper marking.

50.1.6 System and equipment level test and maintenance. The following procedures also apply to testing in the field:

(a) Perform testing of ESDS items only in ESD protected areas to the extent practicable;
(b) Observe handling procedures and the following:

    (1) Prior to touching an ESDS item, attach personnel ground strap to wrist and connect the other end to ground. Where personnel ground straps cannot be used, momentarily touch a grounded point prior to removing or inserting an ESDS item;
    (2) Upon removal of the failed ESDS item, place in ESD protective covering or packaging;
    (3) Remove the ESDS item from the ESD protective packaging and install the item in the equipment. Avoid touching parts, connectors, electrical terminals, and circuitry.

50.1.7 Packaging and shipping. Procedures are as follows:

(a) Ensure all ESDS items submitted for shipment have been received in ESD protective covering or packaging and are properly marked or labeled;

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(b) Remove items from interim packaging only at an ESD protected area observing handling procedures;
(c) Package the ESDS item in ESD protective material for shipment as required by the contract.

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APPENDIX I

ESD PROTECTIVE MATERIALS AND EQUIPMENT

10. SCOPE

10.1 Scope. This appendix provides information on the selection, procurement, and proper use of ESD protective materials and equipment which is of the utmost importance during design and implementation of an effective ESD control program. Care must be exercised to ensure that the items selected will provide the degree of protection required before any procurement action is taken. In addition, particular care must be exercised during the use of ESD protective materials and equipment to ensure that these materials are performing "as advertised" and as required. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

20.1 Government documents.

20.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

STANDARDS

FEDERAL

Code of Federal Regulations Occupational Safety and Health Standard, Air Contaminants, Part 1910.1000, Chapter XVII, Title 29.

Federal Test Method Standard No. 101, Test Method No. 4046, "Electrostatic Properties of Material."

MILITARY

MIL-STD-1695 - Environments, Working, Minimum Standards for.

MIL-STD-2000 - Standard Requirements for Soldered Electrical and Electronic Assemblies.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Bldg. 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

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20.1.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues are those cited in the solicitation.

JOHN F. KENNEDY SPACE CENTER (KSC)
MMA-1985 - Standard Test Method for Evaluating Triboelectric Charge Generation and Decay.

(Application for copies should be made to John F. Kennedy Space Center, NASA, Kennedy Space Center, FL 32899.)

DEPARTMENT OF TRANSPORTATION (DOT)
Code of Federal Regulations, Title 29, Part 1910.1000 - Hazard Communication Standard.

(The Code of Federal Regulations (CFR) and the Federal Register (FR) are for sale on a subscription basis by the Superintendent of Documents, U.S. Government Printing Office, Washington, DC 20402. When indicated, reprints of certain regulations may be obtained from the Federal agency responsible for issuance thereof.)

20.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)
D 257 - Standard Test Method for D-C Resistance or Conductance of Insulating Materials.
D 991 - Standard Test Method for Rubber Property - Volume Resistivity of Electrically Conductive and Antistatic Products.

(Application for copies should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONIC INDUSTRIES ASSOCIATION
EIA-541-1988 - Packaging Material Standards for ESD Sensitive Items.

(Application for copies should be addressed to the Electronic Industries Association, 2001 Eye Street, NW, Washington, DC 20006.)

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(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

30. ESD PROTECTIVE MATERIALS

30.1 General. The characteristics of ESD protective materials include but are not limited to:

(a) Protection against direct discharge from contact with charged people or a charged object;
(b) Protection against triboelectric generation;
(c) Protection from electrostatic fields.

It is difficult to find one material that provides all of the above characteristics. Often, it is necessary to use a combination of different protective materials to achieve the desired results. The characteristics of materials needed to protect ESDS items is dependent upon factors such as resistivity, decay time, and triboelectric properties. A discussion of these factors is provided in the following sections.

30.1.1 Triboelectric protection. Protection against the generation of electrostatic charges is the best method of ESD control. Factors related to the ability of a material to generate triboelectricity include its composition and the electron configuration of elemental atoms and their bonding. Once a charge is generated, the distribution of that charge is dependent upon the volume and surface resistivity and the surface area of the material. The more conductive the material the faster the charge is distributed.

30.1.2 Charge bleed-off. Conductivity is an important characteristic of ESD protective materials. It allows charges to distribute equally over a material and allows charges to be bled off to ground. ESD protective materials (both conductive and dissipative materials) have this characteristic. The higher the conductivity of a material, the more rapidly charges on a given material can be bled off or distributed.

30.1.3 Shielding. Shielding from electrostatic fields or ESD spark induced electromagnetic pulse (EMP) requires enclosing the item in a suitable conductive material that provides the desired level of attenuation.

30.2 ESD protective material measurement parameters. Measurement parameters used in describing the properties of materials used for protection against ESD are commonly referred to as:

(a) Volume resistivity (ohm-cm)
(b) Surface resistivity (ohms per square)

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(c) Decay time (seconds)
(d) Triboelectric properties

30.2.1 Volume resistivity. Volume resistivity (ρ_v), also referred to as bulk resistivity, is a constant for a given homogeneous material and is mathematically derived as follows:

From electrical theory, the resistance (R) of a piece of material is inversely proportional to the cross-sectional area (A) perpendicular to the flow of current and directly proportional to the length of material (L) parallel to the flow of the current. The constant of proportionality is known as volume resistivity (ρ_v), of the material.

$$R = \frac{\rho_v L}{A}$$

The volume resistivity (ρ_v), is published for various homogeneous materials, and has the unit of ohm-cm.

30.2.2 Surface resistivity. Surface resistivity (ρ_s) is normally used as a resistivity measurement of a thin conductive layer of material over a relatively insulative base material. ρ_s has the dimensions of ohms per square and is a measure of resistance for surface conductive material. The value in ohms per square is independent of the size of the square. This resistance represents the average resistance through very small thicknesses at the material surface.

Of the two resistivity parameters, surface resistivity is the more representative resistivity measurement for surface conductive material and volume resistivity is the more representative for volume conductive material. However, surface resistivity (ρ_s) and volume resistivity (ρ_v) are related by the formula

$$\rho_v = (T)\ (\rho_s)$$

where T is the thickness of the surface conductive layer. This relationship is valid only for a very thin surface conductive layer of the material and is used extensively in the semiconductor industry to find the thickness of a diffused layer. This is not an appropriate formula to relate ρ_s and ρ_v for ESD protective materials.

Since surface resistivity is commonly used as a resistance measurement parameter of laminated materials having a thin conductive surface over an insulative base, it is used to measure the resistivity of surface conductive materials such as: hygroscopic ESD protective polyethylenes, nylon and virgin cotton, metal or carbon coated paper, plastics, and other conductively coated or laminated insulative materials. Conductive layers on these materials are

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usually of near uniform thickness such as the sweat layer of hygroscopic material.

Surface resistivity (ρ_s) should be measured in accordance with ASTM D 257 with unitless correction factor (L/W) for the measured resistance in ohms. The equation relating measured resistance (ohms) and the surface resistance (ohms per square) is given below.

$$(\rho_s) \text{ (ohms per square)} = R \text{ (ohm)} \times \frac{L}{W}$$

where:

ρ_s = surface resistivity (ohms per square)
R = total resistance measured (ohms)
W = distance between the probes
L = probe length

To comply with the requirements of ASTM D 257 and to avoid end effects, circular probes can be used with very similar results to those of rectangular configuration.

30.2.3 Resistivity measurement. Two existing test procedures for measuring the resistivities of conductive and dissipative materials are ASTM D 991 and ASTM D 257.

30.2.4 Decay time. Decay time is another measurement parameter used in describing the property of materials used for protection against ESD. Decay time is measured by charging a section of material with a specified voltage and measuring the time for the voltage to decay to a given level, such as 10 percent of its original value. Hygroscopic ESD protective materials will show variations in decay time at different relative humidities.

30.2.5 Decay time measurement. The method for measuring decay time is provided in Federal Test Method Standard No. 101, Test Method No. 4046, "Electrostatic Properties of Material".

30.2.6 Other material test methods. The Electronic Industries Association has prepared "Packaging Material Standards for ESD Sensitive Items" (EIA-541-1988). This standard uses ASTM D 991, ASTM D 257 and Federal Test Method No. 4046 for material testing.

30.3 Classification of ESD protective materials. There are two basic classifications of ESD protective materials which are based upon ranges of resistivity.

30.3.1 Conductive protective materials. Surface conductive ESD protective materials are defined herein as materials having a surface resistivity less

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than 10^5 ohms/square. Volume conductive ESD protective materials are defined herein as materials having a volume resistivity less than 10^4 ohm-cm.

30.3.2 Dissipative protective materials. Surface conductive dissipative ESD protective materials are defined herein as materials having a surface resistivity equal to or greater than 10^5 ohms/square but less than 10^{12} ohms/square. Volume conductive dissipative ESD protective materials are defined herein as materials having a volume resistivity equal to or greater than 10^4 ohm-cm but less than 10^{11} ohm-cm.

30.3.3 Insulative materials. Insulative materials are defined herein as those materials not classified as either conductive or dissipative ESD protective materials. Insulative materials are not classified as ESD protective materials.

30.4 Triboelectric properties. Many ESD protective materials provide protection against generation of static electricity from triboelectric effects. Many conductive and dissipative ESD protective materials provide protection from triboelectric generation. Hygroscopic type ESD protective materials are generally poor generators of static electricity. Some metals, however, will create significant charges from triboelectric generation as is indicated in the triboelectric series. Aluminum, for example, when rubbed with a common plastic can generate substantial electrostatic charges.

30.4.1 Triboelectric measurement. The National Aeronautics and Space Administration, Kennedy Space Center (KSC) Materials Testing Branch, has prepared a "Standard Test Method For Evaluating Triboelectric Charge Generation and Decay" (MMA-1985-79 Revision 2 July 15, 1988). This test method is used to evaluate the triboelectric charge generated by the test apparatus on the material sample, and the rate of discharge for a given test sample under controlled environmental conditions. The acceptance criteria (pass/fail) used by KSC for materials has been determined in accordance with KSC requirements and could be suitably modified as required. The KSC test method has been used to evaluate the performance of thin plastic materials, pressure sensitive adhesive tapes, and flooring materials. As with the other tests discussed, the correlation of triboelectrification, and surface or volume resistivity, is uncertain for all resistivity values.

30.5 Material testing issues. At the present time, there are three widely used methods for testing materials:

ASTM D 257
ASTM D 991
Federal Standard No. 101 Method 4046

Each of these methods presents the experimentalist with unique problems when testing material. As discussed earlier, volume resistivity (bulk resistivity)

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is a constant for a given homogeneous material. Surface resistivity is normally used as a resistivity measurement of a thin conductive layer of material over a relatively insulative base material. From the above, it can be seen that volume or surface resistivity measurements for materials of complex construction, that is, laminates/multilayer materials or materials that are not clearly either bulk conductive or surface conductive can pose unique measurement problems. Federal Standard No. 101 Method 4046 testing poses unique problems of its own. Decay time measurements, for an induced voltage on a given sample, may not correlate with surface or volume resistivity measurements for materials of complex construction. Additionally, decay time measurements can become complex from the viewpoint of understanding exactly how materials of complex construction, that is, laminates/ multilayer materials, are performing. Each of the three test methods does not, and was not designed to, meet the testing requirements of the entire range of potential ESD protective materials available.

At the current level of technology related to material testing there are fundamental questions related to data obtained by the three test methods discussed above. Each of the three test methods presents complex measurement problems when the material tested is not within the specific boundaries of (1) homogeneous material (bulk conductive), or (2) surface conductive. Material systems that are non-homogeneous and both volume and surface conductive (as are virtually all materials to a degree) present extremely complex measurement problems. This aspect of the problem does not address any uncertainties that may be introduced by either the test apparatus or procedure. Conjunctively, there are additional issues which must also be addressed. It can be postulated that the Method 4046 test does not replicate real world events that is, it demonstrates only a material's propensity to dissipate an induced charge when grounded in accordance with the specified test conditions. The correlation of material resistivity (volume or surface) to other parameters such as static decay time may be inconsistent for materials of complex construction.

30.6 Protective covering and packaging materials. Protective covering materials are selected based upon the user's determination of their technical adequacy to provide the desired level of ESD protection. Protective packaging materials pose unique problems of their own in the context of Government contracts. Government contracts that specify the exact packaging requirements for ESDS items in accordance with military specifications and standards are contractual requirements mandating compliance. The use of military specifications to mandate packaging materials may require that the contractor use only military specification Qualified Products List (QPL) materials. The QPL for the applicable specification lists the approved vendors for a specific material. The substitution of materials from vendors not listed on the QPL is not permissible or acceptable.

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40. ESD PROTECTIVE EQUIPMENT

40.1 General. Various types of equipment are available for controlling or monitoring static electricity. Examples include the following.

40.1.1 Personnel ground straps. Personnel handling ESDS items should wear a skin-contact wrist, leg or ankle ground strap. The function of such straps is to dissipate personnel static charges to ground. In lieu of a personnel ground strap, alternate personnel grounding methods could be used consisting of conductive shoes or heel grounders, and ESD protective floors.

40.1.1.1 Personnel ground strap considerations. Personnel ground straps should have adequate resistance to ground to prevent safety hazards. The ground strap should have sufficient resistance to ground to limit current to the perception level as shown in MIL-STD-454, Requirement 1. Examples of personnel ground straps include:

(a) Carbon impregnated volume conductive plastic ground straps
(b) Volume conductive plastic ground straps
(c) Expandable metallic ground straps
(d) Expandable metallic ground straps with insulative exterior surfaces
(e) Elastic cloth ground straps incorporating conductive wires or conductive fibers.

Each of the ground straps above may have protective resistance incorporated either in the ground strap itself or in the ground cord. For personnel safety, the resistor should be located near the point of contact with the individual's skin to reduce the chances of the cable shorting to ground and shunting the strap's resistance. Metallic exterior surface or carbon impregnated ground straps should have insulative exterior surfaces to prevent inadvertent hard grounding of personnel.

The personnel ground strap should be connected via a protective resistor directly to ground (see Figure 7). The personnel ground strap should contain a quick release mechanism so that the strap will release in emergencies.

Personnel ground straps should be carefully assessed from the perspective of both personnel safety and potential particulate or other contamination caused by ground strap constituents. Materials impregnated with carbon and/or metal wiring can shed conductive particles as can metal plated synthetics used in some types of ground straps.

40.1.2 Protective flooring. Protective flooring materials are available in the form of conductive or dissipative carpeting, vinyl sheeting, vinyl floor tiles and terrazzo. Conductive adhesives should be used in applying conductive vinyl flooring. Hard surfaced protective flooring may require special waxes. Conductive shoes, shoe covers or heel grounders should be used

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to discharge personnel on conductive floors. These items should only be worn in the ESD protected areas and should be kept clean so that contaminants do not inhibit their conductive interface with the floor. People sitting at work benches in an ESD protected area often lift their feet from the floor to the work stool, thus eliminating the benefits of the flooring. Therefore, grounded conductive work stools are often needed with protective flooring.

The protective flooring should have sufficient resistance to ground to limit current to the perception level as shown in MIL-STD-454, requirement 1.

Painted or sealed concrete floors and finished wood floors are typically prime generators of static electricity and should be covered with ESD protective flooring or floor mats or treated to provide ESD protection.

Some areas may preclude the use of protective flooring due to electrical safety requirements. This is particularly true of certain applications in military facilities and platforms which require the use of insulative floor mats for electrical safety. In these cases, personnel ground straps should provide the required degree of ESD protection.

40.1.3 ESD protective floor mats. ESD protective floor mats are available in a variety of materials in the conductive or dissipative resistivity ranges. These floor mats are designed for temporary or semi-permanent installation over existing flooring. Floor mats are technically effective only when considered as part of a continuous personnel grounding system consisting of the floor mat and conductive shoes or heel grounders.

40.1.4 Work bench surfaces. Work benches which contact ESDS items and personnel should have ESD protective work surfaces. Work bench surfaces should be connected to ground through a ground cable. The resistance in the bench top ground cable should be located at or near the point of contact with the work bench top and should have sufficient resistance to ground to limit current to the perception level in MIL-STD-454, requirement 1, considering all parallel resistances to ground such as wrist ground straps, table tops and conductive floors. ESD protective work surfaces are available in a variety of materials. These materials are either conductive or dissipative and may be temporarily or permanently installed on the work bench. Examples of materials which may be used for work surfaces are:

(a) Metallic materials such as stainless steel
(b) Carbon impregnated plastics
(c) Surfactant treated plastics
(d) Laminates
(e) Other materials manufactured or constructed in a manner to be conductive or dissipative

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40.1.5 Electrostatic detectors. Types of electrostatic detectors include electrometer amplifiers, electrostatic voltmeters, electrostatic field meters, and leaf deflection electroscopes. Commonly used detectors include electrostatic field meters which are battery operated and portable. Field meters provide readings of the electrostatic fields produced by charged bodies using a non-contact probe or sensor, and provide readings in electrostatic field strength or electrostatic voltage at a calibrated distance from a charged body. Some electrostatic field meters use radioactive sources similar to those of radioactive ionizers. Nuclear meters will cause beta fogging of radiation detecting film badges under certain circumstances, resulting in possible false radiation exposure indications. Their use aboard nuclear powered vehicles or in other areas containing nuclear equipment is not advisable. Electrostatic detectors can be used for monitoring the magnitude of electrostatic charges existing on materials, objects or people. Additionally, they can be used to measure the approximate magnitude of electrostatic charges generated by personnel movements and triboelectric charges.

40.1.5.1 Electrostatic detector selection considerations. A basic limitation of simple analog electrostatic meters is their response time. Most meters are incapable of responding to pulses with fast rise times and short pulse widths. A high speed storage oscilloscope can be used to measure static charges that are generated and dissipated in shorter times than the response time of a meter. When measuring transient ESD voltages, analog meters may be preferable to digital meters due to their faster response time.

For monitoring and certifying ESD protected areas portable electrostatic field meters may be used. Where class 1 items are handled, more accurate laboratory-type detectors may be required.

Characteristics to consider when selecting an electrostatic detector are:

(a) Sensitivity in terms of minimum voltage level that can be accurately measured;
(b) Response time;
(c) Range of voltage that can be measured;
(d) Accuracy;
(e) Radioactive or electrically operated;
(f) Portability;
(g) Ruggedness;
(h) Simplicity of operation and readability;
(i) Accessories such as remote probes and strip chart recorder output
(j) Calibration requirements
(k) Repairability.

40.1.6 Static sensors and alarms. Static sensor and alarm systems are available for constantly monitoring the levels of static electricity generated

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in a protected area. Some systems have multiple remote sensors which can monitor several stations simultaneously. Some systems also contain strip chart recorders which provide a permanent record of static levels within an area.

40.1.7 Other equipment. At this time there is a wide variety of supplementary equipment available to assist users in establishing protected areas and monitoring the materials in protected areas. This equipment consists of miniaturized static voltage detectors preset to sound an alarm at predetermined voltage levels, surface resistivity checkers with light emitting diode readouts indicating resistivity ranges, and continuous wrist strap monitoring units. Selection and use of these units should be predicated upon complete knowledge of precisely how they function. Additionally, the ability to calibrate any detectors, monitors, alarms, or other instruments used in ESD control program implementation or surveillance is highly desirable. The ability to locally repair and calibrate each of these items should be considered as part of the selection process.

40.1.8 Electrical equipment, tools, soldering irons, solder pots, flow soldering equipment. Soldering irons, solder pots, or flow soldering equipment should be properly grounded. The resistance reading from the tip of a hot soldering iron to workstation ground shall not exceed 5.0 ohms and the potential voltage differences between workstation ground and the tip of the hot soldering iron shall not exceed 2 millivolts RMS in accordance with MIL-STD-2000. Other electrical power equipment which comes into contact with ESDS items should also be properly grounded. ESD protective solder suckers should be used.

40.1.9 Assembly, test, and packaging equipment. Often overlooked during ESD control program design and implementation is the potential for ESD damage caused by assembly, test and packaging equipment. For example, during electronic assembly operations, vacuum pickup and desoldering tools can cause air flows resulting in triboelectric charging. Automated and semi-automated part handling machines used to pickup, position and solder surface mount devices can also be sources of damaging ESD voltage levels. Other sources of potentially damaging ESD voltages include automated processes which use part magazines, integrated circuit rails, and continuous reel part containers, as well as the movements of robotic assembly arms and fixtures during board population. Automated testers, for example "bed of nails" testers, are also potential sources of static voltages during operation.

Automated packaging equipment, including blister and shrink wrap machinery and foam in place equipment are additional sources of potentially damaging static voltage levels.

Due to the wide diversity of manual semi-automated, automated, and robotic assembly, test and packaging equipment available, no universal statements can

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be made about the suitability, or non-suitability, of any specific tool, machine or technique. Quantified data relating to ESD induced damage during operations of this type is extremely difficult to obtain. For these reasons, each user should assess operations based upon the susceptibility levels of the products handled and the specific manual, semi-automated, automated, and robotic equipment selected for use.

Care should be exercised during any assessments to ensure that practical issues are addressed. Measurable static voltages are an inherent part of any process that includes contact and separation of items. These voltages may not be inherently damage producing by themselves unless the charge magnitude is sufficient to damage ESD susceptible items. In addition, the limitations of portable field meters must be well understood, as measurements made with field meters can be highly inaccurate.

40.1.10 Vacuum cleaners. Cleaning operations requiring the use of vacuum cleaners pose the inherent risk of generating static voltage levels of sufficient magnitude to damage ESDS items. Vacuum cleaners are presently available that are constructed of ESD protective materials that provide a continuous electrical grounding path from the nozzle to the electrical power connection. Additionally, some units are available that incorporate natural bristle brushes on the end of the nozzle. Even though these vacuum cleaners provide conductive paths to dissipate static charges, caution must be exercised in their use. Triboelectrification of the object being cleaned, due to particulate contaminated air flow, is still possible. Careful technical evaluation of these products should be performed prior to their use.

40.1.11 Ionizers. Ionizers dissipate electrostatic charges by ionizing air molecules, forming both positive and negative ions. The positive ions are attracted to negatively charged bodies and negative ions to positively charged bodies, resulting in charge neutralization. Ionizers may be either portable units for localized use or systems installed for complete room ionization.

40.1.11.1 Types of ionizers. Ionized air may be used where effective grounding cannot be accomplished to bleed-off static charges, or to dissipate charges on insulators. Ionizers may be useful in dissipating charges where spraying actions are performed. Three methods commonly employed to ionize air are radioactive, electric and static comb. Radioactive material provides alpha particles which ionize the air. The electrical method employs a high voltage square wave signal to ionize air. The static comb employs needle points where the charge concentration on the point can ionize air. This is based on the principle that self-repulsion of charge from a nonspherical body will cause the charge to concentrate on the surface having the least radius of curvature. The radioactive material used in ionized air blowers is provided under license from the U.S. Nuclear Regulatory Commission. Therefore, ionizers using radioactive materials must be leased. In addition, due to

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half-life considerations, the radioactive materials must be replaced periodically, typically once a year.

40.1.11.2 Ion balance considerations. Air from ionizers should contain equal amounts of positive and negative ions to dissipate both the negative and positive charges produced when static electricity is generated. An imbalance of positive or negative ions can result in residual voltages over the ionized area. Ionizers should be periodically evaluated to ensure they are producing equal amounts of positive and negative ions. Placement of ionizers should be in accordance with the manufacturer's recommendations or as determined through monitoring or testing. Manufacturer's specifications normally provide data with respect to decay time versus the distance and the angle of the ionizer to the area requiring protection. Ionizers can take several seconds or even minutes to dissipate charges, depending upon the amount of charge and the distance of the charge from the ionizing source. Ionizers should be turned on for at least 2 to 3 minutes to allow charges in the area to be neutralized. Some ionizers can leave residual voltages high enough to damage ESDS items. Selection and placement of ionizers for adequate ESD control will require measurement of residual voltages in the area to be protected and comparison with the voltage sensitivity levels of ESDS items being handled.

40.1.11.3 Ozone considerations. From an occupational health standpoint it should be noted that some ionizers utilize high voltage which could cause the production of ozone. This can affect personnel adversely. (NOTE: Code of Federal Regulations Occupational Safety and Health Standard, Air Contaminants, Part 1910.1000, Chapter XVII, Title 29, defines the maximum allowable concentration for ozone in a personnel work area).

40.1.12 Spraying, cleaning, and painting equipment. Ionized air blowers may be used as applicable to dissipate electrostatic charges in the work area when spraying, cleaning, or painting ESDS items.

40.1.13 Shunting bars, clips, conductive foams. The terminals of ESDS items should be shorted together using metal shunting bars, metal clips or noncorrosive conductive foams. To act as an adequate shunt, the resistance of the shunting material should be orders of magnitude below the minimum impedance between any two pins of the ESDS part. Shunts will not always protect an item from an ESD. ESDS parts with non-conductive cases, or assemblies subjected to electrostatic fields or direct ESD could result in damaging induced current flow within the ESDS item to the shunt. For parts with metal cases the shunt should also contact the case. For parts with non-conductive cases and for ESDS assemblies, the shunting materials should be wrapped around the ESDS item.

40.1.14 Personnel apparel. Personnel handling ESDS items may wear ESD protective smocks or clothing. Some working situations could require additional protection. Finger cots or gloves, where used, should also be of

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ESD protective materials. Protective apparel should be frequently checked, especially after cleaning to ascertain proper performance.

40.1.15 Test equipment. Test equipment should be properly grounded in accordance with the manufacturer's recommendations. The placement of test equipment in ESD protective areas or on ESD protective surfaces requires careful evaluation to ensure that personnel safety is not compromised. Ground fault interrupters can be used in electrical receptacles used for powering test equipment as an added personnel safety precaution.

40.1.16 Temperature chambers. Temperature chambers may require precautionary techniques to minimize or control the generation of electrostatic charges. The thermal and humidity stability of ESD protective materials used in temperature chambers should be suitable over the test temperature ranges.

40.1.17 Relative humidity. Humid air helps to dissipate electrostatic charges by keeping surfaces moist, therefore increasing surface conductivity. Substantial electrostatic voltage levels can accumulate with a decrease in relative humidity (see appendix A, table IV). However, it is also evident from table IV that significant electrostatic voltages can still be generated with relative humidity as high as 90 percent. Relative humidity between 40 percent and 60 percent in ESD protective areas is desirable as long as it does not result in corrosion or in other detrimental effects such as PWB delamination during soldering. Where high relative humidity levels cannot be maintained, ionized air can be used to dissipate electrostatic charges.

MIL-STD-1695 specifically addresses relative humidity control in the context of static electricity protection. The MIL-STD-1695 requirement is for relative humidity levels in the range of 30-70 percent in areas where electronic parts and hybrid microcircuits (MIL-STD-1695, work areas 5 and 6) are handled or processed. MIL-STD-1695 requires the same level of relative humidity controls for handling and storage areas (MIL-STD-1695, work area 13), except when items are covered or protected.

40.2 Surfactants. Surfactants (surface-active agents), are used to alter surface effects. Cleaning products employ surfactants to "make the water wetter," that is, to promote the ease of evenly dispersing the active ingredients across the surfaces being treated. Surfactants, for static electricity control, consist of topical antistats and internally blended antistats.

40.2.1 Topical antistats. Topical antistats, when applied to the surface of a material, perform a static control function. Topical antistats are generally liquids consisting of a carrier and an antistat. The carrier is the vehicle used to transport the antistat to the material. It acts as a solvent and can be water or alcohol or some other compatible material. The antistat is the agent that remains deposited on the material surface after the carrier

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evaporates. Some antistats are detergents which combine with the moisture in the air in order to wet the surface to which they are applied. These antistats are classified as hygroscopic and their effectiveness is dependent upon the relative humidity. Other antistats are not humidity dependent. In general, the conductivity or the ability to dissipate static can be varied by changing the ratio of antistat to carrier. Topical antistats can be brushed, sprayed, rolled, dipped, mopped, wiped or otherwise applied to floors, carpets, walls, ceilings, tools, work bench tops, parts trays, and clothing, to provide varying degrees of conductivity.

Topical antistats increase conductivity and therefore should not be applied to electronic parts or printed circuit boards. Circuit malfunction could occur because of leakage paths formed by the antistat. Personnel, after applying topical antistats, should thoroughly wash their hands to avoid possible contamination of parts and circuit boards from antistat residue. Also, surface sensitive items, such as precision opticals and miniature bearings, should not come in contact with topical antistats or be packaged in ESD protective materials. Contamination of sensitive surfaces could result from contact transfer, solvent transfer or from vaporization/condensation transfer. Topical antistats can be removed during handling and cleaning operations and the surfaces may then need retreatment.

Items made of ESD protective materials, that require periodic treatment with a topical antistat, should have a label attached to indicate the periodicity for measurement and retreatment.

40.2.2 Internally blended antistats. Products intended for use in ESD protected areas can be treated with internally blended antistats prior to shipping, thus eliminating the need to apply topical antistats later. Internally blended antistats can be added during the manufacturing process of thermoplastics such as polystyrene and PVC. The resulting materials exhibit lower surface resistivities and improved static dissipation.

40.2.3 Selection considerations. Considerations for selecting an antistat, in addition to its ESD preventive properties, include:

(a) Binding capability.
(b) Contamination factors.
(c) Longevity and wear characteristics.
(d) Decay performance and controllability.
(e) Ease of application.
(f) Cost effectiveness.
(g) Bacteria growth inhibition.
(h) Conductivity in critical applications.
(i) Nonhazardous to personnel and the environment.
(j) Noncorrosivity.

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40.3 Computer and Video Display Terminals (Cathode Ray Tubes). All Cathode Ray Tube (CRT) display terminals located in or near ESD protected areas (see MIL-HDBK-263B 5.4) should incorporate measures to reduce electrostatic potentials on face plates or be modified to eliminate electrostatic potentials generated by the CRT at the face of the display terminals. This is to be implemented with an electrically grounded CRT ESD shield mounted to the face of the display terminal.

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APPENDIX J

PERSONNEL TRAINING AND CERTIFICATION

10. SCOPE

10.1 Scope. This appendix provides information on ESD training and certification. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

20.1 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

D 257 - Standard Test Method for D-C Resistance or Conductance of Insulating Materials.

D 991 - Standard Test Method for Rubber Property - Volume Resistivity of Electrically Conductive and Antistatic Products.

(Application for copies should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

541-1988 - Packaging Material Standards for ESD Sensitive Items.

(Application for copies should be addressed to the Electronic Industries Association, 2001 Eye Street, NW, Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

30. INTRODUCTION

30.1 General. Initial and recurrent training in ESD awareness should be provided to all personnel who specify, procure, design, or handle ESDS items. The most extensive ESD protected areas and ESD protective handling procedures will not provide the protection needed if personnel are not properly trained

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in their correct use. ESD training programs should be oriented to the facility and the types of ESD materials and equipment that have been found to be effective for a particular application. Personnel should be trained to effectively employ the ESD protective materials and equipment provided, and to understand the theory behind many of the ESD precautions included in the ESD handling procedures and grounding safety precautions. ESD awareness should also be a part of equipment training courses prepared for the users. Such training should include identification of ESDS items in the equipment, some basic ESD theory, ESD handling precautions, the need for, use of and types of ESD protective packaging and the safety aspects involved where grounding is a part of the ESD handling procedures. Certification of satisfactory completion of the training course should be documented for personnel who have attended and demonstrated a comprehension of the elements of the approved training course.

30.1.1 Skill level. The skill level of both instructors and trainees also has a bearing on the ESD training to be given. The depth of theory on static electricity should depend on the trainee's ability to comprehend the information provided, and the functions the trainee will be expected to perform. For example, engineers require more theoretical training for design of protective circuitry than stock room personnel need for kitting ESDS items.

30.2 Course outline. An example of a detailed ESD training course outline is provided below. Training courses should be tailored to provide the definitive knowledge required by personnel to perform their assigned functions.

(a) Section 1: Introduction to ESD

Course objectives
Definitions
Historical background
Causes and effects of ESD problems
Level of ESD awareness
ESDS parts
Failures not easily recognized as ESD related
Effective use of ESD controls
Case histories I--Manufacturing processes causing ESD problems
Case histories II--ESD failures due to improper handling/packaging

(b) Section 2: Theory of Static Electricity and ESD

Terms commonly used
Capacitance
Types of capacitors encountered in ESD
Dielectric constant of a material
Example: A parallel plate capacitor
Dielectric strength of a material

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Energy stored in a capacitor
Example: Charge and energy in a capacitor
Example: Maximum charge and maximum potential
Charge decay
Material relaxation time
The human body ESD model
Human body equivalent capacitance
Experimental determination of human body ESD model parameters
The ESD pulse
Example: Oscilloscope photos of a typical ESD pulse
Frequency spectrum of the ESD pulse
Example: Frequency spectrum of an ESD pulse
Analysis of human body ESD model test circuit
Electrostatic field
Mathematical expressions for electrostatic fields
Example: Electrostatic field between two charges
Example: Applications of Gauss's law
Example: Electrostatic field intensity
Example: Static voltage versus distance for MOSFET device damage
Electrostatic field shielding
Example: Voltage induced on a device in an insulative bag
Methods of static charging
Contact charging in materials
Example: Voltage generated by contact charging
Factors affecting triboelectric charge generation
A typical triboelectric series
Example: Static charging of solid surfaces
Induction charging
Example: Charge induced on a grounded conductive object by point charge
Ion or electron beam charging
Other methods of charging
Distribution of static charges
Methods of static discharging
Example: Resistance to ground for charge dissipation
Example: Effect of ionization on static voltages
Example: Neutralization of space charges
Example: Effect of relative humidity on static voltages

(c) Section 3: Sources of Static Charges

Prime static generators in the work environment
Commonly overlooked static sources
Typical static voltages in a facility
Manufacturing processes generating charges I.- PCB processing operations
Manufacturing processes generating charges II.- Fluid flow processes

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Human body as a static generator
Static generated from personnel clothing
Packaging materials as static generators
Effects of humidity on static charge generation

(d) Section 4: ESD Sensitive Parts and ESD Sensitivity Testing.

ESD sensitive parts
ESD sensitivity classification
Class 1 ESDS parts
Class 2 ESDS parts
Class 3 ESDS parts
Part electrical parameters typically affected by ESD
Examples of part electrical parameters affected by ESD
Curve tracer waveforms of bipolar transistors
Curve tracer waveforms of JFET
Curve tracer waveforms of GaAs FET
Progressive deterioration of input characteristics of bipolar devices during handling
Curve tracer waveforms of a bipolar op-amp
I-Reverse curve of a Schottky diode
Curve tracer waveforms of TTL
Curve tracer waveforms of LSTTL
Curve tracer waveforms of ECL RAM
Hybrid thin-film resistor/capacitor failures
Parameters affecting part sensitivity to ESD
Human body model equivalent circuit for ESDS testing
Part pin combinations for ESDS testing
MIL-STD-883 Method 3015 testing
ESD sensitivity classification testing
Other models for ESD sensitivity determinations
Charged device model
Field induced model
Machine model
Charged chip model
Other ESD sensitivity testing techniques

(e) Section 5: ESD Related Failure Mechanisms

Part failures
Equipment level failures
Thermal breakdown in a 54L04 TTL gate
SEM photo of bipolar op-amp input transistor damage
Dielectric (oxide) breakdown in a MOS structure
SEM photo of MOS device dielectric breakdown damage
Example of a MOSFET device damaged due to static fields from various charged objects

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Gate oxide dimensions versus breakdown voltage for current MOS technologies
SEM photo of a charged (1000 V) bipolar device discharged to ground
Typical damage paths in ESDS parts

(f) Section 6: Analytical Calculations for Device ESD Sensitivity Determination

Failure models for device ESD sensitivity calculations
The Wunsch-Bell thermal model
Typical Wunsch-Bell model curve
Validity of W-B model for ESD sensitivity calculations
Estimation of W-B constant from discrete device parameters
Example of W-B damage constant for some diodes and transistors
Value of W-B damage constant for some diodes and transistors
ESD sensitivity calculation of an E-B junction based on W-B model
ESD sensitivity calculation procedure
Example: Power transistor ESD sensitivity calculation
Example: CMOS protection diode ESD sensitivity calculation
A metallization failure model
An empirical failure model for integrated circuits
Example: TTL IC ESD sensitivity calculation
Example: Linear IC ESD sensitivity calculation
Example: MOS IC ESD sensitivity calculation
Calculated versus actual test data on ESD sensitivity of some devices
Effects of human body ESD model parameters on Vzap failure voltages

(g) Section 7: ESDS Part/Assembly Design Protection

Design approaches and criteria
Typical protective circuitry for bipolar and MOS ESDS Parts
Phantom emitter for bipolar transistors and linear ICs
Diodes and resistor/diode combinations
Spark gap/diodes and zener diodes
Protective circuitry comparison for MOS ICs
Protective circuitry comparison for high density NMOS ICs
Assembly/equipment ESD protection
PCB zoning, shielding and grounding
Transient suppressors as ESD protective devices

(h) Section 8: ESD Protective Materials

Volume resistivity
Surface resistivity
ESD protective material resistivity ranges
Static decay time

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Charge generation properties
Electrostatic shielding properties
Test methods for ESD protective material properties
Surface and volume resistivity measurements--ASTM D 257
Test setup for ASTM D 257 measurements
Volume resistivity measurement--ASTM D 991
Static decay time measurement--Federal Test Standard No 101 - Method 4046
Test setup for decay time measurements
Triboelectric charge generation measurement
Electrostatic shielding measurements--ANSI/EIA-541-1988
Basic considerations
Relationships between material ESD control properties
Basic considerations in the selection of the ESD protective materials
Forms available in ESD protective materials
Work surfaces
Material samples--work samples
Part/assembly containers
Material samples--containers, shorting bars/clips
Foam
Cushioning for packaging
Material samples--foam, cushioning
Bags
Material samples--bags
Other flexible materials
Personnel apparel
Personnel ground straps
Material samples--wrist ground straps
Flooring, carpeting
Material samples--flooring, carpeting
Liquids and sprays
Typical antistatic agents
Material samples--liquids and sprays
ESD protective packaging considerations
Comparison of some ESD protective packaging materials
ESD protective packaging and labeling alternatives
Environmental effects on ESD protective material properties
Accelerated aging effects on some antistatic bags
ESD protective materials military specifications
National stock numbers for some ESD protective materials

(i) Section 9: ESD Control and Test Equipment

ESD protective tools
Equipment samples--ESD protective tools
Plastic solder removal tool

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Ionization equipment
Principle of operation of high voltage ionizers
Equipment samples--ionized air blowers
Equipment samples--ionizing bars, guns, nozzles
Equipment samples--ionizing grids
Equipment samples--grounded ionizing workstation
Equipment samples--nuclear ionizers
Test methods for ionizers
Biased metal plate method (BPM)
Electrostatic voltage decay method (EDM)
Ion flux method (IFM)
Comparison of some portable electrical ionizers
Electrostatic meters/detectors
Equipment samples--static level alarm systems
ESD simulation equipment
Some commercially available ESD simulators
Equipment samples--ESD simulators
Test fixtures/equipment for measuring the properties of ESDS materials
Equipment samples--static decay meter
Equipment samples--resistivity probe/meter
Equipment samples--ESD analyzer with sensors
Equipment samples--wrist strap/grounding system testers

(j) Section 10: Design and Certification of ESD Protected Work Areas

Basic principles and economic considerations
Minimum requirements for ESD protected work stations
Additional requirements for ESD protected work stations
ESD protected work station basic schematic
Selection of ESD protective materials/equipment
Typical problems at ESD protected work stations
Design of ESD protected areas for equipment
Grounding and safety considerations
A procedure to check work station effectiveness and safety
Certification of ESD protected work areas

(k) Section 11: ESD Control Procedures

Functions/organizations affected
General handling precautions
Operational, intermediate and depot level ESD control maintenance considerations
Equipment level ESD preventative maintenance procedure
ESD protective packaging/marking methods

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(l) Section 12: Evaluating an ESD Control Program in a Facility

MIL-STD-1686 requirements
MIL-HDBK-263 guidelines
ESD control program (ESDCP) general considerations
Functions/organizations affected in a facility
Typical ESDCP responsibilities--acquisition
Typical ESDCP responsibilities--receiving
Typical ESDCP responsibilities--incoming inspection
Typical ESDCP responsibilities--shipping
Typical ESDCP responsibilities--stockroom and staging
Typical ESDCP responsibilities--design engineering
Typical ESDCP responsibilities--manufacturing
Typical ESDCP responsibilities--test engineering
Typical ESDCP responsibilities--quality assurance
Typical ESDCP responsibilities--reliability engineering
ESD training program
ESD program monitoring
ESDCP survey/evaluation checklist--work stations and protected areas
ESDCP survey/evaluation checklist--packaging, marking and shipping
ESDCP survey/evaluation checklist--procedures and training
ESDCP survey/evaluation checklist--other ESDCP requirements

30.3 Training aids. Training aids are extremely helpful in ESD awareness training. Suggested training aids for use in ESD training programs include the following elements.

30.3.1 Video cassette training tapes. A variety of such tapes is available at different technical levels. Each user should carefully assess video tapes prior to use to ensure they are technically accurate and suitable for the intended use. The Naval Sea Systems Command has prepared a video tape entitled "ESD: The Invisible Threat", number 803784DN. This video tape provides an overview of ESD and controls required during handling, maintenance, and packaging procedures.

30.3.2 ESD control program samples. Typical ESD control program material and equipment samples which should be made available to the students would include the following:

(a) ESD sensitivity symbols

(1) EIA RS-471

(b) Various ESD protective materials
(c) ESD protective tools and equipment
(d) Electrostatic voltmeter, ohmmeter, megohmmeter

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30.3.3 Visual aids. Other visual aids such as vu-graphs, diagrams of grounded work stations, pictures and brochures of ESD protective tools and equipment, and photo-micrographs of damaged ESDS items should also be included in a comprehensive ESD training course.

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APPENDIX K

ESD DAMAGE PREVENTION CHECKLIST

10. SCOPE

10.1 Scope. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only. Generic checklists of this nature cannot be prepared that will cover all operations in all facilities in a comprehensive manner. Elements should be added to or deleted from the checklist to reflect the actual control program requirements in a given facility or operation. The checklist, in its final form, should reflect the requirements of the ESD control program plan and should complement the program plan. The primary purpose of a checklist is to assess program implementation, effectiveness and personnel performance.

The checklist is structured such that "YES" is the preferred answer, however, "YES" may not be appropriate in all areas based on program considerations. Judgment must be exercised to establish the appropriate prevention program for specific contract and system requirements.

20. APPLICABLE DOCUMENTS

20.1 Government documents.

20.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

STANDARDS

MILITARY

MIL-STD-129 - Marking for Shipment and Storage.

30. CHECKLIST INDEX

To assist the user in quickly finding the specific topic of interest, the following checklist subject index is included.

Section	Subject	Appendix K
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40. ELECTROSTATIC DISCHARGE (ESD) DAMAGE PREVENTION CHECKLIST

40.1 Management.

40.1.1 Does the organization have an ESD policy? YES/NO
Policy Number _____

(a) Is there an overall plan that encompasses the entire program or multiple documents for specific areas? YES/NO
(b) Is it tailored to be product oriented?
(c) Does it assign responsibility for implementation as part of TQM?
(d) Does it provide authority for implementation? YES/NO
(e) Are formal audits provided for in the policy? YES/NO
(f) Does it provide for maintenance of logs on checks and tests performed? YES/NO
(g) Are standard forms provided for tests? YES/NO
(h) Does it provide for all ESDS items to receive the same level of protection? YES/NO
(i) Does it implement the requirements of MIL-STD-1686? YES/NO
(j) Is it part of the policy that ESDS items are still protected after they are inserted into the next higher assembly? YES/NO

40.1.2 Is there a document that tailors the policy to meet specific contractual requirements? YES/NO
(a) Is this document in agreement with MIL-STD-1686? YES/NO

40.1.3 Is there a statement in the purchase orders to ensure that suppliers of ESDS parts will provide adequate packaging protection and proper marking and labeling in accordance with MIL-STD-1686? YES/NO
(a) If a supplier fails to provide such packaging, marking and labeling are his products rejected? YES/NO

40.1.4 Are audits performed on suppliers, distributors, and manufacturers of parts to ensure they are providing adequate ESD protection in their facilities? YES/NO
(a) Have these auditors been properly trained and

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	certified to audit for ESD?	YES/NO
(b)	Are the results of these audits sufficient evidence to qualify a supplier or cause a supplier to be removed from the qualified suppliers list?	YES/NO
40.1.5	Is it part of the organization's policy to maintain a preferred products list for ESD damage prevention program equipment and materials?	YES/NO
40.1.6	Are ESD protective materials and equipment subjected to an incoming inspection to determine if they will perform as expected?	YES/NO
40.1.7	Are ESD protective bags, tote boxes and trays recycled for use?	YES/NO
(a)	Are there tests performed on these items prior to allowing them to be reused?	YES/NO
(b)	Are these items cleaned prior to reissue for use?	YES/NO
40.1.8	Is there a designated individual whose responsibility is to ensure that ESD protective procedures are being followed and that corrective action is taken when necessary?	YES/NO
(a)	Is there an ESD committee to resolve any and all questions?	YES/NO
(b)	Does this committee have the support of senior management?	YES/NO
(c)	Is there an ESD trouble-shooter or point of contact whenever problems are encountered?	YES/NO
(d)	Is there a feedback plan that allows this group to know when problems have been resolved?	YES/NO
40.1.9	Are audits required?	YES/NO
(a)	Formal?	YES/NO
(b)	Informal?	YES/NO
(c)	Are internal audits performed by a "QA" group?	YES/NO
40.1.10	Are ESD protective work stations certified?	YES/NO
(a)	Are provisions made to keep personnel who have not received ESD awareness training from entering these work stations?	YES/NO
(b)	Are these work stations recertified periodically by the "QA" group?	YES/NO
(c)	Are supervisors required to inspect work areas?	YES/NO
40.1.11	Are parts classified as ESDS?	YES/NO
(a)	Are classification tests run on parts to determine ESD sensitivity?	YES/NO

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(b) Is a human body model equivalent to MIL-STD-883 Method 3015 used? YES/NO
(c) Are classification tests performed on samples of all electronic part types that are used? YES/NO
(d) Are other sources such as the VZAP database used for determining part ESD sensitivity? YES/NO
(e) Are people who handle ESDS items informed of what sources are available to identify ESDS items? YES/NO

40.1.12 Is everything that is received in ESD protective packaging materials treated as ESDS? YES/NO

40.1.13 Is the use of personal hygiene products, food, drinks, smoking, and common plastics prohibited in the ESD protective work areas? YES/NO

40.1.14 Are there controls for humidity in areas where ESDS items are handled? YES/NO
(a) Is the humidity level monitored? YES/NO
(b) Is there a log maintained of the daily humidity level indications? YES/NO
(c) Is there a minimum level which must be maintained? YES/NO
(d) Is there a procedure that explains what to do if these levels are not maintained? YES/NO

40.1.15 Is there an ESD training plan? YES/NO
(a) Are provisions for recurrent training for employees in the plan? YES/NO
(b) Who determines which employees will receive training:
(1) Upper Management? YES/NO
(2) Program Manager? YES/NO
(3) ESD Coordinator? YES/NO
(4) Immediate Supervisor? YES/NO
(5) Other _____ ? YES/NO

(c) Are employees required to have recurrent training after:
(1) changing jobs? YES/NO
(2) every six months, etc.? Periodically? Period_____ YES/NO

(d) Is training provided for all people who specify, acquire, design, assemble, test, inspect, rework, install, and maintain ESDS items? YES/NO

40.1.16 Are custodial personnel given special training for proper cleaning procedures in an ESD protected work

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area? YES/NO

(a) Is it understood special waxes must be used on ESD protective floors? YES/NO

(b) Are trash cans and liners made of ESD protective materials? YES/NO

40.1.17 Is the same protection provided for "failed" items that are provided "good" items, to prevent further degradation to a failed part? (To keep from complicating analysis.) YES/NO

(a) Are failure analysis facilities available? YES/NO

(b) Is there an alternative approach to FA for failures? YES/NO

40.1.18 Are design criteria and protective circuits incorporated to prevent ESD damage? YES/NO

40.2 Training.

40.2.1 Is there a training plan? Plan number _____ YES/NO

(a) Do all personnel receive training in ESD? YES/NO

(b) How long (minutes/hours) is the training course? _____

(c) How often is it scheduled? _____

(d) Who decides which people shall receive training:

(1) The supervisor? YES/NO

(2) The project manager? YES/NO

(3) The quality assurance group? YES/NO

(4) Other _____

(e) Is there any form of an examination given? YES/NO

Oral ____ Written ____

(f) Are training records maintained and available for inspection? YES/NO

(g) Is there an alternate plan for personnel with indirect responsibilities? YES/NO

(h) Is there any recurrent training? YES/NO

(i) How long (minutes/hours) and how often is the recurrent training? _____

(j) Is training provided for the people who perform the following functions with ESDS items? YES/NO

(1) Specify? YES/NO

(2) Acquire? YES/NO

(3) Design? YES/NO

(4) Assemble? YES/NO

(5) Test? YES/NO

(6) Inspect? YES/NO

(7) Package? YES/NO

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(8) Rework? YES/NO
(9) Install? YES/NO
(10) Maintain? YES/NO
(11) Field service? YES/NO
(12) Supervise and manage personnel who handle ESDS items? YES/NO

40.2.2 Who teaches the training course? _____
(a) Where did the instructor receive his training?
_____

40.2.3 Are people who satisfactorily complete this training issued a certification card? YES/NO
(a) Does the certification card have an expiration date? YES/NO
(b) If an individual makes an ESD related mistake, is there a requirement for remedial training? YES/NO

40.2.4 Does the training address:
(a) Organizational policy? YES/NO
(b) Local policy? YES/NO
(c) Theory? YES/NO
(d) Handling precautions? YES/NO
(e) Packaging considerations? YES/NO
(f) Personnel safety? YES/NO
(g) Contractual requirements? YES/NO
(h) TQM YES/NO

40.2.5 Does everyone entering an ESD protected work area receive training? YES/NO

40.2.6 Does everyone who handles an ESDS part, both in and out of the protective packaging, receive training? YES/NO

40.2.7 Is training offered at various levels, each designed for the level of people who will be receiving it? YES/NO

40.2.8 Are the terms "static dissipative" and "conductive" explained in the training? YES/NO

40.2.9 Does the training explain the sources available for identifying items as ESDS? YES/NO
(a) Is it explained how to use these sources? YES/NO

40.2.10 Does the training explain what to do with parts that are improperly labeled, marked, or packaged? YES/NO

40.2.11 Does the training explain the procedures to be used

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	in the event that a part is suspected as being ESDS, but is not marked as such?	YES/NO
40.2.12	Does the training explain why food, drinks, smoking, personal hygiene products or common plastics are not to be used in ESD protective work areas?	YES/NO
40.2.13	Is the subject of ESD protective clothing, including footwear, discussed in the training program?	YES/NO
40.2.14	Is the operation and function of ESD protective circuitry explained during the training?	YES/NO
40.2.15	Does the training explain what to do, or who to see if:	
(a)	a problem arises that is not covered by a procedure?	YES/NO
(b)	there is an error in a procedure?	YES/NO
40.2.16	Is the operation of ionizers and how they remove electrostatic charges explained?	YES/NO
40.2.17	Is it explained why aerosol spray cans (such as circuit coolant) cannot be used on ESDS items or in ESDS protective work areas, unless special precautions are observed?	YES/NO
40.2.18	Does the training promote an awareness of ESD caution markings and symbols on packaging, drawings, parts and assemblies?	YES/NO
40.2.19	Are the approved ESD caution symbols and statements shown during the training?	YES/NO
40.2.20	Are custodial personnel given special training for proper procedures in an ESD protected work area?	YES/NO
(a)	Do they know to use special wax on ESD protective floors?	YES/NO
(b)	Do they know to use only ESD protective trash cans and liners in ESD protected work areas?	YES/NO
40.2.21	Is the training process formally audited?	YES/NO
(a)	How often? _____	
40.3	Engineering.	
40.3.1	Have all personnel supporting the engineering process been trained in ESD awareness?	YES/NO

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40.3.2	Have all electronic parts in the design been classified into one of the following classes?	YES/NO
(a)	Class 1: 0 to 1,999 volts.	
(b)	Class 2: 2,000 to 3,999 volts.	
(c)	Class 3: 4,000 to 15,999 volts.	
40.3.3	Have ESD design guidelines been developed for use?	YES/NO
40.3.4	Have parts with the greatest immunity to ESD been selected for the designs?	YES/NO
40.3.5	Has protective circuitry been incorporated into the design at the lowest circuit level to prevent ESD damage to ESDS items?	YES/NO
40.3.6	Has circuit analysis been performed to verify the adequacy of protective circuitry?	YES/NO
(a)	Have tests proven the effectiveness of the protective circuitry?	YES/NO
40.3.7	Do all drawings (reference DOD-STD-100 section 402.16.8) of ESDS items identify the items as ESDS, reference applicable ESD precautionary procedures, and identify the sensitive pins or terminals on the following?	
(a)	Parts?	YES/NO
(b)	Printed circuit boards?	YES/NO
(c)	Modules?	YES/NO
(d)	Sub-assemblies?	YES/NO
(e)	Assemblies?	YES/NO
(f)	Drawers?	YES/NO
(g)	External connectors?	YES/NO
(h)	Equipment?	YES/NO
40.3.8	Do the drawings show the placement of ESDS markings?	YES/NO
(a)	Can these be readily seen by anyone entering the item?	YES/NO
40.3.9	Do design engineers assist in failure analysis and implementation of corrective action?	YES/NO
40.3.10	Are ESD design considerations and conformance to ESD requirements included in all design reviews?	YES/NO
40.3.11	Are the approved ESDS caution labels and symbols commensurate with MIL-STD-1686?	YES/NO
40.3.12	Are audits performed to ensure that:	

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(a) Procedures, instructions, policies, etc. are:
  (1) current? YES/NO
  (2) adequate? YES/NO
  (3) in use? YES/NO
(b) Adequacy of personnel training can be assessed during audits of handling operations? YES/NO
(c) All technical ESD damage prevention techniques are in place? YES/NO
(d) All ESD damage prevention personnel actions are being properly implemented? YES/NO

40.4 Procurement.

40.4.1 The ESD damage prevention requirements for the receiving area are defined by:
(a) Procedure number? _____
(b) Instruction number? _____
(c) Other? _____
(d) Does everyone know the location of this document? YES/NO

40.4.2 Have all personnel who procure ESDS items been trained in ESD awareness? YES/NO

40.4.3 Do standard ESD contract requirements exist for inclusion of ESD control requirements in procurement documentation? YES/NO

40.4.4 Are pre-award and in-process audits performed on subcontractors to assure that they have established effective ESD control programs? YES/NO
(a) Are these audits also performed on suppliers of ESDS items to assure they have an established ESD control program? YES/NO
(b) Is there a list of subcontractors and suppliers who have a suitable ESD control program as a result of these audits? YES/NO

40.4.5 Are qualified suppliers required to have a suitable ESD control program? YES/NO

40.4.6 Are all ESDS items to be procured identified to procurement personnel by engineering to ensure that ESD control program requirement clauses can be included in the purchase orders? YES/NO
(a) Are items classified as either Class 1, Class 2, or Class 3? YES/NO

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40.4.7 Are ESD control program requirements incorporated in procurement documents for all procurements of ESDS items? YES/NO

40.4.8 Are subcontractors, suppliers and vendors required to certify that ESDS items are manufactured, handled, and packaged using ESD controls? YES/NO

40.4.9 Has procurement ensured that suppliers and subcontractors will participate in feedback for corrective action programs? YES/NO

40.4.10 Is procurement included on distribution of product deficiency reports from internal organizations? YES/NO

40.4.11 Are audits performed to ensure that:
(a) Procedures, instructions, policies, etc. are:
(1) current? YES/NO
(2) adequate? YES/NO
(3) in use? YES/NO
(b) Adequacy of personnel training can be demonstrated during audit of handling operations? YES/NO
(c) All technical ESD damage prevention techniques are in place? YES/NO
(d) All ESD damage prevention personnel actions are being properly implemented? YES/NO

40.5 Receiving area.

40.5.1 The damage prevention requirements for the receiving area are defined by:
(a) Procedure number? _____
(b) Instruction number? _____
(c) Other? _____
(d) Does everyone know the location of this document? YES/NO

40.5.2 Are special markings used for identifying ESDS items? YES/NO
(a) If not, how are they distinguished? YES/NO
(b) Is there a master list of ESDS items? YES/NO
(c) Are updates to this list received in this area? YES/NO

40.5.3 Can it be determined that a part is ESD sensitive from the shipping document without opening the actual shipping container? YES/NO
(a) Are all intermediate and final shipping containers inspected to verify that an ESD caution label is affixed to their exterior? YES/NO

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40.5.4	Are there procedures that explain what to do in the following situations?	YES/NO
(a)	How to handle ESDS items that are improperly packaged?	YES/NO
(b)	How to handle ESDS items that are improperly labeled?	YES/NO
(c)	What to do with ESDS items that are being worked at the end of the work shift and at breaks?	YES/NO
40.5.5	Are ESDS parts packaged inside a protective container?	YES/NO
(a)	Are all fillers and packing inside the protective container either static dissipative or conductive?	YES/NO
(b)	Is a sample of these materials checked to verify they conform to the appropriate requirements?	YES/NO
40.5.6	When an item is received in ESD protective packaging material, is it treated as ESDS, until Engineering verifies otherwise?	YES/NO
40.5.7	Is protective packaging of the ESDS items that have been received checked to ensure adequate ESD protection has been provided during shipment?	YES/NO
40.5.8	If a part is received that is not marked as ESDS, but is suspected as being such, is there a procedure to verify its sensitivity?	YES/NO
40.5.9	Are ESDS parts maintained in protective packaging throughout this area?	YES/NO
(a)	If this protection is removed, is it done at an ESD protective work area?	YES/NO
40.5.10	When ESDS items are removed from ESD protective packaging for inspection or test, are they repackaged in the ESD protective material prior to leaving the area?	YES/NO
40.5.11	Is there an ESD protected work station in this area?	YES/NO
40.5.12	Does this work area require use of any of the following:	
(a)	Conductive carts?	YES/NO
(b)	Protective smocks?	YES/NO
(c)	Conductive shoes?	YES/NO
(d)	Ionizers?	YES/NO

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(e)	Conductive floors?	YES/NO
(f)	Static detectors or monitors?	YES/NO
(g)	Heel or leg straps?	YES/NO
(h)	Wrist straps?	YES/NO
(i)	Conductive chairs or seat covers?	YES/NO
(j)	Protective IC rails?	YES/NO
(k)	Table coverings?	YES/NO
(l)	Non-static generating tools?	YES/NO
(m)	ESD protective bags?	YES/NO
(n)	ESD caution labels and signs?	YES/NO
(o)	Protective foam?	YES/NO
(p)	Protective bubble wrap?	YES/NO
(q)	Protective tote boxes or trays?	YES/NO
40.5.13	Are drinking, eating, smoking, the use of personal hygiene products and common plastics prohibited in the ESD protected work area?	YES/NO
40.5.14	Is the relative humidity of the ESD protected work area controlled between specified limits?	YES/NO
(a)	Is it monitored on a regular basis?	YES/NO
(b)	Is there a log maintained of these checks?	YES/NO
(c)	Is there a minimum level which must be maintained?	YES/NO
(d)	Is there a procedure for corrective action if the corrective levels are not maintained?	YES/NO
40.5.15	Is there an ESD discrepancy reporting system?	YES/NO
(a)	Is there a designated individual that receives these reports?	YES/NO
(b)	Is there a record maintained of any discrepancies that have been found and corrective action taken?	YES/NO
40.5.16	Are audits performed to ensure that:	
(a)	Procedures, instructions, policies, etc. are:	
	(1) current?	YES/NO
	(2) adequate?	YES/NO
	(3) in use?	YES/NO
(b)	Adequacy of personnel training can be demonstrated during audit of handling operations?	YES/NO
(c)	All technical ESD damage prevention techniques are in place?	YES/NO
(d)	All ESD damage prevention personnel actions are being properly implemented?	YES/NO

40.6 <u>Storage area</u>.

40.6.1 Are the ESD damage prevention requirements for

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storage defined by:

(a)	Procedure number?_____	YES/NO
(b)	Instruction number?_____	YES/NO
(c)	Other documents?_____	YES/NO
(d)	Does everyone know the location of this document?	YES/NO
40.6.2	Are ESDS parts packaged with adequate protection when received into this area?	YES/NO
40.6.3	Are there special markings for ESDS items?	YES/NO
(a)	Is there a master list of ESDS items?	YES/NO
(b)	Are updates to this list received in this work area?	YES/NO
40.6.4	Is there a procedure to explain what to do in the following situations:	
(a)	How to handle ESDS items that are improperly packaged?	YES/NO
(b)	How to handle ESDS items that are improperly labeled?	YES/NO
(c)	What to do with ESDS items that are being worked at the end of a shift or at breaks?	YES/NO
40.6.5	Are ESDS items marked so they may be readily recognized without the paperwork?	YES/NO
(a)	Is the marking for ESDS items adequate to prevent opening the protective packaging for identification?	YES/NO
40.6.6	Is there an ESD discrepancy reporting system?	YES/NO
(a)	Is there a designated individual that receives these reports?	YES/NO
(b)	Is there a record maintained of any discrepancy found and corrective action taken?	YES/NO
40.6.7	Is there an ESD protected work station in this area?	YES/NO
40.6.8	Does this work area require the use of any of the following:	
(a)	Conductive carts?	YES/NO
(b)	ESD protective smocks?	YES/NO
(c)	Conductive shoes?	YES/NO
(d)	Ionizers?	YES/NO
(e)	Conductive floors?	YES/NO
(f)	Electrostatic detector or monitors?	YES/NO
(g)	Heel or leg straps?	YES/NO
(h)	Wrist straps?	YES/NO
(i)	Conductive chairs or seat covers?	YES/NO
(j)	Protective IC rails?	YES/NO
(k)	Table Coverings?	YES/NO

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(l) ESD protective bags? YES/NO
(m) ESD caution labels and signs? YES/NO
(n) Protective bubble wrap? YES/NO
(o) Protective tote boxes or trays? YES/NO
(p) Other _____

40.6.9 Are drinking, eating, smoking, the use of personal hygiene products and common plastics prohibited in the ESD protected work area? YES/NO

40.6.10 Are ESDS items maintained in protective covering or packaging at all times, except whenever they are actually being handled? YES/NO
(a) Is ESD protective packaging provided when moving parts from area to area? YES/NO

40.6.11 Are ESDS items that are to be shipped from this area packed with proper ESD precautions? YES/NO
(a) Are partial issues maintained in protective covering or packaging? YES/NO
(b) Are ESDS items only kitted at ESD protective work areas? YES/NO

40.6.12 Is the relative humidity of the ESD protected work area controlled between specified limits? YES/NO
(a) Is it monitored on a regular basis? YES/NO
(b) Is a log maintained of these checks? YES/NO
(c) Is there a minimum level which must be maintained? YES/NO
(d) Is there a procedure for corrective action if these levels are not maintained? YES/NO

40.6.13 Are audits performed to ensure that:
(a) Procedures, instructions, policies, etc. are:
(1) current? YES/NO
(2) adequate? YES/NO
(3) in use? YES/NO
(b) Adequacy of present training can be demonstrated during audit of handling operations? YES/NO
(c) All technical ESD damage prevention techniques are in place? YES/NO
(d) All ESD damage prevention personnel actions are being properly implemented? YES/NO

40.7 Work areas. (Receiving, Receiving Inspection Storage, Assembly, Test Repair, Quality Inspection, Installation, Check-out, Failure Analysis)

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40.7.1	Is there an ESD operating procedure for these areas? Procedure number _____	YES/NO
(a)	Does everyone know the location of the operating procedure and have access to it?	YES/NO
(b)	Are all documents in ESD protective containers?	YES/NO
(c)	Do all work instructions reference the ESD procedure to be implemented for each process?	YES/NO
(d)	Is it explained what to do with ESDS items at end of each workshift or at breaks?	YES/NO
40.7.2	Is there an ESD protected work station in this area?	YES/NO
40.7.3	Which of the following are required in this work area:	
(a)	Conductive carts?	YES/NO
(b)	ESD protective smocks?	YES/NO
(c)	Conductive shoes?	YES/NO
(d)	Ionizers?	YES/NO
(e)	Conductive floors?	YES/NO
(f)	Electrostatic detectors or monitors?	YES/NO
(g)	Heel or leg straps?	YES/NO
(h)	Wrist straps?	YES/NO
(i)	Conductive chairs or seat covers?	YES/NO
(j)	Protective IC rails?	YES/NO
(k)	Table covering?	YES/NO
(l)	Non-static generating tools?	YES/NO
(m)	ESD protective bags?	YES/NO
(n)	ESD caution labels and signs?	YES/NO
(o)	Protective foam?	YES/NO
(p)	Protective bubble wrap?	YES/NO
(q)	Protective tote boxes or trays?	YES/NO
(r)	Protective solder suckers?	YES/NO
(s)	Grounded tip soldering irons?	YES/NO
40.7.4	Are ESD protective solder suckers used?	YES/NO
(a)	Are they checked to ensure that charges are not generated?	YES/NO
40.7.5	Are insulated handles on tools used?	YES/NO
(a)	Are all the tools of a metallic or conductive nature?	YES/NO
(b)	Are soldering iron tips connected to ground?	YES/NO
40.7.6	Where brushes are used for cleaning of ESDS items, are they made from natural fibers and not synthetic?	YES/NO
40.7.7	Are drinking, eating, smoking, the use of personal hygiene products and common plastics prohibited in this area?	YES/NO

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40.7.8	Is the relative humidity of the ESD protected work area controlled between specified limits?	YES/NO
(a)	Are the humidity levels checked on a regular basis?	YES/NO
(b)	Is there a log maintained of these checks?	YES/NO
(c)	Is there a minimum level which must be maintained?	YES/NO
(d)	Is there a procedure for corrective action if these levels are not maintained?	YES/NO
40.7.9	Has everyone who may enter an ESD protected work area been trained in ESD precautions?	YES/NO
(a)	Are there restraints to keep a person who has not been trained from entering an ESDS protected work area?	YES/NO
40.7.10	Is there an ESD discrepancy reporting system?	YES/NO
(a)	Is there a designated individual to receive these reports?	YES/NO
(b)	Are records maintained of any discrepancy that has been found?	YES/NO
40.7.11	Does any electrical equipment in the area have hard grounded working surfaces?	YES/NO
(a)	Are these surfaces isolated from the ESD protective work surface?	YES/NO
40.7.12	Are ionizers used in this area to remove static charges?	YES/NO
(a)	Are air guns and heat guns equipped with an ionizer to keep from generating an electrostatic charge?	YES/NO
40.7.13	Are ESDS items properly covered or packaged when received in this area?	YES/NO
40.7.14	Are ESD items maintained in protective covering or packaging except when actually being handled?	YES/NO
(a)	Are ESDS items stored in ESD protective cabinet or bins while awaiting work?	YES/NO
(b)	Are distinguishing marks placed on ESDS circuit boards?	YES/NO
(c)	Are ESDS items enclosed in ESD protective material after completion of assembly or test?	YES/NO
(d)	Are all exposed connectors, pins, terminals, test points, etc. protected from ESD events throughout the entire process?	YES/NO
(e)	Are ESDS items packaged with proper ESD cautions, including labeling, when shipped from this area?	YES/NO
(f)	Is the same protection provided for "failed" items	

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that is provided for "good" items, to keep from further degrading the part? YES/NO

40.7.15 Are audits performed in this area to ensure that:

(a) Procedures, instructions, policies, and so forth are:

(1) current? YES/NO

(2) adequate? YES/NO

(3) in use? YES/NO

(b) Adequacy of present training can be demonstrated during audit of handling operations? YES/NO

(c) All technical ESD damage prevention techniques are in place? YES/NO

(d) All ESD damage prevention personnel actions are being properly implemented? YES/NO

40.8 Shipping area.

40.8.1 Is there an ESD operating procedure for this area? YES/NO
Procedure number _____

(a) Does everyone know the location of the operating procedure and have access to it? YES/NO

(b) Are all documents in ESD protective containers? YES/NO

(c) Do all work instructions reference the ESD procedure to be implemented for each process? YES/NO

(d) Does the procedure specify the protective packaging requirements? YES/NO

(e) Is it explained what to do if a part is received in this area that is not properly protected/identified? YES/NO

(f) Is it explained what to do with ESDS items at the end of each workshift or during breaks? YES/NO

40.8.2 Are ESDS items maintained in protective covering or packaging at all times, except when they are actually being handled? YES/NO

(a) Are all ESDS items properly packaged in ESD protective packaging and properly marked prior to leaving this area? YES/NO

(b) When parts are divided for kitting, is it accomplished at an ESD protected work station? YES/NO

(c) Are all exposed connectors, pins, terminals, test points, etc. protected from ESD events throughout the entire process? YES/NO

(d) Is the same protection provided for "failed" items that is provided for "good" items, to keep from further degrading the part? YES/NO

40.8.3 Is the MIL-STD-129 ESD caution label used on the exterior of intermediate and final shipping

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	container?	YES/NO
40.8.4	Does packaging provide protection against:	
(a)	triboelectric generation?	YES/NO
(b)	instantaneous discharge?	YES/NO
(c)	electrostatic fields?	YES/NO
(d)	Is there a conductive container provided in the shipping process?	YES/NO
(e)	Are fillers and packing materials inside the conductive container made of ESD protective materials?	YES/NO
40.8.5	Is there an ESD protected work station in this area?	YES/NO
(a)	Has everyone who enters an ESD protected work area been trained in ESD precautions?	YES/NO
(b)	Are wrist straps readily available for visitors?	YES/NO
(c)	Are drinking, eating, smoking, the use of personal hygiene products and common plastic prohibited in this area?	YES/NO
40.8.6	Which of the following are required in this work area:	
(a)	Conductive carts?	YES/NO
(b)	ESD protective smocks?	YES/NO
(c)	Conductive shoes?	YES/NO
(d)	Ionizers?	YES/NO
(e)	Conductive floors?	YES/NO
(f)	Electrostatic detectors or monitors?	YES/NO
(g)	Heel or leg straps?	YES/NO
(h)	Wrist straps?	YES/NO
(i)	Conductive chairs or seat covers?	YES/NO
(j)	Protective IC rails?	YES/NO
(k)	Table covering?	YES/NO
(l)	Non-static generating tools?	YES/NO
(m)	ESD protective bags?	YES/NO
(n)	ESD caution labels and signs?	YES/NO
(o)	Protective foam?	YES/NO
(p)	Protective bubble wrap?	YES/NO
(q)	Protective tote boxes or trays?	YES/NO
(r)	Other _____	
40.8.7	Is the relative humidity of the ESD protected work area controlled between specified limits?	YES/NO
(a)	Is the humidity level monitored on a regular basis?	YES/NO
(b)	Is there a log maintained of these checks?	YES/NO
(c)	Is there a minimum level which must be maintained?	YES/NO
(d)	Does the procedure explain corrective actions necessary if the levels are not maintained?	YES/NO

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40.8.8	Is there an ESD discrepancy reporting system?	YES/NO
(a)	Is there a designated individual who receives these reports?	YES/NO
(b)	Are records maintained of all discrepancies detected?	YES/NO
40.8.9	Are audits performed in this area to ensure that:	
(a)	Procedures, instructions, policies, etc. are:	
	(1) current?	YES/NO
	(2) adequate?	YES/NO
	(3) in use?	YES/NO
(b)	Adequacy of present training can be demonstrated during audit of handling operations?	YES/NO
(c)	All technical ESD damage prevention techniques are in place?	YES/NO
(d)	All ESD damage prevention personnel actions are being properly implemented?	YES/NO
40.9	Intra-plant and inter-plant movement.	
40.9.1	Is there a document that explains how ESDS items will be handled while being moved from area to area?	YES/NO
(a)	From plant to plant?	YES/NO
(b)	Does this document explain the difference in "inter" and "intra" plant movement?	YES/NO
(c)	Does the document explain how the item will be packaged and labeled to prevent damage?	YES/NO
(d)	Does it explain what to do with ESDS items at the end of each shift or during breaks?	YES/NO
40.9.2	When the following ESDS items are transported within the organization, either in the same building or between buildings, are they maintained in protective covering or packaging:	
(a)	piece parts?	YES/NO
(b)	printed circuit boards?	YES/NO
(c)	modules?	YES/NO
(d)	subassemblies?	YES/NO
(e)	assemblies?	YES/NO
(f)	completed equipment?	YES/NO
40.9.3	Is there a group that is responsible for determining the protection that should be provided for ESDS items?	YES/NO
(a)	Are all exposed connectors, pins, terminals, test points, etc. protected from ESD events?	YES/NO
(b)	Is the same protection provided for "failed" items that is for "good" items, to keep from further degrading the part?	YES/NO

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(c)	Are ESDS items maintained in protective covering or packaging at all times?	YES/NO
(d)	Are the containers for ESDS items adequately marked with ESDS symbols and cautions so that the contents can be recognized as ESDS without opening the container?	YES/NO
40.9.4	Are all ESDS items properly marked and packaged prior to moving them?	YES/NO
40.9.5	Is there a group that is responsible for checking protective materials for compliance?	YES/NO
40.9.6	Should any of the following be required to do this work:	
(a)	Conductive carts?	YES/NO
(b)	ESD protective smocks?	YES/NO
(c)	Conductive shoes?	YES/NO
(d)	Ionizers?	YES/NO
(e)	Conductive floors?	YES/NO
(f)	Heel or leg straps?	YES/NO
(g)	Wrist straps?	YES/NO
(h)	Conductive chairs or seat covers?	YES/NO
(i)	Protective IC rails?	YES/NO
(j)	ESD protective bags?	YES/NO
(k)	ESD caution labels and signs?	YES/NO
(l)	Protective foam?	YES/NO
(m)	Protective bubble wrap?	YES/NO
(n)	Protective tote boxes or trays?	YES/NO
40.9.7	Is there an ESD discrepancy reporting system?	YES/NO
(a)	Is there a designated individual who receives these reports?	YES/NO
(b)	Is there a record of discrepancies that have been found and corrective actions taken?	YES/NO
40.9.8	Are audits performed in this area to ensure that:	
(a)	Procedures, instructions, policies, etc. are:	
	(1) current?	YES/NO
	(2) adequate?	YES/NO
	(3) in use?	YES/NO
(b)	Adequacy of present training can be demonstrated during audit of handling operations?	YES/NO
(c)	All technical ESD damage prevention techniques are in place?	YES/NO
(d)	All ESD damage prevention personnel actions are being properly implemented?	YES/NO

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40.10 ESDS protected work stations.

40.10.1	Is there a document for the configuration management of the ESD work station?	YES/NO
	Document number _____	
(a)	Does this document make provisions for logs to be maintained for checks that are performed on the items of the work station?	YES/NO
(b)	Does it specify that work stations will be certified?	YES/NO
(c)	Does it specify that the station will be marked with caution signs?	YES/NO
(d)	Does it specify that all persons that enter must be trained in ESD awareness at a minimum?	YES/NO
(e)	Does it explain what to do with ESDS items at the end of each shift or during breaks?	YES/NO
40.10.2	Is ESD damage prevention provided through implementation of ESD controls such as:	
(a)	Selection and application considerations for ESD protective materials and equipment?	YES/NO
(b)	Certification of ESD protected work areas?	YES/NO
(c)	Other? _____	YES/NO
40.10.3	When selecting ESD protective materials, are the following protective properties taken into account:	
(a)	Protection against triboelectric generation?	YES/NO
(b)	Protection against electrostatic fields?	YES/NO
(c)	Protection against direct discharge?	YES/NO
40.10.4	Is the relative humidity of the ESD protected work area controlled between specified limits?	YES/NO
(a)	Are the humidity levels monitored on a regular basis?	YES/NO
(b)	Is there a log maintained of these checks?	YES/NO
(c)	Is there a minimum level which must be maintained?	YES/NO
(d)	Is there a procedure for corrective action if these levels are not maintained?	YES/NO
40.10.5	Is there an ESD protective work station in these operational areas?	
(a)	Receiving?	YES/NO
(b)	Receiving Inspection?	YES/NO
(c)	Storage?	YES/NO
(d)	Assembly?	YES/NO
(e)	Wave Soldering?	YES/NO
(f)	Manufacturing?	YES/NO
(g)	Test?	YES/NO
(h)	Repair?	YES/NO

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(i)	Quality Inspection?	YES/NO
(j)	Process packaging?	YES/NO
(k)	Installation?	YES/NO
(l)	Failure Analysis?	YES/NO
(m)	Other _____	

40.10.6 Which of the following are required in this work area:

(a)	Conductive carts?	YES/NO
(b)	ESD protective smocks?	YES/NO
(c)	Conductive shoes?	YES/NO
(d)	Ionizers?	YES/NO
(e)	Conductive floors?	YES/NO
(f)	Electrostatic detectors or monitors?	YES/NO
(g)	Heel or leg straps?	YES/NO
(h)	Wrist straps?	YES/NO
(i)	Conductive chairs or seat covers?	YES/NO
(j)	Protective IC rails?	YES/NO
(k)	Table covering?	YES/NO
(l)	Non-static generating tools?	YES/NO
(m)	ESD protective bags?	YES/NO
(n)	Grounded storage cabinets or bins?	YES/NO
(o)	ESD caution labels?	YES/NO
(p)	Protective foam?	YES/NO
(q)	Protective bubble wrap?	YES/NO
(r)	Protective tote boxes or trays?	YES/NO
(s)	Grounded tip soldering irons?	YES/NO
(t)	Non-static generating solder suckers?	YES/NO
(u)	Ionizers for air lines and hot air guns	YES/NO
(v)	Grounded thermal wire strippers	YES/NO
(w)	Other _____	

40.10.7	If carts are used to transport ESDS items, are the carts constructed of ESD protective materials?	YES/NO
(a)	Are the carts connected to ground prior to insertion or removal of ESDS items?	YES/NO
(b)	Is the ground connection checked frequently to assure that it makes a good ground connection?	YES/NO
(c)	Is the surface of the cart checked frequently to determine if it generates a charge?	YES/NO
40.10.8	Is ESD protective clothing required to be worn?	YES/NO
(a)	Is the clothing checked to determine if it generates a charge?	YES/NO
(b)	Is clothing cleaned on a regular basis?	YES/NO
(c)	How is cleaning performed? _____	
(d)	Is a log maintained of the cleaning and checks?	YES/NO

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40.10.9	Are the use of conductive shoes or heel or leg straps required?	YES/NO
(a)	Is there a check to see if these generate a charge?	YES/NO
(b)	Are these cleaned or replaced when dirty?	YES/NO
(c)	Are tests performed after each cleaning?	YES/NO
40.10.10	Are ionizers used to minimize the charges from unavoidable materials?	YES/NO
(a)	Does the blower motor provide a smooth flow of air across the area that it protects?	YES/NO
(b)	If radioactive type ionizers are used, are they on a recall program with the manufacturer?	YES/NO
(c)	If electronic type ionizers, check the following requirements:	
	(1) Is the ozone level checked at least every 6 months?	YES/NO
	(2) Is the output checked to assure that it has a balanced output of positive and negative ions?	YES/NO
	(3) Is it in use near a sensitive EMI operation?	YES/NO
(d)	Are ionizers used on air lines and sprayers?	YES/NO
40.10.11	Is the floor of the ESD protected work area covered with ESD protective material?	YES/NO
(a)	Are there special maintenance requirements for the floors?	YES/NO
(b)	Is it understood that waxes cannot be used on protective flooring?	YES/NO
(c)	Are resistance checks performed on the floors to assure that they meet the manufacturer's specifications?	YES/NO
(d)	Is a log maintained of these checks?	YES/NO
40.10.12	Is there an electrostatic detector or monitor located in this area?	YES/NO
(a)	Is it the continuous monitor type?	YES/NO
(b)	Is it the spot check type?	YES/NO
(c)	Does it have the sensitivity to detect a static field of 50V?	YES/NO
40.10.13	Do wrist straps have an insulative outer covering?	YES/NO
(a)	Do they use a swivel connector at both ends to allow maximum freedom of movement?	YES/NO
(b)	Do they have an easy break-away connector at one end?	YES/NO
(c)	Is there a resistor in the cord located in such a way that it cannot be shorted?	YES/NO
(d)	Are the wrist straps checked every day prior to use?	YES/NO
(e)	Is there a log maintained of these checks?	YES/NO

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(f)	Are failed wrist straps investigated?	YES/NO
(g)	Are there extra wrist straps available for visitors?	YES/NO
40.10.14	Are protective chairs or seat covers used?	YES/NO
(a)	Are tests performed on the items?	YES/NO
(b)	Is the ground connection checked to assure it makes a good connection?	YES/NO
(c)	Are the items made with protective material?	YES/NO
40.10.15	Are the bench tops made of static protective material?	YES/NO
(a)	Is there a resistor in the ground cord that cannot be short circuited?	YES/NO
(b)	Are the tops cleaned on a regular basis?	YES/NO
(c)	Are checks performed on the tops to see if they dissipate charges and will not generate a charge?	YES/NO
(d)	Is there a log maintained of these checks?	YES/NO
40.10.16	Are all the hand tools used in the ESD work station made from non-static generating material?	YES/NO
(a)	Is testing performed on the tools to assure the tools do not generate a charge?	YES/NO
40.10.17	Do the soldering irons used in the ESD work station have the tip at ground potential?	YES/NO
(a)	Are they checked weekly?	YES/NO
(b)	Is testing performed on the soldering iron to ensure that it does not generate a charge?	YES/NO
40.10.18	Are all ESD damage prevention equipment and materials:	
(a)	Procured based upon a specification?	YES/NO
(b)	Verified at a receiving inspection for proper performance?	YES/NO
40.10.19	Are all of the required ESD damage prevention equipment and materials selected from a qualified vendors or procurement list?	YES/NO
40.10.20	Are all personnel who have not received training in ESD awareness prevented from entering ESD work stations?	YES/NO
40.10.21	Is there an individual whose responsibility it is to ensure that ESD rules are being followed and that corrections of discrepancies are closed out?	YES/NO
(a)	Does this individual have the authority to stop anyone from entering the ESD area?	YES/NO
(b)	Can this individual stop work at an ESD work station	

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	due to policies or procedures not being followed?	YES/NO
(c)	Does this individual have a direct reporting route to upper management without going through area supervisors to resolve an ESD problem?	YES/NO
40.10.22	Are ESD protective trash cans used?	YES/NO
(a)	Are liners for these trash cans made from non-static generating materials?	YES/NO
40.10.23	Does the ESD work station have a supply of consumable ESD damage prevention materials such as bags, shunts, heel straps, bubble wrap, labels, etc.?	YES/NO
40.10.24	Who decides when ESDS protective materials such as bags, boxes and wrist straps will be replaced?	
(a)	Area supervisor?	YES/NO
(b)	QA inspector?	YES/NO
(c)	ESD monitor?	YES/NO
(d)	Engineering?	YES/NO
(e)	Other? _____	
40.10.25	Are the ESD protective materials and equipment subjected to an incoming inspection upon receipt to ensure they perform as expected?	YES/NO
(a)	Is there an individual responsible for this action?	YES/NO
(b)	Is there established criteria for acceptance?	YES/NO
(c)	Are records maintained of these checks?	YES/NO
40.10.26	Are audits performed to ensure that:	
(a)	Procedures, instructions. policies, etc. are:	
	(1) Current	YES/NO
	(2) adequate?	YES/NO
	(3) in use?	YES/NO
(b)	Adequacy of present training can be demonstrated during audit of handling operations?	YES/NO
(c)	All technical ESD damage prevention techniques are in place?	YES/NO
(d)	All ESD damage prevention personnel actions are being properly implemented?	YES/NO
40.11	Quality functions.	
40.11.1	Are all inspectors and quality control personnel trained in ESD awareness?	YES/NO
40.11.2	Are all inspection areas where ESDS items are handled or tested considered to be ESD protected work areas?	YES/NO

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40.11.3	Are ESD precautionary procedures provided for all quality functions and documented in the quality assurance manual?	YES/NO
40.11.4	Do quality control personnel certify and label all ESD protected work areas?	YES/NO
40.11.5	Do quality control personnel review the adequacy of ESD markings and cautions on drawings, documentation, assemblies, and equipment?	YES/NO
40.11.6	Are quality control personnel responsible for reviewing all procurement specifications to ensure that ESD controls are in the contract and purchase orders?	YES/NO
40.11.7	Are quality control personnel part of the pre-award survey to ensure that ESD controls are implemented by:	
(a)	Contractors?	YES/NO
(b)	Subcontractors?	YES/NO
(c)	Suppliers?	YES/NO
40.11.8	Do quality control personnel perform audits of all in-house ESD protected work areas?	YES/NO
(a)	Are records available from these audits?	YES/NO
40.11.9	To ensure that a reliable ESD control program is maintained, do quality control personnel perform periodic audits of all:	
(a)	Contractors?	YES/NO
(b)	Subcontractors?	YES/NO
(c)	Suppliers?	YES/NO
40.11.10	Do quality control personnel review all drawings and procedures to ensure proper ESD precautionary measures are included?	YES/NO
40.11.11	Do quality control personnel ensure that all ESD failures are maintained in a data bank and that data on causes, trends, and corrective actions are maintained?	YES/NO

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APPENDIX L

BIBLIOGRAPHY

10. SCOPE

10.1 Scope. The following list of reference documents has been used in the preparation of this handbook. Additionally, other documents are included which are recommended for further information relating to electrostatics, electrostatic discharge, and electrostatic discharge damage prevention. Due to the wide range of topics covered in each of these documents all documents are listed alphabetically rather than by subject categorization. This appendix is not a mandatory part of the handbook. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. INFORMATION SOURCES

Amerasekera, E.A., and Campbell, D.S., "An Investigation of the Nature and Mechanisms of ESD Damage in NMOS Transistors", Solid State Electronics, Vol. 32 No. 3, 1989;

Bhar, T.N., "Monitoring ESD in the Production Workplace", Electronic Packaging and Production, June 1990;

Bhar, T.N. and McMahon, E., "Electrostatic Discharge Control", Hayden Book Co., 1983;

Bhatti, I.S., Fuller, E., and Jo., F.B., "VMOS Electrostatic Protection", IEEE Proceedings, 16th Annual Reliability Physics, 1978;

Boxleitner, W., "Electrostatic Discharge and Electronic Equipment", IEEE Press, 1989;

Boxleitner, W., "How to Defeat Electrostatic Discharge", IEEE Spectrum, August 1989;

Brown, W.O., "Semiconductor Device Degradation by High Amplitude Current Pulses", IEEE Transactions Nuc. Sci. Vol. NS-19 No. 6, December 1972;

Chen, K.L., "The Effects of Interconnect Process and Snapback Voltage on ESD Failure Threshold of NMOS Transistors, IEEE Trans. on Electron Devices, Vol. 35 No. 12, 1988;

Source: https://assist.dla.mil -- Downloaded: 2017-02-09T05:49Z
Check the source to verify that this is the current version before use.

Chen, K.L., Giles, G., and Scott, B., "Electrostatic Discharge Protection for One Micron CMOS Devices and Circuits", IEDM Digest, 1986;

Clark, O.M., "Transient Voltage", Quality, September 1989;

"Distributor Requirements for Handling Electrostatic-Discharge Sensitive (ESDS) Devices", JEDEC Solid State Products Engineering Council, November 1985;

Dobson, J.J., and Doyle, E.A., "RADC FFRP, Its Impact on System Operational Readiness and Reliability", Government Microcircuit Applications Conference Proceedings, 1990;

Dorcas, D.S. and Scott, R.N., "Instrumentation for Measuring the dc Conductivity of Very High Resistivity Materials", The Review of Scientific Instruments,, Vol. 35, No. 9 Canada, September 1964;

Duvvury, C., et. al., "Internal Chip ESD Phenomena Beyond the Protection Circuit", Proc. IRPS, 1988;

Dylis, D.D., and Ebel, G.H., "The DoD Microcircuit Field Failure Return Program", Institute of Environmental Sciences Proceedings, 1990;

Dylis, D.D., and Ebel, G.H., "Field Failure Return Program, The Missing Link", Institute of Environmental Sciences Proceedings, 1990;

Dylis, D.D., "A Review of the Field Failure Return Program", Government Microcircuit Applications Conference Proceedings, 1990;

Dylis, D.D., "Selected Case Histories from the DoD Field Failure Return Program", International Society of Testing and Failure Analysis Proceedings, 1992;

Dylis, D.D., "Organization and Operation of the DoD Field Failure Return Program", Government Microcircuit Applications Conference Proceedings, 1992

Dylis, D.D., "Field Failure Return Program (FFRP) Final Report", Reliability Analysis Center, RL-TR-93-155, June, 1993;

Ebel, G.H., "Long Term Failure Mechanisms of Microcircuits", Government Microcircuit Applications Conference Proceedings, 1990;

Ebel, G.H., "Practical Statistical Process Control Tools for Predictive Technology", Predictive Technology Symposium Proceedings, 1991;

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-1, Reliability Analysis Center, 1979;

Source: https://assist.dla.mil -- Downloaded: 2017-02-09T05:49Z
Check the source to verify that this is the current version before use.

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-2, Reliability Analysis Center, 1980;

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-3, Reliability Analysis Center, 1981;

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-4, Reliability Analysis Center, 1982;

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-5, Reliability Analysis Center, 1983;

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-6, EOS/ESD Association, Inc., 1984;

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-7, EOS/ESD Association, Inc., 1985;

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-8, EOS/ESD Association, Inc., 1986;

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-9, EOS/ESD Association, Inc., 1987;

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-10, EOS/ESD Association, Inc., 1988;

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-11, EOS/ESD Association, Inc., 1989;

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-12, EOS/ESD Association, Inc., 1990;

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-13, EOS/ESD Association, Inc., 1991;

"Electrical Overstress/Electrostatic Discharge Symposium Proceedings", EOS-14, EOS/ESD Association, Inc., 1992;

"Electromagnetic Compatibility for Aircraft Electrical and Electronic Equipment", North Atlantic Treaty Organization, Military Agency For Standardization, STANAG NO. 3516, undated;

"Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment, Part 2: Electrostatic Discharge Requirements", International Electrotechnical Commission, IEC Standard, Publication 801-2, 1984;

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Check the source to verify that this is the current version before use.

"Electromagnetic Fields Radiated from Electrostatic Discharges Theory and Experiment", Department of Commerce/National Bureau of Standards, NBS Technical Note 1314, February 1988;

"Electrostatic Control for Cleanroom Applications", Working Group -022, IES Recommended Practice, Institute of Environmental Sciences, IES-WG-022 draft, undated;

"Electrostatic Discharge (ESD) Control Information Manual, Volume 1 and Volume 2, National Aeronautics and Space Administration, D-TM-82-1A, undated;

"Electrostatic Discharge Immunity Testing of Information Technology Equipment", European Computer Manufacturers Association, TR/40, July, 1987;

Electrostatic Discharge Susceptibility Data 1991, Reliability Analysis Center, Catalog Number, VZAP-91, 1991;

EOS/ESD Standard S3.1-1991, "Ionization", EOS/ESD Association, Inc., June 1991;

EOS/ESD Standard S4.1-1990 "Work Surfaces-Resistive Characterization", EOS/ESD Association, Inc., April 1990;

EOS/ESD Standard S5.1-1991, "Human Body Model (HBM) Electrostatic Discharge Sensitivity Testing", EOS/ESD Association, Inc., June 1991;

EOS/ESD Draft Standard DS5.2-1992, "Machine Model (MM) Electrostatic Discharge Sensitivity Testing", EOS/ESD Association, Inc., 1992;

EOS/ESD Standard S6.1-1991, "Grounding-Recommended Practice", EOS/ESD Association, Inc., September 1991;

EOS/ESD Draft Standard DS7.1-1992, "Floor Materials-Resistive Characterization of Materials", EOS/ESD Association, Inc., September 1992;

EOS/ESD Standard S1.0-1987, "Wrist Straps", EOS/ESD Association, Inc., August 1987;

EOS/ESD Technology Abstracts, Reliability Analysis Center, Catalog Number TRS-3A, 1982;

ESD Protective Material and Equipment: A Critical Review, Reliability Analysis Center, Catalog Number SOAR-1, Spring 1982;

Farrell, J.P. and Ebel, G.H., "New Approaches to Microcircuit Quality and Reliability", National Aerospace & Electronics Conference Proceedings, 1990;

Source: https://assist.dla.mil -- Downloaded: 2017-02-09T05:49Z
Check the source to verify that this is the current version before use.

Freeman, E.R., and Beall, J.R., "Control Electrostatic Discharge Damage to Semiconductors", IEEE Proceedings, 12th Annual Reliability Physics Symposium, 1974;

Gallace, L.J. and Pujol, H.L., "The Evaluation of CMOS Static-Charge Protection Networks and Failure Mechanisms Associated with Overstress Conditions as Related to Device Life," IEEE Proceedings, Reliability Physics Symposium, 1977;

Gallace, L.J., and Pujol, H.L., "Reliability of CMOS Integrated Circuits", Computer Magazine, October 1978;

Green, T.J., "Getting the Facts from the Field... Real World Failure Data Collection and Analysis", Government Microcircuit Applications Conference Proceedings, 1987;

Green, T.J., "A Review of IC Fabrication, Design, and Assembly Defects Manifested as Field Failures in Air Force Avionics Equipment", International Reliability Physics Symposium Proceedings, 1988;

Green, T.J. and Denson, W.K., "A Review of EOS/ESD Field Failures in Military Equipment", Electrical Overstress/Electrical Static Discharge Symposium Proceedings, 1988;

Grimmet, C., "Removal of Conformal Coatings by Abrasive Blasting", GIDEP Document Summary Sheet R4-F-78-01, Hughes Aircraft Company, January 1978;

"Guidance for Electrostatic Sensitive Device Utilization and Protection", Aeronautical Radio, Inc., Supplement 1 to ARINC Report 606, March 28, 1988;

"Guide for Characterization of Electrostatic Discharge From Personnel and Mobile Furnishings", SPDC Working Group 3.6.8, Institute of Electrical and Electronics Engineers, Inc., draft, June 1, 1989;

Hickernell, F.S., and Crawford, J.J., "Voltage Breakdown Characteristics of Close Spaced Aluminum Arc Gap Structure on Oxidized Silicon", IEEE 15th Annual Reliability Physics Proceedings, 1977;

Hickernell, F.S., Klein, R.S., and Ware, M.R., "Arc Gap Input for CMOS LSI Circuitry", Proceedings of the 1976 GOMAC Conference, November, 1976;

Hickernell, F.S., "DC Voltage Effects on SAW Device Interdigital Electrodes", IEEE Proceedings of the 15th Annual Reliability Physics, 1977;

Himmel, R.P., "The Effect of Static Electricity on Thick Film Resistors", Insulation/Circuits Magazine, September 1972;

Source: https://assist.dla.mil -- Downloaded: 2017-02-09T05:49Z
Check the source to verify that this is the current version before use.

Ho, R., "Electrostatic Effects on Film Resistors", Insulation/Circuits, April 1971;

Horvath, T. and Berta, I., "Static Elimination", Research Studies Press, John Wiley and Sons Ltd., 1982;

Huang, C.L., et al, "Reliability Aspects of 0.5 mm and 1.0 mm Gate Low Noise GaAs FETs", IEEE Proceedings, 17th Annual Reliability Physics, 1979;

Jowett, C.E., "Static Electrification Hazards in Microelectronics Production", Microelectronics and Reliability, Vol. 13, 1974, Great Britain;

Kirk, Jr., W.J., Carter, L.S. and Waddel, M.L., "Eliminate Static Damage to Circuitry", Electronic Design, March 29, 1976;

Kroeger, J., "Heed the Limitations of MOS I/O Circuitry and You'll Avoid Electrostatic Damage to ICs and Eliminate Noise Problems and Excessive Power Dissipation", Electronic Design, May 10, 1974;

Lacy, E., "Protecting Electronic Equipment From Electrostatic Discharge", TAB Books Inc., 1984;

Leibowitz, M.R., "Introducing ESD Testing That Works", Test and Measurement World, May, 1989;

Lenzlinger, M., "Gate Protection of MIS Devices", IEEE Transactions on Electron Devices, Vol. ED-18, No. 4, April 1971;

Lin, D.L., Strauss, M.S., Welsher, T.L., "On the Validity of ESD Threshold Data Obtained Using Commercial Human-Body Model Simulators", 1987 IEEE International Symposium in Reliability Physics, 1987;

Linholm, W. and Plachy, F., "Electrostatic Gate Protection Using an ARC Gap Device", IEEE Proceedings, 11th Reliability Physics Symposium, 1973;

Lyons, D., "Protect Your MOS for Better Reliability", Quality, Management and Engineering, April 1973;

Madzy, T.M., "FET Circuit Destruction Caused by Electrostatic Discharge", IEEE Transactions on Electron Devices, September 1976;

McAteer, O.J., "Electrostatic Damage in Hybrid Assemblies", IEEE Proceedings of Annual Reliability and Maintainability Symposium, 1978;

McAteer, Owen J., "Shocking Blow to Military Electronics", Military Electronics/Countermeasures, June 1979;

Source: https://assist.dla.mil -- Downloaded: 2017-02-09T05:49Z
Check the source to verify that this is the current version before use.

Moore, A.D., "Electrostatics and its Applications", John Wiley and Sons, 1973;

Pakulsi, E.J. and Touw, T.R., "Electric Discharge Trimming of Glaze Resistors", Proceedings, Hybrid Microelectronics Symposium, 1968;

"Pan-Am Standard Analytical Method No. 6-703, Measurement of Electrostatic Potential Formation on Materials", GIDEP Report D83-D7182, NASA/KSC;

Pancholy, R.K., "Gate Protection for CMOS/SOS", IEEE Proceedings, 15th Annual Reliability Physics, 1977;

Rose, E., "Static Can Cause Bipolar IC Failures", Evaluation Engineering, May/June 1971;

Rountree, R.N. and Hutchins, C.L., "NMOS Protection Circuitry", IEEE Trans. Electron Devices, ED-32, 1985;

Scanlon, J.B., "An Overview of MIL-STD-1686A", EOS/ESD Technology, April/May 1989;

Scanlon, J.B., "MIL-STD-1686A Revisited", EOS/ESD Technology, April/May 1990;

Scanlon, J.B., "MIL-HDBK-263A: The New Handbook", EOS/ESD Technology, June/July 1991;

Schreier, L.A., "Electrostatic Damage Susceptibility of Semiconductor Devices", IEEE Proceedings, 16th Annual Reliability Symposium, April 1978;

Search and Retrieval Index to EOS/ESD Symposium Proceedings 1979 to 1984, Reliability Analysis Center, Catalog Number TRS-4, Spring 1985;

Search and Retrieval Index to EOS/ESD Symposium Proceedings 1979 to 1988, EOS/ESD Association, Inc., Catalog Number SRI-7988, 1989;

Smith, J.S., "Electrical Overstress Failure Analysis in Microcircuits", IEEE Proceedings, 16th Annual Reliability Physics, 1976;

Smith, J.S., "Electrical Overstress Failure Analysis in Microcircuits", International Reliability Physics Symposium, 1978;

Speakman, T.S., "A Model for the Failure of Bipolar Silicon Integrated Circuits Subjected to Electrostatic Discharge", International Reliability Physics Symposium Proceedings, 1974;

Source: https://assist.dla.mil -- Downloaded: 2017-02-09T05:49Z
Check the source to verify that this is the current version before use.

Speakman, T.S., "A Model for the Failure of Bipolar Silicon Integrated Circuits Subjected to Electrostatic Discharge", IEEE International Symposium on EMC, 1987;

Stegmaier, R.W., "RADC Field Failure Return Program (FFRP), An Overview", Government Microcircuit Applications Conference Proceedings, 1990;

Stapper, C.H., F.M. Armstrong and K. Saji, "Integrated Circuit Yield Statistics", Proceedings of the IEEE, Vol. 71, No. 4, April 1983;

State of the Art Report, ESD Control in the Manufacturing Environment, Reliability Analysis Center, Catalog Number SOAR-6, Summer 1986;

Tasca, D.M., "Pulse Power Failure Modes in Semiconductors", IEEE Transactions on Nuclear Science, Vol. NS-15, No.6;

Technical Support Package, "Safe Handling Practices for Electrostatic Sensitive Devices", NASA Tech Briefs, Vol. 2, No.3, MSC-16642, Fall 1977.

Tolliver, D., and Schroeder, H.G., "Particle Control in Semiconductor Process Streams", Microcontamination Magazine, June/July 1983.

"Triboelectric Testing", Final Report, Reliability Analysis Center, Rome Air Development Center, RAC-TR-83-03-E01, August 15, 1983;

Trigonis, A.C., "Electrostatic Discharge in Microcircuits", IEEE Proceedings, Reliability and Maintainability Symposium, 1976.

Welsher, T.L., "Electrostatic Discharge Sensitivity Testing of Integrated Circuits", Proceedings IEEE Southcon/89, IEEE, Atlanta, GA, 1989;

Woods, M.N. and Gear, G. "A New Electrostatic Discharge Failure Mode", IEEE Proceedings, 16th Annual Reliability Physics Symposium, April 1978;

Wunsch, D.C. and Bell, R.R., "Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors Due to Pulse Voltages", IEEE Transactions N5-15, No. 6, December 1968.

Wunsch, D.C., "The Application of Electrical Overstress Models to Gate Protective Networks", IEEE 16th Annual Proceedings, Reliability Physics, 1978;

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I RECOMMEND A CHANGE:	1. DOCUMENT NUMBER MIL-HDBK-263B	2. DOCUMENT DATE (YYMMDD) 940731

3. DOCUMENT TITLE

ELECTROSTATIC DISCHARGE CONTROL HANDBOOK FOR PROTECTION OF ELECTRICAL AND ELECTRONIC PARTS, ASSEMBLIES AND EQUIPMENT (EXCLUDING ELECTRICALLY INITIATED EXPLOSIVE DEVICES) (METRIC)

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