The documentation and process conversion measures necessary to comply with this revision shall be completed by 30 June 2016.

INCH-POUND

MIL-PRF-19500/543P
30 March 2016
SUPERSEDING
MIL-PRF-19500/543N
29 March 2013

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, FIELD EFFECT, N-CHANNEL, SILICON
REPETITIVE AVALANCHE, ENCAPSULATED (THROUGH-HOLE PACKAGES) AND
UN-ENCAPSULATED (DIE), TYPES 2N6764, 2N6766, 2N6768,
2N6770, AND JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for N-channel, enhancement-mode, MOSFET, power transistors. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each encapsulated device. Two levels of product assurance (JANHC and JANKC) are provided for each unencapsulated die, with avalanche energy ratings (E_{AS} and E_{AR}) and maximum avalanche current (I_{AR}).

1.2 Physical dimensions. See figure 1 (TO-204AE for types 2N6764 and 2N6766; TO-204AA for types 2N6768 and 2N6770 (formerly TO-3)), see figure 2 (TO-254AA for types 2N6764T1, 2N6766T1; 2N6768T1, and 2N6770T1), and figures 3, 4, and 5 for JANHC and JANKC (die) dimensions.

1.3 Maximum ratings. (T_A = +25°C, unless otherwise specified).

Type	P_T (1) T_C = +25°C	P_T T_A = +25°C	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) T_C = +25°C	I_S	I_{D2} (3) (4) T_C = +100°C
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc
2N6764, 2N6764T1	150	4	0.83	100	100	±20	38.0	38.0	24.0
2N6766, 2N6766T1	150	4	0.83	200	200	±20	30.0	30.0	19.0
2N6768, 2N6768T1	150	4	0.83	400	400	±20	14.0	14.0	9.0
2N6770, 2N6770T1	150	4	0.83	500	500	±20	12.0	12.0	7.75

(1) Derate linearly 1.2 W/°C for T_C > +25°C.
(2) See figure 6, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D limit. I_D is also limited by package and internal wires:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) x (R_{DS}(on) at T_{JM})}}$$

(4) See figure 7, maximum drain current graphs.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

* 1.3 Maximum ratings - Continued.

Type	I_{DM} (5)	E_{AS}	E_{AR}	I_{AR} (5)	V_{ISO} 70,000 ft. attitude	T_{STG} and T_J	Max $r_{DS(on)}$; (6) V_{GS} = 10 V dc, I_D = I_{D2}	
							T_J = +25°C	T_J = +150°C
	A pk	mJ	mJ	A		°C	Ω	Ω
2N6764, 2N6764T1	152	150	15	38.0		-55	0.055	0.105
2N6766, 2N6766T1	120	500	15	30.0		to	0.085	0.170
2N6768, 2N6768T1	56	11.3	15	14.0	400	+150	0.300	0.750
2N6770, 2N6770T1	48	8.0	15	12.0	500		0.400	1.000

(5) I_{DM} = 4 x I_{D1} as calculated in note 3.
(6) Pulsed (see 4.5.1).

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0mA dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ I_D = 0.25 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS}
		V dc		
	V dc	Min	Max	µA dc
2N6764, 2N6764T1	100	2.0	4.0	25
2N6766, 2N6766T1	200	2.0	4.0	25
2N6768, 2N6768T1	400	2.0	4.0	25
2N6770, 2N6770T1	500	2.0	4.0	25

(1) Pulsed (see 4.5.1).

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: “JAN”, “JANTX”, “JANTXV” and "JANS".

* 1.5.2 JAN certification mark and quality level for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHC" and "JANKC".

* 1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

* 1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "6764", "6766", “6768”, and "6770".

* 1.5.3.3 Suffix letters. No suffix is used on devices that are packaged in the TO-204AA or TO-204AE package of figure 1. The suffix letters "T1" are used on devices that are packaged in the TO-254AA package of figure 2.

* 1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

* 1.5.5 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet are "A" and "B" (see figures 3, 4, and 5 and 6.5).

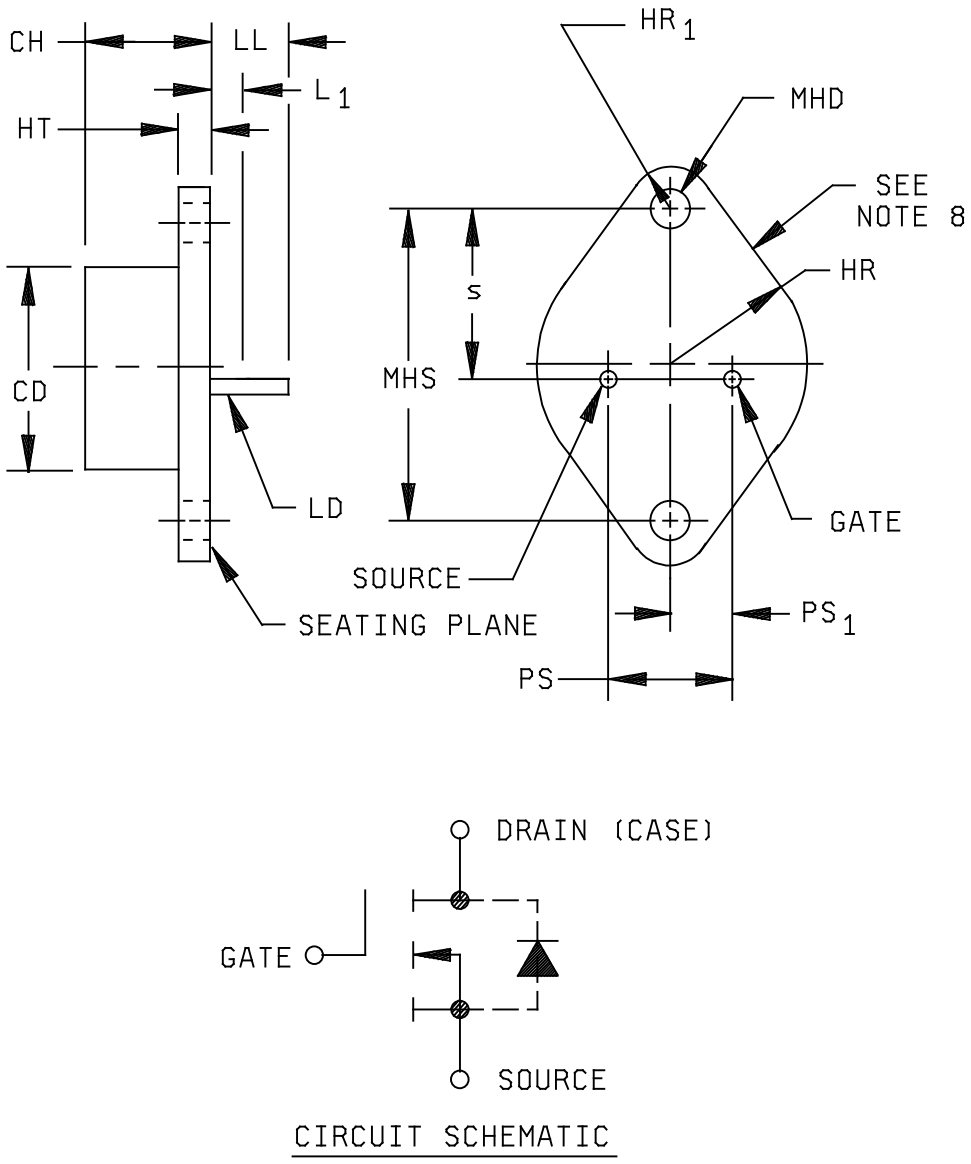
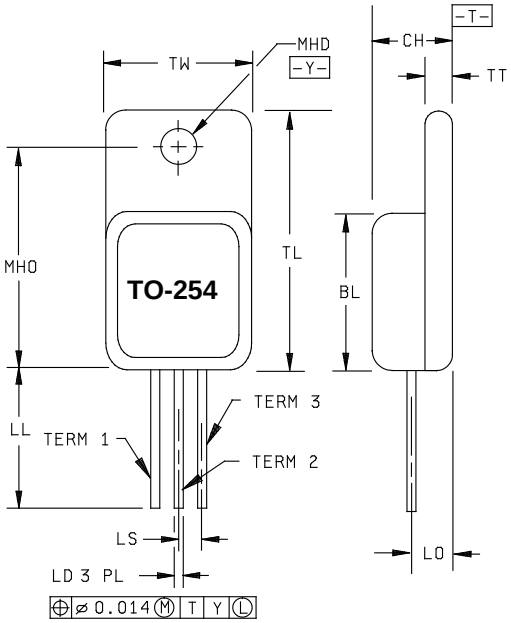


FIGURE 1. Physical dimensions of transistor types 2N6764 and 2N6766, TO-204AE; for types 2N6768 and 2N6770, TO-204AA.

Dimensions					
Ltr	Inches		Millimeter		Notes
	Min	Max	Min	Max	
CD		.875		22.23	
CH	.250	.360	6.35	9.15	
HR	.495	.525	12.57	13.3	
HR_1	.131	.188	3.33	4.78	
HT	.060	.135	1.52	3.43	
LD	.057	.063	1.45	1.60	5
	.038	.043	0.97	1.10	6
LL	.312	.500	7.92	12.70	
L_1		.050		1.27	3
MHD	.151	.165	3.84	4.19	7
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	
PS_1	.205	.225	5.21	5.72	
s	.655	.675	16.64	17.15	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. These dimensions shall be measured at points .050 inch (1.27 mm) and .055 inch (1.40 mm) below the seating plane. When gauge is not used, measurement will be made at the seating plane.
4. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
5. These dimensions pertain to the 2N6764 and 2N6766 types.
6. These dimensions pertain to the 2N6768 and 2N6770 types.
7. Mounting holes shall be deburred on the seating plane side.
8. Drain is electrically connected to the case.
9. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

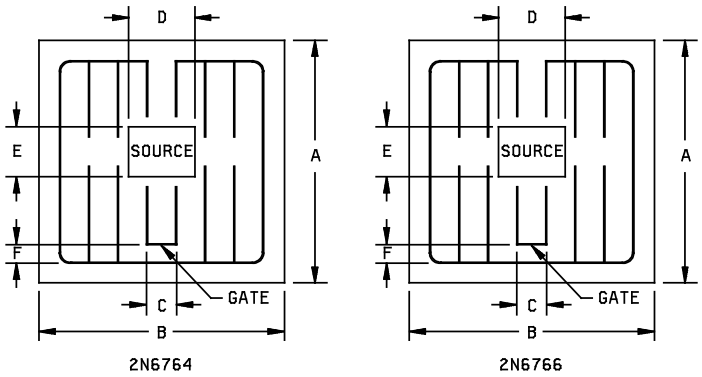
FIGURE 1. Physical dimensions of transistor types 2N6764 and 2N6766 TO-204AE; for types 2N6768 and 2N6770, TO-204AA - Continued.

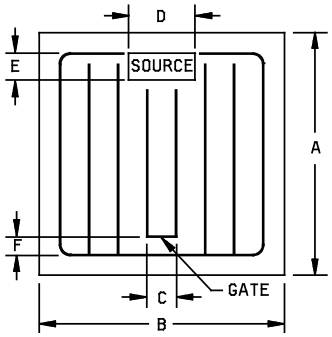


Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
CH	.249	.260	6.32	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.570	12.95	14.48	3, 4
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
MHD	.139	.149	3.53	3.78	
MHO	.665	.685	16.89	17.40	
TL	.790	.800	20.07	20.32	
TT	.040	.050	1.02	1.27	
TW	.535	.545	13.59	13.84	
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Protrusion thickness of ceramic eyelets included in dimension LL.
4. All terminals are isolated from case.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions for 2N6764T1, 2N6766T1, 2N6768T1, and 2N6770T1 (TO-254AA).



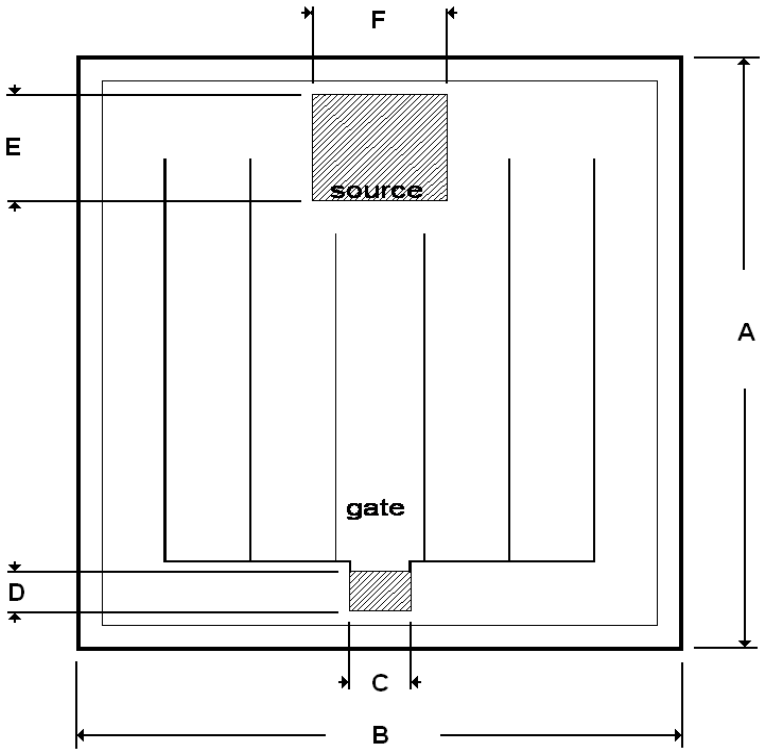


Ltr	Dimensions 2N6764 and 2N6766				Dimensions 2N6768 and 2N6770			
	Inches		Millimeters		Inches		Millimeters	
	Min	Max	Min	Max	Min	Max	Min	Max
A	.252	.262	6.40	6.65	.252	.262	6.40	6.65
B	.252	.262	6.40	6.65	.252	.262	6.40	6.65
C	.027	.037	0.69	0.94	.025	.035	0.64	0.89
D	.012	.022	0.30	0.56	.043	.053	1.09	1.35
E	.057	.067	1.45	1.70	.032	.042	0.81	1.07
F	.013	.023	0.33	0.58	.015	.025	0.38	0.64

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is ± .005 inch (0.13 mm).
4. The physical characteristics of the die thickness are .0187 inch (0.474 mm). The back metals are chromium, nickel and silver. The top metal is aluminum and the back contact is the drain.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 3. JANHC and JANKC A-version die dimensions.

2N6764 and 2N6766

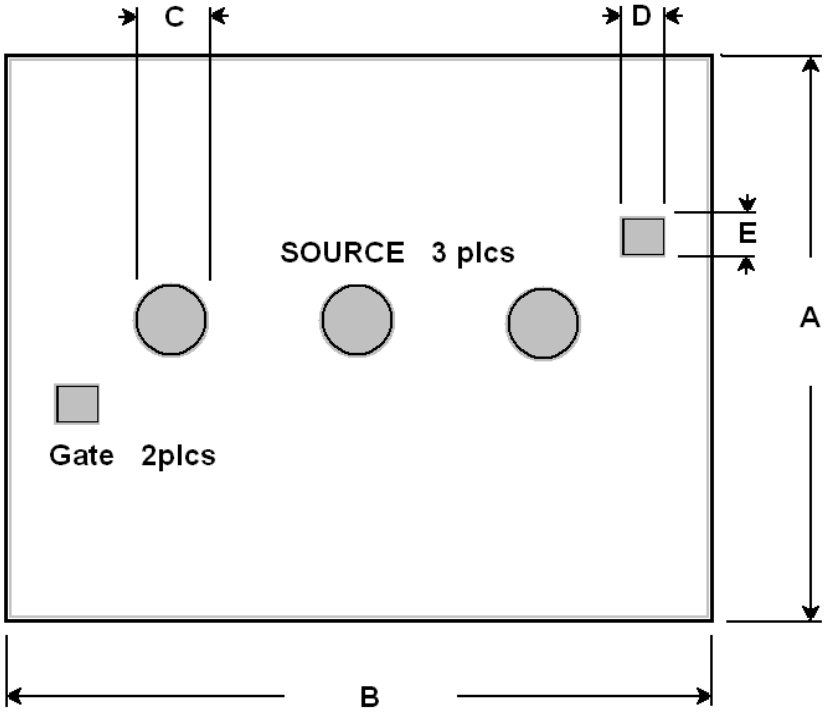


Ltr	Dimensions - 2N6764 and 2N6766			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.254	.260	6.45	6.60
B	.254	.260	6.45	6.60
C	.028	.033	.71	.82
D	.017	.022	.43	.56
E	.047	.053	1.19	1.35
F	.059	.065	1.50	1.65

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 inch (0.13 mm).
4. The physical characteristics of the die are: The back metals are chromium, nickel, and silver and the back contact is the drain. The top metal is aluminum.
5. Die thickness is .015 inch (0.38 mm) ±.001 inch (0.025 mm).

FIGURE 4. JANHCB and JANKCB (B-version) die dimensions for 2N6764 and 2N6766.

2N6768 and 2N6770



Ltr	Dimensions - 2N6768 and 2N6770			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.247	.253	6.27	6.43
B	.287	.293	7.29	7.44
C	.033	.037	.84	.94
D	.016	.020	.41	.51
E	.017	.021	.43	.53

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 inch (0.13 mm).
4. The physical characteristics of the die are: The back metals are chromium, nickel, and silver and the back contact is the drain. The top metal is aluminum.
5. Die thickness is .018 inch (0.46 mm) ±.001 inch (0.025 mm).

FIGURE 5 . JANHCB and JANKCB (B-version) die dimensions for 2N6768 and 2N6770.

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

I_{AS} - Rated avalanche current, nonrepetitive
nC - nano Coulomb
Zthjc – Junction to case transient thermal impedance.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1, 2, 3, 4, and 5.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Internal construction. Multiple chip construction is not permitted to meet the requirements of this specification.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static discharge. The following handling practices are recommended (see 3.6).

a. Devices shall be handled on benches with conductive and grounded surface.

b. Ground test equipment, tools and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care shall be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate shall be terminated to source, $R \leq 100\ k\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.8 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and table I).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANHC and JANKC devices. Qualification for JANHC and JANKC devices shall be as specified in MIL-PRF-19500.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANS, JANTXV and JANTX levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS	JANTX and JANTXV
(3)	Gate stress test (see 4.3.2).	Gate stress test (see 4.3.2).
(3) (4)	Method 3470 of MIL-STD-750, E_{AS} test (see 4.3.3).	Method 3470 of MIL-STD-750, E_{AS} test (see 4.3.3).
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.4).	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.4).
9	I_{GSSF1}, I_{GSSR1}, I_{DSS1}.	Not applicable.
10	Method 1042 of MIL-STD-750, test condition B.	Method 1042 of MIL-STD-750, test condition B.
11	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$, of subgroup 2 of table I herein. ΔI_{GSSF1} = +20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = -20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 µA dc or ±100 percent of initial value, whichever is greater.	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$, of Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A.	Method 1042 of MIL-STD-750, test condition A.
13	Subgroups 2 and 3 of table I herein; ΔI_{GSSF1} = +20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = -20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 µA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.	Subgroup 2 of table I herein; ΔI_{GSSF1} = +20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = -20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 µA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.
17	For TO-254AA packages: Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein.	For TO-254AA packages: Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1} and $V_{GS(th)1}$ shall be invoked.
(3) Shall be performed anytime after temperature cycling, screen 3a. JANTX and JANTXV levels do not need to be repeated in screening requirements.
(4) This test method in no way implies a repetitive avalanche energy rating.

4.3.1 Screening (JANHC and JANKC). Screening of JANHC and JANKC shall be in accordance with appendix G of MIL-PRF-19500. As a minimum, die shall be 100 percent probed in accordance with table I, subgroup 2 except test current shall not exceed 20 A.

4.3.2 Gate stress test. Apply V_{GS} = 30 V minimum for t = 250 µs minimum.

4.3.3 Single pulsed unclamped inductive switching.

a. Peak current .....I_{D1}.

b. Peak gate voltage, V_{GS} .....10 V.

c. Gate to source resistor, R_{GS} .....$25 \leq R_g \leq 200$ ohms.

d. Initial case temperature .....+25°C, +10°C, -5°C.

e. Inductance, L ..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{(V_{BR}-V_{DD})}{V_{BR}}\right]$ mH minimum.

f. Number of pulses to be applied .....1 pulse minimum.

g. Supply voltage (V_{DD}).....50 V, (25 V for devices with minimum $V_{(BR)DSS}$ of 100 V).

* 4.3.4 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). See table II, group E, subgroup 4 herein.

4.3.5 Dielectric withstanding voltage.

a. Magnitude of test voltage……900 V dc.

b. Duration of application of test voltage……..15 seconds (min).

c. Points of application of test voltage……All leads to case (bunch connection).

d. Method of connection……Mechanical.

e. Kilovolt-ampere rating of high voltage source……..1,200 V/1.0 mA (min).

f. Maximum leakage current……1.0 mA.

g. Voltage ramp up time……500 V/second.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

* 4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and as follows.

* 4.4.2.1 Quality level JANS (see table E-VIA of MIL-PRF-19500).

Subgroup	Method	Conditions
B3	1051	Test condition G.
B4	1042	Test condition D; the heating cycle shall be 1 minute minimum.
B5	1042	Test condition A; V_{DS} = rated V_{DS} (see 1.3), T_A = +175° C, t = 120 hours minimum, read and record $V_{BR(DSS)}$ (pre and post) at I_D = 1 mA, read and record I_{DSS} (pre and post), (see table I).
B5	1042	Test condition B; V_{GS} = rated V_{GS} (see 1.3), T_A = +175° C, t = 24 hours minimum.

* 4.4.2.2 Quality levels JAN, JANTX and JANTXV, (see table E-VIB of MIL-PRF-19500).

Subgroup	Method	Conditions
B2	1051	Test condition G.
* B3	1042	Test condition D. The heating cycle shall be 1 minute minimum.
B5		Not applicable.
B6		Not applicable

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in, table E-VII of MIL-PRF-19500.

Subgroup	Method	Conditions
* C2	2036	Test condition A; for 2N6764, 2N6766, 2N6768, and 2N6770, weight = 10 lbs (4.5 kg), t = 15 seconds; for T1 devices, weight = 9.9 lbs (4.5 kg), t = 10 seconds.
C5	3161	See 4.3.4, $R_{\theta JC}$ max = 0.83° C /W.
* C6	1042	Test condition D; The heating cycle shall be 1 minute minimum.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 3/	3161	See 4.3.4	$Z_{\theta JX}$			°C/W
Breakdown voltage, drain to source	3407	V_{GS} = 0; I_D = 1 mA dc, bias condition C	$V_{(BR)DSS}$			
2N6764				100		V dc
2N6766				200		V dc
2N6768				400		V dc
2N6770				500		V dc
Gate to source voltage (threshold)	3404	$V_{DS} \geq V_{GS}$; I_D = 0.25 mA dc	$V_{GS(th)1}$	2.0	4.0	V dc
Gate current	3411	V_{GS} = +20 V dc, bias condition C, V_{DS} = 0	I_{GSSF1}		+100	nA dc
Gate current	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0	I_{GSSR1}		-100	nA dc
Drain current	3413	V_{GS} = 0; V_{DS} = 80 percent of rated V_{DS}, bias condition C	I_{DSS1}		25	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 10 V dc, pulsed (see 4.5.1), condition A, I_D = rated I_{D2} (see 1.3), T_C = +25° C.	$r_{DS}(on)1$			
2N6764					0.055	Ω
2N6766					0.085	Ω
2N6768					0.3	Ω
2N6770					0.4	Ω
Static drain to source on-state resistance	3421	V_{GS} = 10 V dc, pulsed (see 4.5.1), condition A, I_D = rated I_{D1} (see 1.3)	$r_{DS}(on)2$			
2N6764					0.065	Ω
2N6766					0.09	Ω
2N6768					0.4	Ω
2N6770					0.5	Ω
Forward voltage (source-drain diode)	4011	Pulsed (see 4.5.1) V_{GS} = 0 V, I_D = I_{D1}	V_{SD}			
2N6764					1.9	V dc
2N6766					1.9	V dc
2N6768					1.7	V dc
2N6770					1.7	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 3						
High temperature operation:		T_C = +125° C				
Gate current	3411	Bias condition C; V_{GS} = +20 and -20 V dc, V_{DS} = 0 V dc	I_{GSS2}		200	nA dc
Drain current	3413	Bias condition C; V_{GS} = 0 V dc				
		V_{DS} = 100 percent of rated V_{DS}	I_{DSS2}		1.0	mA dc
		V_{DS} = 80 percent of rated V_{DS}	I_{DSS3}		0.25	mA dc
Static drain to source on-state resistance	3421	V_{GS} = 10 V dc pulsed (see 4.5.1), I_D = rated I_{D2} (see 1.3)	$r_{DS}(on)3$			
2N6764					0.094	Ω
2N6766					0.153	Ω
2N6768					0.66	Ω
2N6770					0.88	Ω
Gate to source voltage (threshold)	3404	$V_{DS} \geq V_{GS}$; I_D = 0.25 mA dc	$V_{GS}(th)2$	1.0		V dc
Low temperature operation:		T_C = -55° C				
Gate to source voltage (threshold)	3404	$V_{DS} \geq V_{GS}$; I_D = 0.25 mA dc	$V_{GS}(th)3$		5.0	V dc
Subgroup 4						
Switching time test	3472	I_D = rated I_{D1} (see 1.3), V_{GS} = 10 V dc, gate drive impedance = 2.35 Ω, V_{DD} = 0.5 $V_{BR(DSS)}$				
Turn-on delay time			$t_{d(on)}$		35	ns
Rise time			t_r		190	ns
Turn-off delay time			$t_{d(off)}$		170	ns
Fall time			t_f		130	ns
Subgroup 5						
Safe operating area test	3474	See figure 8, V_{DS} = 80 percent of rated $V_{BR(DSS)}$, t_p = 10 ms, V_{DS} = 200 V max.				
Electrical measurements		Table I, subgroup 2 herein.				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

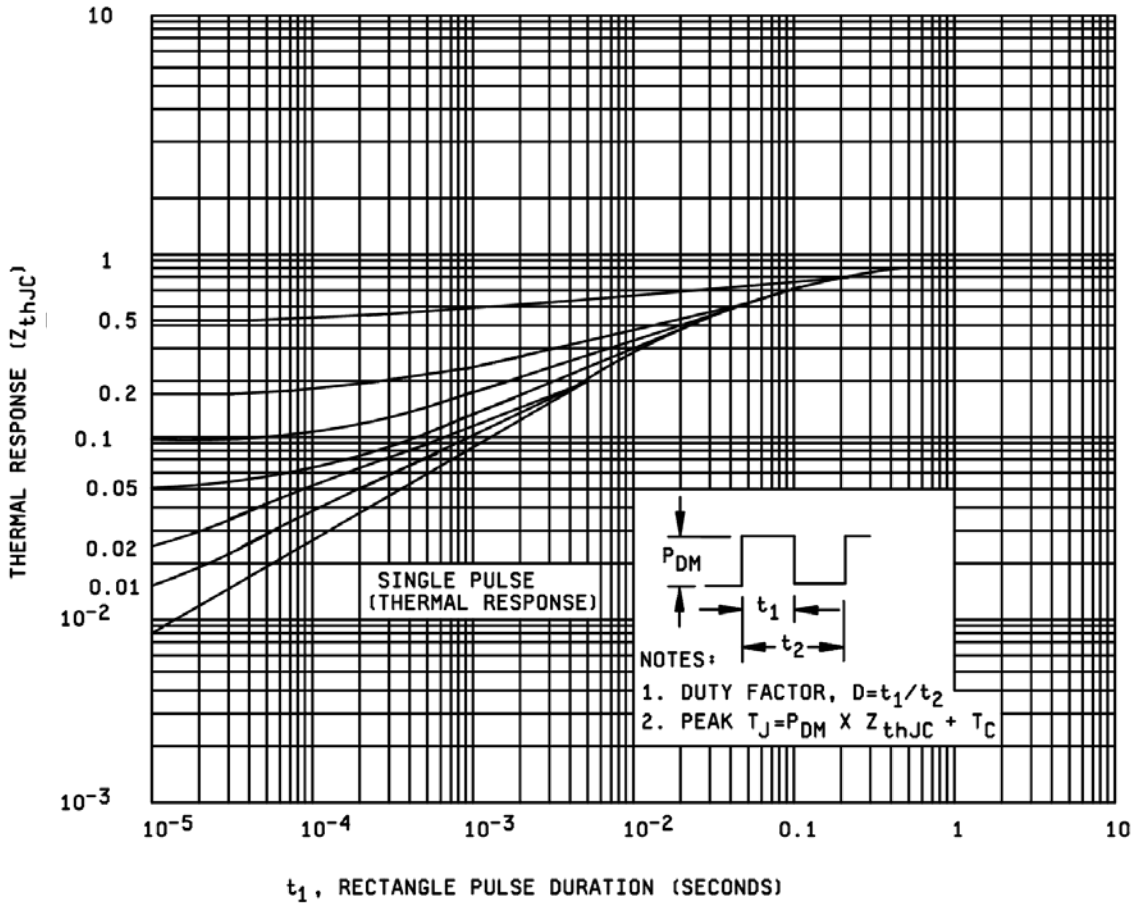
Inspection 1/ 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Bias condition B	$Q_g(on)$			
On-state gate charge						
2N6764					125	nC
2N6766					115	nC
2N6768					110	nC
2N6770					120	nC
Gate to source charge			Q_{gs}			
2N6764					22	nC
2N6766					22	nC
2N6768					18	nC
2N6770					19	nC
Gate to drain charge			Q_{gd}			
2N6764					65	nC
2N6766					60	nC
2N6768					65	nC
2N6770					70	nC
Reverse recovery time	3473	di/dt = 100 A/µs $V_{DD} \leq 30$ V dc, $I_D = I_{D1}$	t_{rr}			
2N6764					500	ns
2N6766					950	ns
2N6768					1,200	ns
2N6770					1,600	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ Unless otherwise specified, electrical characteristics for the T1 suffix devices are identical to the non T1 suffix devices.
3/ This test required for the following end-point measurements only:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JAN, JANTX, JANTXV).
Group C, subgroups 2 and 6.
Group E, subgroup 1.

TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

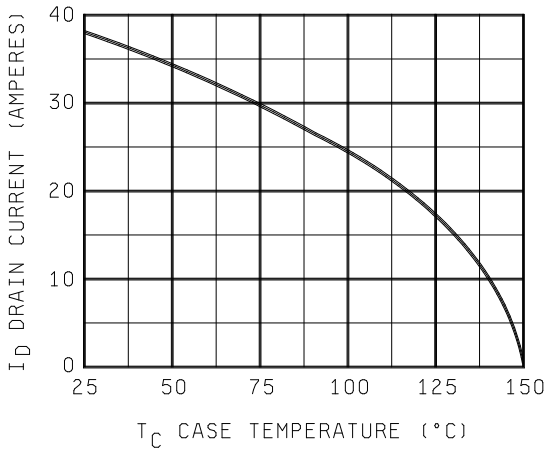
Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2	
Subgroup 2 1/			45 devices c = 0
Steady-state reverse bias	1042	Condition A; 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500	
Subgroup 5			15 devices c = 0
Barometric pressure (reduced) 400 V and 500 V devices only	1001	Test condition C; $I_{(ISO)}$ = .25 mA (max), $V_{(ISO)} = V_{DS}$	
Subgroup 8			5 devices c = 0
Repetitive avalanche energy	3469	$I_{AR} = I_D$; V_{GS} = 10 V; 2.5 ≤ R_{GS} ≤ 200 ohms; T_J = +150°C +10, -0 °C; inductance = $\left[\frac{2E_{AR}}{(I_{D1})^2}\right]\left[\frac{V_{BR}-V_{DD}}{V_{BR}}\right]$ $mH\,\min$ number of pulses to be applied = 3.6 X 10^8; (V_{DD}) = 50 V; time in avalanche = 2 μs minimum, 20 μs maximum; f = 1 KHz.	
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	

1/ A separate sample for each test shall be pulled.

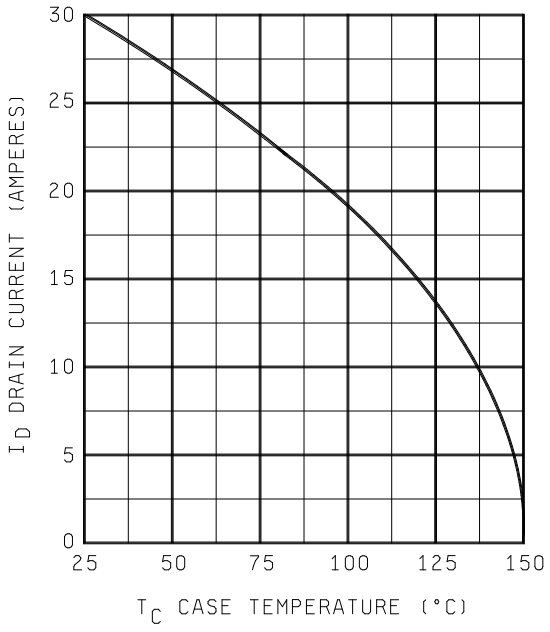


0

FIGURE 6. Thermal response curves.

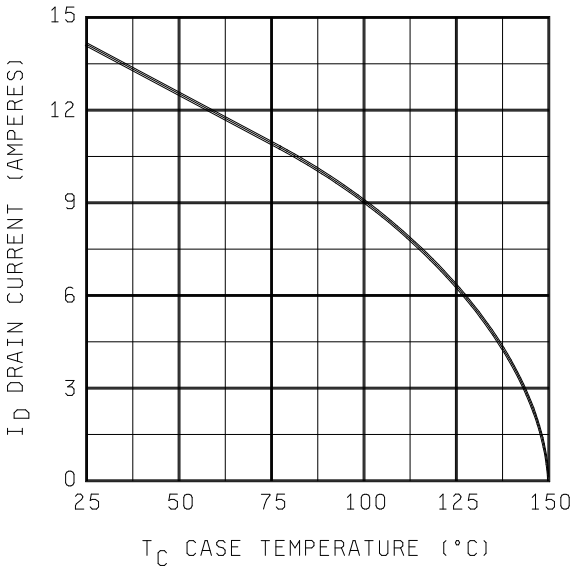


2N6764, 2N6764T1

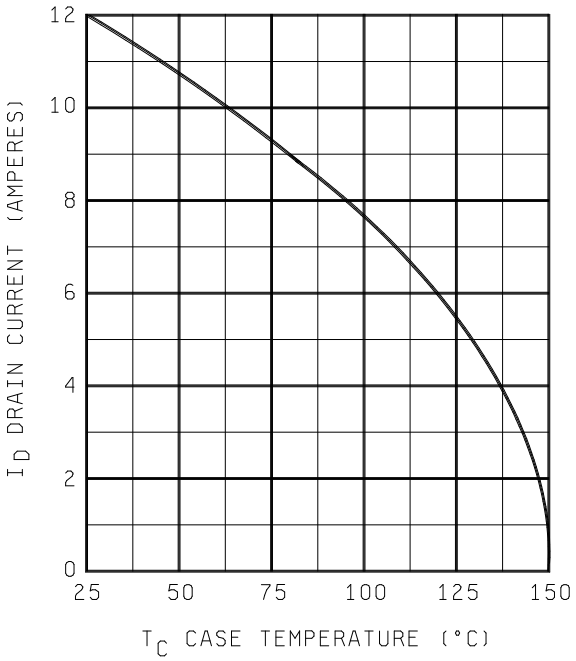


2N6766, 2N6766T1

FIGURE 7. Maximum drain current versus case temperature.

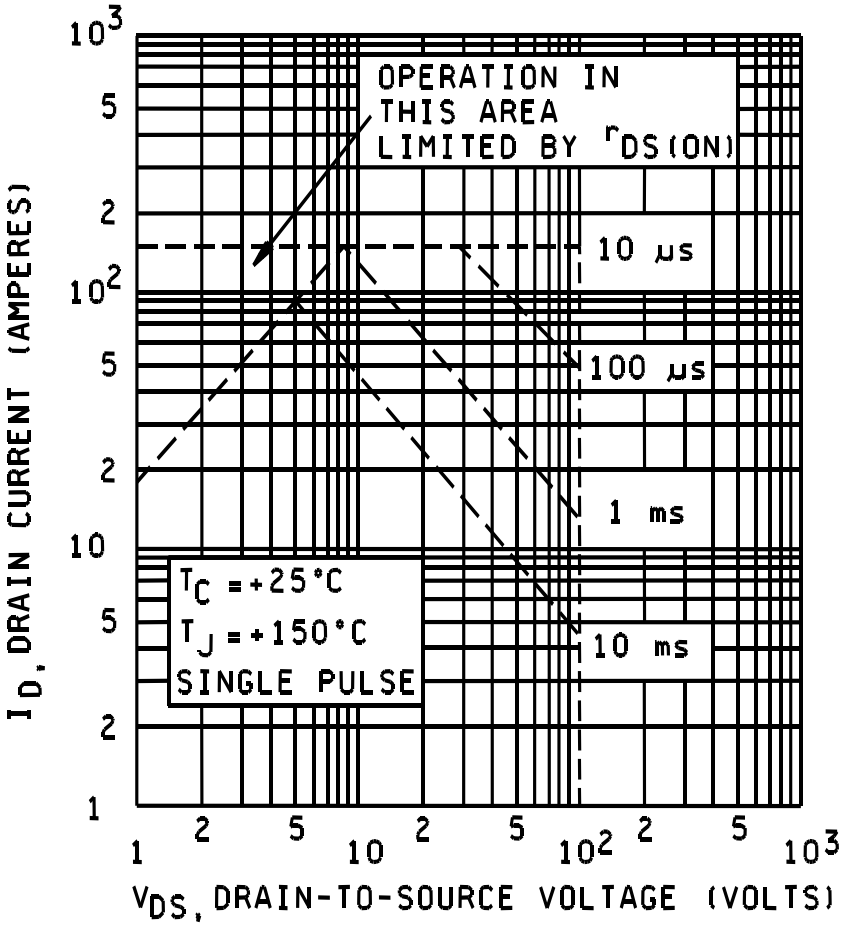


2N6768, 2N6768T1



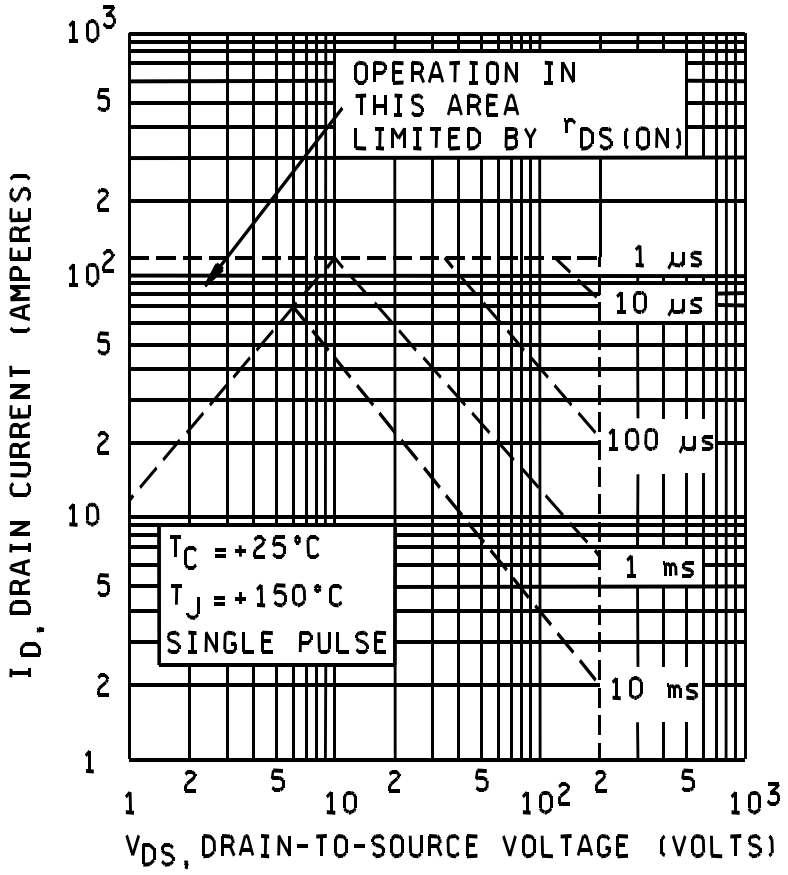
2N6770, 2N6770T1

FIGURE 7. Maximum drain current versus case temperature - Continued.



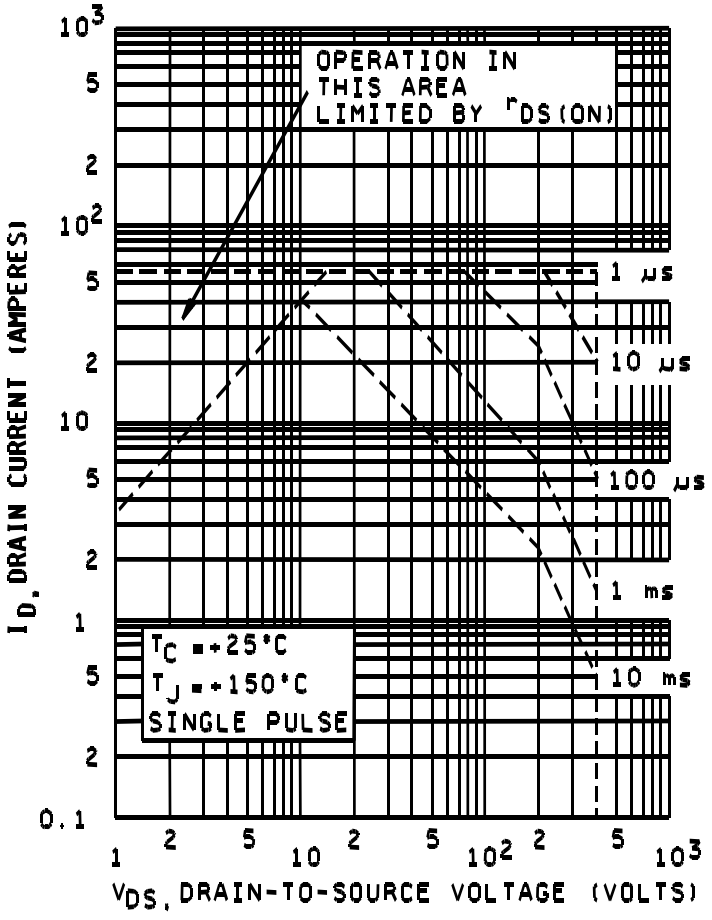
2N6764, 2N6764T1

FIGURE 8. Safe operating area graph.



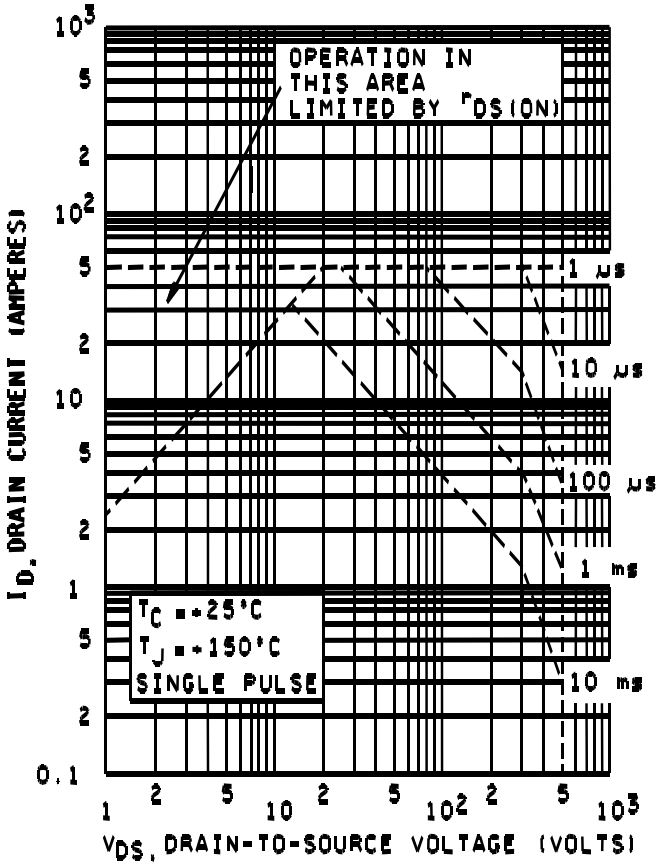
2N6766, 2N6766T1

FIGURE 8. Safe operating area graph - Continued.



2N6768, 2N6768T1

FIGURE 8. Safe operating area graph - Continued.



2N6770, 2N6770T1

FIGURE 8. Safe operating area graph - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead formation and finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.5.

e. For die acquisition, the JANHC or JANKC letter version shall be specified (see figures 3, 4 and 5).

f. Type designation and quality assurance level.

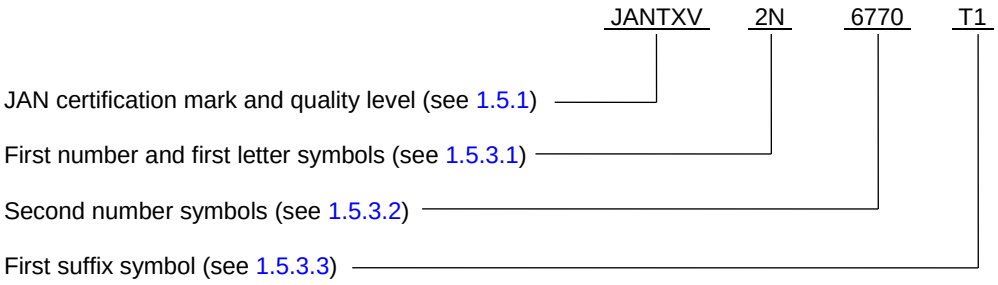
6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's PIN. This information in no way implies that manufacturer's PINs are suitable as a substitute for the military Part or Identifying Number (PIN).

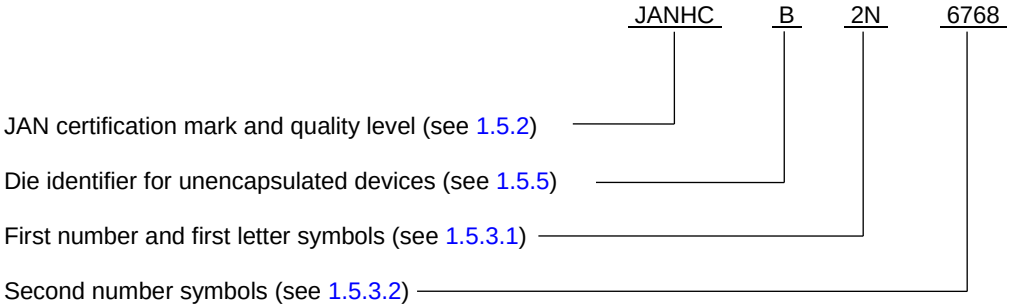
PIN	Manufacturer's CAGE code	Manufacturer's and user's PIN
2N6764	59993, 43611	IRF150, IRF151, IRF152, IRF153
2N6766	59993, 43611	IRF250, IRF251, IRF252, IRF253
2N6768	59993, 43611	IRF350, IRF351, IRF352, IRF353
2N6770	59993, 43611	IRF450, IRF451, IRF452, IRF453

* 6.5 PIN construction example.

* 6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



* 6.5.2 Unencapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



* 6.6 List of PINs.

* 6.6.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN2N6764	JANTX2N6764	JANTXV2N6764	JANS2N6764
JAN2N6764T1	JANTX2N6764T1	JANTXV2N6764T1	JANS2N6764T1
JAN2N6766	JANTX2N6766	JANTXV2N6766	JANS2N6766
JAN2N6766T1	JANTX2N6766T1	JANTXV2N6766T1	JANS2N6766T1
JAN2N6768	JANTX2N6768	JANTXV2N6768	JANS2N6768
JAN2N6768T1	JANTX2N6768T1	JANTXV2N6768T1	JANS2N6768T1
JAN2N6770	JANTX2N6770	JANTXV2N6770	JANS2N6770
JAN2N6770T1	JANTX2N6770T1	JANTXV2N6770T1	JANS2N6770T1

* 6.6.2 List of PINs for unencapsulated devices. The following is a list of possible PINs available on this specification sheet. The qualified JANC suppliers with the applicable letter version (example JANHCA2N6764) will be identified on the QML.

Die ordering information		
PIN	Manufacturer	
	59993	43611
2N6764	JANHCA2N6764 JANKCA2N6764	JANHCB2N6764 JANKCB2N6764
2N6766	JANHCA2N6766 JANKCA2N6766	JANHCB2N6766 JANKCB2N6766
2N6768	JANHCA2N6768 JANKCA2N6768	JANHCB2N6768 JANKCB2N6768
2N6770	JANHCA2N6770 JANKCA2N6770	JANHCB2N6770 JANKCB2N6770

* 6.6 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@.dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Army - AR, MI
Air Force - 19, 70, 99

Preparing activity:
DLA - CC

(Project 5961-2016-033)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil .