The documentation and process conversion measures necessary to comply with this revision shall be completed by 5 May 2010.

INCH-POUND

MIL-PRF-19500/731A
5 February 2010
SUPERSEDING
MIL-PRF-19500/731
26 March 2007

PERFORMANCE SPECIFICATION SHEET

* SEMICONDUCTOR DEVICE, DIODE, SILICON, SCHOTTKY, DUAL, CENTER TAP, TYPES 1N7058CCU3, 1N7058CCU3C, AND SINGLE DIE, TYPE 1N7038U3, JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist ofthis specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for silicon, Schottky dual and single power rectifier diodes for use in high frequency switching power supplies and resonant power converters. Four levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

* 1.2 Physical dimensions. See figure 1, U3 and U3C (with ceramic lid) package.

* 1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Column 1	Column 2	Column 3	Column 4	Column 5		Column 6
Types	V_{RWM}	I_O (1)(2) T_C = +100°C	I_{FSM} t_p = 8.3 ms T_C = +25°C	$R_{\Theta JC}$ (2)	$R_{\Theta JC}$ (3)	T_{STG} and T_J
	V dc	A dc	A (pk)	°C/W	°C/W	°C
1N7038U3	150	30	140 (2)	1.82		-65 to +150
1N7058CCU3 1N7058CCU3C	150	30	130 (2)	1.75	3.5	

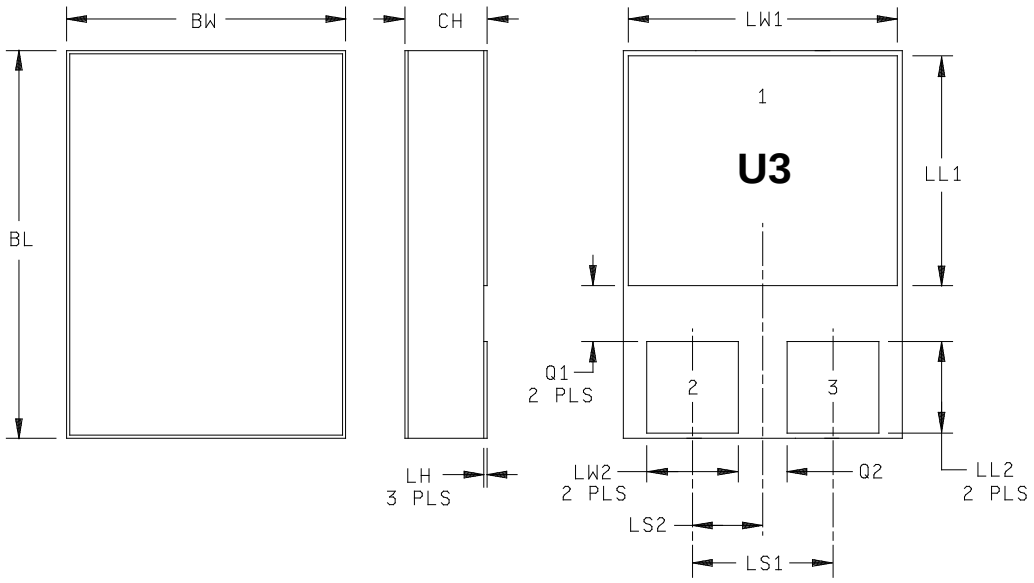
(1) See temperature-current derating curves in figures 2 and 3.
(2) Entire package.
(3) Each leg.

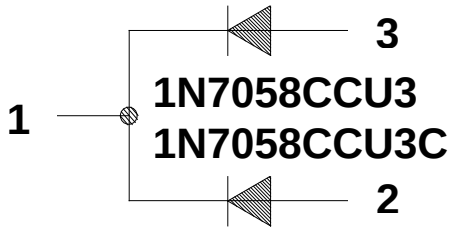
* 1.4 Primary electrical characteristics.

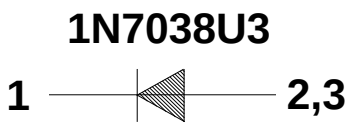
a. $R_{\Theta JC}$ = 1.82°C/W maximum for 1N7038U3 (figure 4).

b. $R_{\Theta JC}$ = 1.75°C/W maximum entire package for 1N7058CCU3 and 1N7058CCU3C (figure 5); $R_{\Theta JC}$ = 3.5°C/W maximum each leg.

Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to semiconductor@dscc.dla.mil . Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.daps.dla.mil .







Ltr	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.395	.405	10.03	10.29	
BW	.291	.301	7.39	7.65	
CH	.108	.122	2.74	3.12	U3 Only
CH	.1195	.1335	3.035	3.39	U3C Only
LH	.010	.020	0.25	0.51	
LL1	.220	.230	5.59	5.84	
LL2	.115	.125	2.92	3.18	
LS1	.150 BSC		3.81 BSC		
LS2	.075 BSC		1.91 BSC		
LW1	.281	.291	7.14	7.39	
LW2	.090	.100	2.29	2.54	
Q1	.030		0.76		
Q2	.030		0.76		

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimensions are in accordance with ASME Y14.5M.
4. Suffix “U3C” indicates a ceramic lid on package.

* FIGURE 1. Dimensions and configuration, 1N7038U3, 1N7058CCU3, and 1N7058CCU3C.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or https://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

* 2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 herein.

3.4.1 Polarity. Polarity and terminal configuration shall be in accordance with figure 1 herein.

3.4.2 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750 and herein. Where a choice of finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in tables I and II herein.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500 and herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II herein).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANS, JANTXV, and JANTX levels). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1)(2) 3b	Method 4066 of MIL-STD-750, condition A, one pulse, I_O = 0, V_{RWM} = 0, see 1.3 herein, column 4.	Method 4066 of MIL-STD-750, condition A, one pulse, I_O = 0, V_{RWM} = 0, see 1.3 herein, column 4.
(2) 3c	Thermal impedance (see 4.3.2)	Thermal impedance (see 4.3.2)
3d	Avalanche energy test (see 4.3.3)	Avalanche energy test (see 4.3.3)
9, 10	Not applicable	Not applicable
11	V_{F1} and I_{R1}	V_{F1} and I_{R1}
12	See 4.3.1	See 4.3.1
13	Subgroup 2 and 3, of table I herein, V_{F1} and I_{R1}, excluding thermal impedance; ΔV_{F1} = ±50 mV (pk); ΔI_{R1} = ±100 percent from the initial value or ±100uA, whichever is greater.	Subgroup 2, of table I herein excluding thermal impedance; V_{F1} and I_{R1}; ΔV_{F1} = ±50 mV (pk); ΔI_{R1} = ±100 percent from the initial value or ±100uA, whichever is greater.

(1) Surge shall precede thermal impedance.
(2) Thermal impedance and surge shall be performed any time after screen 3a and before screen 13.

* 4.3.1 Power burn-in conditions. Burn-in conditions are as follows: Method 1038 of MIL-STD-750, test condition A. V_R = 120 V dc; T_J = +125°C.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3101 or 4081 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD}. Measurement delay time (t_{MD}) = 70 μs max. See table III, subgroup 4 herein.

* 4.3.3 Avalanche energy test. The avalanche energy test is to be performed in accordance with method 4064 of MIL-STD-750 using the circuit as shown on figure 6 or equivalent. The Schottky rectifier under test must be capable of absorbing the reverse energy, as follows: I_{RM} = 170 mA, V_{RSM} = 150 V minimum, L = 150 mH.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500, and table I herein. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of table II herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in tables E-VIa (JANS) and E-VIb (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2, forward voltage test (V_{F1}) and reverse leakage test (I_{R1}) herein. Delta measurements shall be in accordance with table II herein.

* 4.4.2.1 Group B inspection, table E-VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B4	1037	ΔT_C = +85°C, I_F = 2 A minimum for 2,000 cycles.
B5	1038	Condition A, VR = 120 V dc, T_J = +125°C, t = 340 hours min; heat sinking allowed. This test shall be extended to 1000 on each JANS wafer lot.
B6	4081	Limit for thermal resistance for 1N7038U3 is 1.82°C/W. Limit for thermal resistance for 1N7058CCU3 is 3.5°C/W for each diode. Limit for thermal resistance for 1N7058CCU3C is 3.5°C/W for each diode.

* 4.4.2.2 Group B inspection, table E-VIb (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1037	ΔT_C = +85°C, I_F = 2 A minimum for 2,000 cycles.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2, forward voltage test (V_{F1}) and reverse leakage test (I_{R1}) herein. Delta measurements shall be in accordance with table II herein.

Subgroup	Method	Condition
C2	2036	Not required
C6	1037	ΔTC = +85°C, I_F = 2 A minimum for 6,000 cycles.
C6	1038	Condition A, VR = 120Vdc, T_J = +125°C, t = 1000 hours minimum; (heat sinking allowed), for TX, TXV only.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of MIL-PRF-19500, and table III herein. Delta measurements shall be in accordance with table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

* TABLE I. Group A inspection.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance	3101	See 4.3.2	$Z_{\Theta JC}$			°C/W
Forward voltage	4011	Pulsed test (see 4.5.1)	V_{F1}			
1N7038U3		I_F = 15A (pk)			.96	V dc
1N7058CCU3		I_F = 7.5A (pk)			1.05	V dc
1N7058CCU3C		I_F = 7.5A (pk)			1.05	V dc
Forward voltage	4011	Pulsed test (see 4.5.1)	V_{F2}			
1N7038U3		I_F = 30 A (pk)			1.18	V dc
1N7058CCU3		I_F = 15 A (pk)			1.20	V dc
1N7058CCU3C		I_F = 15 A (pk)			1.20	V dc
Reverse current	4016	DC method	I_{R1}			
1N7038U3		V_R = 150 V			.12	mA dc
1N7058CCU3		V_R = 150 V			.02	mA dc
1N7058CCU3C		V_R = 150 V			.02	mA dc
Subgroup 3						
High temperature operation:		T_C = +125 °C				
Forward voltage		Pulsed test (see 4.5.1)	V_{F3}			
1N7038U3		I_F = 15A (pk)			.75	V dc
1N7058CCU3		I_F = 7.5A (pk)			.72	V dc
1N7058CCU3C		I_F = 7.5A (pk)			.72	V dc
Forward voltage		Pulsed test (see 4.5.1)	V_{F4}			
1N7038U3		I_F = 30 A (pk)			.92	V dc
1N7058CCU3		I_F = 15 A (pk)			.85	V dc
1N7058CCU3C		I_F = 15 A (pk)			.85	V dc
Reverse current	4016	DC method;	I_{R2}			
1N7038U3		V_R = 150 V			6.0	mA dc
1N7058CCU3		V_R = 150 V			7.0	mA dc
1N7058CCU3C		V_R = 150 V			7.0	mA dc

See footnotes at end of table.

TABLE I. Group A inspection – Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 3 - continued						
Low temperature operation:		T_C = -55°C				
1N7038U3		I_F = 15A (pk)			1.07	V dc
1N7058CCU3		I_F = 7.5A (pk)			1.06	V dc
1N7058CCU3C		I_F = 7.5A (pk)			1.06	V dc
Forward voltage	4011	Pulsed test (see 4.5.1)	V_{F6}			
1N7038U3		I_F = 30 A (pk)			1.26	V dc
1N7058CCU3		I_F = 15 A (pk)			1.23	V dc
1N7058CCU3C		I_F = 15 A (pk)			1.23	V dc
Subgroup 4						
Junction capacitance	4001	V_R = 5 V dc, f = 1 MHz, V_{SIG} = 50 mV (p-p)	C_J			
1N7038U3					340	pF
1N7058CCU3					130	pF
1N7058CCU3C					130	pF
Subgroup 5						
Not applicable						
Subgroup 6						
Surge	4066	See 1.3, column 4 herein, ten surges each diode. 60 seconds between surges, (see 4.5.1).				
Electrical measurements		See table I, subgroup 2 herein.				
Subgroup 7						
Dielectric withstanding voltage 3/	1016	V_R = 500 V dc; all leads shorted; measure from leads to case.	DWV		10	µA
Scope display evaluation	4023	Stable only.				
Electrical measurements		See table I, subgroup 2 herein.				

1/ For sampling plan, see MIL-PRF-19500.
2/ Electrical characteristics apply to all package styles and polarities.
3/ Not required for 1N7058CCU3C.

* TABLE II. Groups B, C, and E delta requirements. 1/ 2/ 3/ 4/ 5/ 6/

Step	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1.	Forward voltage 1N7038U3 1N7058CCU3 1N7058CCU3C	4011	 I_F = 15 A (pk) pulsed (see 4.5.1) I_F = 7.5 A (pk) pulsed (see 4.5.1)	ΔV_{F1}	±50 mV dc from initial reading.		
2.	Reverse current	4016	V_R = 150V	ΔI_{R1}	±100 pecent from initial reading or ±100uA whichever is greater.		
3.	Thermal impedance	3101	See 4.3.2	$Z_{\Theta JX}$			

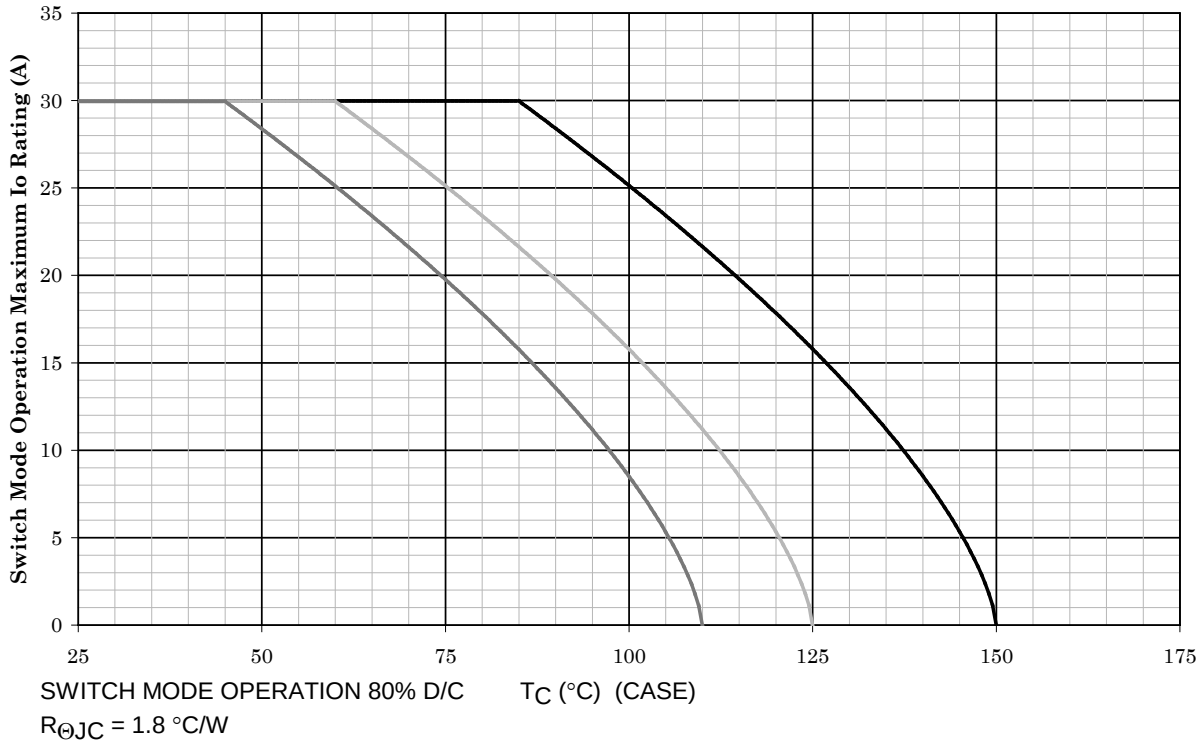
1/ Each individual diode.
2/ The electrical measurements for table E-VIa (JANS) of MIL-PRF-19500 are as follows:
   a. Subgroup 4, see table II herein, steps 1, 2, and 3.
   b. Subgroup 5, see table II herein, steps 1 and 2.
3/ The electrical measurements for table E-VIb (JANTX and JANTXV) of MIL-PRF-19500 are as follows:
   a. Subgroup 2, see table II herein, steps 1, 2, and 3.
   b. Subgroup 3, see table II herein, steps 1, 2, and 3.
   c. Subgroup 6, see table II herein, steps 1 and 2.
4/ The electrical measurements for table E-VII of MIL-PRF-19500 are as follows:
   a. Subgroups 2 and 3, see table II herein, steps 1, 2, and 3 for all levels.
   b. Subgroup 6, see table II herein, steps 1, 2, and 3 for all levels.
5/ Devices which exceed the table I limits for this test shall not be accepted.
6/ The electrical measurements for table E-IX of MIL-PRF-19500 are as follows:
   a. Subgroup 1, see table III herein, steps 1, 2, and 3.
   b. Subgroup 2, see table III herein, steps 1 and 2.

* TABLE III. Group E inspection (all quality levels) – for qualification and requalification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			n = 12, c = 0
Temperature cycling (air to air)	1051	Test condition G, 500 cycles, -55°C to +150°C.	
Hermetic seal	1071		
Electrical measurements		See table I, subgroup 2 and table II herein.	
Subgroup 2			n = 12, c = 0
Life test	1048	t = 1,000 hours, T_J = +125°C, V_R = 80 percent rated voltage (see 1.3, column 2 herein).	
Electrical measurements		See table I subgroup 2 and table II herein.	
Subgroup 4			
Thermal impedance curves	3101	See MIL-PRF-19500.	
Subgroup 6			n = 3
ESD	1020		
Subgroup 10 1/			n = 5, c = 0
Surge			
1N7038U3	4066	Condition A, T_A = +25°C, I_{FSM} = 140 A, 100 surges of 8.3 ms superimposed on I_O. V_R = 0; I_O = 0 A pk half sine wave, continuous.	
1N7058CCU3 1N7058CCU3C		Condition A, T_A = +25°C, I_{FSM} = 130 A, 100 surges of 8.3 ms superimposed on I_O. V_R = 0; I_O = 0 A pk half sine wave, continuous.	
Electrical measurements		See table I subgroup 2 (V_F and I_R only).	

1/ Each individual diode.

TEMPERATURE-CURRENT DERATING CURVE
1N7038U3

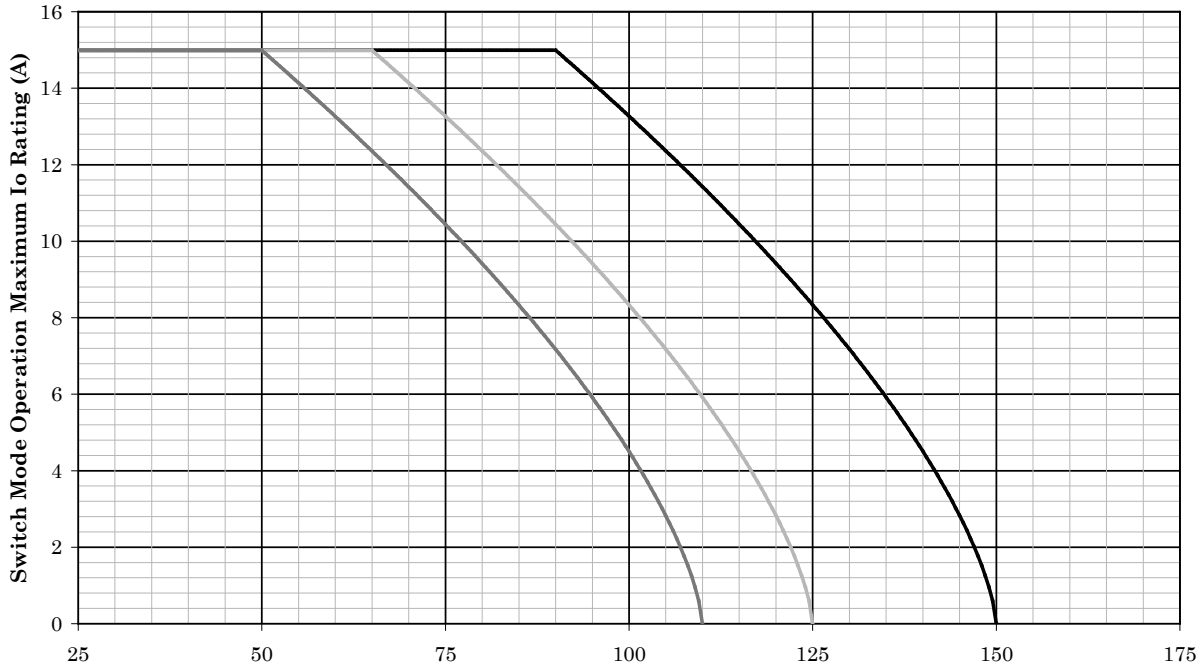


NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate current for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 150°C) and current rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 125°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤, 125°C, and 110°C to show current rating where most users want to limit T_J in their application.

FIGURE 2. Temperature-current derating curve (entire package) 1N7038U3.

TEMPERATURE-CURRENT DERATING CURVE
1N7058CCU3 and 1N7058CCU3C



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate current for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 150°C) and current rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 125°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ 125°C, and 110°C to show current rating where most users want to limit T_J in their application.

* FIGURE 3. Temperature-current derating curve (for each leg) for 1N7058CCU3. and1N7058CCU3C.

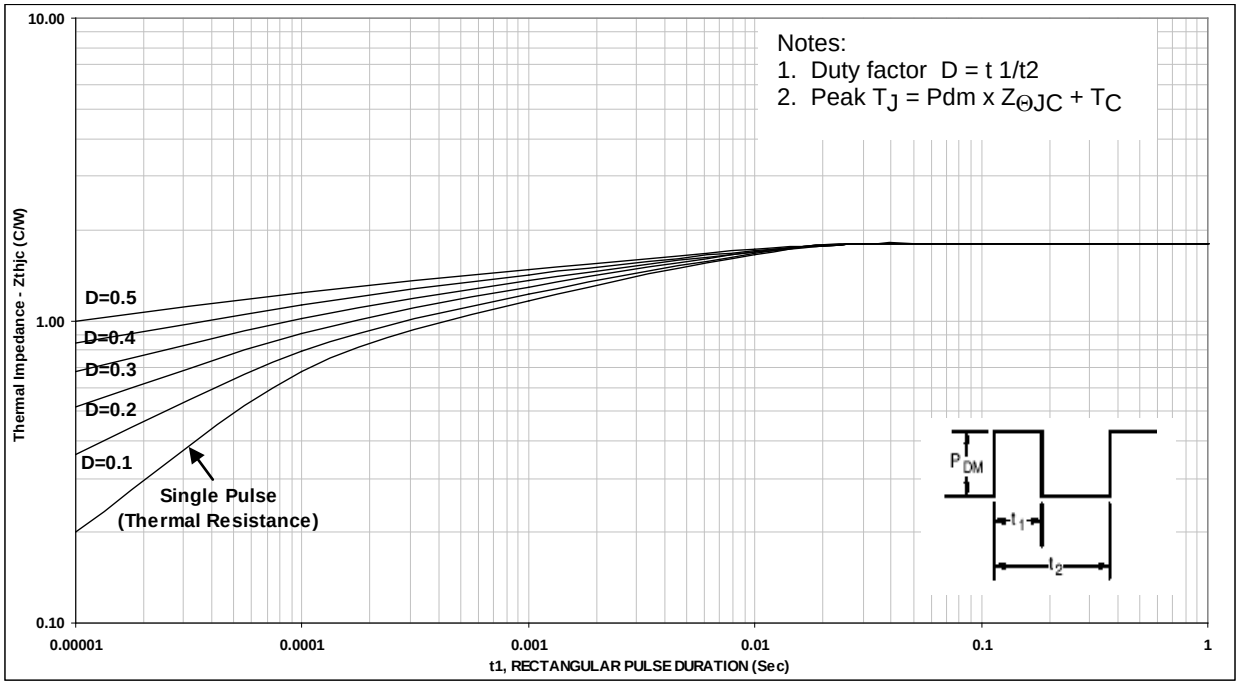
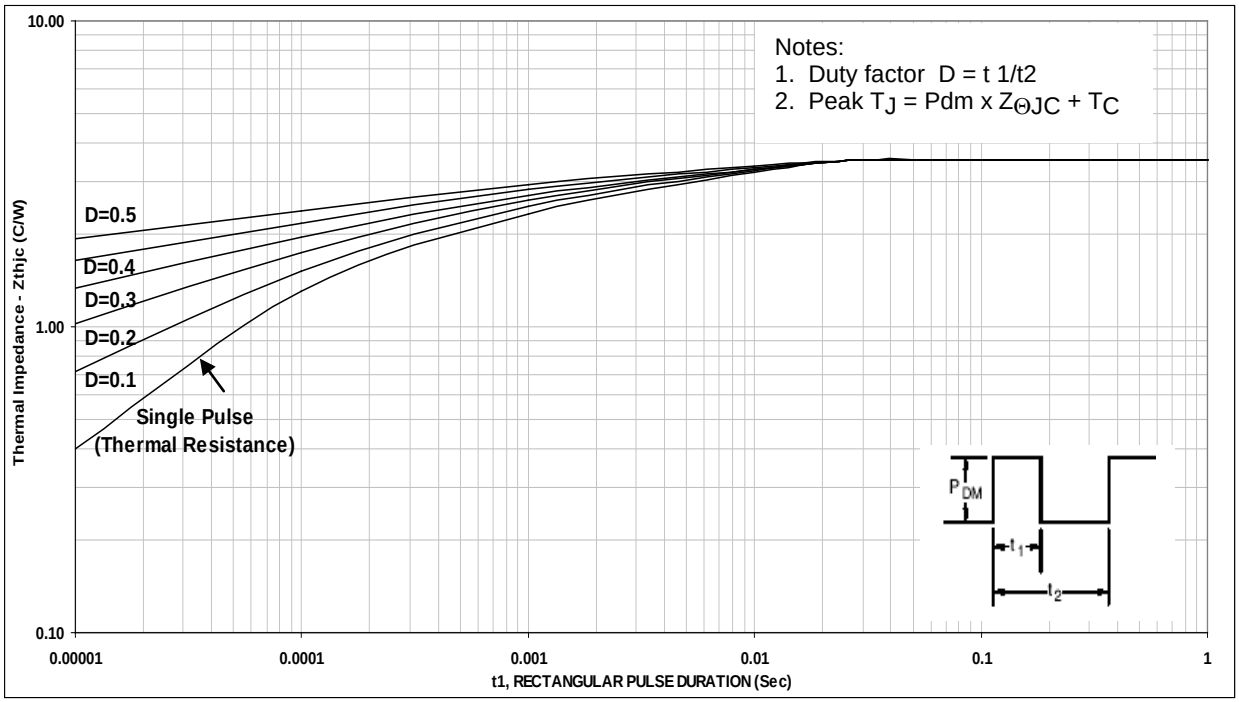
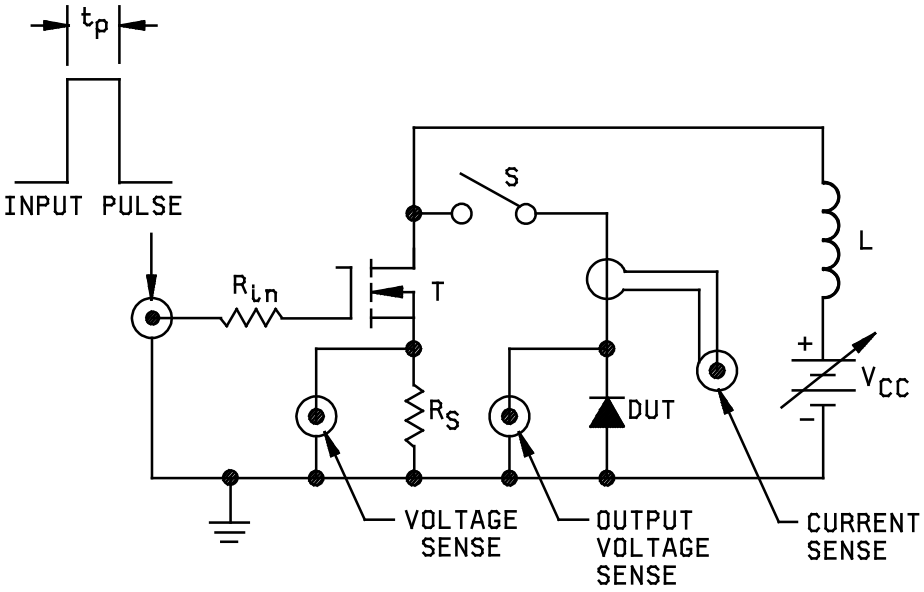


FIGURE 4. Thermal impedance 1N7038U3.



* FIGURE 5. Thermal impedance (for each leg), 1N7058CCU3 and 1N7058CCU3C.



Input pulse R_{in} = 50 ohms
V_G = 10 Volts, R_S = 0.1 ohms
Z_G = 50 ohms
L = 150mH
Duty cycle ≤ 1 percent, T = IRF350/2N6768 or equivalent

Procedure:
1. With S open, adjust pulse width to test current of 1 amp across R_S.
2. Close S, verify test current with current sense.
3. Read peak output voltage (see 4.3.3).

FIGURE 6. Avalanche energy test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead formation and finish (see 3.4.2).

d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil . An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.daps.dla.mil .

* 6.4 Cross reference substitution list. A PIN for PIN replacement table follows, and these devices are directly interchangeable.

Non-preferred PIN	Preferred PIN
30LJQ150	JANS, JANTXV, JANTX, JAN1N7038U3
30CLJQ150	JANS, JANTXV, JANTX, JAN1N7058CCU3
30CLJCQ150	JANS, JANTXV, JANTX, JAN1N7058CCU3C

* 6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2008-115)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.daps.dla.mil .