

The documentation and process conversion measures necessary to comply with this revision shall be completed by 6 January 2016.

INCH - POUND

MIL-PRF-19500/570F
6 October 2015
SUPERSEDING
MIL-PRF-19500/570E
26 August 2010

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, FIELD EFFECT, N-CHANNEL, SILICON LOGIC-LEVEL,
TYPES 2N6901 AND 2N6903,
JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for a logic-level N-channel, enhancement-mode, MOSFET, power transistor. Four levels of product assurance are provided for each encapsulated device (JAN, JANTX, JANTXV, and JANS). Two levels of product assurance are also provided for each unencapsulated device (JANHC and JANKC). See [6.5.2](#) for JANHC and JANKC die versions.

* 1.2 Package outlines. The device package outlines are as follows: TO-205AF (formerly TO-39) in accordance with [figure 1](#) for all encapsulated device types. See [figure 2](#) for unencapsulated devices.

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) $T_C = +25^\circ\text{C}$	I_{D2} (3) $T_C = +100^\circ\text{C}$	I_S	I_{DM}	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A(pk)</u>	<u>$^\circ\text{C}$</u>
2N6901	8.33	0.6	15.0	100	100	± 10	1.69	1.07	1.69	5	-55 to +150
2N6903	8.33	0.6	15.0	200	200	± 10	0.98	0.62	0.98	4	

(1) Derated linearly by 0.067 W/ $^\circ\text{C}$ for $T_C > +25^\circ\text{C}$.

(2) See [figure 3](#), thermal impedance curves.

(3) The following formula derives the maximum theoretical I_D limit. I_D is limited by internal construction and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



1.4 Primary electrical characteristics. Unless otherwise specified, at $T_C = +25^\circ\text{C}$.

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}$	$V_{GS(th)1}$ $V_{DS} \geq V_{GS}$ $I_D = 1\text{ mA}$	Max I_{DSS1} $V_{GS} = 0$ $V_{DS} = 80\text{ percent of}$ rated V_{DS}	Max $r_{DS(on)} (1)$ $V_{GS} = 5\text{ V dc}$	
				$T_J = +25^\circ\text{C}$ at I_{D1}	$T_J = +150^\circ\text{C}$ at I_{D2}
	<u>V dc</u>	<u>V dc</u>		<u>Ohms</u>	<u>Ohms</u>
		<u>Min</u>	<u>Max</u>	<u>μA dc</u>	
2N6901	100	1.0	2.0	1.0	1.4
2N6903	200	1.0	2.0		3.65
					2.9
					8.65

(1) Pulsed (see 4.5.1).

- * 1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.
- * 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".
- * 1.5.2 JAN certification mark and quality level for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHC" and "JANKC".
- * 1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.
- * 1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".
- * 1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "6901" and "6903".
- * 1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).
- * 1.5.5 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifier that is applicable for this specification sheet is "A" (see [figure 2](#) and 6.5) and applies only to the 2N6901.

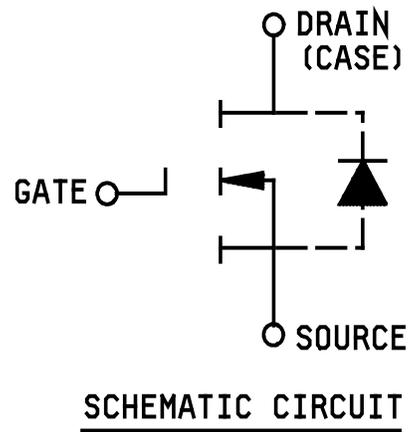
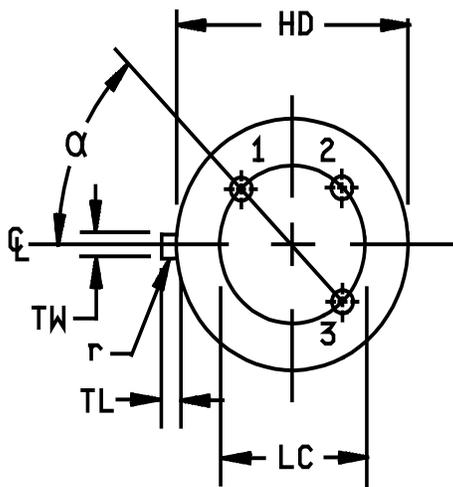
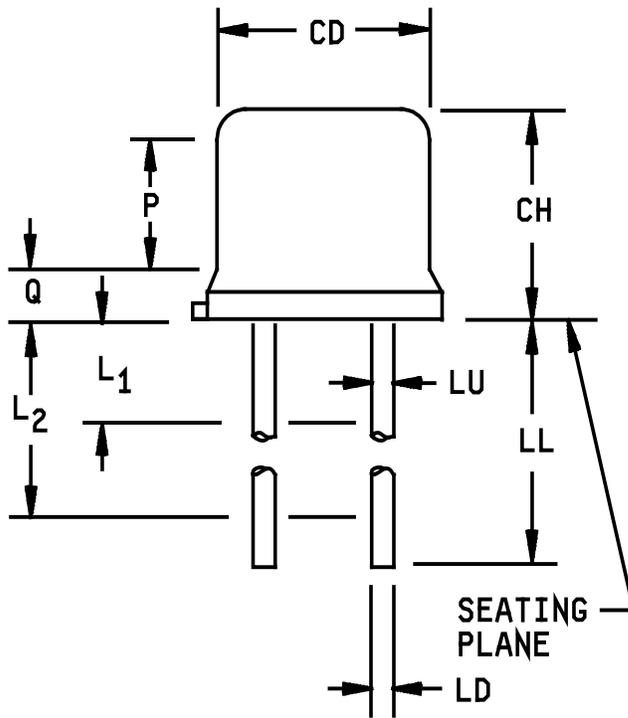


FIGURE 1. Physical dimensions for TO-205 AF.

MIL-PRF-19500/570F

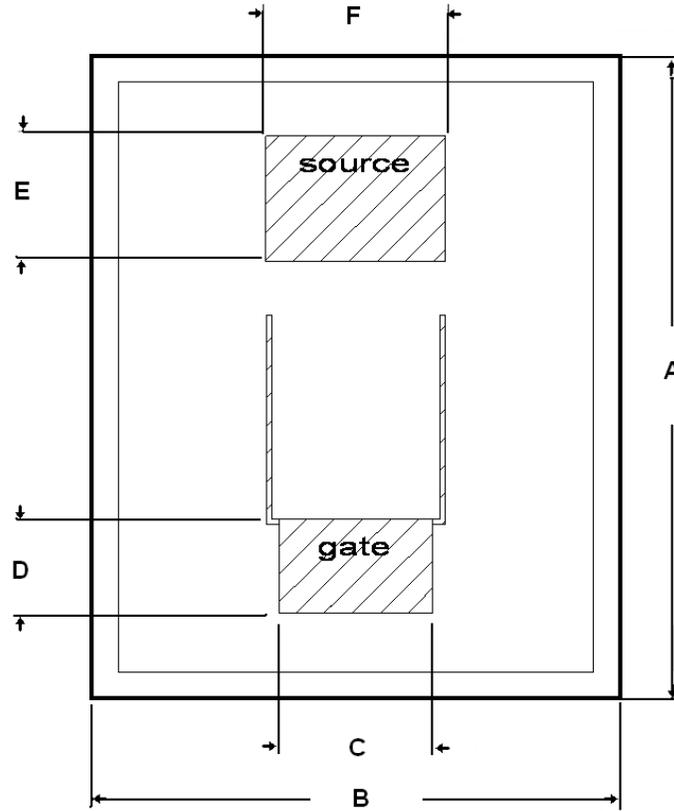
Dimensions					
Ltr	Inches		Millimeters		Notes
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.160	.180	4.07	4.57	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		
LD	.016	.021	0.41	0.53	8,9
LL	.500	.750	12.70	19.05	8,9
LU	.016	.019	0.41	0.48	8,9
L ₁		.050		1.27	8,9
L ₂	.250		6.35		8,9
P	.100		2.54		6
Q		.050		1.27	5
TL	.029	.045	0.74	1.14	4
TW	.028	.034	0.71	0.86	3
r		.010		0.25	10
α	45° TP		45° TP		6

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond radius(r) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Outline in this zone is not controlled.
6. Dimension CD shall not vary more than .010 (0.25 mm) in zone P. This zone is controlled for automatic handling.
7. Leads at gauge plane .054 +.001, -.000 (1.37 +0.03, -0.00 mm) below seating plane shall be within .007 (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
8. LU applies between L₁ and L₂. LD applies between L₂ and LL minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
9. All three leads.
10. Radius(r) applies to both inside corners of tab.
11. Drain is electrically connected to the case.
12. Pin out: 1- source, 2 - gate, 3 - drain (case).
13. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

FIGURE 1. Physical dimensions for TO-205 AF - Continued.

2N6901



Ltr	Dimensions - 2N6901			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.056	.062	1.42	1.58
B	.044	.051	1.12	1.30
C	.012	.016	.30	.41
D	.006	.010	.15	.25
E	.010	.014	.25	.36
F	.015	.019	.38	.48

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is ± 0.005 inch (0.13 mm).
4. The physical characteristics of the die are: The back metals are chromium, nickel, and silver and the back contact is the drain. The top metal is aluminum.
5. Die thickness is .015 inch (0.38 mm) ± 0.001 inch (0.025 mm).

FIGURE 2 . JANHCA and JANKCA (A-version) die dimensions for 2N6901

2. APPLICABLE DOCUMENTS

- * 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

- * (Copies of these documents are available online at <http://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows:

nCnano Coulomb

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#) (TO-205 AF) and [figure 2](#) (JANH C and JANKC die).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#) herein.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.8 Electrostatic discharge (ESD) protection. The devices covered by this specification require electrostatic discharge protection (see [3.8.1](#)).

3.8.1 Handling. Metal oxide semiconductor (MOS) devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.8).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq$ or 100 k Ω , whenever bias voltage is applied drain to source.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2 JANHC and JANKC die. Qualification shall be in accordance with MIL-PRF-19500.

* 4.3 Screening.

* 4.3.1 Screening (JANS, JANTX, and JANTXV levels only). Screening of packaged devices shall be in accordance with table E-IV of [MIL-PRF-19500](#), and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen (see, table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTX and JANTXV levels
(3)	Gate stress test (see 4.3.1.2)	Gate stress test (see 4.3.1.2)
(3)	Method 3470 of MIL-STD-750 , (see 4.3.1.3) optional	Method 3470 of MIL-STD-750 , (see 4.3.1.3) optional
(3) 3c	Method 3161 of MIL-STD-750 , (see 4.3.1.4)	Method 3161 of MIL-STD-750 , (see 4.3.1.4)
9	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , subgroup 2 of table I herein	Not applicable
10	Method 1042 of MIL-STD-750 , test condition B	Method 1042 of MIL-STD-750 , test condition B
11	Subgroup 2 of table I herein; I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(th)1}$ $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 0.2$ μ A dc or ± 100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(th)1}$
12	Method 1042 of MIL-STD-750 , test condition A, t = 240 hours	Method 1042 of MIL-STD-750 , test condition A or t = 48 hours minimum at $+175^{\circ}\text{C}$ minimum.
13	Subgroups 2 and 3 of table I herein; $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 0.2$ μ A dc or ± 100 percent of initial value, whichever is greater $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(th)1} = \pm 20$ percent of initial value.	Subgroup 2 of table I herein; $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 0.2$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(th)1} = \pm 20$ percent of initial value.

(1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} are measured.

(2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} , and $V_{GS(th)1}$ shall be invoked.

* (3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

* 4.3.1.1 Screening of unencapsulated die (JANHC and JANKC). Screening of die shall be in accordance with MIL-PRF-19500. As a minimum, die shall be 100-percent probed in accordance with [table I](#), subgroup 2.

4.3.1.2 Gate stress test. Apply $V_{GS} = 15 \text{ V}$ min. for $t = 250 \text{ } \mu\text{s}$ min.

4.3.1.3 Unclamped inductive switching.

- a. Peak current, I_D rated I_{D1} .
- b. Peak gate voltage, V_{GS} 10 V.
- c. Gate to source resistor, R_{GS} $25 \text{ } \Omega < R_{GS} < 200 \text{ } \Omega$.
- d. Initial case temperature $+25^\circ\text{C}$, $+10^\circ\text{C}$ -5°C .
- e. Inductance $100 \text{ } \mu\text{H} \pm 10$ percent.
- f. Number of pulses to be applied 1 pulse.

4.3.1.4 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (V_C and V_H where appropriate). Measurement delay time (t_{MD}) = $70 \text{ } \mu\text{s}$ max. See [table II](#), group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500, and [table I](#) herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500, and as follows.

4.4.2.1 Group B inspection, table E-VIA (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1051	Test condition G.
B3	2077	SEM.
* B4	1042	Test condition D. The heating cycle shall be 1 minute minimum.
B5	1042	Test condition A, $V_{DS} = \text{rated}$, $T_A = +175^\circ\text{C}$, $t = 120$ hours.
B5	1042	Test condition B, $V_{GS} = \text{rated}$, $T_A = +175^\circ\text{C}$, $t = 24$ hours.
B5	2037	Test condition D.

4.4.2.2 Group B inspection, table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B2	1051	Test condition G.
* B3	1042	Test condition D. The heating cycle shall be 30 seconds minimum.

- * 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#), and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	2036	Test condition E.

C5	3161	See 4.3.1.4, $R_{\theta JC}(\max) = 15^{\circ}\text{C}/\text{W}$.
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- * C6 1042 Test condition D. The heating cycle shall be 30 seconds minimum.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#), and [table II](#) herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Pulse measurements. Conditions for pulse measurements shall be as specified in section 4 of [MIL-STD-750](#).

TABLE I. Group A inspection.

*

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.1.4	$Z_{\theta JC}$			$^{\circ}\text{C} / \text{W}$
Breakdown voltage drain to source	3407	$I_D = 1.0 \text{ mA dc}$, bias condition C, $V_{GS} = 0$	$V_{(BR)DSS}$			
2N6901 2N6903				100 200		V dc V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1.0 \text{ mA dc}$	$V_{GS(th)1}$	1.0	2.0	V dc
Gate current	3411	$V_{GS} = +10 \text{ V dc}$, bias condition C, $V_{DS} = 0$	I_{GSSF1}		+100	nA dc
Gate current	3411	$V_{GS} = -10 \text{ V dc}$, bias condition C, $V_{DS} = 0$	I_{GSSR1}		-100	nA dc
Drain current 2N6901 2N6903	3413	Bias condition C, $V_{GS} = 0$ $V_{DS} = 80 \text{ V dc}$ $V_{DS} = 160 \text{ V dc}$	I_{DSS1}		1.0 1.0	$\mu\text{A dc}$ $\mu\text{A dc}$
Static drain to source on-state resistance 2N6901 2N6903	3421	$V_{GS} = 5 \text{ V dc}$, bias condition A, pulsed (see 4.5.1) $I_D = 1.07 \text{ A dc}$ $I_D = 0.62 \text{ A dc}$	$r_{DS(on)1}$		1.4 3.65	Ω Ω
Drain to source on-state voltage 2N6901 2N6903	3405	$V_{GS} = 5 \text{ V dc}$, bias condition A, pulsed (see 4.5.1) $I_D = 1.69 \text{ A dc}$ $I_D = 0.98 \text{ A dc}$	$V_{DS(on)}$		2.4 6.0	V V
* Forward voltage (source drain diode) 2N6901 2N6903	4011	Condition A, $V_{GS} = 0$ $I_S = 1.69 \text{ A dc}$ $I_S = .98 \text{ A dc}$	V_{SD}	0.8	1.6	V
Forward transconductance	3475	$I_D = \text{rated } I_{D2}$ (see 1.3), pulsed (see 4.5.1)	g_{FS}	0.5	2.0	S

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u>						
High temperature operation:		$T_C = T_J = +125^\circ\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1.0 \text{ mA dc}$	$V_{GS(th)2}$	0.5		V dc
Gate current	3411	$V_{GS} = +10 \text{ V dc}$ and -10 V dc ; $V_{DS} = 0$; bias condition C	I_{GSS2}		± 200	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0 \text{ V}$	I_{DSS2}		50	$\mu\text{A dc}$
2N6901 2N6903		$V_{DS} = 80 \text{ V dc}$ $V_{DS} = 160 \text{ V dc}$				
Static drain to source on-state resistance	3421	$V_{GS} = 5 \text{ V dc}$, pulsed (see 4.5.1)	$r_{DS(on)2}$			
2N6901 2N6903		$I_D = 1.07 \text{ A dc}$ $I_D = 0.62 \text{ A dc}$			2.6 7.7	Ω Ω
Low temperature operation:		$T_C = T_J = -55^\circ\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1.0 \text{ mA dc}$	$V_{GS(th)3}$		3.0	V dc
<u>Subgroup 4</u>						
Switching time test	3472	$I_D = \text{rated } I_{D2}$, (see 1.3); $V_{GS} = 5 \text{ V dc}$, gate drive impedance = 25Ω				
Turn-on delay time			$t_{d(on)}$		25	ns
2N6901 2N6903		$V_{DD} = 50 \text{ V dc}$ $V_{DD} = 100 \text{ V dc}$				
Rise time			t_r		80	ns
2N6901 2N6903		$V_{DD} = 50 \text{ V dc}$ $V_{DD} = 100 \text{ V dc}$				

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u> - Continued						
Turn-off delay time			$t_{d(off)}$			
2N6901		$V_{DD} = 50$ V dc			45	ns
2N6903		$V_{DD} = 100$ V dc			40	ns
Fall time			t_f		80	ns
2N6901		$V_{DD} = 50$ V dc				
2N6903		$V_{DD} = 100$ V dc				
<u>Subgroup 5</u>						
Safe operating area (SOA) test	3474	See figure 4 $V_{DS} = 80$ percent of rated V_{DS} and $V_{DS} \leq 200$ V max				
High voltage dc SOA		$t_p = 1$ ms				
Electrical measurements		See table I , subgroup 2				
Single pulse unclamped inductive switching	3470	See 4.3.1.3 ; $c = 0$, 116 devices				
Electrical measurements		See table I , subgroup 2				
<u>Subgroups 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition A or B				
On-state gate charge			$Q_{g(on)}$			
2N6901					5	nC
2N6903					5	nC

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 7</u> - Continued						
Gate to source charge			Q_{gs}			
2N6901					1.0	nC
2N6903					0.8	nC
Gate to drain charge			Q_{gd}			
2N6901					2.9	nC
2N6903					2.7	nC
Reverse recovery time	3473	$V_{DD} \leq 30 \text{ V}; di/dt = 100 \text{ A}/\mu\text{s}$ $I_F = 1 \text{ A}$	t_{rr}			
2N6901					250	ns
2N6903					500	ns

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ This test required for the following end-point measurements only:
 Group B, subgroups 3 and 4 (JANS).
 Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).
 Group C, subgroup 2 and 6.
 Group E, subgroup 1.

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TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071	As applicable	
Electrical measurements		See table I , subgroup 2.	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		See table I , subgroup 2.	
Steady-state gate bias	1042	Condition B, 1,000 hours.	
Electrical measurements		See table I , subgroup 2.	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	

1/ A separate sample for each test shall be pulled.

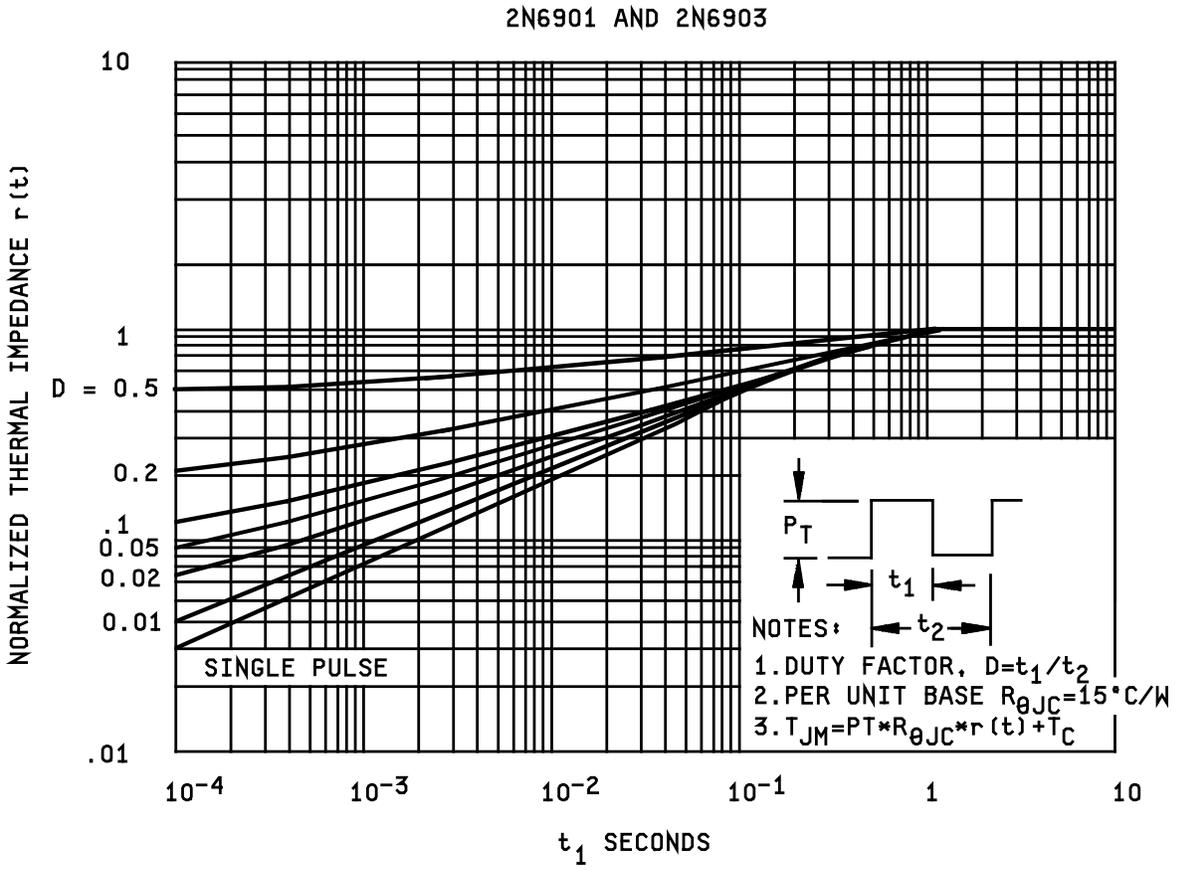


FIGURE 3. Transient thermal response.

2N6901

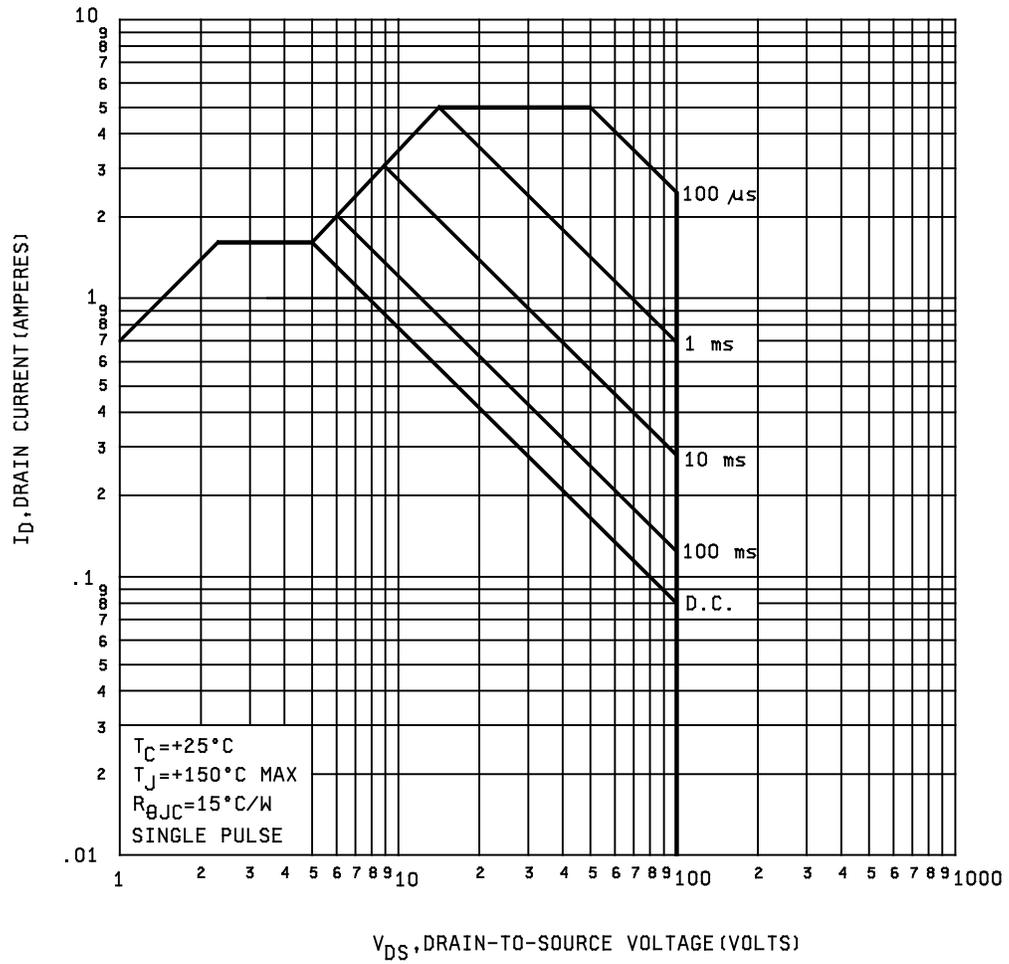


FIGURE 4. Maximum safe operating area.

2N6903

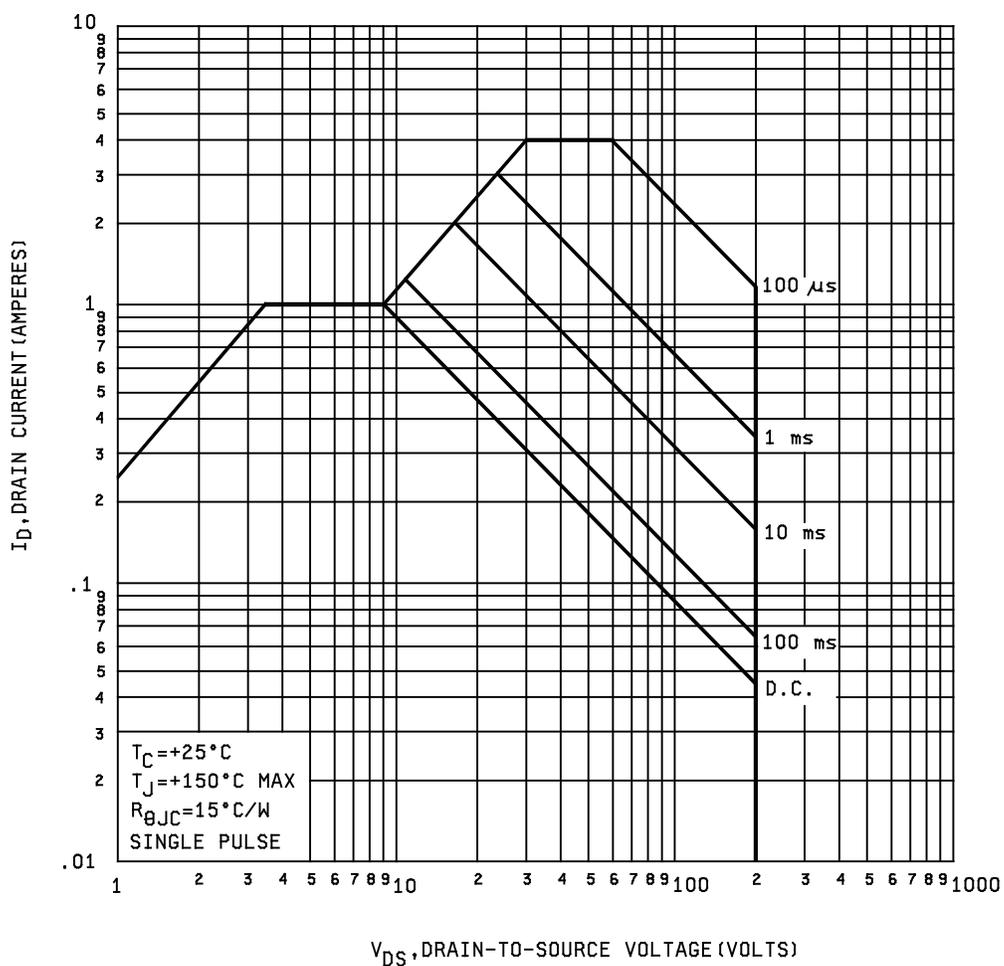


FIGURE 4. Maximum safe operating area - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).

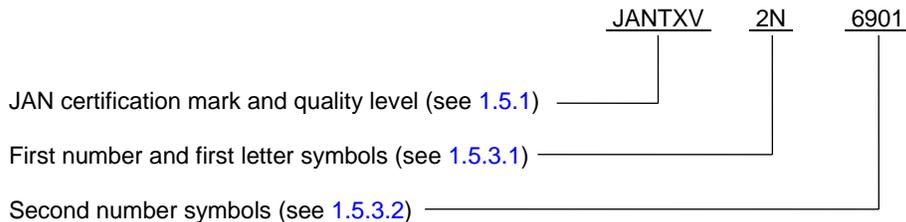
* d. The complete PIN, see 1.5 and 6.5.

* e. For die acquisition, the JANHC or JANKC letter version should be specified (see figure 2).

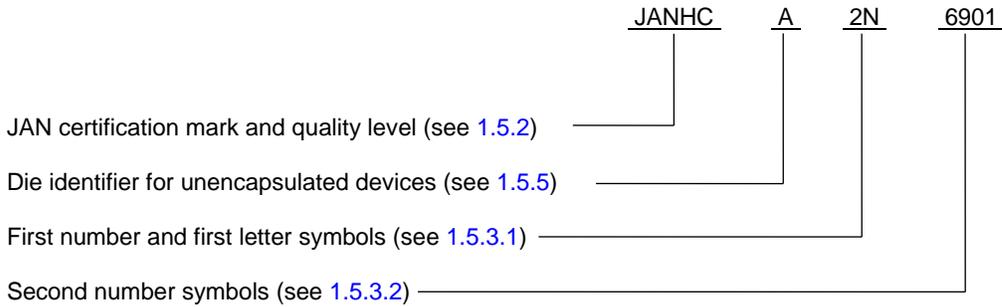
* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

* 6.4 PIN construction example.

* 6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



- * 6.4.2 Unencapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



- * 6.5 List of PINs.

- * 6.5.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN2N6901	JANTX2N6901	JANTXV2N6901	JANS2N6901
JAN2N6903	JANTX2N6903	JANTXV2N6903	JANS2N6903

- * 6.5.2 List of PINs for unencapsulated devices. The following is a list of possible PINs available on this specification sheet. The qualified die suppliers with the applicable letter version (e.g., JANHCA2N6901) will be identified on the QML.

Die ordering information	
PIN	Manufacturer
2N6901 (1)	JANHCA2N6901 JANKCA2N6901

(1) The 2N6903 is not available in the die version.

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
Navy - EC
Air Force - 85
DLA - CC

Preparing activity:

DLA - CC

(Project 5961-2015-094)

Review activities:

Army - AR, MI, SM
Navy - AS, MC, OS, SH
Air Force - 19

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.